Features

- **Very Low Power Design (40 mW)**
- **Single IF Architecture**
- **Excellent Noise Performance**
- **1.5-bit ADC On Chip**
- **Small QFN Package (4 mm × 4 mm, 24 pins)**
- **Highly integrated, Few External Components**
- **Advanced BiCMOS Technology (UHF6s)**
- **RoHS Compliant**

GPS Front-end IC

ATR0601

1. Description

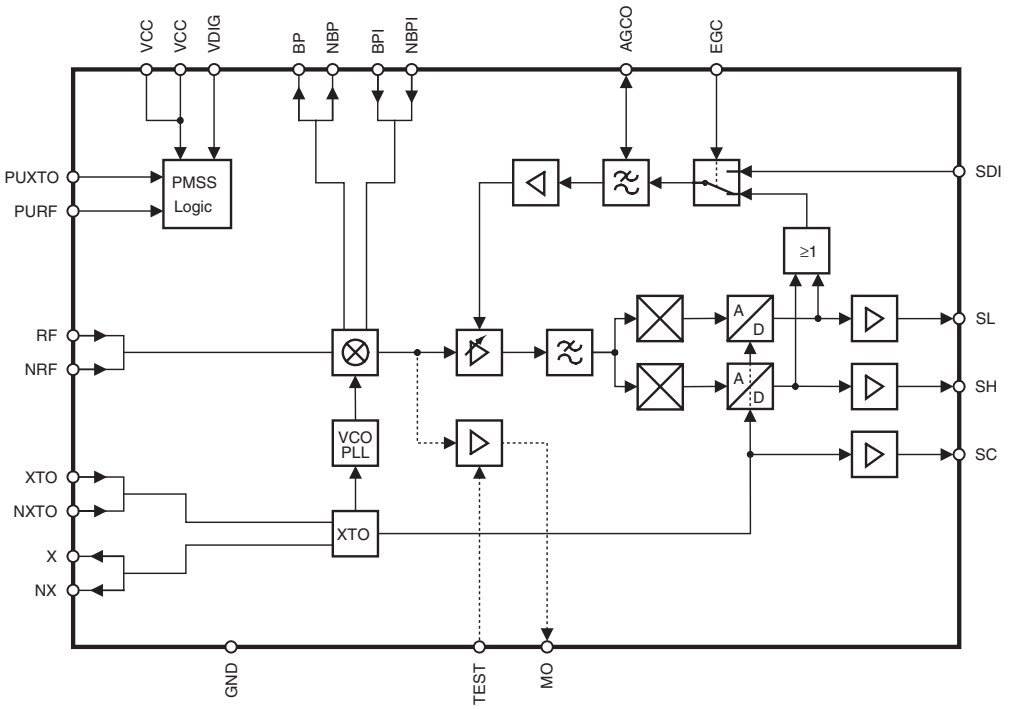
The ATR0601 is a single IF GPS front-end IC, designed to meet the requirements of mobile and automotive applications.

Excellent RF performance combined with low noise figure enables high quality GPS solutions and it's very low power consumption fits perfectly to portable devices. Featuring a balanced XTO and a fully integrated balanced frequency synthesizer, only few external components are required.

The ATR0601 offers a complete autonomous mode, utilizing the on chip AGC in closed loop operation, to set the gain of the IF VGA.

Alternatively, in combination with the Antaris™4 baseband processor family, the optimum gain of the IF VGA can be computed and set by software, using the digital SDI interface.

Figure 1-1. Block Diagram



4866G–GPS–11/06

2. Pin Configuration

Figure 2-1. Pinning QFN24

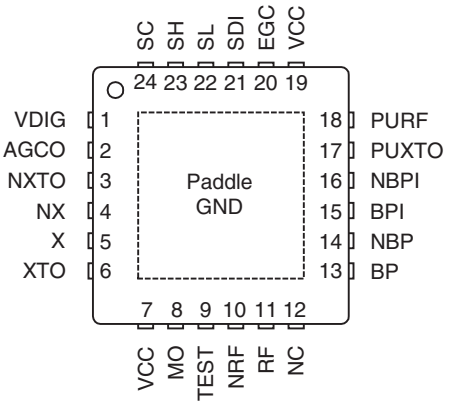


Table 2-1. Pin Description

Pin	Symbol	Type[1]	Function
Paddle	GND	S	Common ground
1	VDIG	S	Digital supply
2	AGCO	A_I/O	AGC: gain control voltage output/corner frequency determination
3	NXTO	A_I	XTO interface (optional: TCXO input)
4	NX	A_O	XTO interface
5	X	A_O	XTO interface
6	XTO	A_I	XTO interface (optional: TCXO input)
7	VCC	S	Analog supply
8	MO	A_O	Testbuffer output (f_{IF})
9	TEST	A_I	Enable testbuffer
10	NRF	A_I	RF input complementary
11	RF	A_I	RF input
12	NC	–	Not connected
13	BP	A_O	IF-Filter interface (mixer output, open collector)
14	NBP	A_O	IF-Filter interface (mixer output complementary, open collector)
15	BPI	A_I	IF-Filter interface (IF-input)
16	NBPI	A_I	IF-Filter interface (IF-input complementary)
17	PUXTO	D_I	Power-up XTO
18	PURF	D_I	Power-up RF
19	VCC	S	Analog supply
20	EGC	D_I	Enable external gain control (high = external; low = internal)
21	SDI	D_I	Input for external gain control signal ($\Sigma\Delta$ modulation)
22	SL	D_O	Data output: “low”
23	SH	D_O	Data output: “high”
24	SC	D_O	Sample clock

Note: 1. Type: A_I Analog input, A_O Analog output, D_I Digital input, D_O Digital output, S Supply

3. Functional Description

3.1 General Description

The ATR0601 GPS receiver IC has been especially designed for GPS applications in both mobile phone and automotive applications. From this system point of view, it incorporates highest isolation between GPS and cellular bands, as well as very low power consumption.

The L1 input signal (f_{RF}) is a Direct Sequence Spread Spectrum (DSSS) signal with a centre frequency of: f_{RF} = 1575.42 MHz. The digital modulation scheme is Bi-Phase-Shift-Keying (BPSK) with a chip rate of 1.023 Mbps. As the input signal power at the antenna is approximately –140 dBm, the desired signal is below the thermal noise floor.

3.2 PMSS Logic

The Power Management, Startup and Shutdown Logic ensures reliable operation within the recommended operating and timing conditions. The external power control signals PUrf and PUxto are passed thru Schmitt-trigger inputs, digital and analog supply voltages are analyzed by monitoring circuits.

3.3 XTO

The XTO is designed for minimum phase noise and frequency perturbations. The balanced topology gives maximum isolation from external and ground coupled noise. The built-in jump start circuitry ensures reliable start-up behaviour of any specified crystal. For use with an external TCXO, the XTO circuitry can be used as a single-ended or balanced input buffer.

The recommended reference frequency is: f_{XTO} = 23.104 MHz.

3.4 VCO/PLL

The frequency synthesizer features a balanced VCO and a fully integrated loop filter, thus no external components are required. The VCO combines very good phase noise behaviour and excellent spurious suppression. The relation between the reference frequency (f_{XTO}) and the VCO centre frequency (f_{VCO}) is given by: $f_{VCO} = f_{XTO} \times 64 = 23.104\ \text{MHz} \times 64 = 1478.656\ \text{MHz}$.

3.5 RF-Mixer/Image-filter

Combined with the antenna an external LNA provides a first band-pass filtering of the signal. For the LNA, Atmel's ATR0610 is recommended, due to it's low Noise Figure, high linearity an low power consumption. The output of the LNA drives an SAW filter, which provides image rejection for the mixer and the required isolation of all GSM bands. The output of the SAW filter is fed into a highly linear mixer with high conversion gain and excellent noise performance.

The IF frequency (f_{IF}) is given by: $f_{IF} = f_{RF} - f_{VCO} = 1575.42\ \text{MHz} - 1478.656\ \text{MHz} = 96.764\ \text{MHz}$.

3.6 IF-filter

The mixer directly drives an external LC band-pass filter via open collector outputs. In order to provide highest selectivity and conversion gain, it is recommended to design the external filter, according to the application proposal, as a 2-pole filter with a quality factor Q > 25.

3.7 VGA/AGC

The output of the IF-Filter drives an on-chip Variable Gain Amplifier (VGA) which is combined with additional low-pass filtering. The on-chip Automatic Gain Control (AGC) stage sets the gain of the VGA in order to optimally charge the input of the following analog-to-digital converter. The AGC control loop can be selected for on-chip closed loop operation or for external gain control mode. For external gain control mode, the loop needs to be closed by the baseband IC ATR0621.

3.8 A/D Converter

The analog-to-digital converter stage has a total resolution of 1.5 bit. It comprises balanced comparators and a sub sampling unit, clocked by the reference frequency (f_{XTO}). The frequency spectrum of the digital output signal (f_{OUT}), present at the data outputs SL and SH, is then given by: $f_{OUT} = \left| f_{IF} - f_{XTO} \times n \right|$. The selected sub sampling factor (n = 4) leads to the designated digital output signal, with a centre frequency given by:
$f_{OUT} = f_{IF} - f_{XTO} \times 4 = 96.764\ \text{MHz} - 23.104\ \text{MHz} - 4 = 4.348\ \text{MHz}$.

3.9 Clock and Data Driver

CMOS output drivers are providing 1.5 bit data (SH, SL) and the system clock (SC). The rail-to-rail output signal level is determined by the digital supply voltage (VDIG).

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Analog supply voltage	V_{CC}	–0.3 to +3.7	V
Digital supply voltage	V_{DIG}	–0.3 to +3.7	V
Input voltage	V_{in}	–0.3 to +3.7	V
Operating temperature	T_{op}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{th}	125	K/W

6. Operating Range

Parameters	Symbol	Value	Unit
Analog supply voltage	V_{CC}	2.70 to 3.30	V
Digital supply voltage	V_{DIG}	1.65 to 2.00	V
Supply voltage difference ($V_\Delta = V_{CC} - V_{DIG}$)	V_Δ	≥ 0.80	V
Temperature range	Temp	–40 to +85	°C
Input frequency	f_{RF}	1575.42	MHz
Reference frequency	f_{XTO}	23.104	MHz

7. ESD Characteristics

Parameters	Symbol	Norm	Value	Unit
ESD level HBM (Human Body Model)	VHBM	ANSI/ESD STM.5.1-2001	2500	V
ESD level MM (Machine Machine Model)	VMM	EIA/JESD22 A115 A	250	V
ESD level CDM (Charged Device Model)	VCDM	ESD STM.5.3.1-1999	1250	V

8. Electrical Characteristics

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Common**								
1.1	Analog supply current[1]	$V_{PUxto} = V_{PUrf} = V_{PU,on}$	7, 19	I_S		14.2		mA	A
1.2	Digital supply current [1],[2]	$V_{PUxto} = V_{PUrf} = V_{PU,on}$	1	I_{DIG}		700		µA	A
1.3	Analog supply current in XTO mode[1]	$V_{PUxto} = V_{PU,on}$, $V_{PUrf} = V_{PU,off}$	7, 19	I_{S_XTO}		2.9		mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. Conditions: V_{CC} = 2.7V; V_{DIG} = 1.65V; Temperature = 27°C
2. Capacitive load (C_L = 3.3 pF) at pins 22, 23, 24
3. Capacitive load (C_L = 3.3 pF) at pin 24

8. Electrical Characteristics (Continued)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.4	Digital supply current in XTO mode(1),(3)	$V_{PUxto} = V_{PU,on}$, $V_{PUrf} = V_{PU,off}$	1	I_{DIG_XTO}		500		µA	A
1.5	Supply current in power down mode(1)	$V_{PUxto} = V_{PUrf} = V_{PU,off}$	1, 7, 19	I_{PD}			2	µA	A
1.6	Maximum total gain	V_{AGCO} = 2.2V		G_{max_tot}		90		dB	B
1.7	Noise figure (SSB)			NF_{tot}			6.8	dB	C
2	**Mixer**								
2.1	Output frequency	f_{XTO} = 23.104 MHz	13, 14	f_{IF}		96.764		MHz	A
2.2	Input impedance (balanced)	f_{RF} = 1575.42 MHz	10, 11	Z_{11}		10-j80		Ω	C
2.3	Conversion Gain	Recommended IF-filter	8	G_{MIX}		20		dB	B
2.4	Noise figure (SSB)		8	NF_{MIX}		5.8		dB	C
3	**VGA/AGC**								
3.1	Minimum gain	V_{AGCO} = 1.0V		$G_{VGA,min}$		0		dB	B
3.2	Maximum gain	V_{AGCO} = 2.2V		$G_{VGA,max}$		70		dB	B
3.3	Control-voltage sensitivity	V_{AGCO} = 2.2V		$N_{VGA,min}$		6.6		dB/V	D
		V_{AGCO} = 1.0V		$N_{VGA,max}$		150		dB/V	D
3.4	AGC cut-off frequency	C_{ext} = open	2	f_{3dB_AGC}		250		kHz	D
3.5	AGC cut-off frequency	C_{ext} = 100 pF	2	f_{3dB_AGC}		33		kHz	D
3.6	Gain-control output voltage		2	V_{AGCO}	0.9		2.3	V	B
4	**Reference Oscillator**								
4.1	XTO phase noise at 100 Hz	With specified crystal	24	Pn_{100}		–80		dBc/Hz	C
4.2	XTO phase noise at 1 kHz	With specified crystal	24	Pn_{1k}		–100		dBc/Hz	C
5	**Clock and Data Driver**								
5.1	Clock driver frequency	f_{XTO} = 23.104 MHz	24	f_{CLK}		23.104		MHz	A
5.2	Clock output level	$C_{load,max}$ = 10 pF	24	$V_{CLK,high}$		$0.9 \times V_{DIG}$		V	B
5.3	Clock output level	$C_{load.max}$ = 10 pF	24	$V_{CLK,low}$		$0.1 \times V_{DIG}$		V	B
5.4	Data output level	$C_{load,max}$ = 10 pF	22, 23	$V_{Data,high}$		$0.9 \times V_{DIG}$		V	B
5.5	Data output level	$C_{load,max}$ = 10 pF	22, 23	$V_{Data,low}$		$0.1 \times V_{DIG}$		V	B
6	**PMSS**								
6.1	Voltage level power-on		17, 18	$V_{PU,on}$	1.3			V	A
6.2	Voltage level power-off		17, 18	$V_{PU,off}$			0.5	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Conditions: V_{CC} = 2.7V; V_{DIG} = 1.65V; Temperature = 27°C

2. Capacitive load (C_L = 3.3 pF) at pins 22, 23, 24

3. Capacitive load (C_L = 3.3 pF) at pin 24

9. Timing

Figure 9-1. Recommended Power-up/down Sequence

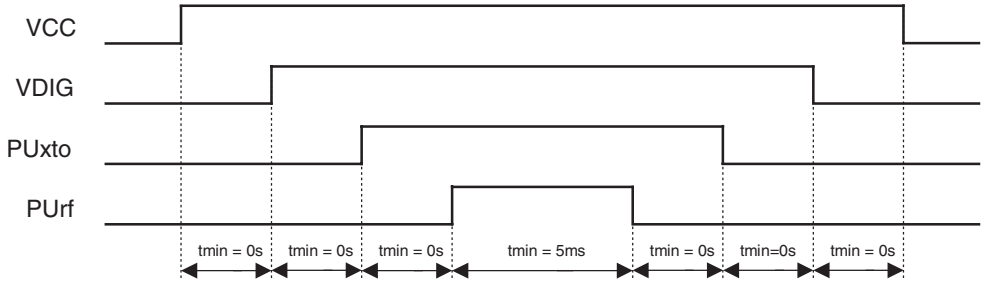


Figure 9-2. Recommended Sleep-mode Sequence

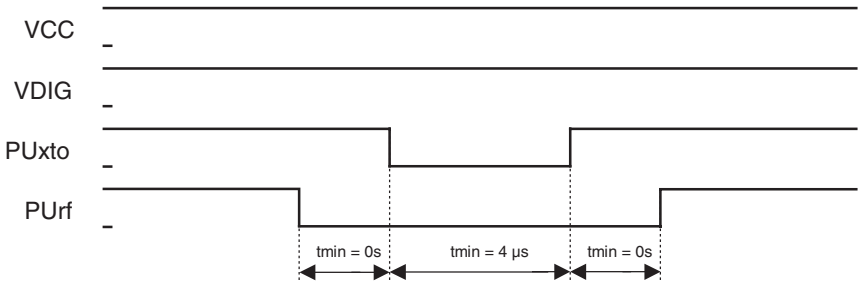


Figure 9-3. Recommended XTO Start-up/Shut-down Sequence

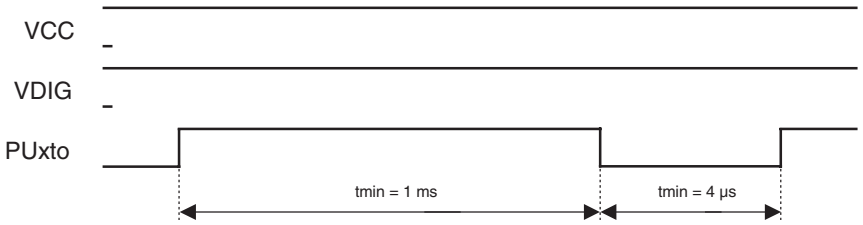


Figure 9-4. Sample Clock Start-up Delay

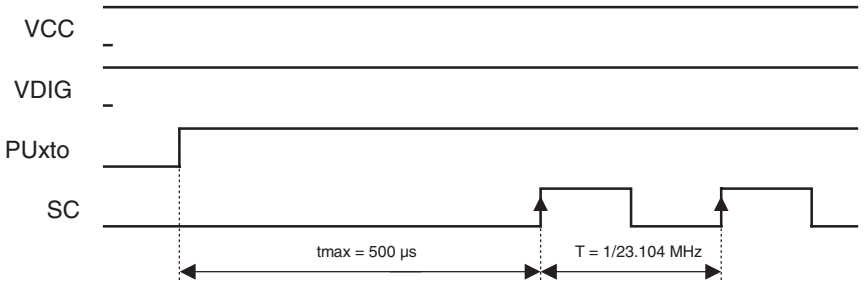


Figure 9-5. Synchronous Shut-down Behavior of SC with Respect to PUxto

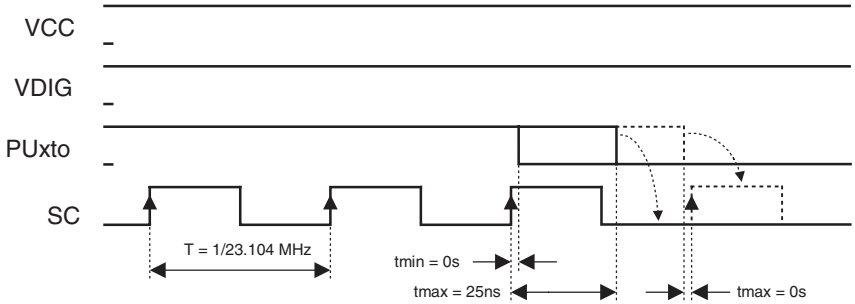
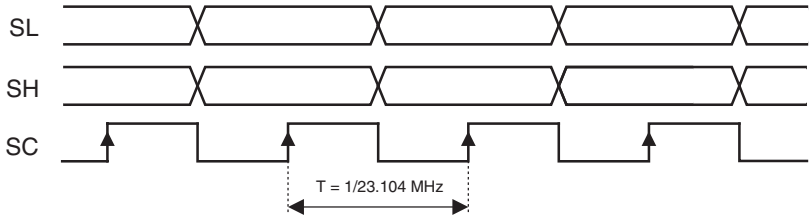
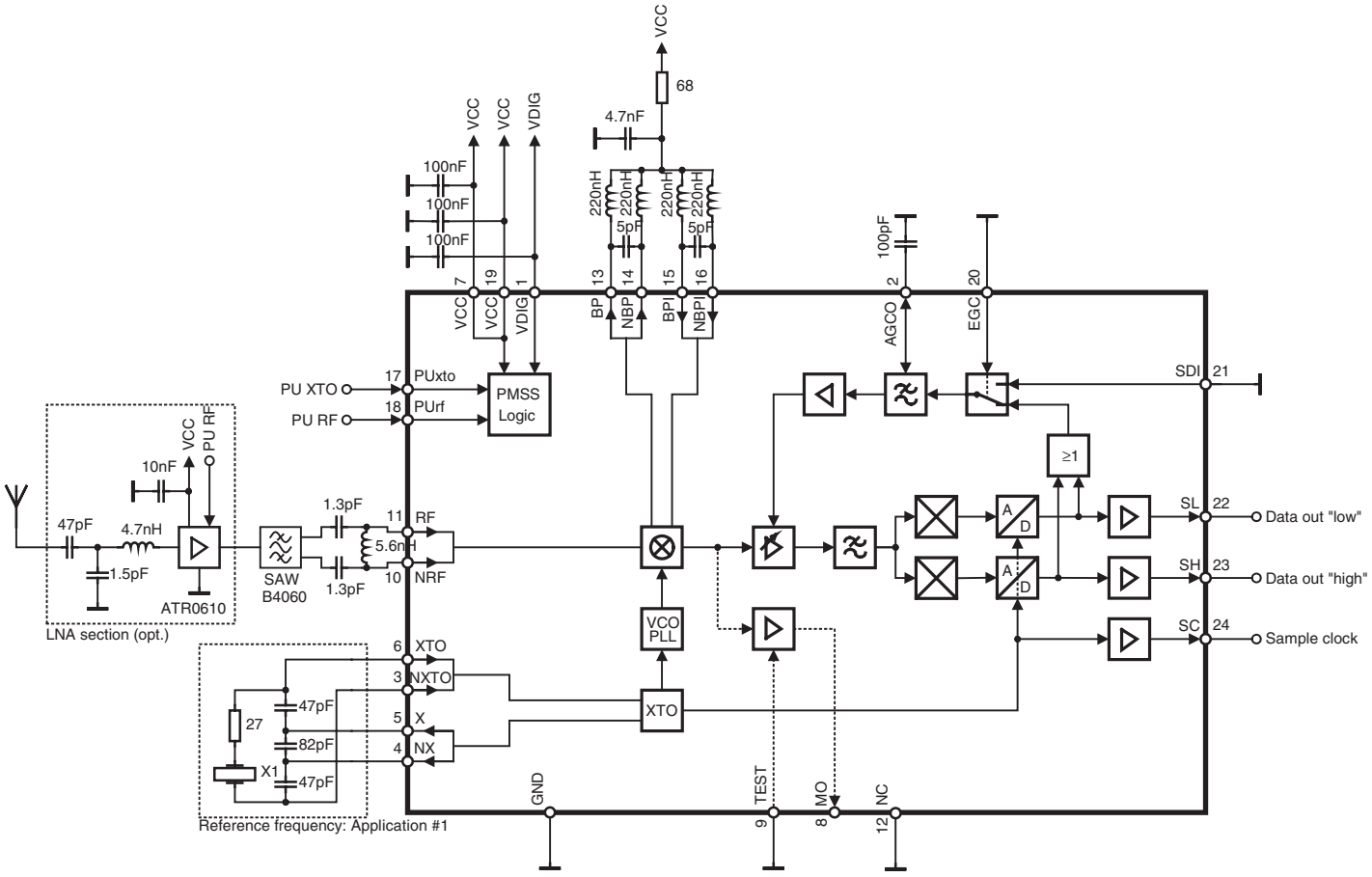


Figure 9-6. Data Outputs SL and SH are Valid with Rising Edge of Sample Clock SC



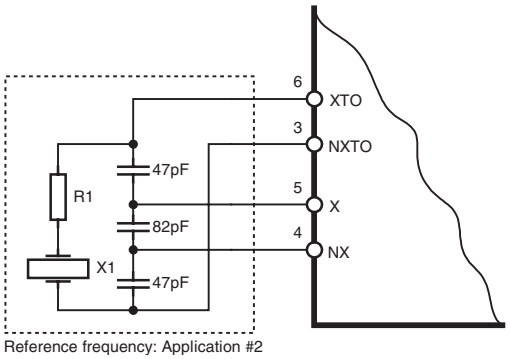
10. Application Circuit

Figure 10-1. Application Example Using a GPS Crystal with ESR_{typ} = 12Ω (Please see Table 10-1 on page 11)



Note: Please consider the recommended IF-filter layout, shown in Figure 10-5 on page 11.

Figure 10-2. Application Example Using a GPS Crystal with ESR_{typ} ≈ 12Ω (Please see Table 10-2 on page 12)



Note: The external series resistor R1 has to be selected depending on the typical value of the crystal ESR. Please refer to Application Note “ATR0601: Crystal and TXCO selection”.

Figure 10-3. Equivalent Application Examples Using a GPS TCXO (Please see Table 10-3 on page 12)

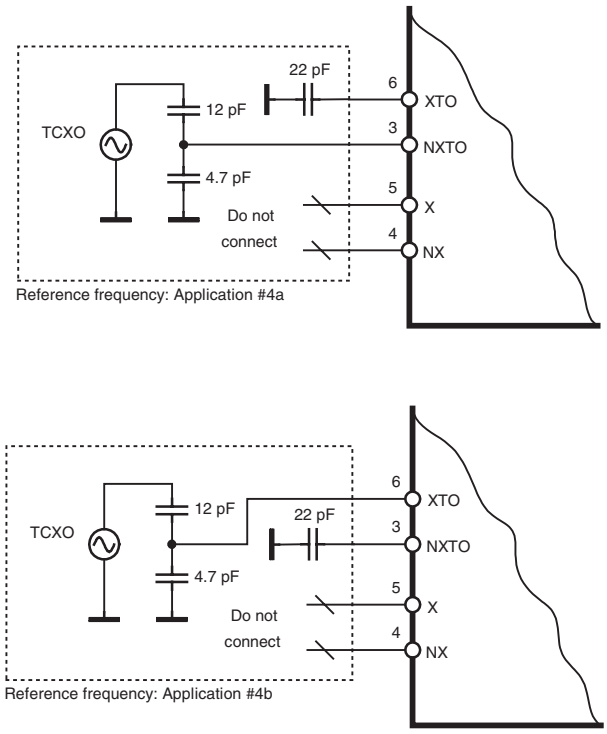


Figure 10-4. Application Example Using an External Reference and Balanced Inputs (Please see Table 10-4 on page 12)

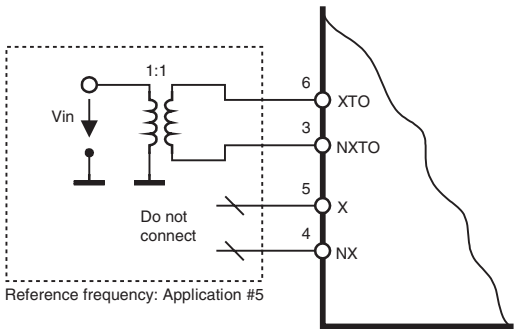
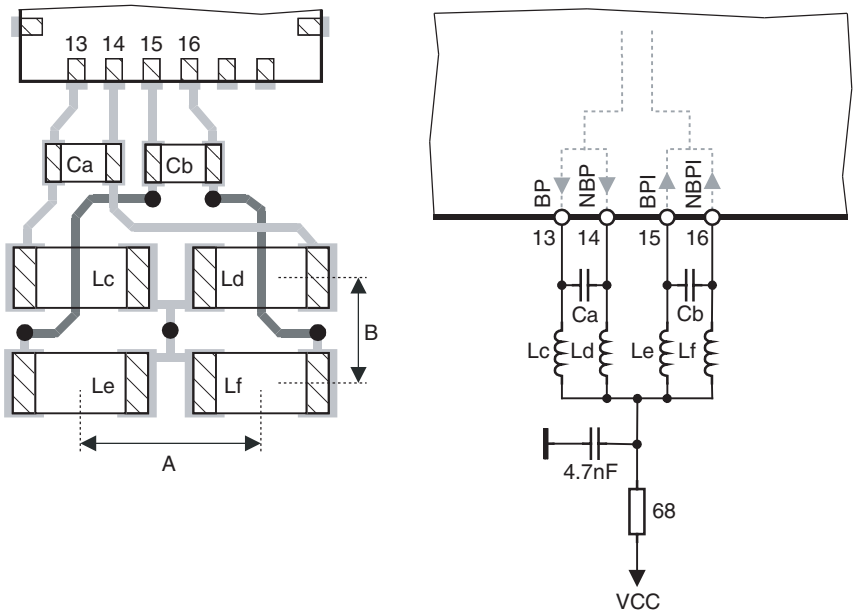


Figure 10-5. Recommended IF-filter: Layout versus Schematic



Note: Mutual inductance between the four inductors Lc - Lf plays an important role in the IF-filter characteristics. In any design, the layout arrangement shown in Figure 10-5 on page 11 should be resembled as close as possible. Measures: A = 2.8 mm; B = 1.4 mm; Lc - Lf: Wirewound SMD inductors, 0603 size. (Please see Table 11-1).

Table 10-1. Specification of GPS Crystals Appropriate for the Application Example Shown in Figure 10-1 on page 9

Parameter	Comment	Min.	Typ.	Max.	Units
Frequency Characteristics					
Fundamental Frequency	Nominal frequency referenced to 25°C		23.104		MHz
Calibration tolerance	Frequency at 23°C ±2°C			7.0	±ppm
Frequency deviation	Over operating temperature range			15.0	±ppm
Temperature range	Operating temperature range	–40.0		+85.0	°C
Electrical					
Load capacitance (CL)		18.5		19.5	pF
Equivalent Series Resistance (ESR)					
Fundamental	Specification	7	12	23	Ω

Table 10-2. Specification of GPS Crystals Appropriate for the Application Example Shown in Figure 10-2 on page 9

Parameter	Comment	Min.	Typ.	Max.	Units
Equivalent Series Resistance (ESR)					
Fundamental	Specification	7		40	Ω

Note: All other parameters as specified in Table 10-1.

Table 10-3. Specification of GPS TCXOs Appropriate for the Application Example Shown in Figure 10-3 on page 10 (For Baseband with SuperSense™ Software)

Parameter	Comment	Min.	Typ.	Max.	Units
Frequency Characteristics					
Nominal Frequency	Nominal frequency referenced to 25°C		23.104		MHz
Frequency deviation	Over operating temperature range			0.5	±ppm
	Including calibration, temperature, soldering and ageing effects			8	±ppm
Temperature range	Operating temperature range	–40.0		+85.0	°C
Electrical					
Output waveform	DC coupled clipped sinewave				
Output voltage (peak-to-peak)	Operating range	0.8		1.5	V
Output load capacitance	Tolerable load capacitance	10			pF

Table 10-4. Specification of an External Reference Signal for the Application Example Shown in Figure 10-4 on page 10

Parameter	Comment	Min.	Typ.	Max.	Units
Signal Characteristics					
Nominal Frequency			23.104		MHz
Waveform	Sinewave or clipped sinewave				
Amplitude	Voltage peak-to-peak	0.6	0.9	1.2	V

11. Demonstration Board

Figure 11-1. Schematic of Demonstration Board

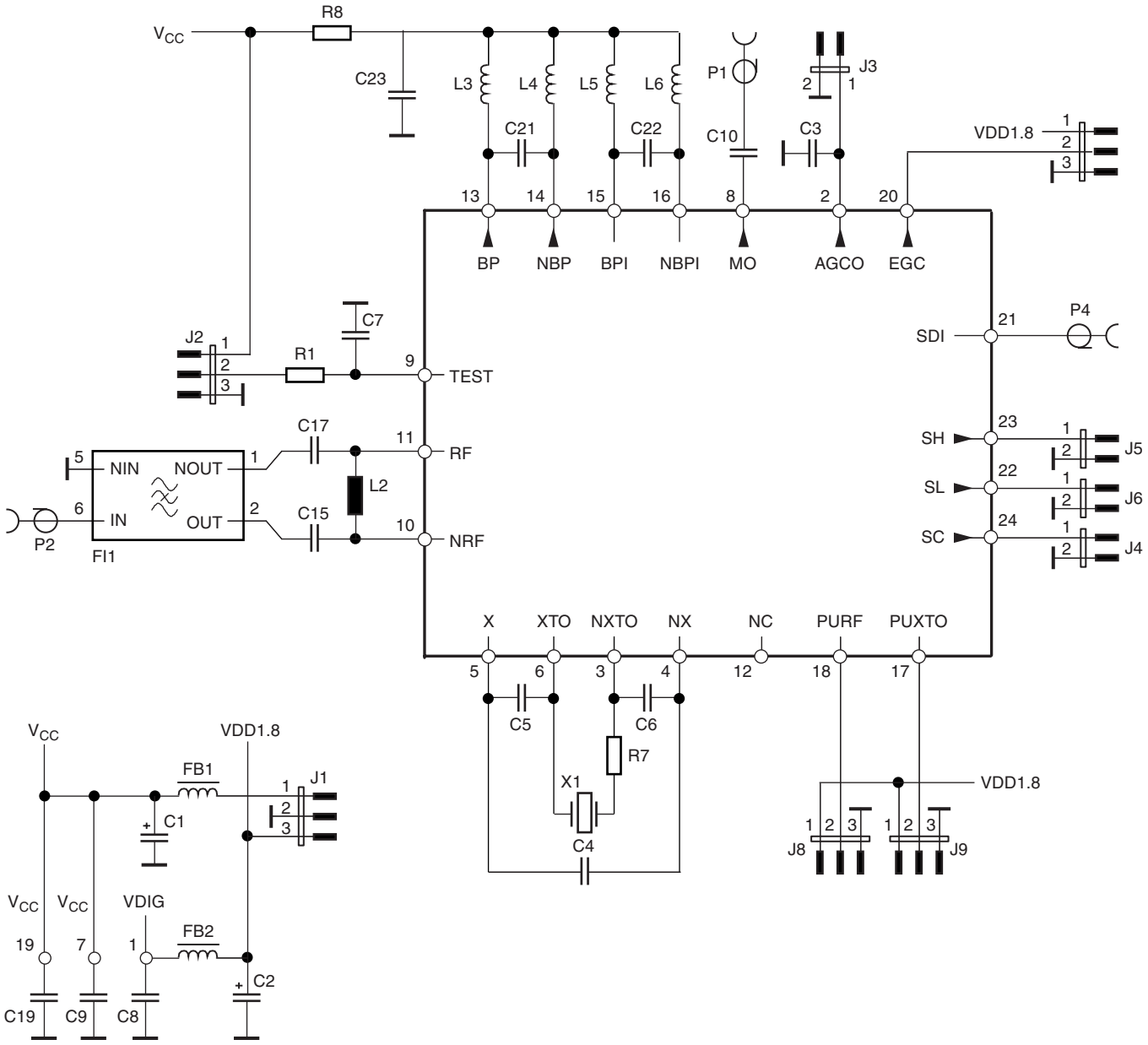


Figure 11-2. Illustration of Demonstration Board

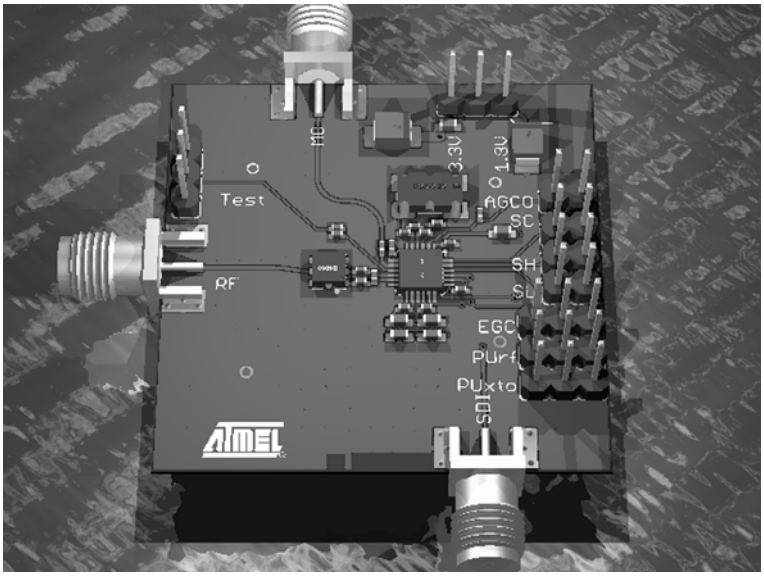
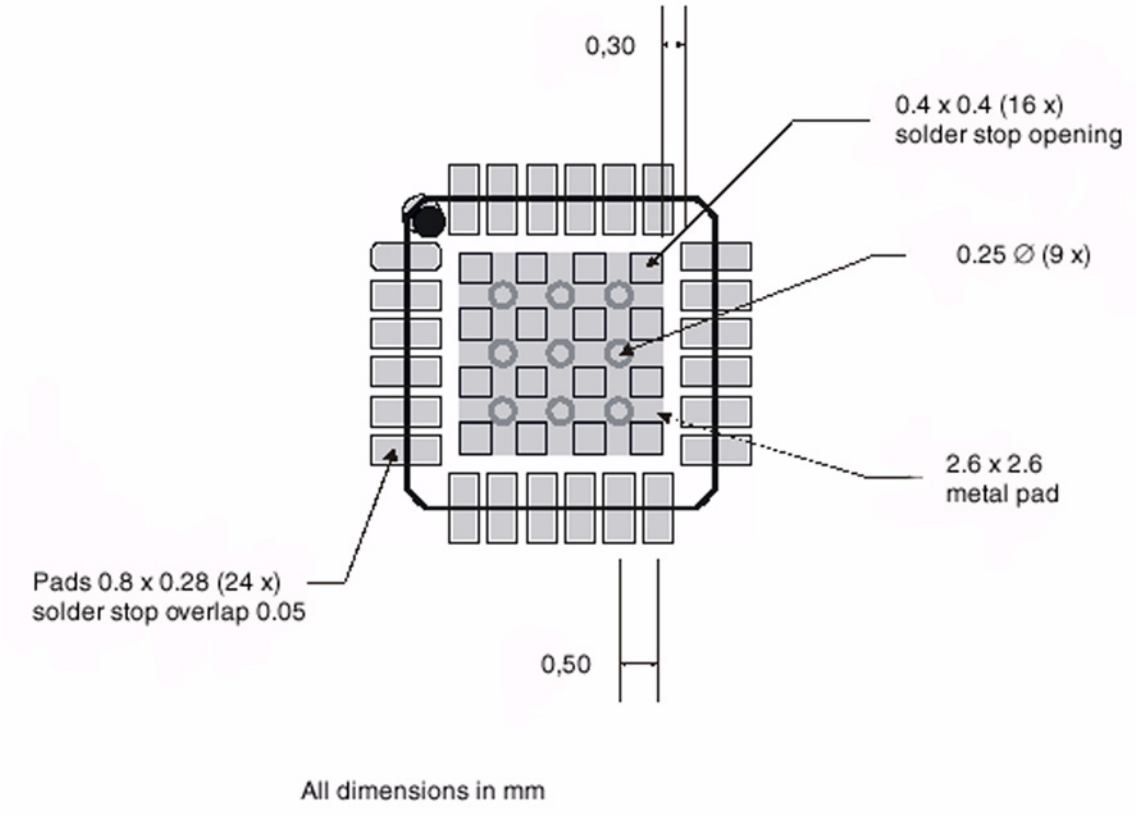


Table 11-1. BOM of Demonstration Board

Qty	Value	Device	Parts	Tolerance	Manufacturer	Mfr. Order Code
4		JP2E	J3, J4, J5, J6		Molex®	90120-0762
5		JP3E	J1, J2, J7, J8, J9		Molex	90120-0763
1	0	RESISTOR-0402	R1		Vishay®	CRCW0402000Z
1	68Ω	RESISTOR-0402	R8	5%	Vishay	CRCW040268RJ
1	2n2	CAPACITOR-0402	C3	5%	Vishay	VJ0402Y222JXJA
2	1p3	CAPACITOR-0402	C15, C17	0.1 pF	Taiyo Yuden®	EVK105CH1R3BW
1	5n6 2% Multilayer	INDUCTOR-0402	L2	2%	Würth® Elektronik	744784056G
2	5p0 ±0p1	CAPACITOR-0402	C21, C22	±0p1	Yageo America	0402CG509C9B200
2	10µ	ELKO-B	C1, C2	20%	Vishay	293D106X0016B2
1	4.7n	CAPACITOR-0402	C23	5%	Vishay	VJ0402Y472JXJA
1	27	RESISTOR-0402	R7	5%	Vishay	CRCW040227RJ
2	47p	CAPACITOR-0402	C5, C6	5%	Vishay	VJ0402A470JXXA.
1	82p	CAPACITOR-0402	C4		Vishay	VJ0402A820JXXA
4	100n	CAPACITOR-0402	C7, C8, C9, C19	5%	Vishay	VJ0402V104JXJ
1	100p	CAPACITOR-0402	C10	5%	Vishay	VJ0402A101JXXA.
3	142-0711-841	COAX-SMA	P1, P2, P4		Johnson Components™	142-0711-841
4	220n 2%	INDUCTOR_WIRE-WOUND-0603	L3, L4, L5, L6	2%	Würth Elektronik	744761222G
2	74279266	FERRITE_BEAD-0603	FB1, FB2		Würth Elektronik	74279266
1	ATR0601-1	ATR0601-1	IC1		Atmel®	ATR0601
1	B4060	FILTER-BALANCED	FI1		Epcos®	B4060
1	RSX-5 23.104 MHz	XTAL-4PIN-6035	X1		Rakon	XZC736 IEC19RSX-5 23.104 MHz

12. Recommended Footprint

Figure 12-1. Recommended Footprint (QFN24 - 4 mm × 4 mm)



13. Ordering Information

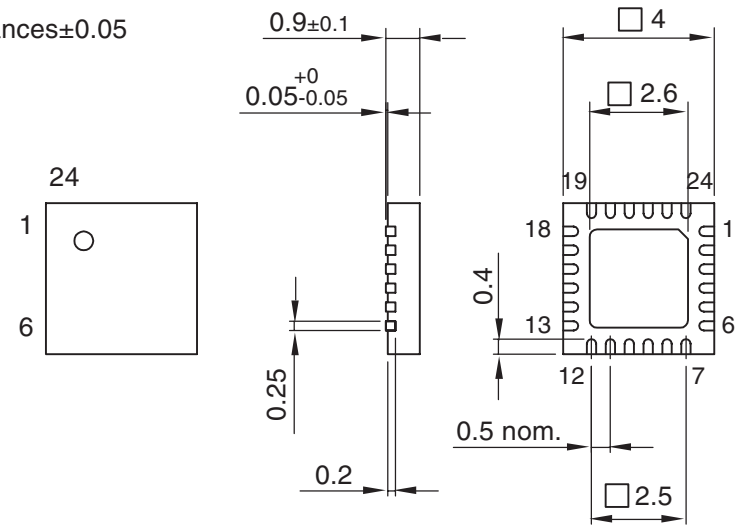
Extended Type Number	Package	Remarks
ATR0601-PFQW	QFN24, 4 × 4	Taped and reeled, Pb-free, RoHS compliant

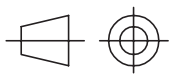
14. Package Information

Package: QFN 24 - 4 x 4
Exposed pad 2.6 x 2.6
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm

Not indicated tolerances±0.05





technical drawings
according to DIN
specifications

Drawing-No.: 6.543-5101.02-4

Issue: 2; 29.11.05

Moisture sensitivity level (MSL) = 2

15. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4866G-GPS-11/06	• Figure 10-1 “Application Example Using a GPS Crystal with ESR_{typ} = 12Ω” on page 9 changed”
4866F-GPS-06/06	• Figure 10-3 “Equivalent Application Examples Using a GPS TCXO” on page 10 changed • Table 10-3 “Specification of GPS TCXOs Appropriate for the Application Example” on page 12 changed • Table 10-4 “Specification of an External Reference Signal for the Application Example” on page 12 changed.

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