Atmel ATA6826C

Triple Half-bridge DMOS Output Driver with Serial Input Control

DATASHEET

Features

- Supply voltage up to 40V
- R_{DSon} typically 0.8Ω at 25°C, Maximum 1.5Ω at 150°C
- Up to 1.0A output current
- Three half-bridge outputs formed by three high-side and three low-side drivers
- Capable of switching all kinds of loads such as DC motors, bulbs, resistors, capacitors and inductors
- No shoot-through current
- Very low quiescent current I_S < 2µA in Standby Mode versus total temperature range
- Outputs short-circuit protected
- Overtemperature protection for each switch and overtemperature prewarning
- Undervoltage protection
- Various diagnostic functions such as shorted output, open-load, overtemperature and power-supply fail detection
- Serial data interface, Daisy Chain capable, up to 2MHz clock frequency
- SO14 power package

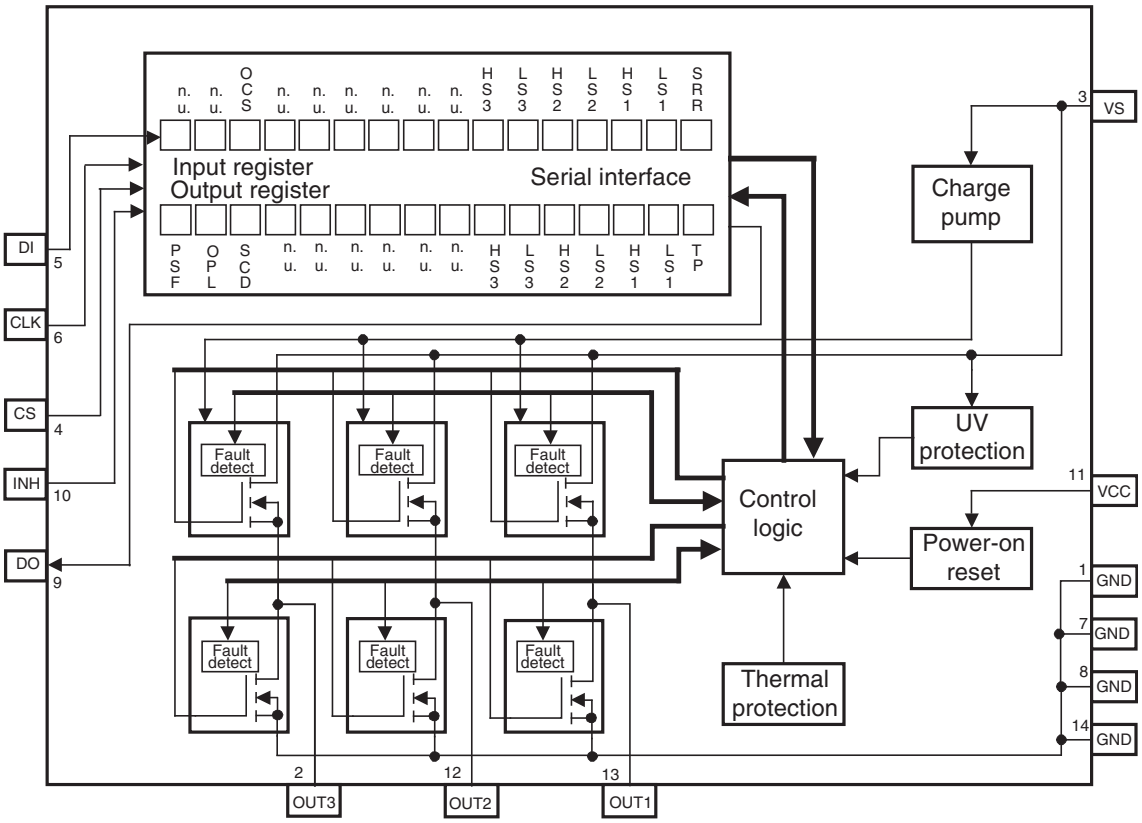
1. Description

The Atmel® ATA6826C is a fully protected Triple Half-bridge designed in Smart Power SOI Technology, used to control up to three different loads by a microcontroller in automotive and industrial applications.

Each of the three high-side and three low-side drivers is capable of driving currents up to 1.0A. The drivers are internally connected to form three half-bridges and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design especially supports the application of H-bridges to drive DC motors.

Protection is guaranteed regarding short-circuit conditions, overtemperature and undervoltage. Various diagnostic functions and a very low quiescent current in standby mode opens a wide range of applications. Automotive qualification gives added value and enhanced quality for exacting requirements of automotive applications.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO14

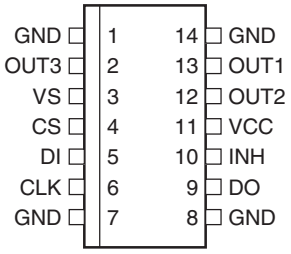


Table 2-1. Pin Description

Pin	Symbol	Function
1	GND	Ground; reference potential; internal connection to pin 7, 8 and 14; cooling tab
2	OUT3	Half-bridge output 3; formed by internally connected power MOS high-side switch 3 and low-side switch 3 with internal reverse diodes; short-circuit protection; overtemperature protection; diagnosis for short and open load
3	VS	Power supply for output stages OUT1, OUT2 and OUT3, internal supply
4	CS	Chip select input; 5V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
5	DI	Serial data input; 5V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
6	CLK	Serial clock input; 5V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register (f_{max} = 2MHz)
7	GND	Ground; see pin 1
8	GND	Ground; see pin 1
9	DO	Serial data output; 5V CMOS logic level tristate output for output (status) register data; sends 16-bit status information to the microcontroller (LSB is transferred first); output will remain tri-stated unless device is selected by CS = low, therefore, several ICs can operate on only one data output line.
10	INH	Inhibit input; 5V logic input with internal pull down; low = standby, high = normal operation
11	VCC	Logic supply voltage (5V)
12	OUT2	Half-bridge output 2; see pin 2
13	OUT1	Half-bridge output 1; see pin 2
14	GND	Ground; see pin 1

3. Functional Description

3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and is accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3-1. Data Transfer

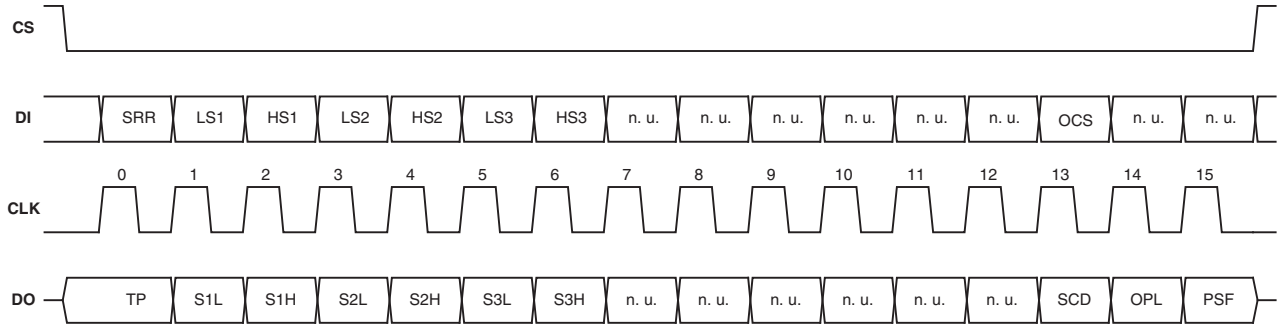


Table 3-1. Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, OPL and SCD in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
14	n. u.	Not used
15	n. u.	Not used

Table 3-2. Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning
1	Status LS1	High = output is on, low = output is off; not affected by SRR
2	Status HS1	High = output is on, low = output is off; not affected by SRR
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	SCD	Short circuit detected: set high when at least one high-side or low-side switch is switched off by a short-circuit condition. Bits 1 to 6 can be used to detect the shorted switch.
14	OPL	Open load detected: set high, when at least one active high-side or low-side switch sinks/sources a current below the open load threshold current.
15	PSF	Power-supply fail: undervoltage at pin VS detected

After power-on reset, the input register has the following status:

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
x	x	H	x	x	x	x	x	x	L	L	L	L	L	L	L

The following patterns are used to enable internal test modes of the IC. It is not recommended to use these patterns during normal operation.

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	H	H	L	L	L	L	L	L	L

3.2 Power-supply Fail

In case of undervoltage at pin VS, the Power-Supply Fail bit (PSF) in the output register is set and all outputs are disabled. To detect an undervoltage, its duration has to be longer than the undervoltage detection delay time t_{dUV}. The outputs are enabled immediately when supply voltage recovers to a normal operating value. The PSF bit stays high until it is reset by the SRR (Status Register Reset) bit in the input register.

3.3 Open-load Detection

If the current through a high-side or low-side switch in the ON-state stays below the open-load detection threshold, the open-load detection bit (OPL) in the output register is set.

The OPL bit stays high until it is reset by the SRR bit in the input register. To detect an open load, its duration has to be longer than the open-load detection delay time t_{dSd}.

3.4 Overtemperature Protection

If the junction temperature of one or more output stages exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word. The status of TP is available at pin DO with the falling edge of CS. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the status of input and output registers.

If the junction temperature of one or more output stages exceeds the thermal shutdown threshold, $T_{j\ switch\ off}$, all outputs are disabled and the corresponding bits in the output register are set to low. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{jswitch\ on}$ and the SRR bit in the input register is set to high. Hysteresis of thermal pre-warning and shutdown threshold avoids oscillations.

3.5 Short-circuit Protection

The output currents are limited by a current regulator. Overcurrent detection is activated by writing a high to the OCS (Overcurrent Shutdown) bit in the input register. When the current in an output stage exceeds the overcurrent limitation and shutdown threshold, it is switched off after a delay time (t_{dSd}). The short-circuit detection bit (SCD) is set and the corresponding status bit in the output register is set to low. For OCS = low the overcurrent shutdown is inactive. The SCD bit is also set if the current exceeds the overcurrent limitation and shutdown threshold, but the outputs are not affected. By writing a high to the SRR bit in the input register the SCD bit is reset and the disabled outputs are enabled.

3.6 Inhibit

Applying 0V to pin 10 (INH) inhibits the Atmel® ATA6826C.

All output switches are then turned off and switched to tri-state. The data in the output register is deleted. The current consumption is reduced to less than 2µA at pin VS and less than 25µA at pin VCC. The output switches can be activated again by switching pin 10 (INH) to 5V which initiates an internal power-on reset.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins.

Parameters	Pin	Symbol	Value	Unit
Supply voltage	3	V_{VS}	–0.3 to +40	V
Supply voltage t < 0.5s; I_S > –2A	3	V_{VS}	–1	V
Logic supply voltage	11	V_{VCC}	–0.3 to +7	V
Logic input voltage	4 to 6, 10	V_{CS},V_{DI}, V_{CLK}, V_{INH}	–0.3 to V_{VCC} + 0.3	V
Logic output voltage	9	V_{DO}	–0.3 to V_{VCC} + 0.3	V
Input current	4 to 6, 10	I_{CS},I_{DI}, I_{CLK}, I_{INH}	–10 to +10	mA
Output current	9	I_{DO}	–10 to +10	mA
Output current	2, 12 and 13	I_{Out3}, I_{Out2}, I_{Out1}	Internally limited, see output specification	
Output voltage	2, 12 and 13	I_{Out3}, I_{Out2}, I_{Out1}	–0.3 to +40	V
Reverse conducting current (t_{pulse} = 150µs)	2, 12 and 13 towards pin 3	I_{Out3}, I_{Out2}, I_{Out1}	17	A
Junction temperature range		T_J	–40 to +150	°C
Storage temperature range		T_{STG}	–55 to +150	°C

5. Thermal Resistance

Parameters	Test Conditions	Symbol	Value	Unit
Junction pin	Measured to GND Pins 1, 7, 8 and 14	R_{thJP}	30	K/W
Junction ambient		R_{thJA}	65	K/W

6. Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_{VS}	V_{UV}[1] to 40	V
Logic supply voltage	V_{VCC}	4.75 to 5.25	V
Logic input voltage	V_{CS},V_{DI}, V_{CLK}, V_{INH}	–0.3 to V_{VCC}	V
Serial interface clock frequency	f_{CLK}	2	MHz
Junction temperature range	T_j	–40 to +150	°C

Note: Threshold for undervoltage detection

7. Noise and Surge Immunity

Parameters	Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Interference suppression	VDE 0879 Part 2	Level 5
ESD (Human Body Model); pins 2, 12, 13 vs. GND ESD (Human Body Model), all other pins	HBM: AEC-Q100-002-Ref-D CEI/IEC 60749-26:2006 ESDA/JEDEC JS-001-2010	8kV 5kV
CDM (Charged Device Model)	ANSI/ESD S5.3.1-2009	1kV
MM (Machine Model)	AEC Q100-003-REV-E ANSI/ESD S5.2-2009	250V

Note: Test pulse 5: V_{smax} = 40V

8. Electrical Characteristics

7.5V < V_{VS} < 40V; 4.75V < V_{VCC} < 5.25V; INH = High; –40°C < T_j < 150° C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	Current Consumption								
1.1	Quiescent current VS	V_{VS} < 20V, INH = low	3	I_{VS}		1	2	µA	A
1.2	Quiescent current VCC	4.75V < V_{VCC} < 5.25V, INH = low	11	I_{VCC}		15	25	µA	A
1.3	Supply current VS	V_{VS} < 20V normal operating, all outputs off	3	I_{VS}		4	6	mA	A
1.4	Supply current VCC	4.75V < V_{VCC} < 5.25V, normal operating	11	I_{VCC}		350	500	µA	A
1.5	Discharge current VS	V_{VS} = 32.5V, INH = low	3	I_{VS}	0.5		5.5	mA	A
1.6	Discharge current VS	V_{VS} = 40V, INH = low	3	I_{VS}	2.5		10	mA	A
2	Undervoltage Detection, Power-on Reset								
2.1	Power-on reset threshold		11	V_{VCC}	3.2	3.9	4.4	V	A
2.2	Power-on reset delay time	After switching on V_{CC}		t_{dPor}	30	95	190	µs	A
2.3a	Undervoltage-detection threshold (down)	V_{CC} = 5V	3	V_{Uv}	5.6		6.5	V	A
2.3b	Undervoltage-detection threshold (up)	V_{CC} = 5V	3	V_{Uv}	6.0		7.0	V	A
2.4	Undervoltage-detection hysteresis	V_{CC} = 5V	3	ΔV_{Uv}		0.6		V	A
2.5	Undervoltage-detection delay time			t_{dUV}	10		40	µs	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of the input signal at pin CS after data transmission and switch on output stages to 90% of final level. Device not in standby for t > 1ms

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.75V < V_{VCC} < 5.25V; INH = High; –40°C < T_j < 150° C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3	Thermal Prewarning and Shutdown								
3.1	Thermal prewarning set			$T_{jPW\ set}$	120	145	170	°C	B
3.2	Thermal prewarning reset			$T_{jPW\ reset}$	105	130	155	°C	B
3.3	Thermal prewarning hysteresis			ΔT_{jPW}		15		°C	B
3.4	Thermal shutdown off			$T_{j\ switch\ off}$	150	175	200	°C	B
3.5	Thermal shutdown on			$T_{j\ switch\ on}$	135	160	185	°C	B
3.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$		15		K	B
3.7	Ratio thermal shutdown off/thermal prewarning set			$T_{j\ switch\ off}$/ $T_{jPW\ set}$	1.05	1.2			B
3.8	Ratio thermal shutdown on/thermal prewarning reset			$T_{j\ switch\ on}$/ $T_{jPW\ reset}$	1.05	1.2			B
4	Output Specification (OUT1-OUT3)								
4.1	On resistance	$I_{Out\ 1-3}$ = –0.9A	2, 12, 13	$R_{DSOn1-3}$		0.8	1.5	Ω	A
4.2		$I_{Out\ 1-3}$ = +0.9A	2, 12, 13	$R_{DSOn1-3}$		0.8	1.5	Ω	A
4.3	High-side output leakage current	$V_{Out\ 1-3}$ = 0V, output stages off	2, 12, 13	I_{Out1-3}	–15			µA	A
4.4	Low-side output leakage current	$V_{Out\ 1-3}$ = V_{VS}, output stages off	2, 12, 13	I_{Out1-3}			200	µA	A
4.5	High-side switch reverse diode forward voltage	$I_{Out\ 1-3}$ = 1.5A	2, 12, 13	$V_{Out1-3} – V_{VS}$			2	V	A
4.6	Low-side switch reverse diode forward voltage	$I_{Out\ 1-3}$ = –1.5A	2, 12, 13	$V_{Out\ 1-3}$	–2			V	A
4.7	High-side overcurrent limitation and shutdown threshold	7.5V < V_S < 20V 20V ≤ V_S < 40V	2, 12, 13	I_{Out1-3}	–1.7 –2.0	–1.3 –1.3	–1.0 –1.0	A A	A
4.8	Low-side overcurrent limitation and shutdown threshold	7.5V < V_S < 20V 20V ≤ V_S < 40V	2, 12, 13	I_{Out1-3}	1 1	1.3 1.3	1.7 2.0	A A	A
4.9	Overcurrent shutdown delay time			t_{dSd}	10		40	µs	A
4.10	High-side open-load detection threshold		2, 12, 13	I_{Out1-3}	–50	–30	–10	mA	A
4.11	Low-side open-load detection threshold		2, 12, 13	I_{Out1-3}	10	30	50	mA	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of the input signal at pin CS after data transmission and switch on output stages to 90% of final level. Device not in standby for t > 1ms

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.75V < V_{VCC} < 5.25V; INH = High; –40°C < T_j < 150° C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.12	Open-load detection delay time			t_{dSd}	200		600	µs	A
4.13	High-side output switch on delay(1)	V_{VS} = 13V R_{Load} = 30Ω		t_{don}			20	µs	A
4.14	Low-side output switch on delay(1)	V_{VS} = 13V R_{Load} = 30Ω		t_{don}			20	µs	A
4.15	High-side output switch off delay(1)	V_{VS} = 13V R_{Load} = 30Ω		t_{doff}			20	µs	A
4.16	Low-side output switch off delay(1)	V_{VS} = 13V R_{Load} = 30Ω		t_{doff}			3	µs	A
4.17	Dead time between corresponding high- and low-side switches	V_{VS} = 13V R_{Load} = 30Ω		$t_{don} - t_{doff}$	1			µs	A
5	Logic Inputs DI, CLK, CS, INH								
5.1	Input voltage low-level threshold		4-6, 10	V_{IL}	0.3 × V_{VCC}			V	A
5.2	Input voltage high-level threshold		4-6, 10	V_{IH}			0.7 × V_{VCC}	V	A
5.3	Hysteresis of input voltage		4-6, 10	ΔV_I	50		700	mV	B
5.4	Pull-down current pin DI, CLK, INH	V_{DI}, V_{CLK}, V_{INH} = V_{CC}	5, 6, 10	I_{PD}	10		65	µA	A
5.5	Pull-up current pin CS	V_{CS} = 0V	4	I_{PU}	–65		–10	µA	A
6	Serial Interface – Logic Output DO								
6.1	Output-voltage low level	I_{DOL} = 2mA	9	V_{DOL}			0.4	V	A
6.2	Output-voltage high level	I_{DOL} = –2mA	9	V_{DOH}	V_{VCC} – 0.7V			V	A
6.3	Leakage current (tri-state)	V_{CS} = V_{CC} 0V < V_{DO} < V_{VCC}	9	I_{DO}	–10		10	µA	A
7	Inhibit Input - Timing								
7.1	Delay time from standby to normal operation			t_{dINH}			100	µs	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of the input signal at pin CS after data transmission and switch on output stages to 90% of final level. Device not in standby for t > 1ms

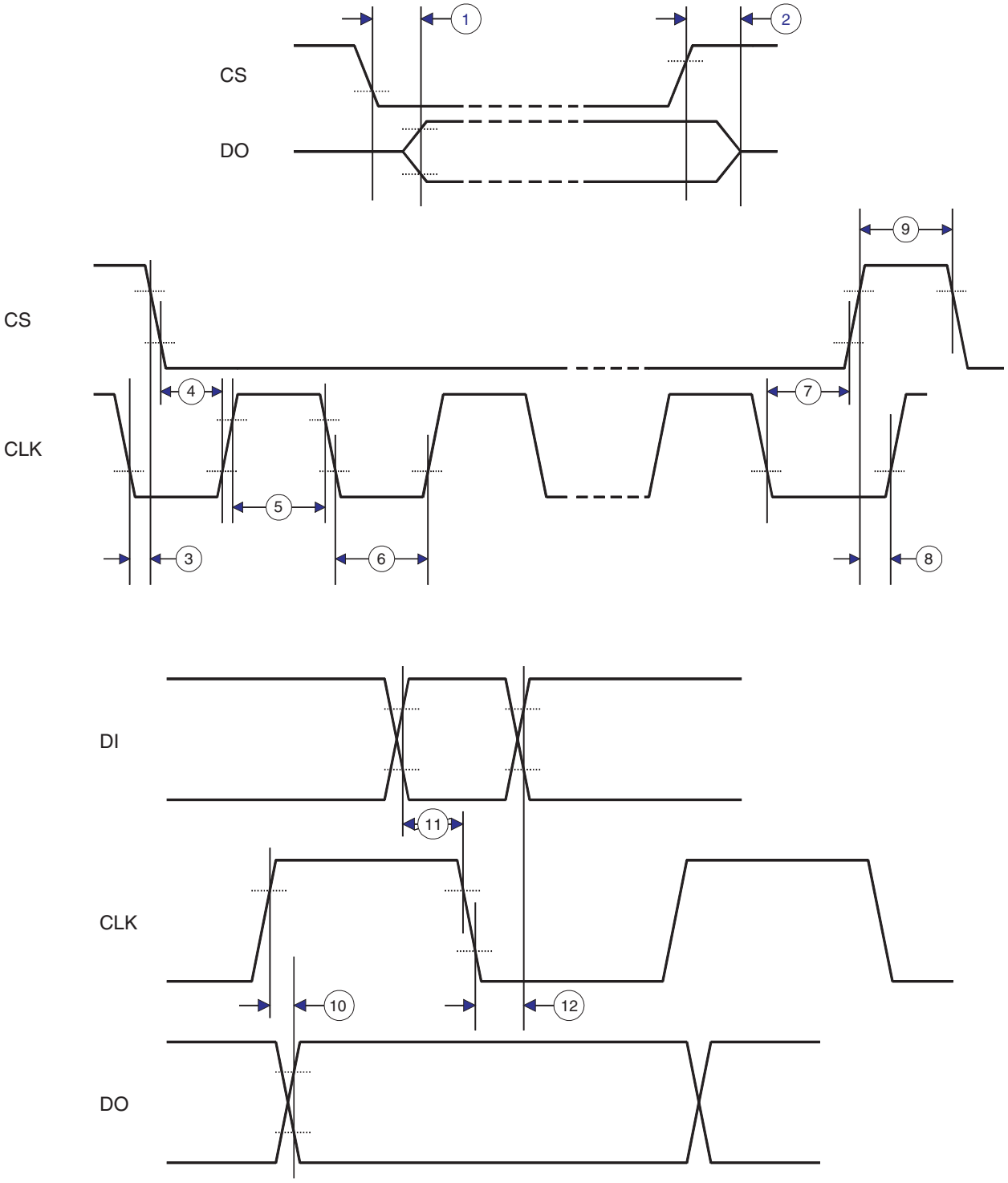
9. Serial Interface – Timing

No.	Parameters	Test Conditions	Pin	Timing Chart No.[1]	Symbol	Min.	Typ.	Max.	Unit	Type*
8.1	DO enable after CS falling edge	C_{DO} = 100pF	9	1	t_{ENDO}			200	ns	D
8.2	DO disable after CS rising edge	C_{DO} = 100pF	9	2	t_{DISDO}			200	ns	D
8.3	DO fall time	C_{DO} = 100pF	9	-	t_{DOf}			100	ns	D
8.4	DO rise time	C_{DO} = 100pF	9	-	t_{DOr}			100	ns	D
8.5	DO valid time	C_{DO} = 100pF	9	10	t_{DOVal}			200	ns	D
8.6	CS setup time		4	4	$t_{CSSethl}$	225			ns	D
8.7	CS setup time		4	8	$t_{CSSetlh}$	225			ns	D
8.8	CS high time		4	9	t_{CSh}	500			ns	D
8.9	CLK high time		6	5	t_{CLKh}	225			ns	D
8.10	CLK low time		6	6	t_{CLKl}	225			ns	D
8.11	CLK period time		6	-	t_{CLKp}	500			ns	D
8.12	CLK setup time		6	7	$t_{CLKSethl}$	225			ns	D
8.13	CLK setup time		6	3	$t_{CLKSetlh}$	225			ns	D
8.14	DI setup time		5	11	t_{DIset}	40			ns	D
8.15	DI hold time		5	12	t_{DIHold}	40			ns	D

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. See Figure 9-1 on page 12 “Serial Interface Timing with Chart Numbers”

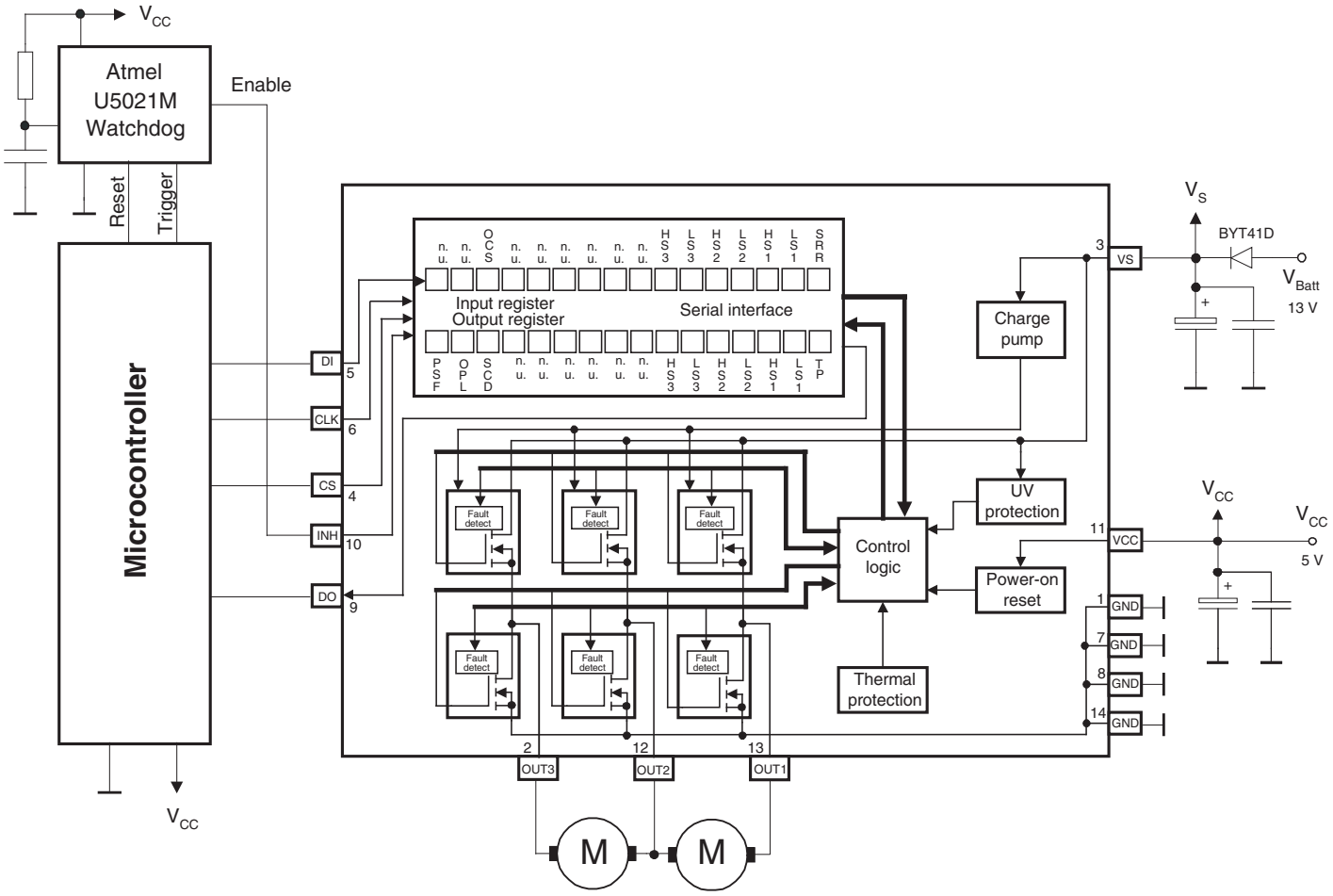
Figure 9-1. Serial Interface Timing with Chart Numbers



Inputs DI, CLK, CS: High level = 0.7 × V_{CC}, low level = 0.3 × V_{CC}
Output DO: High level = 0.8 × V_{CC}, low level = 0.2 × V_{CC}

10. Application Circuit

Figure 10-1. Application Circuit



11. Application Notes

It is strongly recommended to connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S:

Electrolytic capacitor C > 22µF in parallel with a ceramic capacitor C = 100nF. The value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current $I_{Out1,2,3}$ (see “Absolute Maximum Ratings” on page 7).

Recommended value for capacitors at V_{CC}:

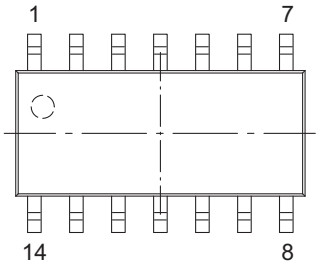
Electrolytic capacitor C > 10µF in parallel with a ceramic capacitor C = 100nF.

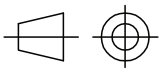
To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to the GND pins.

12. Ordering Information

Extended Type Number	Package	Remarks
ATA6826C-TUQY	SO14	Power package, taped and reeled, lead-free

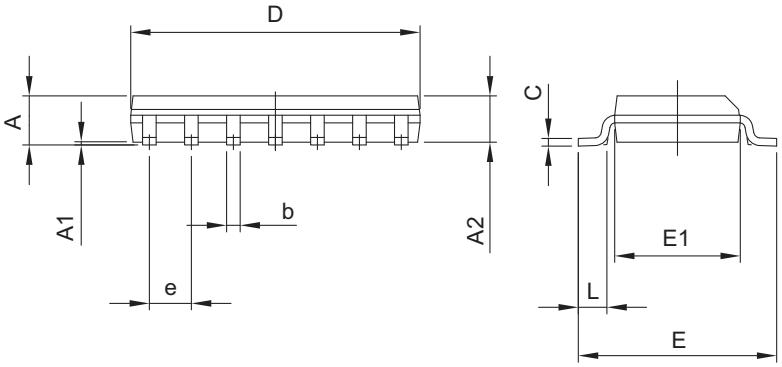
13. Package Information





technical drawings
according to DIN
specifications

Dimensions in mm



Note[1]: Dimensions “D” and “E1” do not include Moldflash or protrusion.
(MAX. 0.15mm per side)

Bemerkung: ASE

COMMON DIMENSIONS (Unit of Measure = mm)			
Symbol	**MIN**	**NOM**	**MAX**
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.38	1.50
b	0.33	0.42	0.51
C	0.19	0.22	0.25
D[1)]	8.55	8.65	8.75
E[1)]	3.80	3.90	4.00
E	5.80	6.00	6.20
e		1.27 BSC	
L	0.40	0.84	1.27

04/13/12

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Package: SO14**		6.541-5053.01-4	1

14. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9213D-AUTO-09/12	• Section 7 “Noise and Surge Immunity” on page 8 changed
9213C-AUTO-05/12	• Section 13 “Package Information” on page 14 changed
9213B-BCD-01/11	• Section 3.6 “Inhibit” on page 6 changed

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