

# **AT91CAP9-STK Starter Kit**

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## **User Guide**







## Table of Contents

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### Section 1

Introduction.....	1-1
1.1 Purpose.....	1-1
1.2 CAP™ Starter Kit Board .....	1-1
1.3 CAP Starter Kit Development Tools.....	1-2
1.4 Related Documents .....	1-2
1.4.1 Standards .....	1-2
1.4.2 Reference Documents.....	1-2
1.5 Glossary.....	1-3

---

### Section 2

Requirements .....	2-1
2.1 General Description .....	2-1
2.2 Interface and Function General Overview .....	2-2
2.3 External Interfaces.....	2-4
2.3.1 EI1: External Lithium-ion Battery .....	2-4
2.3.2 EI2: 5VAC/DC Sector Adapter.....	2-4
2.3.3 EI3: RMII 10/100 Base-T Ethernet.....	2-4
2.3.4 EI4: Serial Port, Connected to the Debug Unit .....	2-4
2.3.5 EI5: SD Card Slot .....	2-5
2.3.6 EI6: Two USB Host Interfaces .....	2-5
2.3.7 EI7: USB High Speed Device Interface .....	2-5
2.3.8 EI8: 1/4 VGA LCD Panel with Touch Screen.....	2-6
2.3.9 EI9: Audio Stereo Headset .....	2-7
2.3.10 EI10: Analog Inputs .....	2-7
2.3.11 EI11: JTAG and Serial Configuration Interfaces.....	2-7
2.3.12 EI12: Manganese-Lithium Coin Battery .....	2-8
2.3.13 EI13: 64-lead Extension Connector for the AT91CAP9 I/O Lines .....	2-9
2.3.14 EI14: Two 64-lead Extension Connectors for the FPGA I/O Lines .....	2-10
2.4 Characteristics .....	2-12
2.4.1 Functional Characteristics .....	2-12
2.4.2 Physical Characteristics.....	2-29

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### Section 3

Board Strap and Switch Configuration .....	3-1
3.1 Connectors 1x2.....	3-1
3.2 Connectors 1x3.....	3-2

3.3 Switches..... 3-3

---

**Section 4**

AT91CAP9-STK Schematics .....4-1  
4.1 This section contains the following appended schematics..... 4-1

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**Section 5**

Revision History .....5-1  
5.1 Revisioin Hisory ..... 5-1





# Section 1

## Introduction

### 1.1 Purpose

This document is a presentation of the hardware associated with the AT91CAP9-STK<sup>®</sup> Starter Kit.

This product is derived from the Atmel AT91CAP9-MZ and AT91CAP9-MB demonstration boards.

### 1.2 CAP<sup>™</sup> Starter Kit Board

The AT91CAP9-STK Starter Kit is built on a single PCB, including:

- AT91CAP9S ARM926EJ-S<sup>™</sup> -based microcontroller system-on-chip
- 64M Bytes of SDRAM application memory
- 512M Bytes of NAND Flash
- DataFlash<sup>®</sup> with up to 8M Bytes
- External interfaces for:
  - 10/100 Base-T Ethernet
  - USB Host and Full Speed/High Speed Device
  - ¼ VGA LCD Panel with Touch Screen
  - SD Card
  - 4 analog inputs
  - audio headphones
- Altera<sup>®</sup> Stratix<sup>®</sup>2 EP2S15F484 FPGA and its associated EPCS16 serial configuration memory. The FPGA provides 15600 four-input Lookup Table (LUT) equivalents, corresponding to approximately 124800 gates in the CAP MP Block.
- 64 general-purpose I/O connections from the AT91CAP9S, and 2 banks of 64 I/Os from the FPGA, for application-specific external interfaces
- CE-JTAG interface for CAP9 JTAG programming, and a USB-Blaster-JTAG interface for Stratix2 JTAG programming. These facilitate system debug.
- Atmel's AT73C224 and AT73C239 ICs for power supply and battery management.
- Atmel's AT73C213 for audio DAC
- Atmel's AT73C205 for battery charger

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## 1.3 CAP Starter Kit Development Tools

The CAP Starter Kit is supplied with an essential set of development tools in order to get started immediately. These include:

- KickStart™ version of IAR™ Embedded Workbench® for ARM®
- Microsoft® Windows CE® Board Support Package and demonstration from Adeneo
- Instructions for downloading Altera's free Quartus® 2 Web Edition tools for FPGA programming

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## 1.4 Related Documents

### 1.4.1 Standards

JTAG IEEE® 1149.1 Standard.

### 1.4.2 Reference Documents

**Table 1-1.** Reference Documents

Description	Reference
Evaluation motherboard ORCAD schematics	20061027_11H20_AT91CAP9.dsn
Evaluation motherboard BOM	20061212_BOMASSY_ID2400_MOTHERBOARD.xls
Evaluation mezzanine board ORCAD schematics	20061122_09H00_AT91CAP9_MEZ.dsn
Evaluation mezzanine board BOM	20061207_ID2399_BOMASSY_MEZZANINE.xls
Atmel Specification	New Specification CAP9 Starter Kit
CAP9-STK hardware description.doc	ref. 4658D03
CAP9-STK ORCAD schematics	ref. ADEC101389001
CAP9-STK BOM	ref. ADEC101389003
CAP9-STK equipment plan	ref. ADEC101389EQ2

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## 1.5 Glossary

BOM	Bill Of Materials
ICE	In-Circuit Emulator
JTAG	Joint Test Action Group
CAP	Customizable Microcontroller-based SoC Platform
CAP9-STK	CAP9 Starter Kit
FPGA	Field Programmable Gate Array
I/O	Input/Output
MCI	Multimedia Card Interface
MPB	Metal Programmable Block
MPIO	Metal Programmable I/O
NC	Not Connected
OHCI	Open Host Controller Interface
PLL	Phase Locked Loop
PMC	Power Management Circuit



## Section 2

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# Requirements

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### 2.1 General Description

The CAP9-STK's objective is to provide a rapid evaluation of the AT91CAP9 product and its derivatives. It does not allow a full emulation of a customized version of the CAP9, but is intended to familiarize the user with the customization concept and architecture of the CAP9.

It also demonstrates the operations of the analog companions provided by Atmel's AT73C family of products and the availability of the operating systems and software layers.



## 2.2 Interface and Function General Overview

AT91CAP9-STK interfaces and functions are as follows:

(Refer also to [Figure 2-1 on page 2-3.](#))

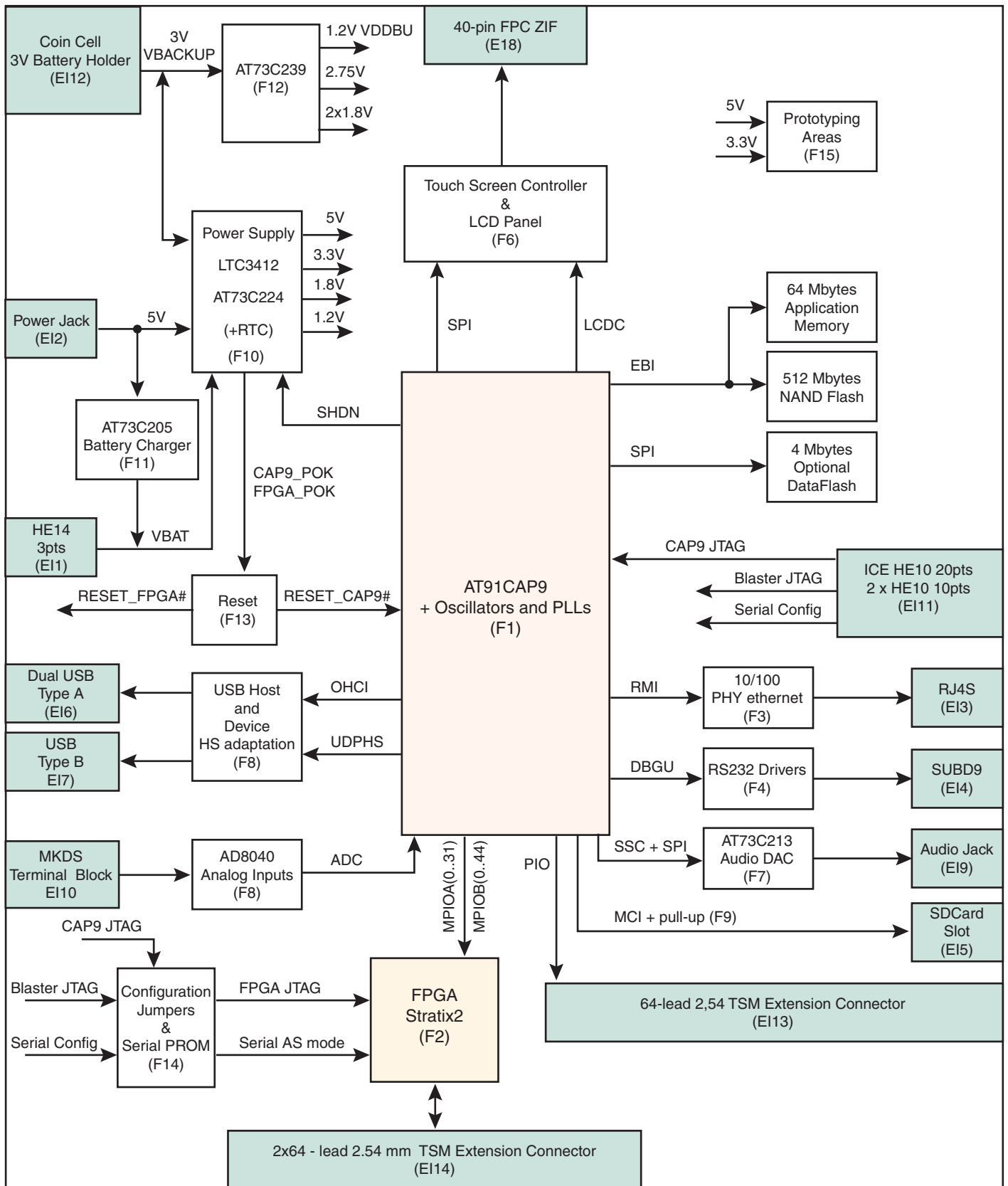
### Interface

- EI1: 1 external Lithium-Ion battery
- EI2: 5V AC/DC sector adapter
- EI3: 1 RMII 10/100 Base-T Ethernet
- EI4: 1 Serial port, connected to the Debug Unit
- EI5: 1 SD Card slot
- EI6: 2 USB HOST interface
- EI7: 1 USB High Speed Device interface
- EI8: ¼ VGA LCD panel with Touch Screen
- EI9: 1 Audio stereo headset
- EI10: 4 Analog inputs
- EI11: 2 JTAG and 1 serial configuration interfaces
- EI12: 1 Manganese-Lithium coin battery
- EI13: 64-lead extension connector for the CAP9 I/O lines
- EI14: Two 64-lead extension connectors for the FPGA I/O lines

### Function

- F1: AT91CAP9 microcontroller
- F2: FPGA and MPIO bus
- F3: RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX.
- F4: RS232 driver
- F5: USB Host and Device
- F6: Touch screen controller and LCD panel
- F7: Audio DAC
- F8: Analog Inputs adaptation
- F9: SD Card
- F10: Power supplies and low power mode
- F11: Battery charger
- F12: RTC and Backup
- F13: Reset configuration
- F14: Programming and configuration
- F15: Prototyping Area

Figure 2-1. AT91CAP9-STK Interface and Function Overview



## 2.3 External Interfaces

### 2.3.1 EI1: External Lithium-ion Battery

The AT91CAP9-STK board implements one external Li-Ion battery 3-pin HE14 type connector..

**Table 2-1.** HE 14-3 Pinout

Pin	Signal Name	Description	Type	Level
1	VBAT	Battery power	I/O	4,5V
2	GND	Electrical ground	O	-
3	BAT_TS	Thermistor temperature sense	I	4,5V

### 2.3.2 EI2: 5VAC/DC Sector Adapter

CAP9-STK board implements one RAPC722 Switchcraft right angle miniature power jack with the following electrical characteristics:

- Contact resistance: 30 mΩ max
- Current carrying capability: 5A

### 2.3.3 EI3: RMII 10/100 Base-T Ethernet

An RJ45 8-pin Integrated Magnetics Connector is implement for the 10/100 Base-T Ethernet interface.

The connector integrates a 1 nF capacitor for HF shielding of the signal with chassis ground. (External connection between chassis and electrical ground is possible too.)

**Table 2-2.** RJ45-8 Pinout

Pin	Signal Name	Description	Type
1	TX+	Positive differential emission	O
2	TX-	Negative differential emission	O
3	RX+	Positive differential reception	I
6	RX-	Negative differential reception	I
4, 5, 7, 8	NC	-	-

### 2.3.4 EI4: Serial Port, Connected to the Debug Unit

A Debug right angle SUBD-9 connector is available in order to communicate with the AT91CAP9 micro-controller debug unit. This port is an electrical RS232 type connection. The connector integrates 2 additional pins (10, 11) for signal shielding.

**Table 2-3.** SUBD-P Pinout

Pin	Signal Name	Description	Type	Level
2	RXD	RS232 receive	I	±30V
3	TXD	RS232 transmit	O	±5V to ±5.2V
5, 10, 11	GND	Electrical ground	-	-
1, 4, 6, 7, 8, 9	NC	-	-	-

### 2.3.5 EI5: SD Card Slot

The AT91CAP9-STK board implements a 12-pin short type SDCARD slot on the bottom side.

**Table 2-4.** SD CARD Pinout

Pin	Signal Name	Description	Type	Level
1	MCI_DA3	Data 3	I/O	3.3V
2	MCI_CDA	Command/response	I/O open-drain	3.3V
3	GND	Electrical ground	-	-
4	3V3	3.3V power supply	O	3.3V
5	MCI_CK	Clock	O	3.3V
6	GND	Electrical ground	-	-
7	MCI_DA0	DATA 0	I/O	3.3V
8	MCI_DA1	DATA 1	I/O	3.3V
9	MCI_DA2	DATA 2	I/O	3.3V
10	MCI_CD	Card Detect	I	3.3V
11	GND	Electrical ground	-	-
12	NC	-	-	-

### 2.3.6 EI6: Two USB Host Interfaces

Two USB HOST connectors are available on a sign dual-port Type A connector.

**Table 2-5.** Dual-port Type A Connector Pinout

Pin	Signal Name	Description	Type
A1	5V	5V power supply (fuse 500mA)	O
A2	HDMA	Negative differential port A	I/O
A3	HDP A	Positive differential port A	I/O
A4	GND	Electrical ground	-
B1	5V	5V power supply (fuse 500mA)	O
B2	HDMB	Negative differential port B	I/O
B3	HDPB	Positive differential port B	I/O
B4	GND	Electrical ground	-
1 to 4	GND	Electrical ground	-

### 2.3.7 EI7: USB High Speed Device Interface

One USB Device High/Full Speed connector is available on a Type B connector.

**Table 2-6.** Type B Connector Pinout

Pin	Signal Name	Description	Type	Level
1	VBUS	<small>Dr supply</small>	I	1
2	HSDM / FSDM	Negative differential port A	I/O	2
3	HSDP / FSDP	Positive differential port A	I/O	3
4, 5, 6	GND	Electrical	-	4, 5, 6

## Requirements

### 2.3.8 EI8: 1/4 VGA LCD Panel with Touch Screen

The AT91CAP9-STK board implements a 0.5 FPC, 40-pin ZIF LCD Panel connector, with contact on the bottom side. The connector integrates two additional pins (MC1, MC2) for signal shielding.

**Table 2-7.** 40-pin ZIF Connector Pinout

Pin	Signal Name	Description	Type	Level
1	3V3	3.3V power supply	O	3.3V
2	3V3	3.3V power supply	O	3.3V
3	3V3	3.3V power supply	O	3.3V
4	LCDDOTCK	Dot clock	O	3.3V
5	GND	Electrical ground	-	-
6	LCDHSYNC	Horizontal synchronization pulse	O	3.3V
7	GND	Electrical ground	-	-
8	LCDDEN	Timing signal for data	O	3.3V
9	GND	Electrical ground	-	-
10	NC	-	-	-
11	GND	Electrical ground	-	-
12	LCDD7	RED data 5	O	3.3V
13	LCDD6	RED data 4	O	3.3V
14	LCDD5	RED data 3	O	3.3V
15	GND	Electrical ground	-	-
16	LCDD4	RED data 2	O	3.3V
17	LCDD3	RED data 1	O	3.3V
18	LCDD2	RED data 0	O	3.3V
19	GND	Electrical ground	-	-
20	LCDD15	GREEN data 5	O	3.3V
21	LCDD14	GREEN data 4	O	3.3V
22	LCDD13	GREEN data 3	O	3.3V
23	GND	Electrical ground	-	-
24	LCDD12	GREEN data 2	O	3.3V
25	LCDD11	GREEN data 1	O	3.3V
26	LCDD10	GREEN data 0	O	3.3V
27	GND	Electrical ground	-	-
28	LCDD23	BLUE data 5	O	3.3V
29	LCDD22	BLUE data 4	O	3.3V
30	LCDD21	BLUE data 3	O	3.3V
31	GND	Electrical ground	-	-
32	LCDD20	BLUE data 2	O	3.3V
33	LCDD19	BLUE data 1	O	3.3V
34	LCDD18	BLUE data 0	O	3.3V
35	PCI	Power control	O	3.3V



**Table 2-7.** 40-pin ZIF Connector Pinout (Continued)

Pin	Signal Name	Description	Type	Level
36	VCTRL	LED current control	O	3.3V
37	Y_UP	Touch panel upper side	O	3.3V
38	X_LEFT	Touch panel left side	O	3.3V
39	Y_LOW	Touch panel low side	O	3.3V
40	X_RIGHT	Touch panel right side	O	3.3V

### 2.3.9 EI9: Audio Stereo Headset

A headset audio interface connector is available for a 3.5 phone jack stereo plug.

SMT 1503-03 Lumberg is used.

### 2.3.10 EI10: Analog Inputs

The AT91CAP9-STK board implements a 3.81mm-pitch Phoenix MKDS 6-pin terminal block. This connector receives four analog inputs.

**Table 2-8.** MKDS 6-pin Terminal Block Pinout

Pin	Signal Name	Description	Type	Level
1	ANALOG_I1	Analog input 1	I	3.3V
2	ANALOG_I2	Analog input 2	I	3.3V
3	ANALOG_I3	Analog input 3	I	3.3V
4	ANALOG_I4	Analog input 4	I	3.3V
5	GND	Electrical ground	-	-
6	NC (3V3)	- (It can be connected to 3.3V by 0Ω strap)	- (O)	- (3.3V)

### 2.3.11 EI11: JTAG and Serial Configuration Interfaces

Two programming JTAG interfaces and one serial configuration device interface are available on the board.

#### 2.3.11.1 ICE-JTAG Interface

One ICE-JTAG interface is a right angle male, HE10 2x10-pin connector, to receive CAP9 ICE debugger probe for CAP9 JTAG programming.

**Table 2-9.** HE10 2x10-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	3V3	3.3V power supply	O	3.3V
3	NTRST	Test Reset	I	3.3V (active low)
5	TDI	Test Data In	I	3.3V
7	TMS	Test Mode Select	I	3.3V
9	TCK	Test Clock	I	3.3V
11	RTCK	Returned Test Clock	O	3.3V
13	TDO	Test Data Out	O	3.3V

## Requirements

**Table 2-9.** HE10 2x10-pin Connector Pinout (Continued)

Pin	Signal Name	Description	Type	Level
15	NRST	Microcontroller Reset	I/O	3.3V (active low)
17, 19	NC	-	-	-
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	Electrical ground	-	-

### 2.3.11.2 USB-Blaster-JTAG Interface

One USB-Blaster-JTAG interface is a straight male, HE10 2x5-pin connector, to receive the Altera FPGA USB Blaster probe for Stratix2 JTAG programming.

**Table 2-10.** HE10 2x5-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	TCK	Test Clock	I	3.3V
3	TDO	Test Data Out	O	3.3V
5	TMS	Test Mode Select	I	3.3V
9	TDI	Test Data In	I	3.3V
4, 6	3V3	3.3V power supply	O	3.3V
7, 8	NC	-	-	-
2, 10	GND	Electrical ground	-	-

### 2.3.11.3 Serial Configuration Device Interface

The serial configuration device interface is a straight male, HE10 2x5-pin connector, to receive the Altera FPGA USB Blaster probe for serial EPCS Device programming.

**Table 2-11.** HE10 2x5-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	DCLK	Configuration Clock pin	O	3.3V
3	CONF_DONE	Configuration Status pin	I/O	3.3V open-drain
5	nCONFIG	Configuration Control input	I	3.3V
6	nCE	Configuration Chip enable	I	3.3V (active low)
7	DATA0	Configuration Data input	I	3.3V
8	nCSO	Configuration Chip select	O	3.3V
9	ASDO_FPGA	Configuration Read enable	O	3.3V
4	3V3	3.3V power supply	O	3.3V
2, 10	GND	Electrical ground	-	-

### 2.3.12 EI12: Manganese-Lithium Coin Battery

The AT91CAP9-STK board implements a coin cell battery holder for 12 mm rechargeable 3V Manganese-Lithium coin battery, Panasonic ML1220 type.

**3V non-rechargeable Lithium coin batteries are not supported.**



### 2.3.13 EI13: 64-lead Extension Connector for the AT91CAP9 I/O Lines

A straight male, 2.54 mm-pitch, 64-pin connector is available on the board as a CAP9 extension connector.

**Table 2-12.** 64-pin Connector Pinout

Pin	Signal Name	Level	Pin	Signal Name	Level
1	5V	5V	2	5V	5V
3	5V	5V	4	GND	-
5	GND	-	6	GND	-
7	3V3	3.3V	8	3V3	3.3V
9	PA2/SPI0_SPCK	3.3V	10	GND	-
11	GND	-	12	PA0/SPI0_MISO	3.3V
13	PA9	3.3V	14	GND	-
15	GND	-	16	PA1/SPI0_MOSI	3.3V
17	PD1/SPI0_NPCS3	3.3V	18	PD0	3.3V
19	GND	-	20	3V3	3.3V
21	TWCK	3.3V open-drain	22	PA10/IRQ0	3.3V
23	GND	-	24	PA14/IRQ1	3.3V
25	TWD	3.3V open-drain	26	PA22/TXD0	VDDIOP1
27	PA24/RTS0	VDDIOP1	28	PA23/ RXD0	VDDIOP1
29	GND	-	30	PB12/SPI1_MISO	3.3V
31	PA27/PCK1	VDDIOP1	32	PB13/SPI1_MOSI	3.3V
33	VDDIOP1	3.3V or 1.8V	34	GND	-
35	PA26	VDDIOP1	36	PB14/SPI1_SPCK	3.3V
37	PA29	VDDIOP1	38	GND	-
39	PA30	VDDIOP1	40	PB15/SPI1_NPCS0	3.3V
41	PA31	VDDIOP1	42	PB16/SPI1_NPCS1	3.3V
43	VDDIOP1	3.3V or 1.8V	44	3V3	3.3V
45	GND	-	46	3V3	3.3V
47	PC12	3.3V	48	PC29	3.3V
49	PC13	3.3V	50	GND	-
51	PD2	3.3V	52	PD5/DMARQ2	3.3V
53	PC3	3.3V	54	GND	-
55	GND	-	56	PD6/NWAIT	1.8V
57	PD8/NCS5	1.8V	58	PD7/NCS4	1.8V
59	PD10/SCK1	1.8V	60	PD9/SCK2	1.8V
61	PD13/A24	1.8V	62	PD12/A23	1.8V
63	PD14 / A25	1.8V	64	1V8_CAP9	1,8V



## Requirements

### 2.3.14 EI14: Two 64-lead Extension Connectors for the FPGA I/O Lines

Two straight male, 2.54 mm-pitch, 64-pin connectors are available on the board as FPGA extension connectors.

The pinouts for both FPGA connectors are given in [Table 2-13](#) and [Table 2-14](#)

**Table 2-13.** 64-pin Connector Pinout and Bank Assignment

Pin	FPGA IO/Power Name	Bank	Pin	FPGA IO/Power Name	Bank
1	GND	-	2	VCCIO4	BANK4
3	FPGA_IO0	BANK4	4	VCCIO4	BANK4
5	FPGA_IO1	BANK4	6	FPGA_IO2	BANK4
7	FPGA_IO3	BANK4	8	FPGA_IO4	BANK4
9	FPGA_IO5	BANK4	10	GND	-
11	FPGA_IO6	BANK4	12	FPGA_IO7	BANK4
13	FPGA_IO8	BANK4	14	FPGA_IO9	BANK4
15	FPGA_IO10	BANK4	16	FPGA_IO11	BANK4
17	FPGA_IO12	BANK4	18	FPGA_IO13	BANK4
19	GND	-	20	FPGA_IO14	BANK4
21	FPGA_IO15	BANK4	22	FPGA_IO16	BANK4
23	FPGA_IO17	BANK4	24	FPGA_IO18	BANK4
25	FPGA_IO19	BANK4	26	FPGA_IO20	BANK4
27	FPGA_IO21	BANK4	28	GND	-
29	FPGA_IO22	BANK4	30	FPGA_IO23	BANK4
31	FPGA_IO24	BANK4	32	FPGA_IO25	BANK4
33	FPGA_IO26	BANK4	34	FPGA_IO27	BANK4
35	GND	-	36	FPGA_IO28	BANK6
37	FPGA_IO29	BANK6	38	FPGA_IO30	BANK6
39	FPGA_IO31	BANK6	40	FPGA_IO32	BANK6
41	FPGA_IO33	BANK6	42	FPGA_IO34	BANK6
43	FPGA_IO35	BANK6	44	FPGA_IO36	BANK6
45	FPGA_IO37	BANK6	46	GND	-
47	FPGA_IO38	BANK6	48	FPGA_IO39	BANK6
49	FPGA_IO40	BANK6	50	FPGA_IO41	BANK6
51	FPGA_IO42	BANK6	52	FPGA_IO43	BANK6
53	FPGA_IO44	BANK6	54	FPGA_IO45	BANK6
55	GND	-	56	FPGA_IO46	BANK6
57	FPGA_IO47	BANK6	58	FPGA_IO48	BANK6
59	FPGA_IO49	BANK6	60	FPGA_IO50	BANK6
61	VCCIO6	BANK6	62	FPGA_IO51	BANK6
63	VCCIO6	BANK6	64	GND	-

Table 2-14. 64-pin Connector Pinout and Bank Assignment

Pin	FPGA IO/Power Name	Bank	Pin	FPGA IO/Power Name	Bank
1	GND	-	2	VCCIO6	BANK6
3	FPGA_IO	BANK6	4	VCCIO6	BANK6
5	FPGA_IO	BANK6	6	FPGA_IO	BANK6
7	FPGA_IO	BANK6	8	FPGA_IO	BANK6
9	FPGA_IO	BANK6	10	GND	-
11	FPGA_IO	BANK7	12	FPGA_IO	BANK7
13	FPGA_IO	BANK7	14	FPGA_IO	BANK7
15	FPGA_IO	BANK7	16	FPGA_IO	BANK7
17	FPGA_IO	BANK7	18	FPGA_IO	BANK7
19	GND	-	20	FPGA_IO	BANK7
21	FPGA_IO	BANK7	22	VCCIO7	BANK7
23	FPGA_IO	BANK7	24	VCCIO7	BANK7
25	FPGA_IO	BANK7	26	FPGA_IO	BANK7
27	FPGA_IO	BANK7	28	GND	-
29	FPGA_IO	BANK7	30	FPGA_IO	BANK7
31	FPGA_IO	BANK7	32	FPGA_IO	BANK7
33	FPGA_IO	BANK7	34	FPGA_IO	BANK7
35	FPGA_IO	BANK7	36	FPGA_IO	BANK7
37	GND	-	38	FPGA_IO	BANK7
39	FPGA_IO	BANK7	40	FPGA_IO	BANK7
41	FPGA_IO	BANK7	42	FPGA_IO	BANK7
43	VCCIO8	BANK8	44	FPGA_IO	BANK7
45	VCCIO8	BANK8	46	GND	-
47	FPGA_IO	BANK8	48	FPGA_IO	BANK8
49	FPGA_IO	BANK8	50	FPGA_IO	BANK8
51	FPGA_IO	BANK8	52	FPGA_IO	BANK8
53	FPGA_IO	BANK8	54	FPGA_IO	BANK8
55	GND	-	56	FPGA_IO	BANK8
57	FPGA_PLLOUTp	3.3V	58	GND	-
59	GND	-	60	FPGA_IO	BANK8
61	FPGA_PLLOUTn	3.3V	62	GND	-
63	GND	-	64	3V3	3.3V

## 2.4 Characteristics

### 2.4.1 Functional Characteristics

#### 2.4.1.1 F1: AT91CAP9 Microcontroller

The AT91CAP9-STK microcontroller core block implements the necessary digital-system core functions. It's composed of the following elements:

- One 32-bit-ARM9® AT91CAP9 microcontroller core and its power supplies (see below).
- One 1.8V, 512 Mbytes, 8-bit NAND Flash,
- One 1.8V, 64 Mbytes, 32-bit SDRAM Application Volatile Memory
- One optional 3.3V DataFlash® memory from 512 Kbytes to 8 Mbytes
- One Debug and JTAG Test unit (See “F14: Programming and Configuration” on page 2-27.)
- One MPB

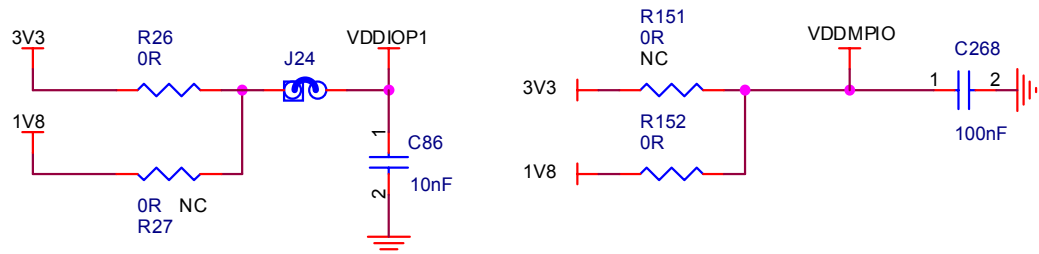
##### 2.4.1.1.1 AT91CAP9 Power Supplies

The power supply of the AT91CAP9 Microcontroller is shown below.

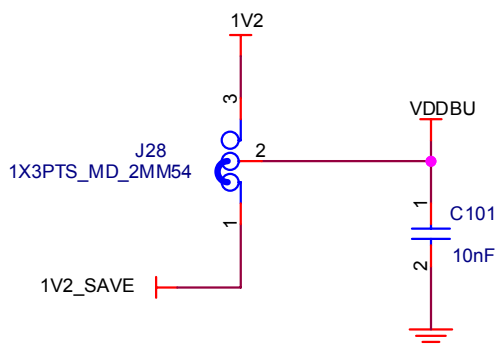
**Table 2-15.** AT91CAP9 Power Supply

Power Supply Name	Power Supply
VDDCORE	1V2_CAP9
VDDPLL	3V3
VDDUPLL	1V2_CAP9 (RC filtered)
VDDUTMII	3V3
VDDIOP0	3V3
VDDIOP1	3V3 or 1V8_CAP9
VDDUTMIC	1V2_CAP9
VDDIOM	1V8
VDDMPIO	3V3 or 1V8_FPGA
VDDBU	1V2_SAVE or 1V2_CAP9
VDDANA	3V3 filtered
VREFP	VREFP (3V)

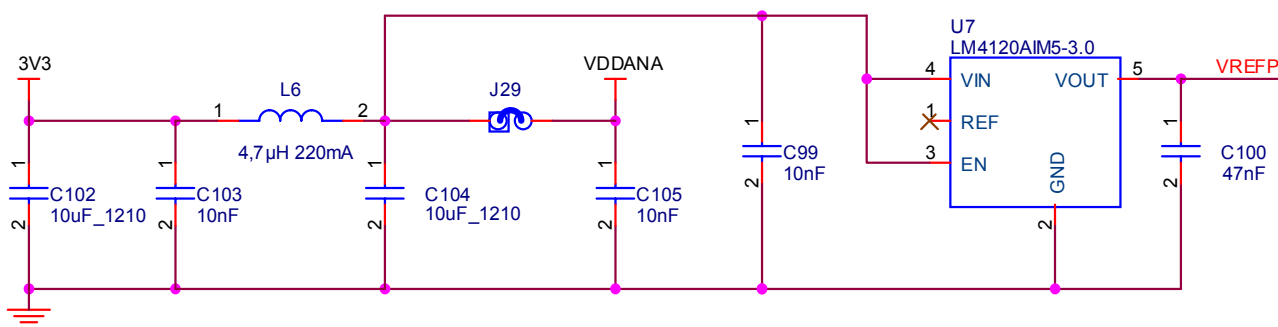
- For VDDIOP1 and VDDMPIO, the choice is made by 0Ω resistors:



- For VDDBU, the choice is made by a jumper on the 3-pin J28 connector:



- The implementation of VDDANA and VREFP is shown below.



#### 2.4.1.1.2 AT91CAP9 Clocks

The internal clocks of the AT91CAP9 are generated by two external quartz sources:

- 12 Mhz quartz for the MAINCK internal clock
- 32,768 kHz quartz for the SLCK internal slow clock

#### 2.4.1.2 F2: FPGA and MPIO Bus

##### 2.4.1.2.1 FPGA Characteristics

This function is performed by an Altera Stratix2, EP2S15F484 FPGA and its EPCS16 serial configuration device.

Stratix2 EP2S,15F484 FPGA characteristics are:

- 15600 equivalent LE (LE is four-input LUT-based architecture),
- 1.2V core power supply, 3.3V or 1.8V I/O bank power supplies,
- 484-pin FBGA,
- -5 speed grade.

The FPGA aims to emulate the logic to be implemented in the MPB through 5 metal layers.

The FPGA also manages the EI14 interface.

## Requirements

### 2.4.1.2.2 MPIO Bus Characteristics

The FPGA is connected to the AT91CAP9 microcontroller through the two MPIO buses:

- First MPIO bus: MPIOA[0:31], connected to FPGA bank 1
- Second MPIO bus: MPIOB[0:44], connected to FPGA banks 2 and 5
- Bus frequency: 100MHz
- Dedicated MPIO bus clock: MPIOB24

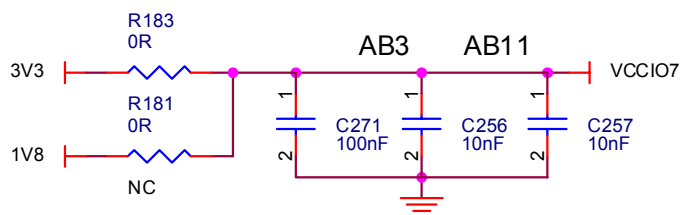
### 2.4.1.2.3 FPGA Power Supplies

**Table 2-16.** FPGA Bank Power Supplies

Bank 1	VDDMPIO (default 1V8_FPGA)
Bank 2	VDDMPIO (default 1V8_FPGA)
Bank 3	3V3
Bank 4	VCCIO4 (default 3V3)
Bank 5	VDDMPIO (default 1V8_FPGA)
Bank 6	VCCIO6 (default 1V8_FPGA)
Bank 7	VCCIO7 (default 3V3)
Bank 8	VCCIO8 (default 3V3)
Bank 9	3V3
Bank 10	3V3

Power for VDDMPIO, VCCIO4, VCCIO6, VCCIO7, and VCCIO8 can be supplied either by 3V3 or 1V8 (1V8\_CAP9) power supplies. (See “F10: Power Supplies and Low-power Mode” on page 2-22.)

Choice is made by 0Ω resistor as shown below (VCCIO7 example):



Each of the six FPGA PLL blocks have two power supply pins: VCCA\_PPLw and VCCD\_PPLx (x = from 0 to 5).

**Table 2-17.** FPGA PLL Block Power Supply

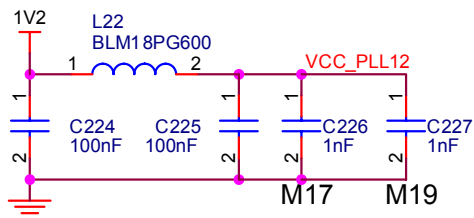
PLL Supply Pin Name	Power Supply
VCCA_PPL1	VCC_PLL12
VCCA_PPL2	VCC_PLL12
VCCA_PPL3	VCC_PLL34
VCCA_PPL4	VCC_PLL34
VCCA_PPL5	VCC_PLL56



**Table 2-17.** FPGA PLL Block Power Supply (Continued)

PLL Supply Pin Name	Power Supply
VCCA_PPL6	VCC_PLL56
VCCD_PPL1	1V2_CAP9
VCCD_PPL2	1V2_CAP9
VCCD_PPL3	1V2_CAP9
VCCD_PPL4	1V2_CAP9
VCCD_PPL5	1V2_CAP9
VCCD_PPL6	1V2_CAP9

VCC\_PLL12, VCC\_PLL34, VCC\_PLL56 are 1V2 (1V2\_CAP9) ferrite isolated power supplies as shown below (VCC\_PLL12 example):



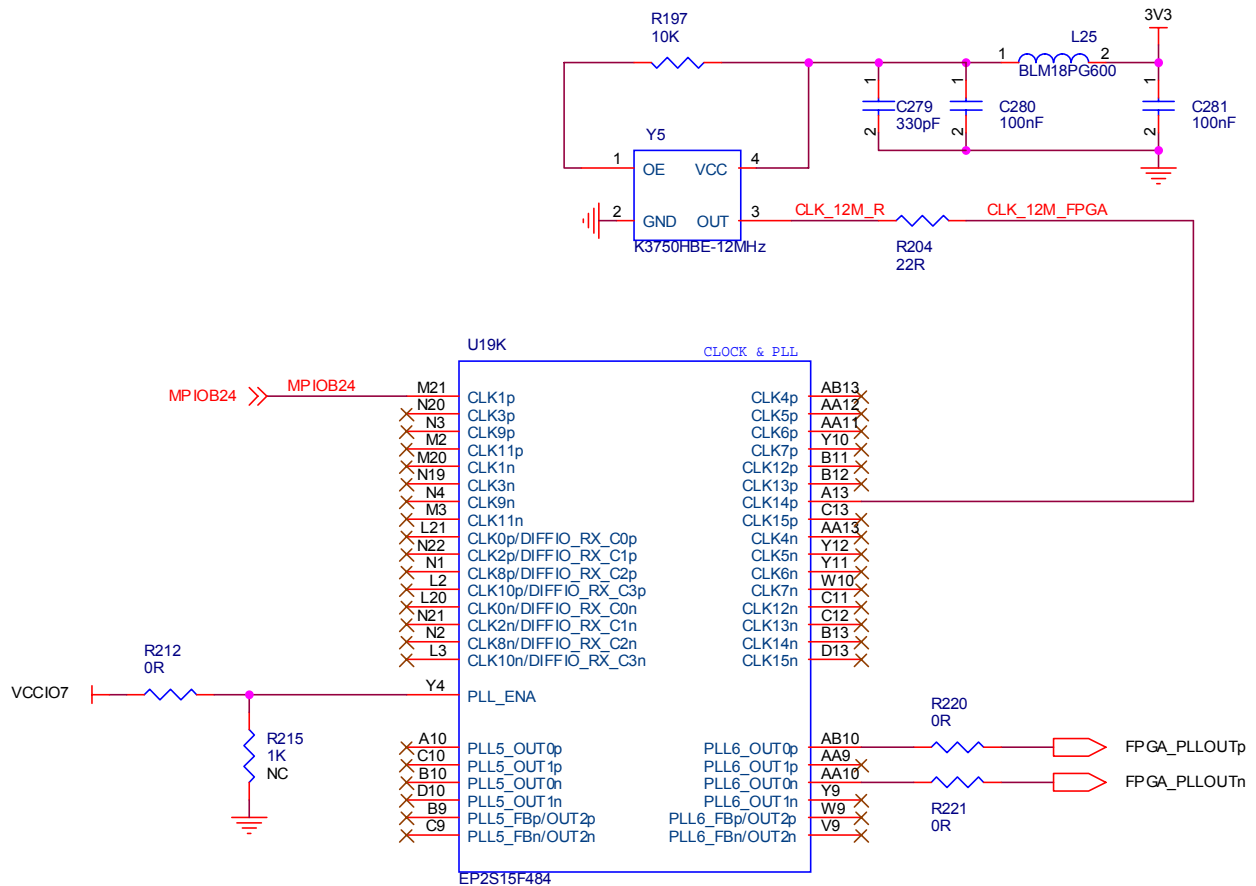
## Requirements

### 2.4.1.2.4 FPGA Clock

The MPIO Bus clock MPIOB24 is connected to the CLK1p clock input pin of the FPGA. An additional external 12 MHz oscillator generates clock to the CLK14p clock input pin of the FPGA.

Spare clock PLL\_OUTp and PLL\_OUTn are connected to the EI14 interface.

FPGA clock part electrical connection is shown below.

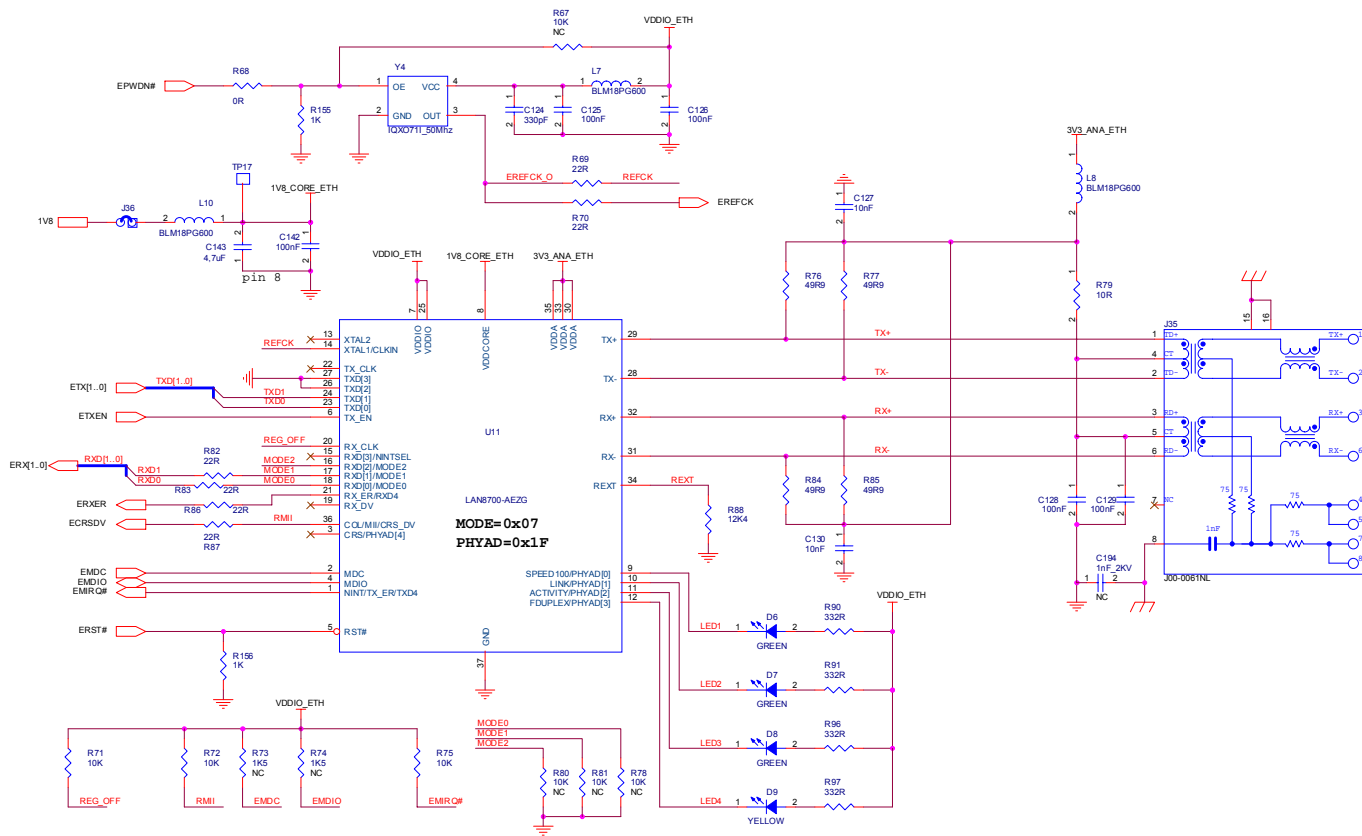


2.4.1.3 F3: RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX

The 10/100 Ethernet MAC function is implemented in the AT91CAP9 EMAC module.

This module manages an RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX (SMSC LAN8700) to implement a 10/100 Base-T Ethernet port.

The implementation is shown below.



The 1.8V power supply is external by default, to minimize 3.3V power consumption.

Use of LAN8700 3.3V/1.8V internal regulator can be done by disconnected J36 and R71 REG\_OFF Pull-up.



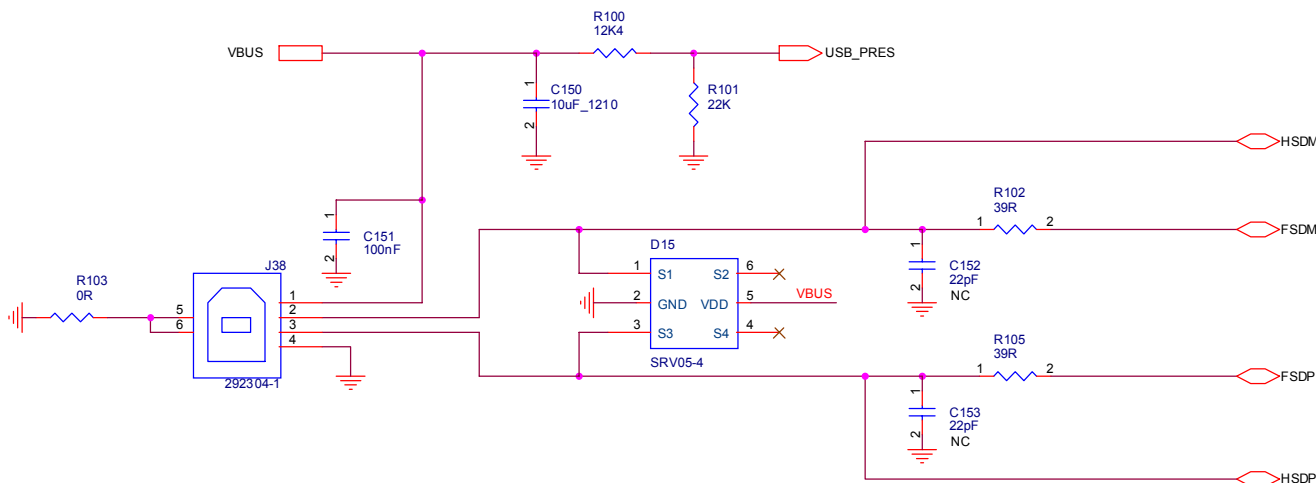


### 2.4.1.5.2 USB High Speed Device

The USB v2.0 High Speed Device interface is managed by the AT91CAP9 USB High Speed Device port compliant with the USB rev 2.0 High Speed device specification.

**The necessary 1.5kΩ Pull-up to 3.3V on HSDP (and FSDP) is included in the AT91CAP9 USB device port.**

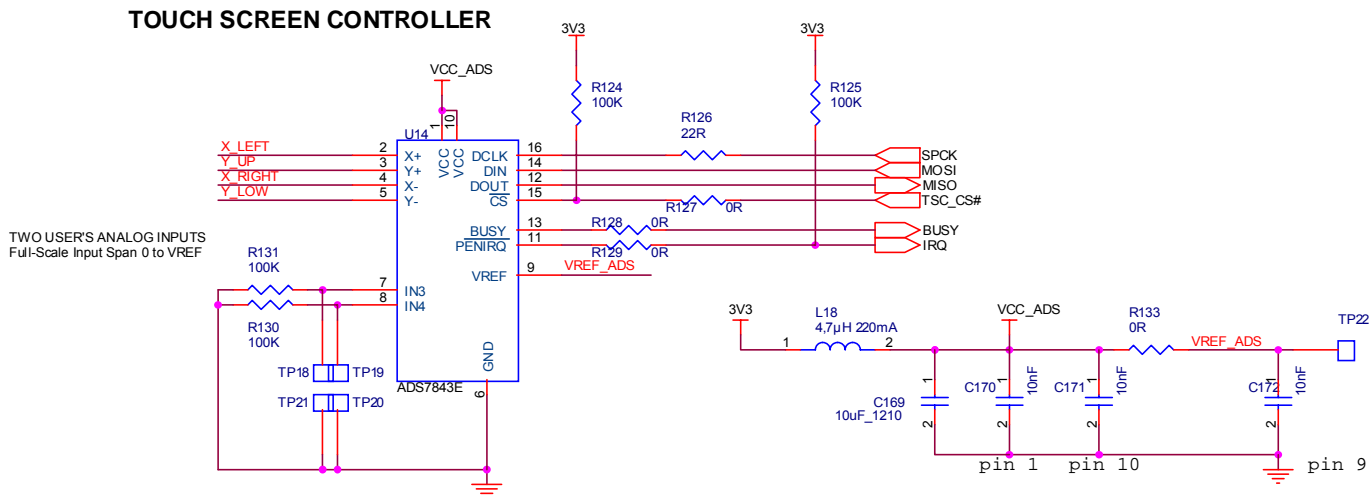
The implementation is shown below:



### 2.4.1.6 F6: Touch Screen Controller and LCD Panel

An ADS7843E touch screen controller is implemented on the board. It's controlled by the AT91CAP9 SPI0 bus, with SPI0\_NPCS1 chip select.

The figure below, derived from the AT91SAM9261-EK schematics, shows the implementation:



The LCD panel controlled the AT91CAP9 LCD Controller.

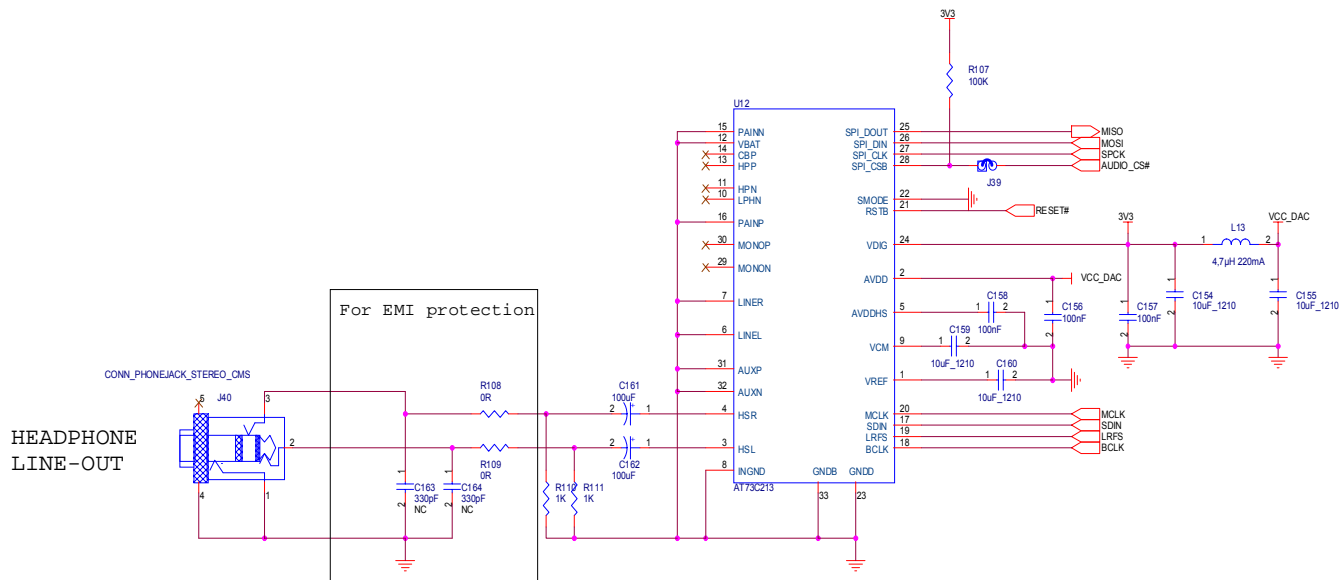


## Requirements

### 2.4.1.7 F7: Audio DAC

The AT73C213 DAC is used for the I<sup>2</sup>S audio output. It's controlled by the AT91CAP9 SPI0 bus, with SPI0\_NPCS2 chip select. I<sup>2</sup>S DAC dedicated serial interface is managed by AT91CAP9 SCC0 bus.

The implementation is shown below:



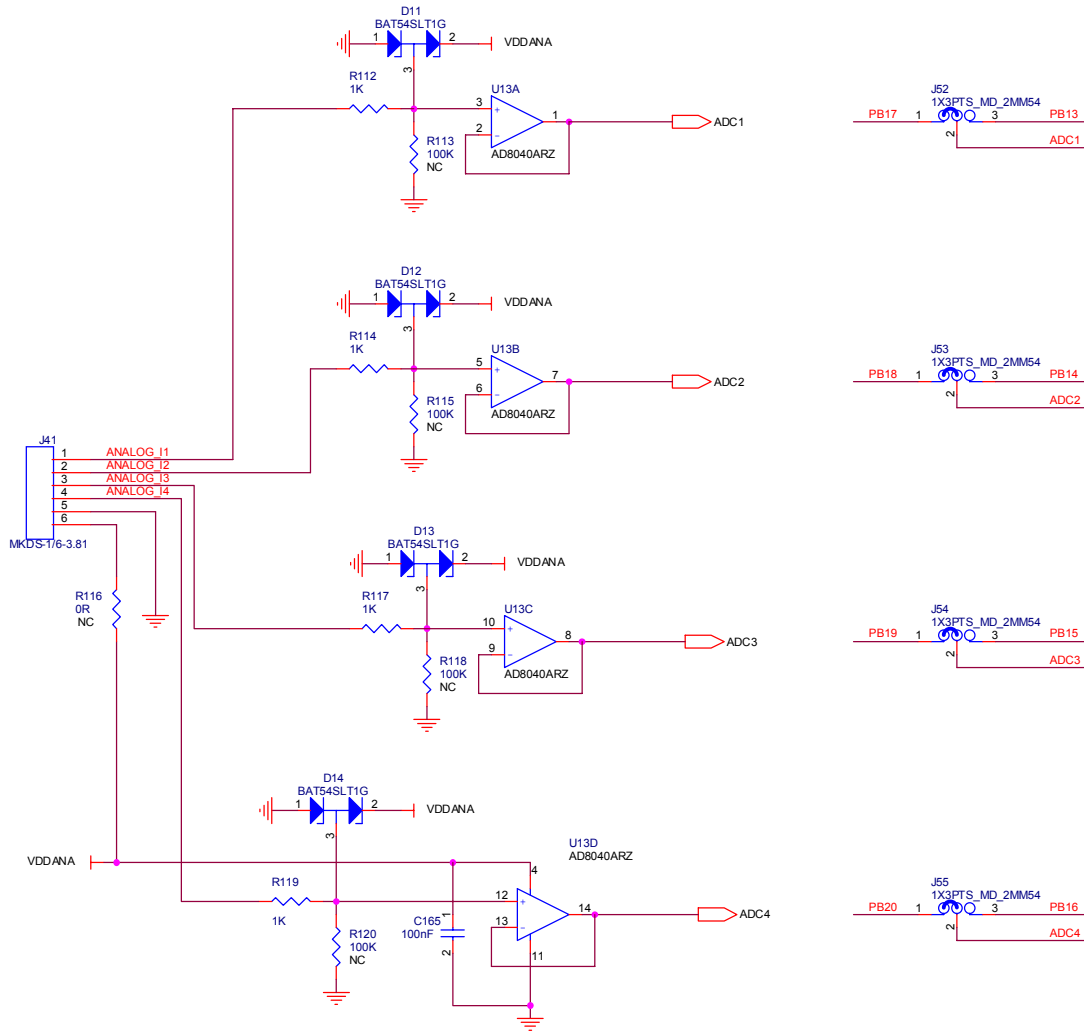
### 2.4.1.8 F8: Analog Input Adaptation

Analog input adaptation is realized by an AD8040 low-power high-speed rail-to-rail IO amplifier. ADC[1..4] output signals of the amplifier drive the AD[0..7] ADC embedded in the AT91CAP9.

**Table 2-18.**

Analog Signal Name	J52 jumper Position	J53 jumper Position	J54 jumper Position	J55 jumper Position	AT91CAP9 ADC Name
ADC1	1-2 (default)	-	-	-	AD4
ADC1	2-3	-	-	-	AD0
ADC2	-	1-2 (default)	-	-	AD5
ADC2	-	2-3	-	-	AD1
ADC3	-	-	1-2 (default)	-	AD6
ADC3	-	-	2-3	-	AD2
ADC4	-	-	-	1-2 (default)	AD7
ADC4	-	-	-	2-3	AD3

The implementation is shown below

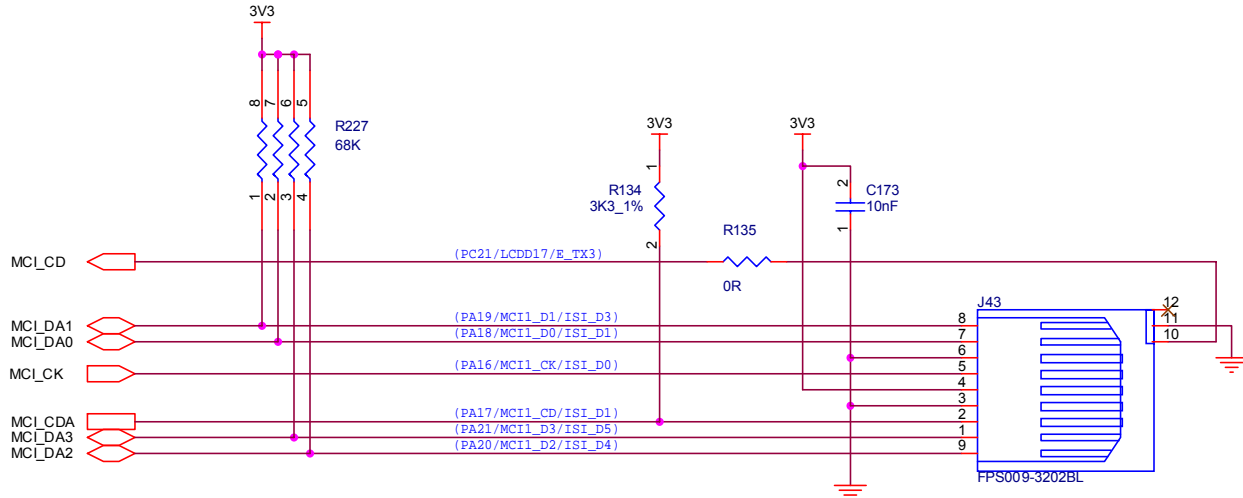


## Requirements

### 2.4.1.9 F9: SD Card

The AT91CAP9 MCI is directly connected to the SD Card slot. 68k pull-up resistors are added on the MCI\_DA[0..3] data signals.

The implementation is shown below:

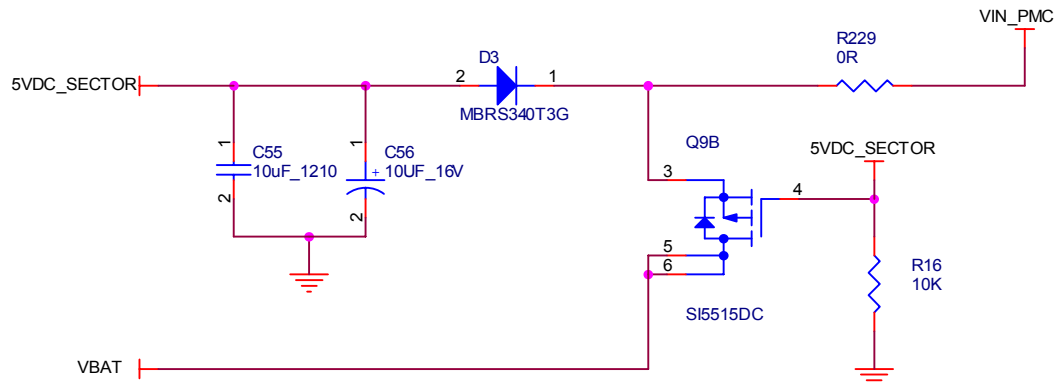


### 2.4.1.10 F10: Power Supplies and Low-power Mode

0603 footprint (0Ω resistor) or jumpers are implemented on power supplies in order to measure the current.

#### 2.4.1.10.1 Power Supplies

Power supply of the board is assumed either by an external 5V/10W AC/DC sector adapter or Li-Ion external battery (VIN\_PMC):

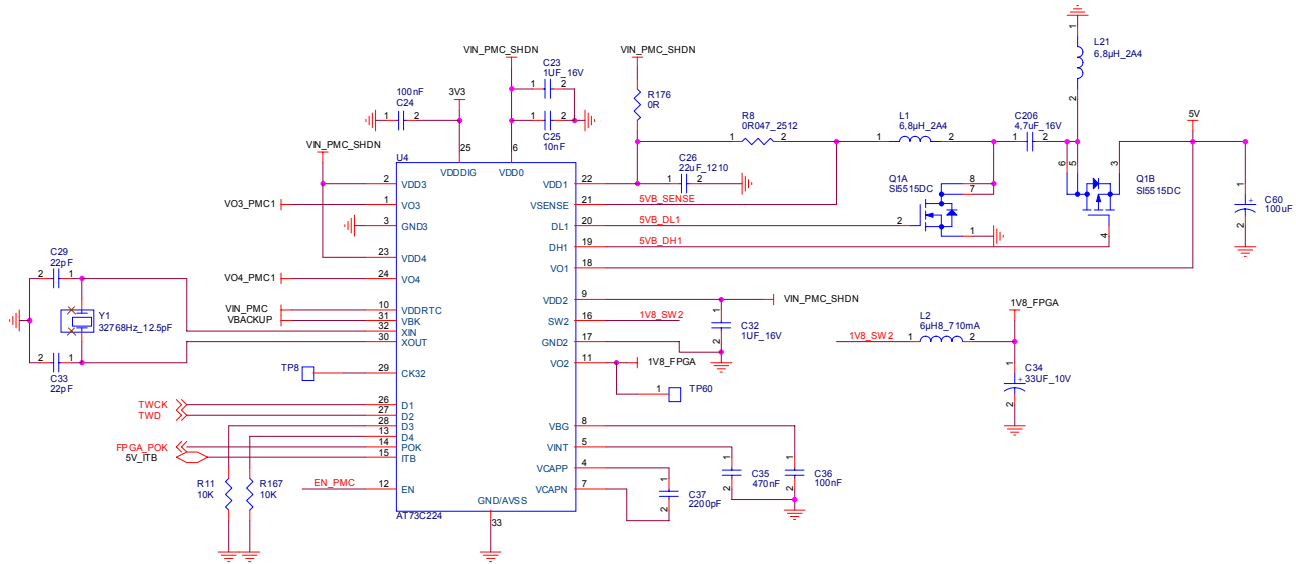


The different power supplies of the board are provided by two AT73C224 chips from the Atmel family of AT73 products (controlled by the AT91CAP9 TWI bus) and one LTC3412 as shown below:



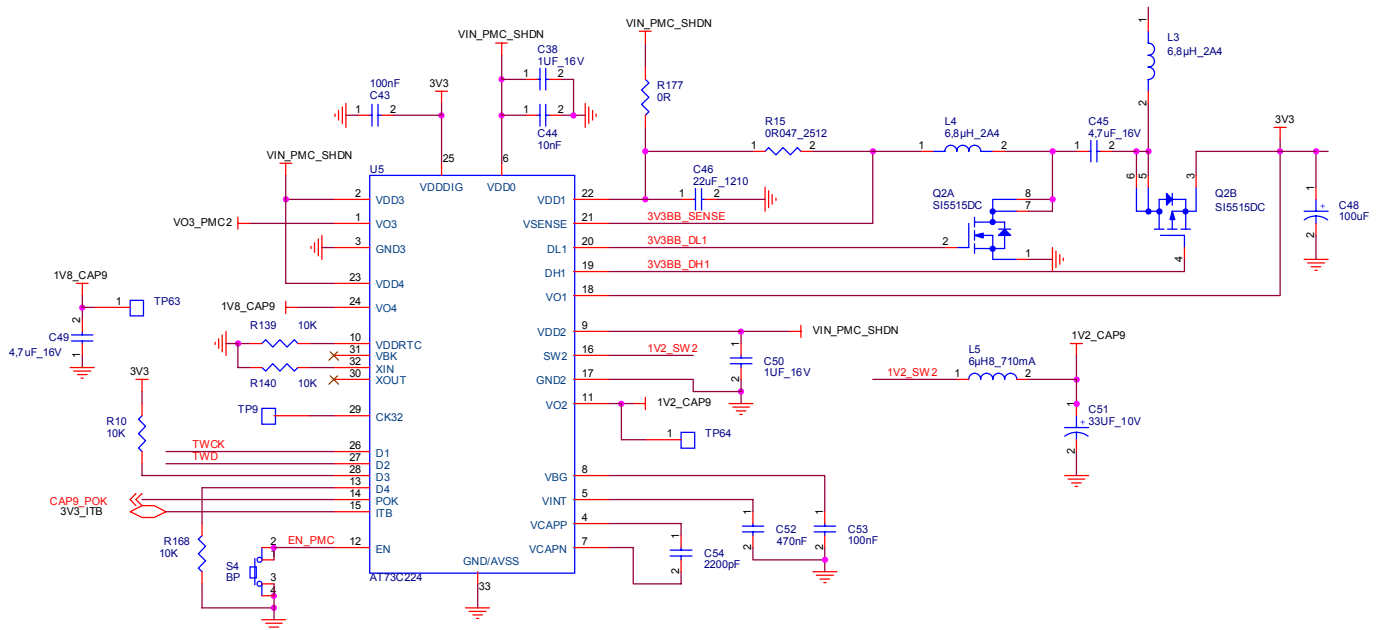
■ First AT73C224

- 5V/1A (SEPIC buck boost)
- 1.8V\_FPGA/500mA (boost)
- 1.2V VBACKUP



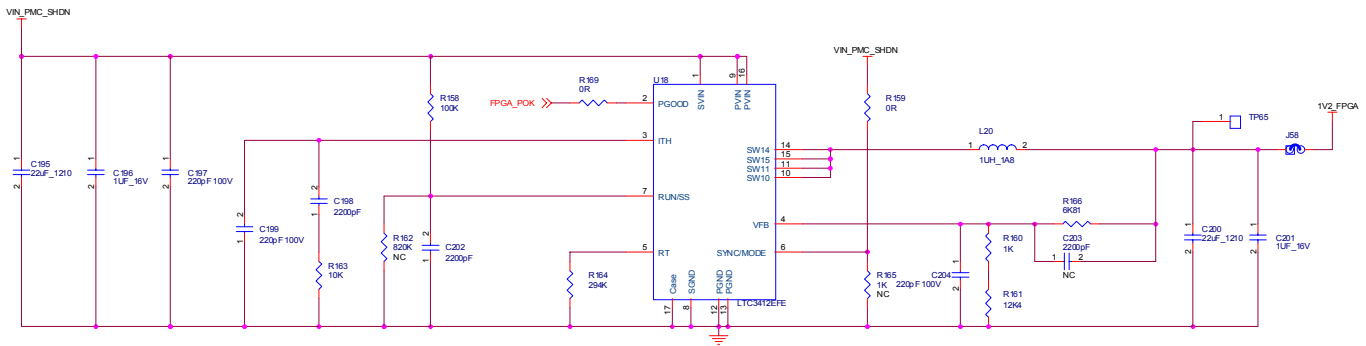
■ Second AT73C224

- 3.3V/1AZ (SEPIC buck boost)
- 1.2V\_CAP9/500 mA (boost)
- 1.8V\_CAP9/200 mA (LDO)



## Requirements

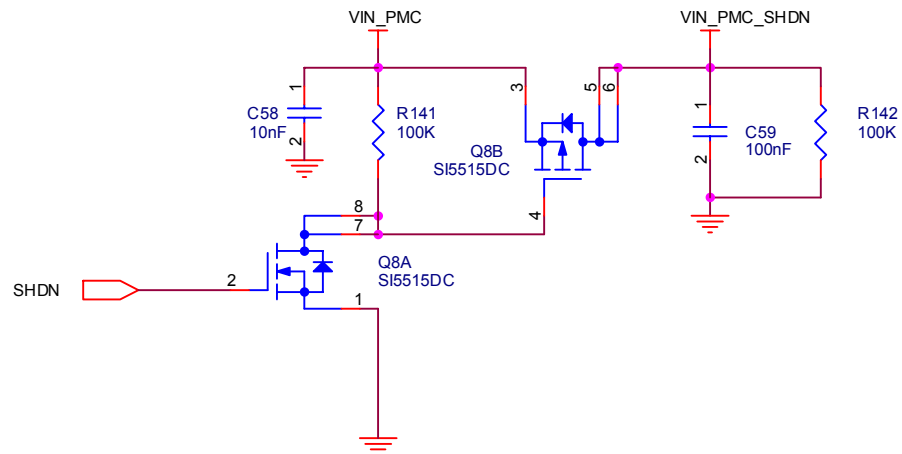
### ■ LTC3412: 1.2V\_FPGA/1A



#### 2.4.1.10.2 Low-power Mode

The power supply of this 3 PMC (VIN\_PMC\_SHDN) is managed by the AT91CAP9 SHDN signal (power by VDDBU). (See “F12: RTC and Backup” on page 2-25.)

When AT91CAP9 commands low power mode, it drives its SHDN pin low and so switches off the 3 PMC power supply. The implementation of the switch is shown below:



**No external pull-up is required on the SHDN signal (even at start-up).**

### 2.4.1.11 F11: Battery Charger

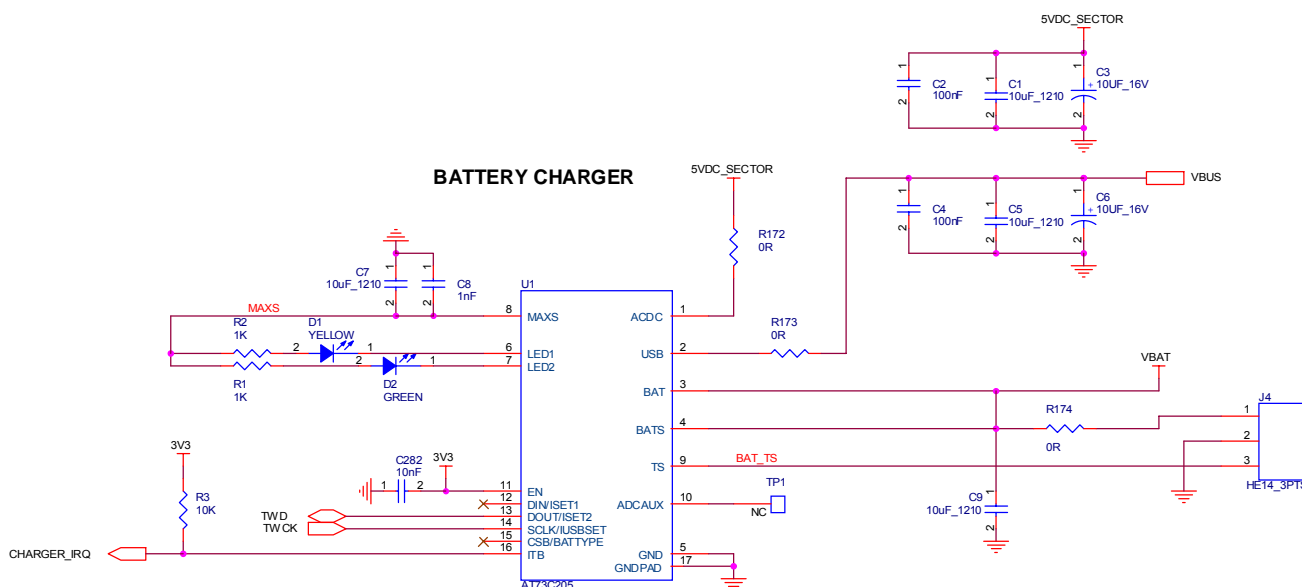
An Atmel AT73C205 stand alone battery charger is implemented on the board.

It manages the charge of an external Li-Ion battery plugs on the E11 interface, from 5V AC/DC sector adapter or VBUS USB Device external power source.

The battery charger is controlled by the AT91CAP9 TWI bus.

Two LEDs (yellow and green) indicate the charge status.

The implementation of the AT73C205 battery charger is shown below.



### 2.4.1.12 F12: RTC and Backup

#### 2.4.1.12.1 Backup

The first AT73C224 PMC provides a 3V VBACKUP power supply on its VBK power pin, from non-managed VIN\_PMC supply on its VDDRTC power in.

This VBACKUP power supply recharges a manganese-lithium rechargeable coin battery in the E112 interface. It also supplies the AT73C239 chip on its VBAT power pin, which generates (VO4 output) 1.2V\_SAVE to supply the VDDBU AT91CAP9 power supply.

When no external power supplies are applied on the board, the AT73C239 is only supplied by the manganese-lithium rechargeable coin battery to maintain the VDDBU AT91CAP9 power supply

#### 2.4.1.12.2 RTC

The first AT73C224 PMC described above integrates an RTC module with an external 32,768 kHz quartz connection. (See "First AT73C224" on page 2-23.)

The RTC module is powered by a non-managed VIN\_PMC source on its VDDRTC power pin. When no external power supplies are applied on the board, the RTC module is powered on its VBK power pin by the manganese-lithium rechargeable coin battery, VBACKUP supply.

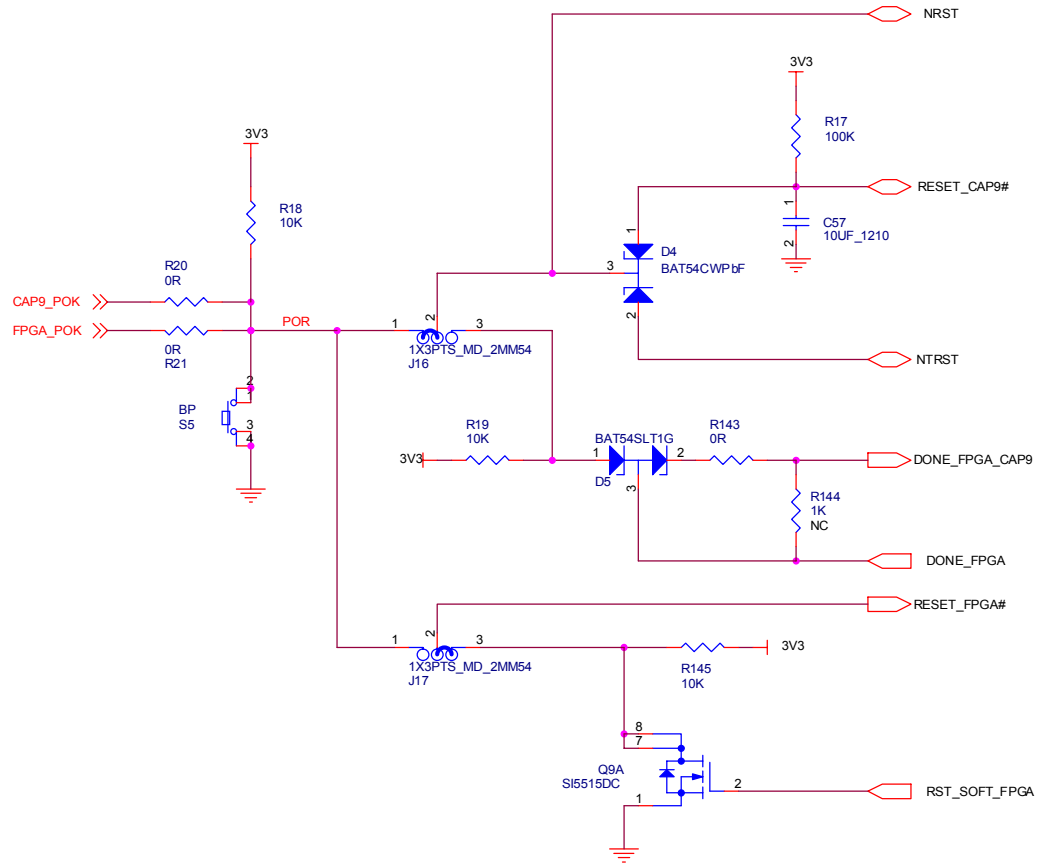




## Requirements

### 2.4.1.13 F13: Reset Configuration

Reset of the board is assumed by the reset circuit as shown below.



Each AT73C224 PMC provides an active low reset signal when an error occurs on one of its power supply outputs. These open-drain output signals, CAP9\_POK and FPGA\_POK, with 10k to 3.3V pull-up, are connected to a push button for manual hardware reset and provide the POR signal.

Reset signals are:

- POR: Power On Reset signal, managed by CAP9\_POK, FPGA\_POK or manual hardware reset push button (active low)
- NRST: ICE probe AT91CAP9 microcontroller reset signal (active low)
- RESET\_CAP9: AT91CAP9 microcontroller reset signal (active low)
- NTRST: test reset (active low)
- RESET\_FPGA: FPGA reset signal, it drives the nCONFIG signal of the FPGA (active low)
- RST\_SOFT\_FPGA: FPGA reset from AT91CAP9 microcontroller (active high)

Two jumpers on the 3-pin connectors, J16 and J17 define reset configuration of the board and the way status reset signals are driven.

Status reset signals are:

- DONE\_FPGA: the CONF\_DONE FPGA configuration status signal
- DONE\_FPGA\_CAP9: indicates the FPGA configuration status to the AT91CAP9 microcontroller (PIO)

**Table 2-19.** Reset Configuration

Reset Configuration	Reset Description	J16 Jumper Position	J17 Jumper Position
1	Uncontrolled reset-then-start CAP9 and FPGA order	1-2	1-2
2	Reset CAP9 resets FPGA, start CAP9 and then start FPGA	1-2	2-3
3	Reset FPGA resets CAP9, start FPGA and then start CAP9	2-3	1-2
4	Forbidden (no reset available)	2-3	2-3

#### 2.4.1.14 F14: Programming and Configuration

##### 2.4.1.14.1 JTAG Programming

Two different JTAG programming chains are implemented on the board:

- Stand-alone JTAG chains (default)

Each programmable device (microcontroller and FPGA) has its own JTAG programming chain. (See [“EI11: JTAG and Serial Configuration Interfaces” on page 2-7.](#))

- ICE-JTAG chain for AT91CAP9 JTAG programming
- USB-Blaster chain for FPGA JTAG programming

- ICE-only JTAG daisy chain

It's possible to use only the ICE-JTAG interface to program microcontroller and FPGA on a unique JTAG daisy chain. AT91CAP9 is the first device in the daisy chain, FPGA is the second one.

Configuration of the jumper positions must be as shown in the table that follows.

**Table 2-20.** Jumper Position Configuration

JTAG Programming Chain	J59 Jumper Position	J60 Jumper Position	J61 Jumper Position	J62 Jumper Position	J63 Jumper Position	J64 Jumper Position	Note
Stand-alone JTAG chains	1-2	2-3	2-3	2-3	2-3	2-3	Default chain
ICE-only JTAG daisy chain	2-3	1-2	1-2	1-2	1-2	1-2	-

##### 2.4.1.14.2 Serial Device Configuration

Three ways can be used to program the FPGA EPCS16 serial device.

- Serial device configuration port

The FPGA EPCS16 serial device configuration can be programmed via the EI11 serial device configuration port with Altera USB Blaster probe.

- Altera SFL (Serial Flash Loader) function



## Requirements

In this case, the serial device is programmed via FPGA JTAG interface.

The **advantage** is that it makes it possible to configure the FPGA and program serial configuration devices using the same JTAG interface. The **disadvantage** is that programming is very slow because SFL needs to configure the FPGA before programming the serial configuration device.

- Microcontroller programs serial configuration device

In this case, the AT91CAP9 microcontroller drives the following signals via its PIO

**Table 2-21.** AT91CAP9 PIO Signal Control

Signal Name	Signal Description	AT91CAP9 I/O
nCE	Configuration Chip enable	PB6
nCSO	Configuration Chip select	PB3
DCLK	Configuration Clock pin	PB7
ASDO_FPGA	Configuration Read enable	PB8

To use this mode of programming, **R216 to R219 0Ω resistors must be mounted and reset configuration must be set to 2.** (See “F13: Reset Configuration” on page 2-26.)

Once the serial configuration device is programmed, FPGA configuration is initiated at start-up between FPGA and the serial configuration device via the DATA0, DCLK, nCSO and ASDO signals.

The FPGA AS mode configuration scheme is set by the MSEL[0..3] signals (default Fast AS).

**Table 2-22.** FPGA AS Mode Configuration

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0
Fast AS (40 MHz)	1	0	0	0
Remote system upgrade fast AS (40 MHz)	1	0	0	1
AS (20 MHz)	1	1	0	1
Remote system upgrade AS (20 MHz)	1	1	1	0

### 2.4.1.15 F15: Prototyping Area

Two prototyping areas are implemented on the board.

- The first one is a 20x18 points, 1.24 mm-pitch matrix, with two 1x8 points, 1.24 mm-pitch line, connected to 5V and 3.3V added on top of the matrix, and 1x20 points, 1.24 mm pitch line, connected to GND added on the bottom of the matrix.
- The second one is a 10x8 points, 2.54 mm-pitch matrix, with two 1x4 points, 2.54 mm-pitch line, connected to 5V and 3.3V added on top of the matrix, and 1x8 points, 2.54 mm-pitch line, connected to GND added on the bottom of the matrix.

## **2.4.2 Physical Characteristics**

### **2.4.2.1 Mechanical**

The format of the CAP9-STK board is 185x120 mm.

#### **2.4.2.1.1 LCD Panel Support**

An LCD panel support is implemented on the board to receive the TX09D70VM1CCA Hitachi LCD.

#### **2.4.2.1.2 BGA Socket**

A 22.225x22.225 mm BGA socket can be implemented on the board to receive the AT91CAP9 400-ball LFBGA.

### **2.4.2.2 Electrical**

The nominal consumption of the board is less than 10 W.

### **2.4.2.3 Environmental**

No requirements are specified. However, the board is designed to run normally under 0°C to 55°C temperature.

All components mounted on the board are RoHS compliant.

### **2.4.2.4 Packaging**

The CAP9-STK packaging includes the following items:

- The CAP9 Starter Kit Standalone Board wrapped in an ESD packaging.
- A CD of documentation and software, including software development tools and FPGA development tools
- The power supply of the board with adaptors for Europe, United Kingdom, China and United States
- A set of communication cables, including cables for USB, Ethernet and serial port.
- A manganese-lithium 3V rechargeable coin battery



## Section 3

# Board Strap and Switch Configuration

### 3.1 Connectors 1x2

**Table 3-1.** Connectors 1x2

Name	Position (default)	Descriptions	
		Closed	Open
J5	Not Connected	VIN_AT73C239 power supply is 5V if S1 in 1-3	
J6 <sup>(1)</sup>	Connector not Mounted	VIN_AT73C239 power supply is VIN_PMC if S1 is in 1-2 position and S2 is in 1-3 position.	VIN_SURV_AT73C239 power supply is 3V3 if S2 is in 1-2 position.
J7	1-2	Reset out of AT73C239 (U3) if VIN_AT73C239 < 2.6V on FIQ# (Fast Interrupt) of CAP9	FIQ# = open (not used by CAP9)
J8	1-2	TP2 = VO1 of AT73C239 (U3)	Measure VO1 current of AT73C239 (U3) if a charge is connected between TP2 and TP3
J9	1-2	TP4 = VO2 of AT73C239 (U3)	Measure VO2 current of AT73C239 (U3) if a charge is connected between TP4 and TP5.
J11	1-2	V <sub>BAT</sub> of AT73C239 (U3) supply by VIN_AT73C239 if S9 is in 1-3 position.	V <sub>BAT</sub> of AT73C239 (U3) is not connected.
J12	1-2	TP6 = VO3 of AT73C239 (U3)	V <sub>BAT</sub> of AT73C239 (U3) supply by VBACKUP if S9 is in 1-2 position.
J20	1-2	V <sub>DDCORE</sub> supply by 1V2	Measure VO3 current of AT73C239 (U3) if a charge is connected between TP6 and TP7.
J21	1-2	V <sub>DDIOM</sub> supply by 1V8	V <sub>DDCORE</sub> is off.
J22	1-2	V <sub>DDPLL</sub> supply by 3V3	V <sub>DDIOM</sub> is off.
J23	1-2	V <sub>DDIOP0</sub> supply by 3V3	V <sub>DDPLL</sub> is off.
J24	1-2	V <sub>DDIOP1</sub> supply by 3V3 if R26 is connected but R27 is not connected. V <sub>DDIOP1</sub> supply by 1V8 if R27 is connected but R26 is not connected.	V <sub>DDIOP1</sub> is off.
J25	1-2	V <sub>DDUPLL</sub> supply by 1V2	V <sub>DDUPLL</sub> is off.
J26	1-2	V <sub>DDUTMIC</sub> supply by 1V2	V <sub>DDUTMIC</sub> is off.
J27	1-2	V <sub>DDUTMI</sub> supply by 3V3	V <sub>DDUTMI</sub> is off.
J29	1-2	V <sub>DDANA</sub> supply by 3V3 filtered	V <sub>DDANA</sub> is off.
J39	1-2	Chip select audio DAC (U12) by CAP9	The audio DAC (U12) not selected.

**Table 3-1.** Connectors 1x2 (Continued)

Name	Position (default)	Descriptions	
		Closed	Open
J44	1-2	Chip select SPI DATA FLASH (U17) by CAP9	The SPI DATA FLASH (U17) not selected
J48	1-2	TP24 = VO3_PMC1 of AT73C224 (U4)	Measure VO3_PMC1 current of AT73C224 (U4) if a charge is connected between TP24 and TP25
J49	1-2	TP26 = VO4_PMC1 of AT73C224 (U4)	Measure VO4_PMC1 current of AT73C224 (U4) if a charge is connected between TP26 and TP27
J50	1-2	TP28 = VO3_PMC2 of AT73C224 (U5)	Measure VO3_PMC2 current of AT73C224 (U5) if a charge is connected between TP28 and TP29
J58	1-2	1V2_FPGA is connected	1V2_FPGA is off
J66	1-2	Flash NAND CE# signal is driven by FN_CE# CAP9 signal	Flash NAND CE# signal is pull-up to 1V8
J67	1-2	1V2_FPGA is connected	1V8_FPGA is off

Note: 1. J6 connector is not mounted on the prototype.

### 3.2 Connectors 1x3

**Table 3-2.** Connectors 1x3

Name	Position (default)	Descriptions	
		1-2	2-3
J16	1-2	POR (manually or AT73C224) resets the CAP9	Reset sthe CAP9 during the programming of FPGA
J17	2-3	POR (manually or AT73C224) resets the FPGA	Resest the FPGA by CAP9 software
J28	1-2	VDDBU supply by 1V2_SAVE	VDDBU supply by 1V2
J31	1-2	BMS pull-up to 3V3	BMS tied to GND
J52	1-2	Analog input 1 on CAP9 ADC channel 4	Analog input 1 on CAP9 ADC channel 0
J53	1-2	Analog input 2 on CAP9 ADC channel 5	Analog input 2 on CAP9 ADC channel 1
J54	1-2	Analog input 3 on CAP9 ADC channel 6	Analog input 3 on CAP9 ADC channel 2
J55	1-2	Analog input 4 on CAP9 ADC channel 7	Analog input 4 on CAP9 ADC channel 3
J59	1-2	TDO ICE port signal is CAP9 TDO signal (with J60 on 2-3).	FPGA TDI signal is CAP9 TDO signal (with J64 on 1-2).
J60	2-3	TDO ICE port signal is FPGA TDO signal (with J63 on 1-2).	TDO ICE port signal is CAP9 TDO signal (with J59 on 1-2).
J61	2-3	FPGA TMS JTAG signal is ICE port TMS signal.	FPGA TMS JTAG signal is FPGA JTAG port TMS signal.
J62	2-3	FPGA TCK JTAG signal is ICE port TCK signal.	FPGA TCK JTAG signal is FPGA JTAG port TCK signal.
J63	2-3	TDO ICE port signal is FPGA TDO signal (with J60 on 1-2).	FPGA JTAG port TDO signal is FPGA JTAG TDO signal.
J64	2-3	FPGA TDI JTAG signal is CAP9 TDO signal (with J59 on 2-3).	FPGA JTAG TDI signal is FPGA JTAG port TDI signal.

### 3.3 Switches

**Table 3-3.** Switches

Name	Position (default)	Descriptions	
		1-2	1-3
S1	1-3	VIN_AT73C239 power supply is VIN_SURV_AT73C239 power supply.	VIN_AT73C239 power supply is 5V if J5 is connected. Not connected by default for AT73C239 (connected for AT73C237 mounting).
S2	1-3	VIN_SURV_AT73C239 power supply is 3V3 power supply.	VIN_SURV_AT73C239 power supply is VBACKUP (J6 connector not mounted, VBACKUP strap on S2 pin 3).
S7	1-2	AT73C239 TWCK signal is pull -up to VIN_SURV_AT73C239 and controlled by CAP9 PA7 PIO (allows hibernate mode).	AT73C239 TWCK signal is CAP9 I2C bus TWCK signal.
S8	1-2	AT73C239 TWCK signal is VIN_SURV_AT73C239 power supply.	AT73C239 TWD signal is CAP9 I2C bus TWD signal.
S9	1-2	AT73C239 $V_{BAT}$ power supply is $V_{BACKUP}$	AT73C239 $V_{BAT}$ power supply is VIN_AT73C239 power supply.





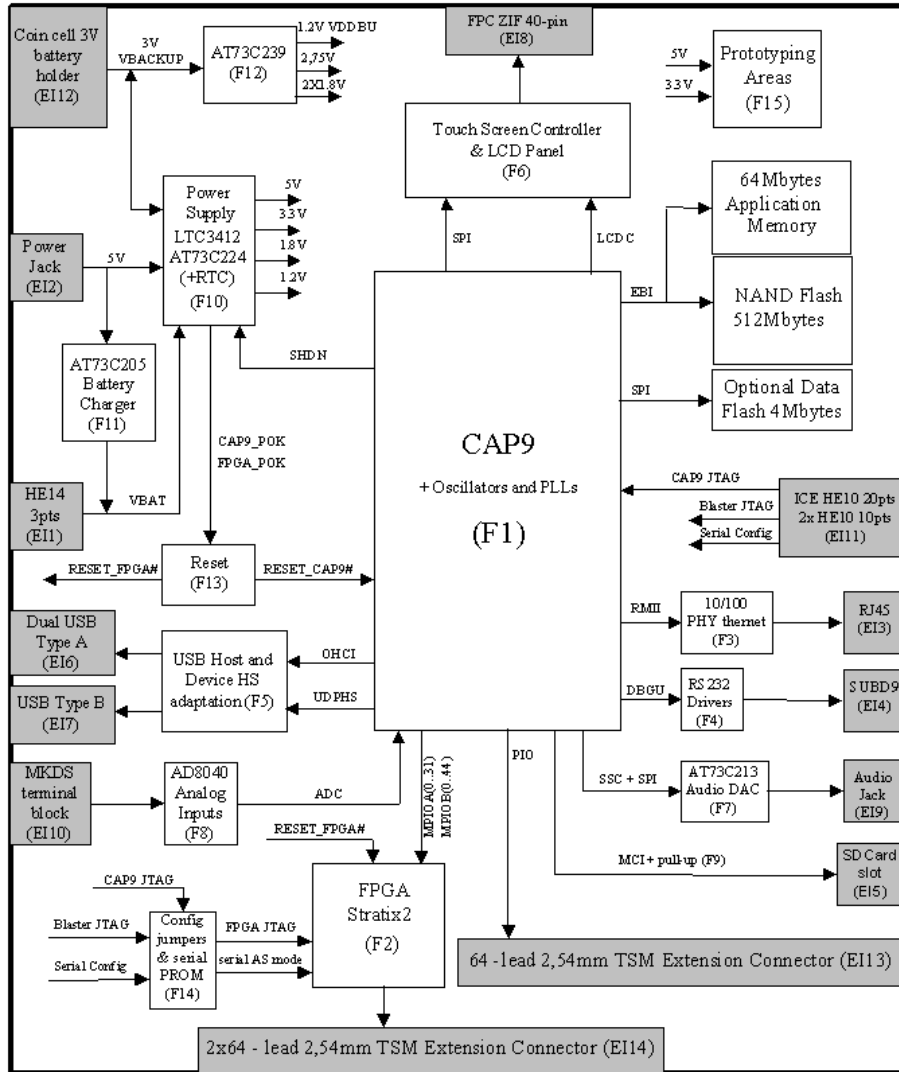


# AT91CAP9-STK Schematics

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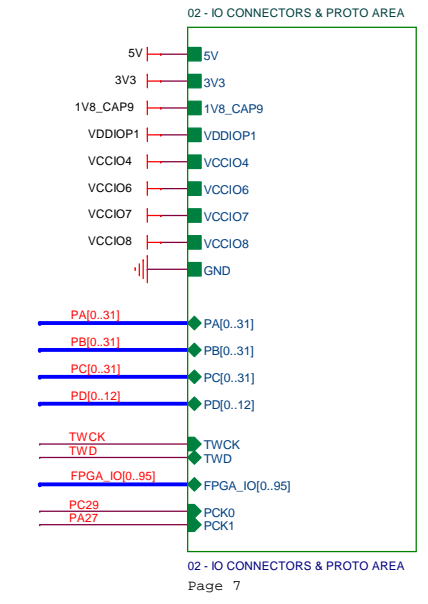
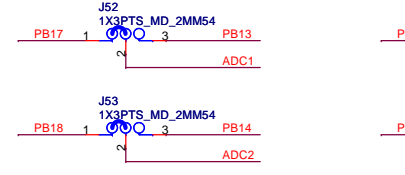
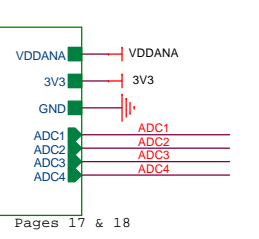
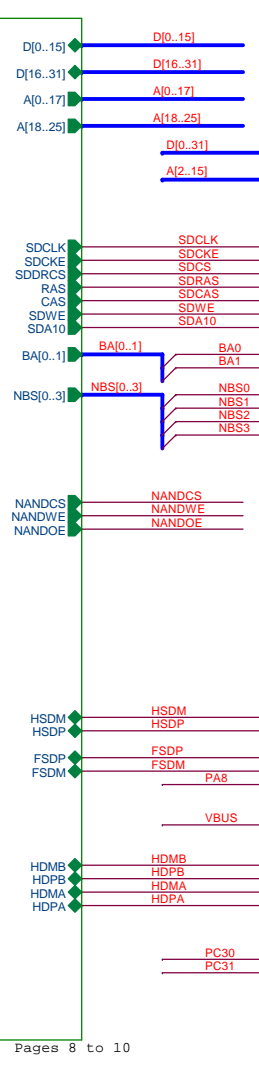
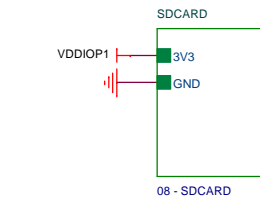
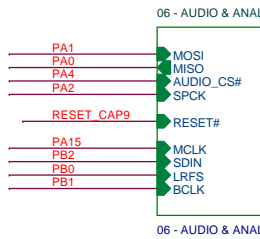
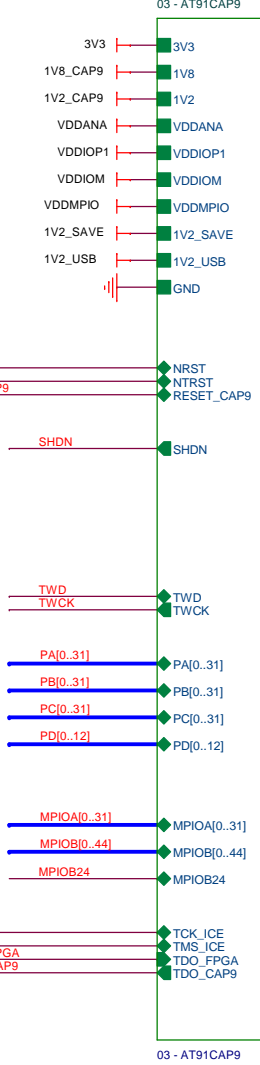
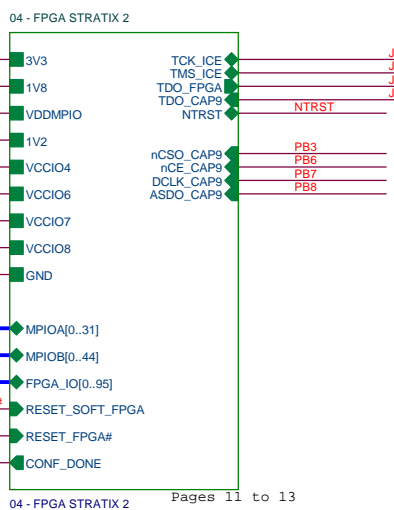
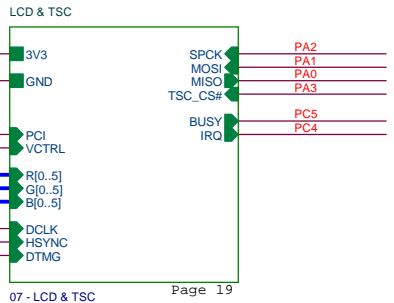
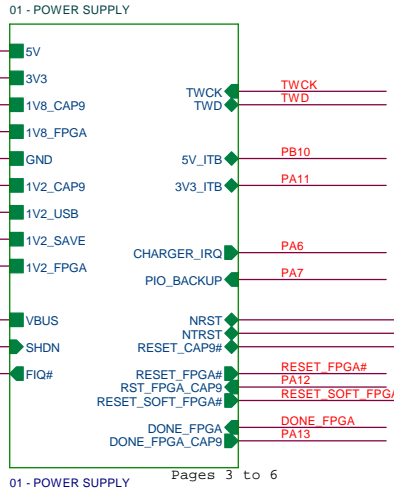
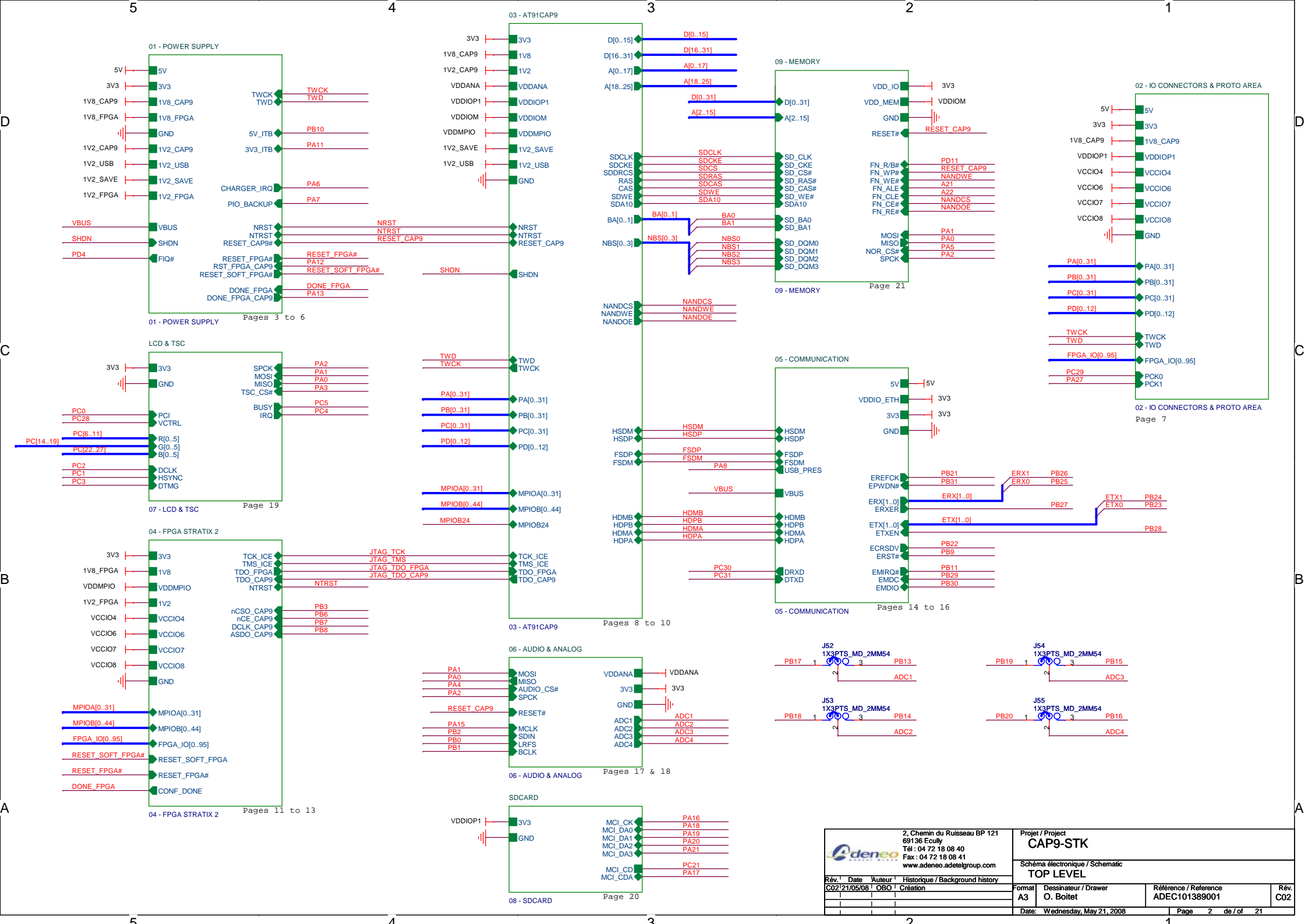
### 4.1 This section contains the following appended schematics

- Top View
- Battery Charger and Backup
- PMC AT73C224
- Power Switch and Reset
- FPGA Core Supply
- IO Connectors and Proto Area
- CAP9 Power
- EBI and PIO
- System USB Clock
- FPGA Power
- FPGA IO Bank
- FPGA IO Bank
- FPGA Clock and Configuration
- Debug
- Ethernet SMSC
- USB Host and Device
- Audio
- Analog
- LCD and TSC
- SDCARD
- SDRAM, NAND and DataFlash



- PAGE 01 : TITLE
- PAGE 02 : TOP VIEW
- PAGE 03 : BATTERY CHARGER & BACKUP
- PAGE 04 : PMC AT73C224
- PAGE 05 : POWER SWITCH & RESET
- PAGE 06 : FPGA CORE SUPPLY
- PAGE 07 : IO CONNECTORS & PROTO AREA
- PAGE 08 : CAP9 POWER
- PAGE 09 : EBI & PIO
- PAGE 10 : SYSTEM USB CLOCK
- PAGE 11 : FPGA POWER
- PAGE 12 : FPGA IO BANK
- PAGE 13 : FPGA CLOCK & CONFIG
- PAGE 14 : DEBUG
- PAGE 15 : ETHERNET SMSC
- PAGE 16 : USB HOST & DEVICE
- PAGE 17 : AUDIO
- PAGE 18 : ANALOG
- PAGE 19 : LCD & TSC
- PAGE 20 : SDCARD
- PAGE 21 : SDRAM, NAND & DATAFLASH

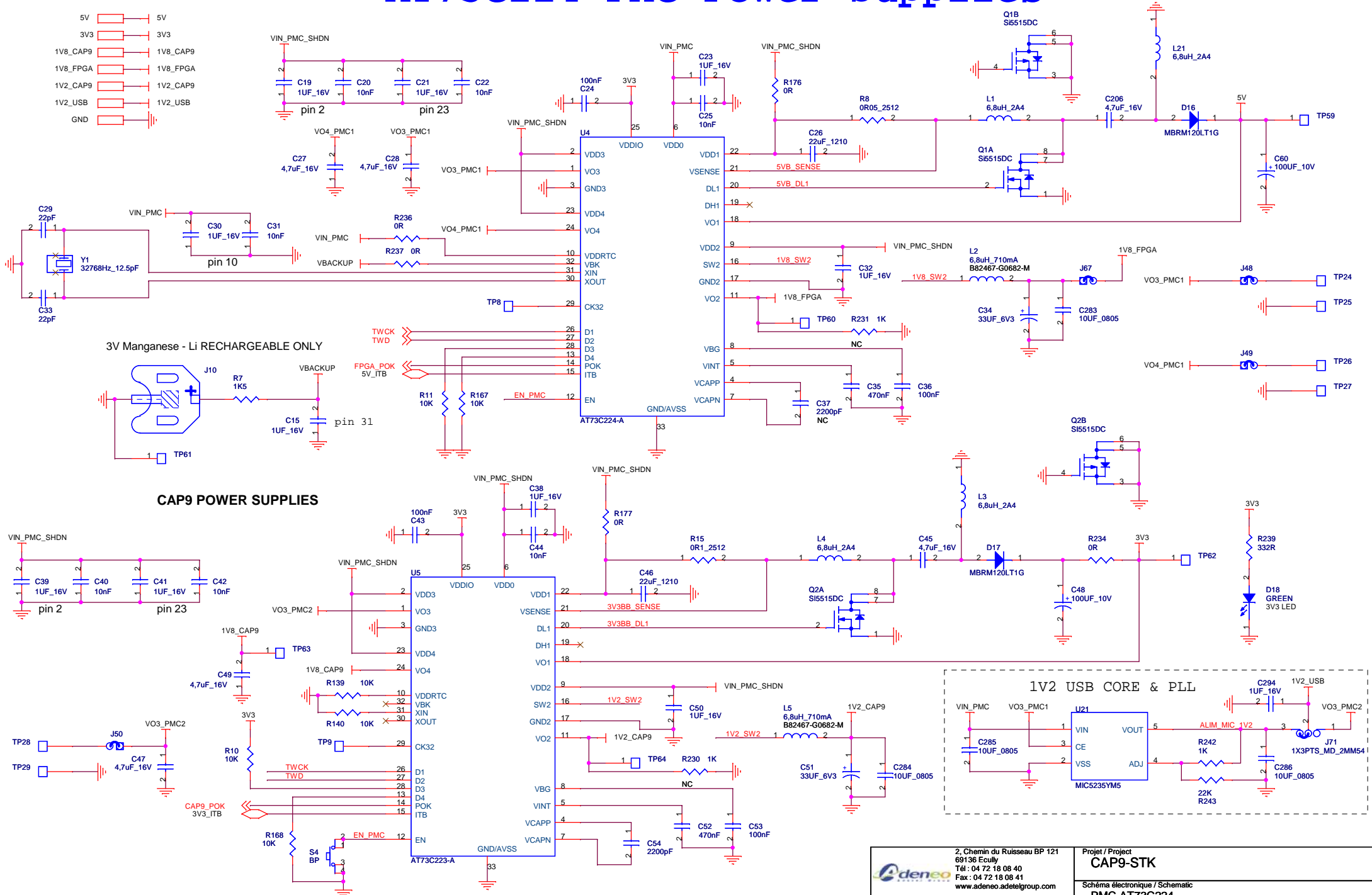
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Rév. Date Auteur Historique / Background history C02/21/05/08 OBO 1 Création				Projet / Project <b>CAP9-STK</b> Schéma électronique / Schematic <b>TITLE</b>	
Format A3	Dessinateur / Drawer O. Boitet	Référence / Reference ADEC101389001		Rév. C02	
Date: Tuesday, May 20, 2008				Page 1 de / of 21	



2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com		Projet / Project <b>CAP9-STK</b>	
Schéma électronique / Schematic <b>TOP LEVEL</b>			
Rev. A3	Date: 02/21/05/08	Auteur / Historique / Background history OBO Creation	Rev. C02
Format	Dessinateur / Drawer O. Boitet	Référence / Reference ADEC101389001	Rev. C02
Date: Wednesday, May 21, 2008	Page 2 de / of 21		

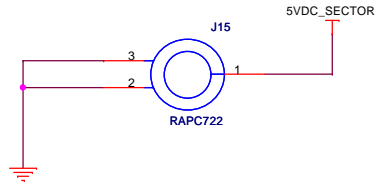


# AT73C224 PMC Power Supplies

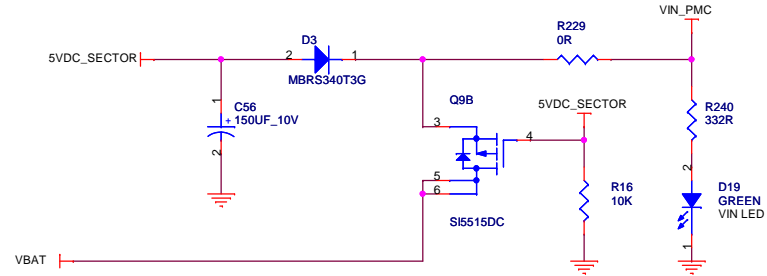


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Date: Wednesday, May 21, 2008				Page 4 de / of 21	

# Power Switch & Reset

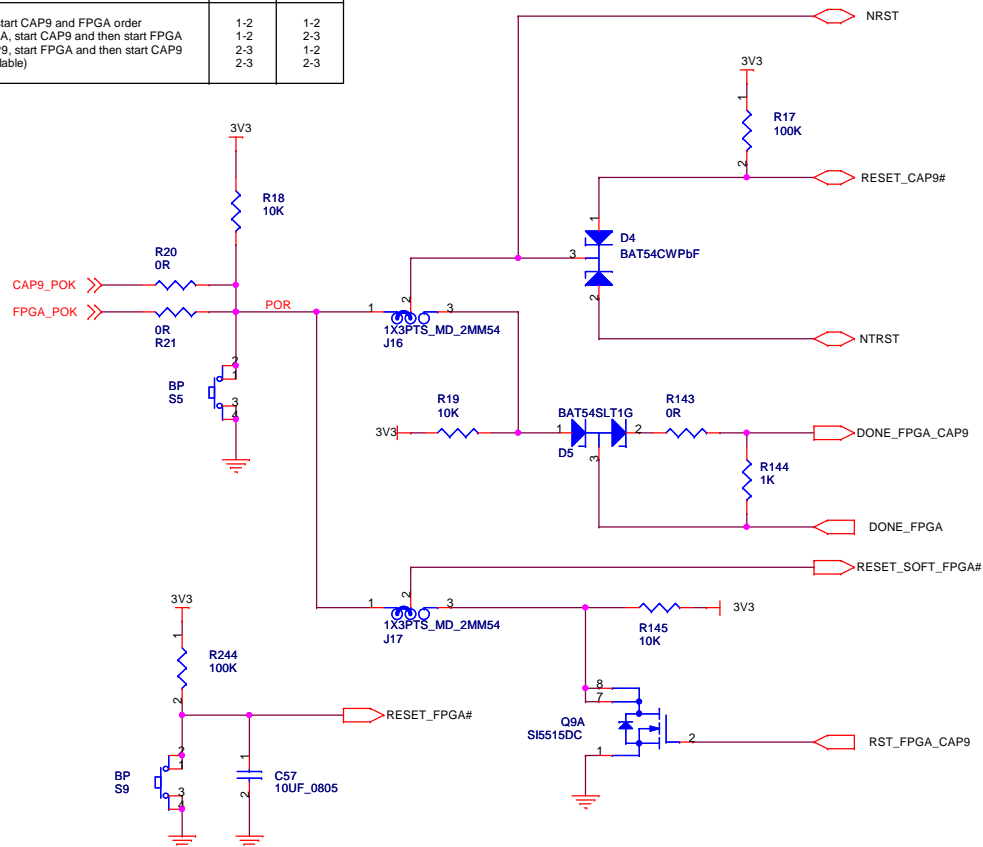


## SWITCH 5VDC\_SECTOR - VBAT

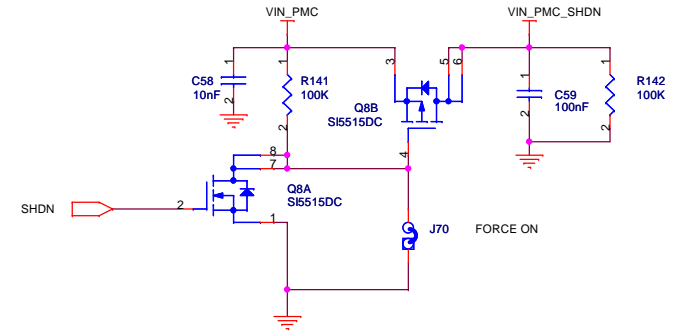


RESET CONFIG	J16 jumper	J17 jumper
Uncontrolled reset then start CAP9 and FPGA order	1-2	1-2
Reset CAP9 resets FPGA, start CAP9 and then start FPGA	1-2	2-3
Reset FPGA resets CAP9, start FPGA and then start CAP9	2-3	1-2
Forbidden (no reset available)	2-3	2-3

## RESET CONTROL

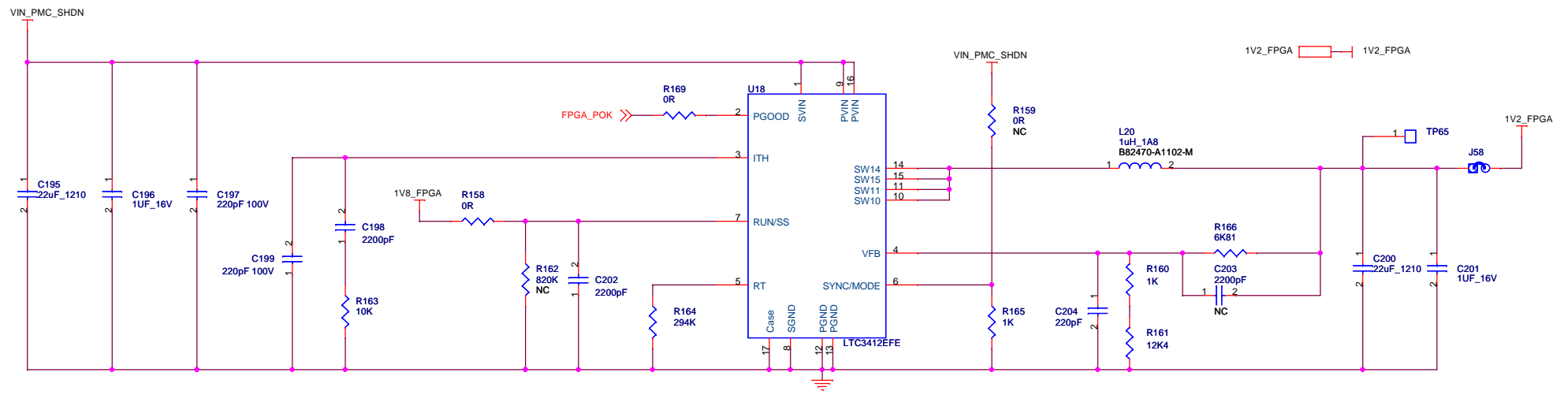


## SHUTDOWN VIN\_PMC



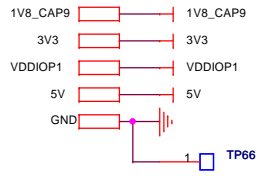
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Rév. Date Auteur Historique / Background history C02/21/05/08 OBO 1 Création				Proj / Project <b>CAP9-STK</b> Schéma électronique / Schematic <b>POWER SWITCH &amp; RESET</b>	
Format A3	Dessinateur / Drawer O. Boitet		Référence / Reference ADEC101389001		Rév. C02
Date: Wednesday, May 21, 2008				Page 5 de / of 21	

# FPGA Core Supply

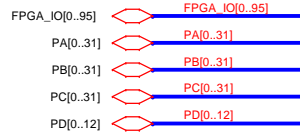


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Rév. C02	Date 21/05/08	Auteur OBO	Historique / Background history Création	Format A3	Dessinateur / Drawer O. Boitet	Référence / Reference ADEC101389001	Rév. C02
Date: Tuesday, May 20, 2008				Page 6 de / of 21			

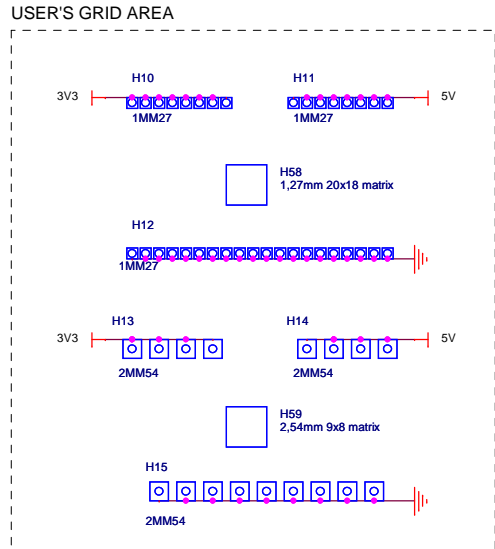
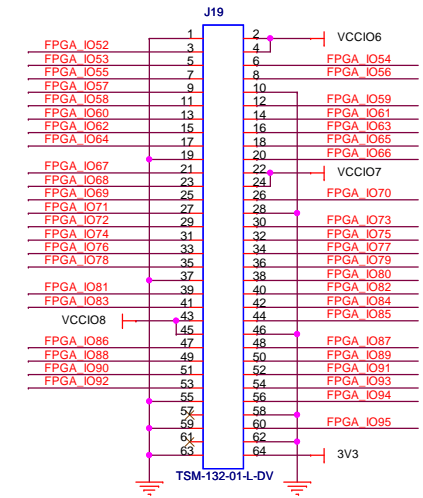
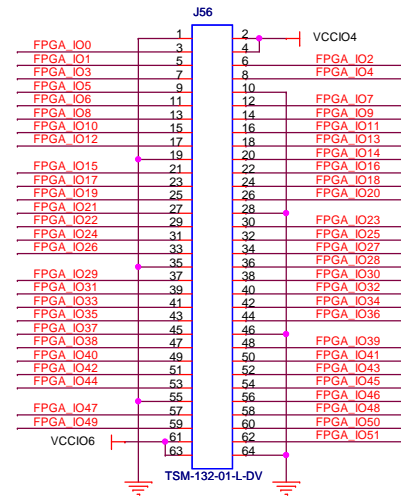
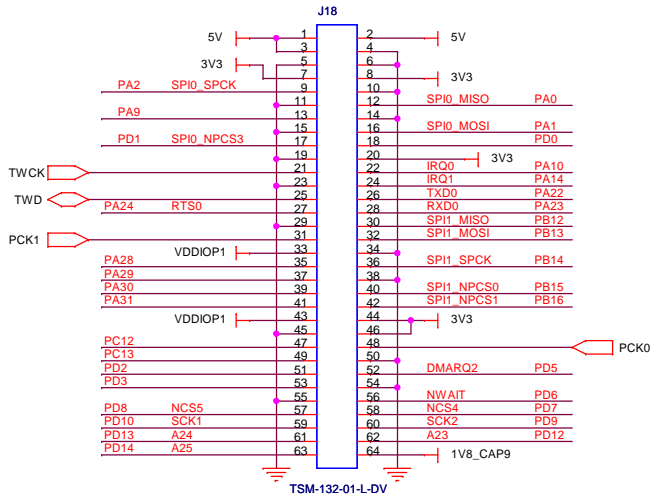
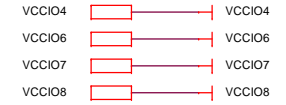
# CAP9 & FPGA PIO Connectors



CAP9 PIO CONNECTOR



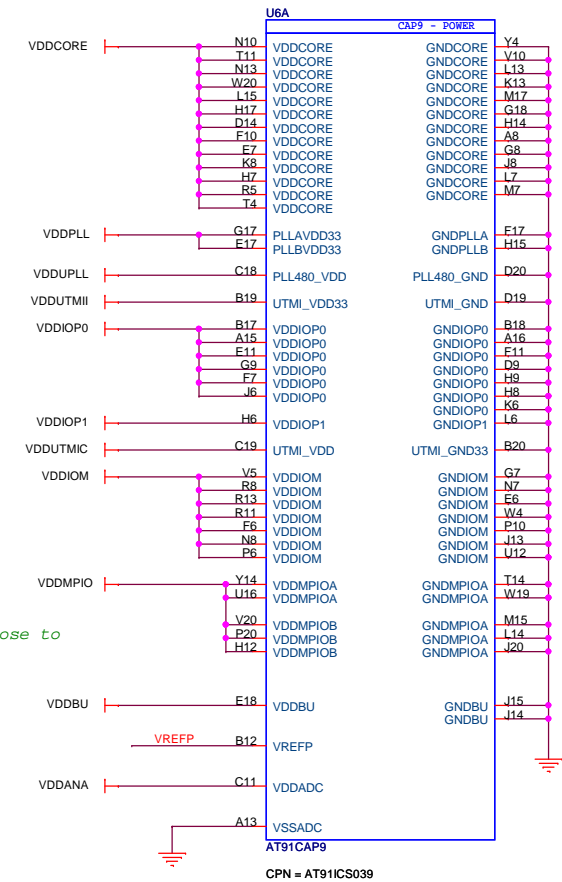
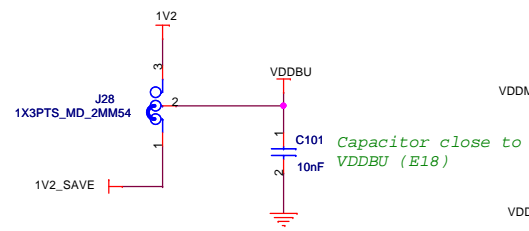
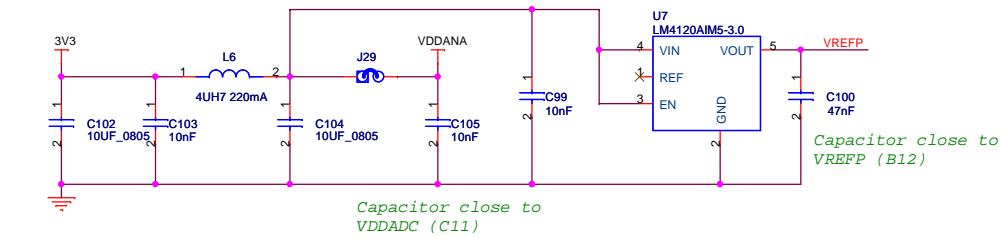
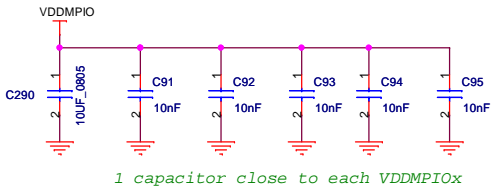
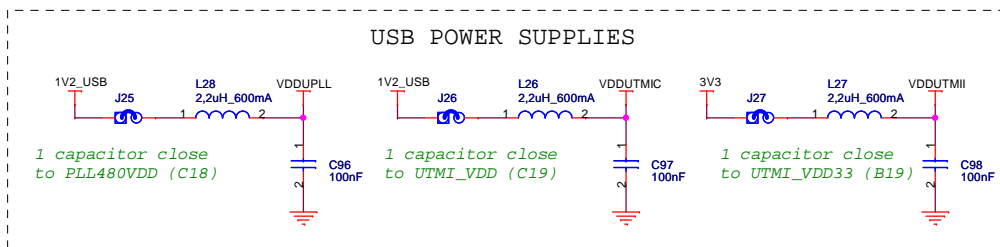
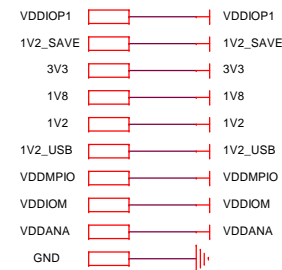
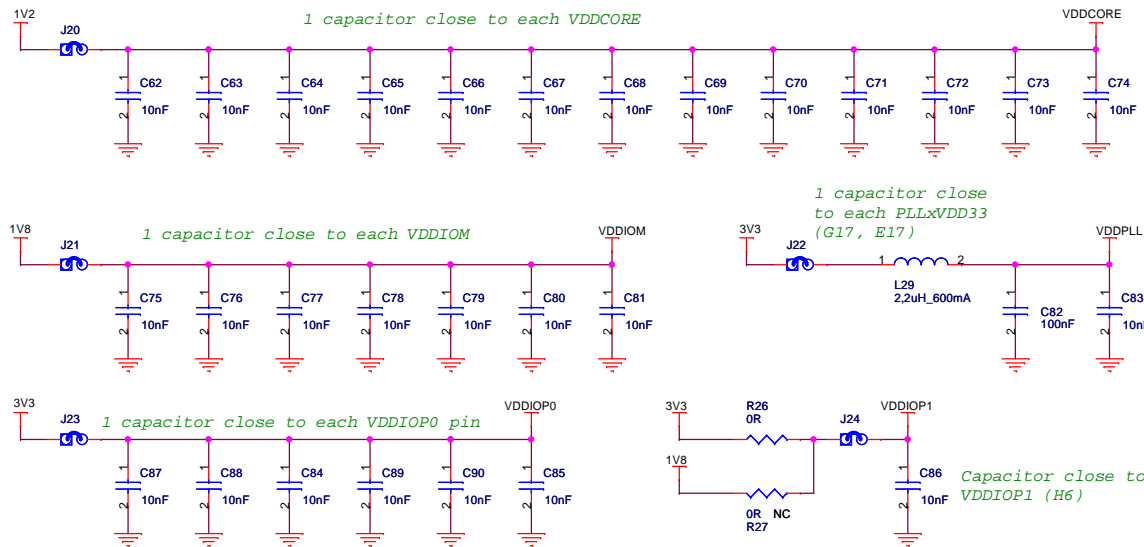
FPGA PIO CONNECTORS



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Schéma électronique / Schematic <b>IO CONNECTORS &amp; PROTO AREA</b>				Dessinateur / Drawer O. Boitet	
Rév. Date Auteur Historique / Background history C02/21/05/08 OBO Création				Référence / Reference ADEC101389001	
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Page 7 de / of 21				Rév. C02	

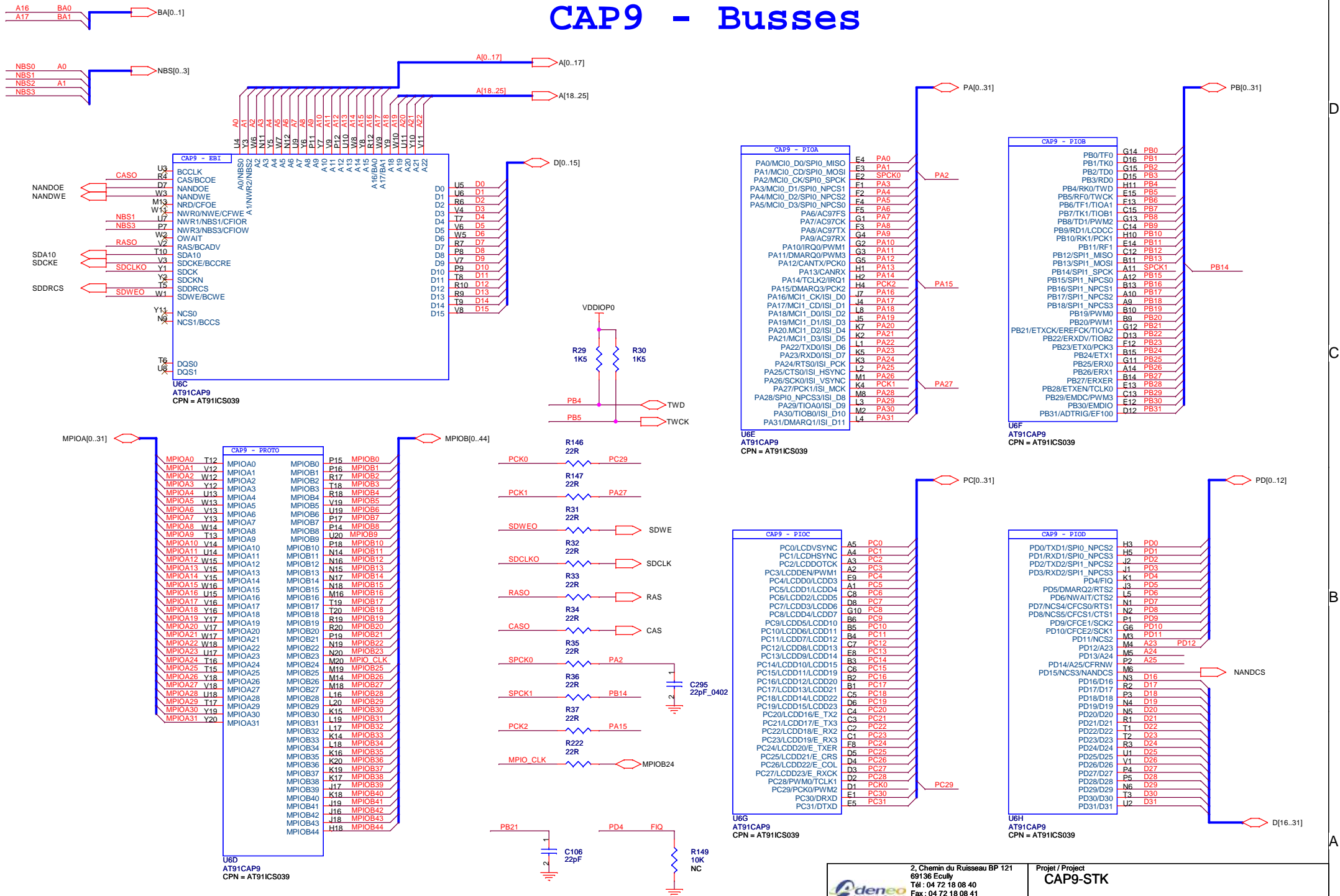


# CAP9 - Power supply

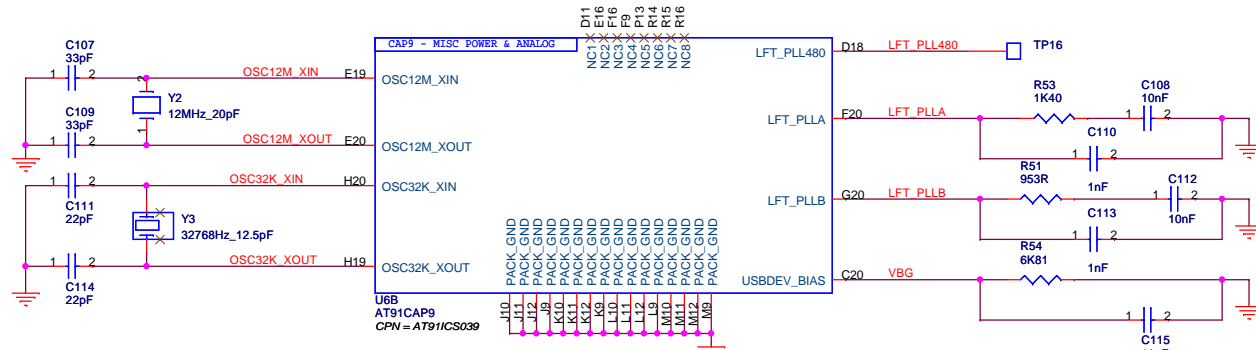
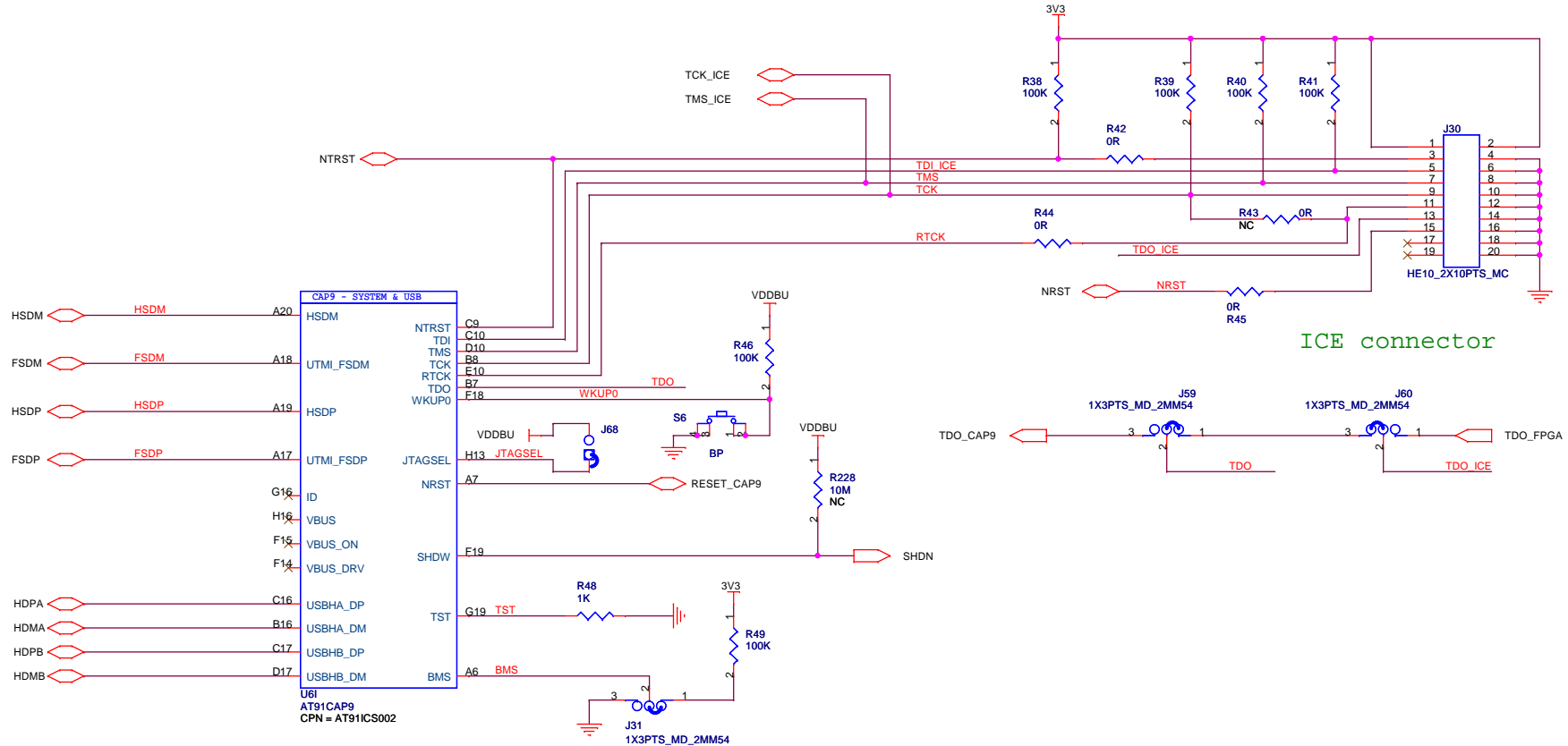
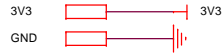


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Schéma électronique / Schematic <b>CAP9 POWER</b>				Dessinateur / Drawer O. Boitet	
Rév. Date Auteur Historique / Background history C02/21/05/08 OBO Création		Format A3		Référence / Reference ADEC101389001	
Date: Tuesday, May 20, 2008				Page 8 de / of 21	

# CAP9 - Busses

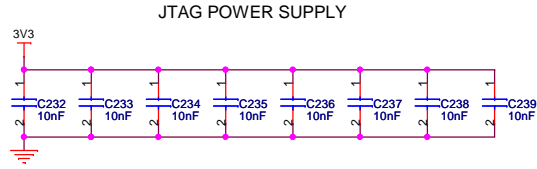
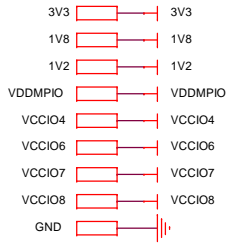


# CAP9 - USB, PLL, ICE

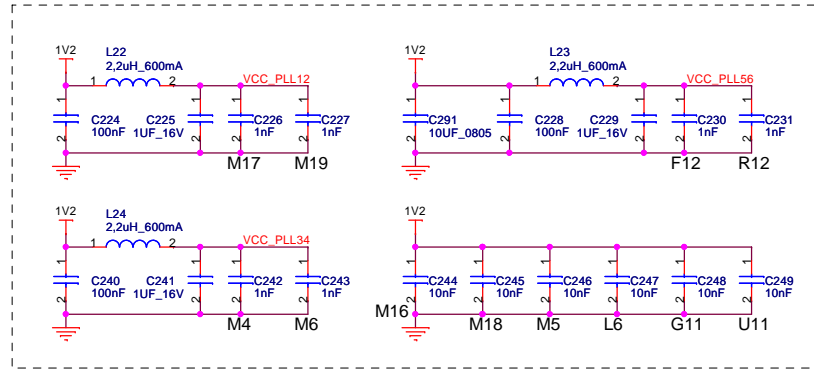


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Schéma électronique / Schematic <b>SYSTEM USB CLOCK</b>				Dessinateur / Drawer O. Boitet	
Rév. Date Auteur Historique / Background history C02/21/05/08 OBO 1 Création				Référence / Reference ADEC101389001	
Format A3		Date: Tuesday, May 20, 2008		Rév. C02	
Page 10 de / of 21				Page 10 de / of 21	

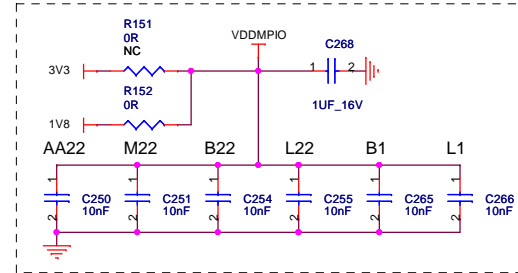
# FPGA Power



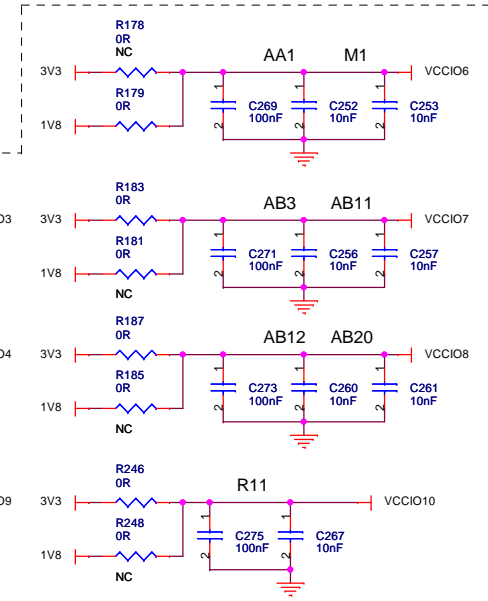
## PLL POWER SUPPLY



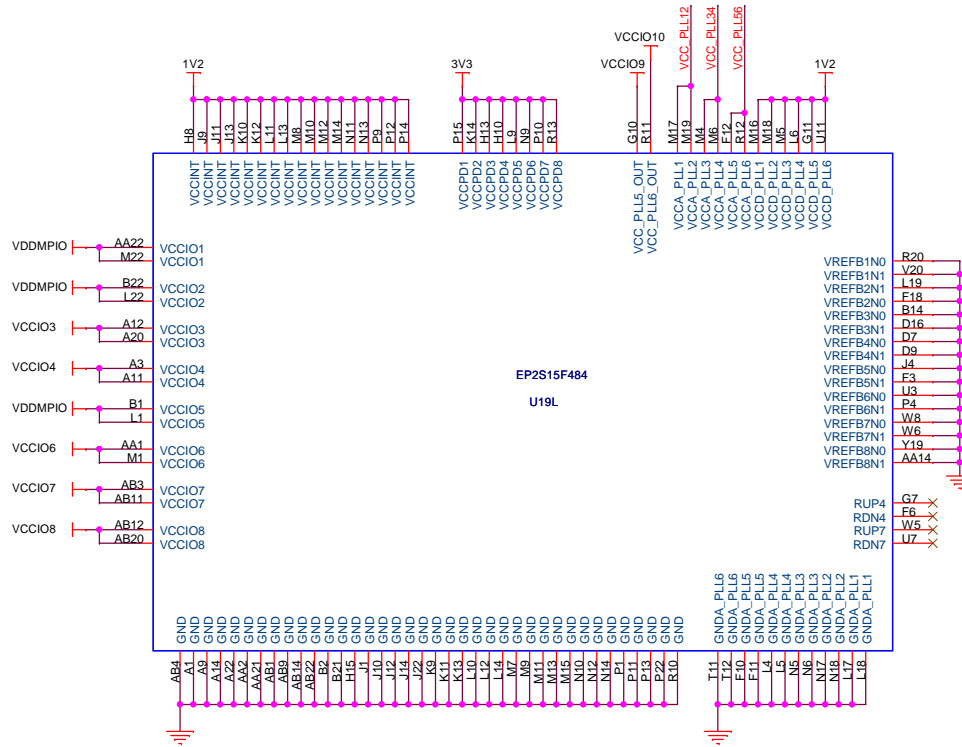
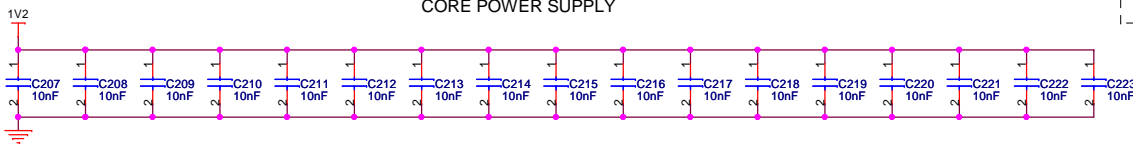
## MPIO POWER SUPPLY



## FPGA I/O POWER SUPPLY



## CORE POWER SUPPLY



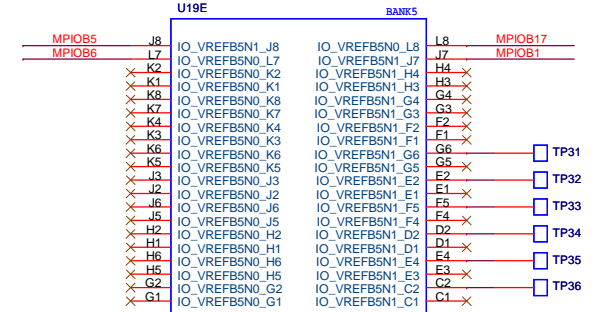
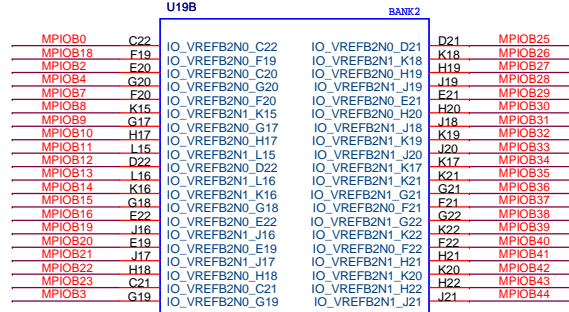
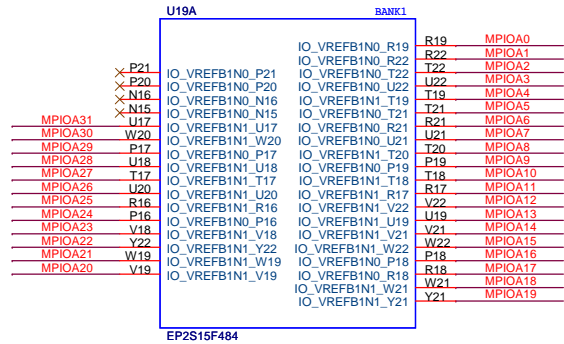
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Proj / Project <b>CAP9-STK</b>					
Schéma électronique / Schematic <b>FPGA POWER</b>					
Rév. / Date C02/21/05/08	Auteur / OBO	Historique / Background history Creation		Format A3	Dessinateur / Drawer O. Boitet
				Référence / Reference ADEC101389001	Rév. C02
Date: Wednesday, May 21, 2008					
				Page 11 de / of 21	

# FPGA IO Bank

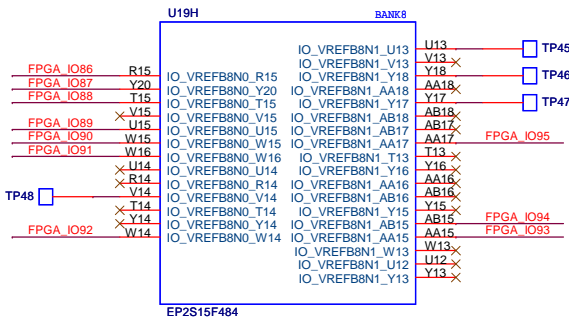
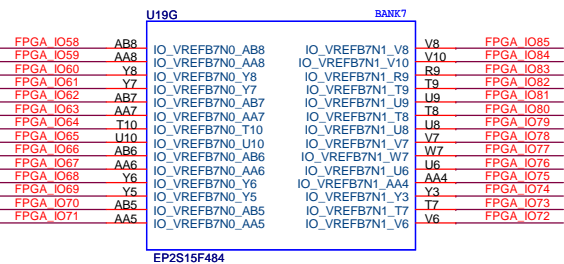
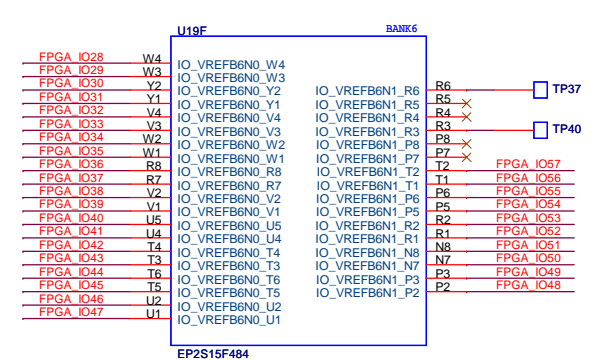
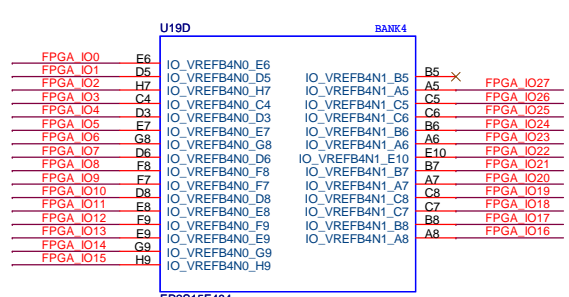
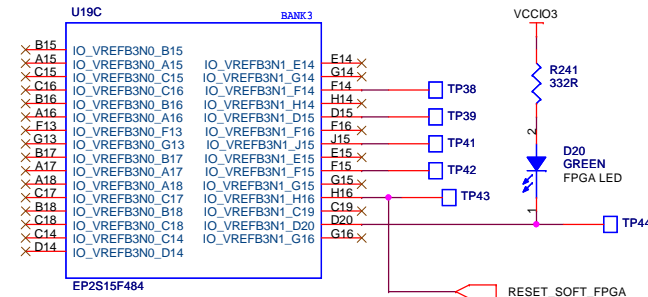
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 MPIOB[0..44] <=> MPIOB[0..44]  
 FPGA\_IO[0..95] <=> FPGA\_IO[0..95]

MPIOB24 <=> MPIOB24

## MPIO BUS

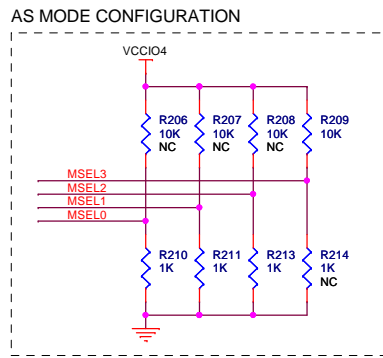
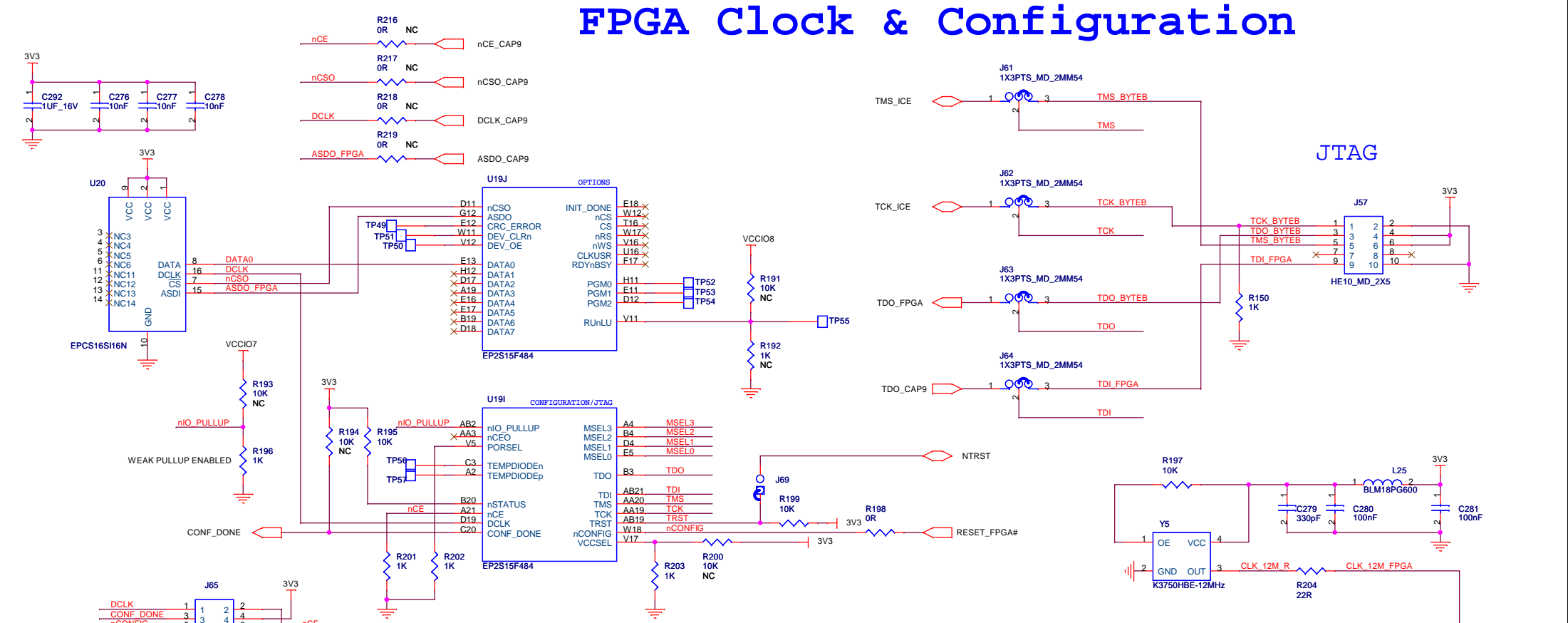


## SPARES IO

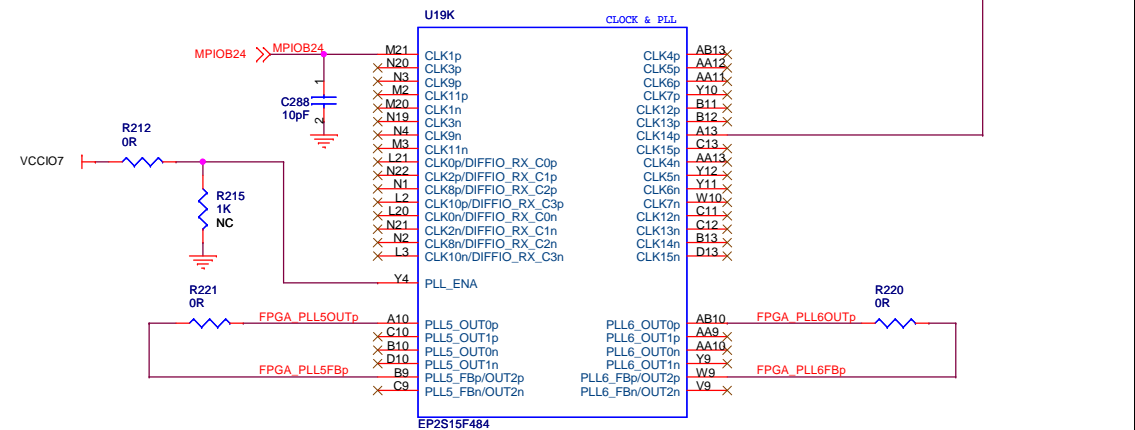


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Rév. : C02/21/05/08 Date : 08/05/2002 Auteur : OBO Historique / Background history : Création	Format : A3 Dessinateur / Drawer : O. Boitet Date : Tuesday, May 20, 2008	Référence / Reference : ADEC101389001	Rév. : C02 Date :	Page : 12 de / of 21	Date : Tuesday, May 20, 2008

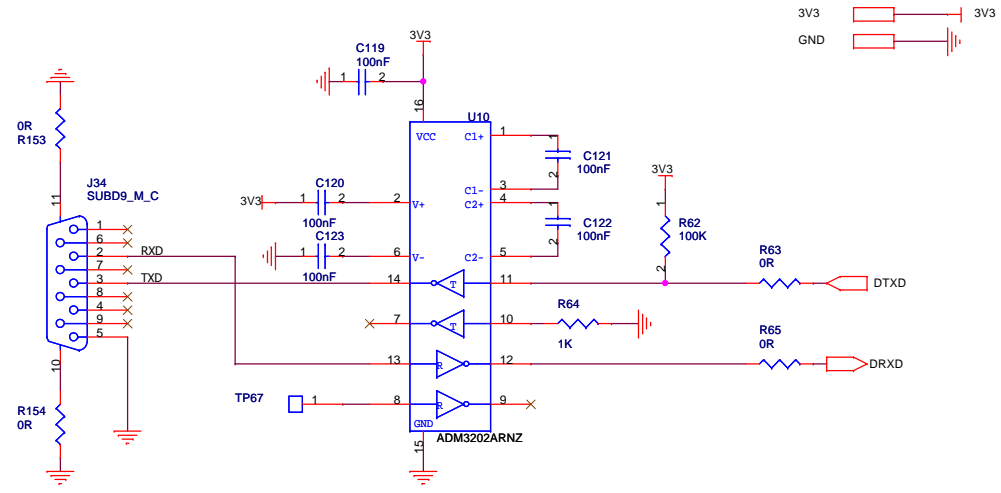
# FPGA Clock & Configuration



CONFIGURATION SCHEME	MSEL3	MSEL2	MSEL1	MSEL0
Fast AS (40 MHz)	1	0	0	0
Remote system upgrade fast AS (40 MHz)	1	0	0	1
AS (20 MHz)	1	1	0	1
Remote system upgrade AS (20 MHz)	1	1	1	0

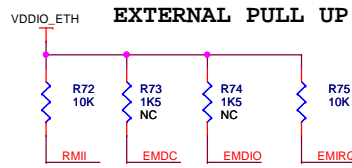
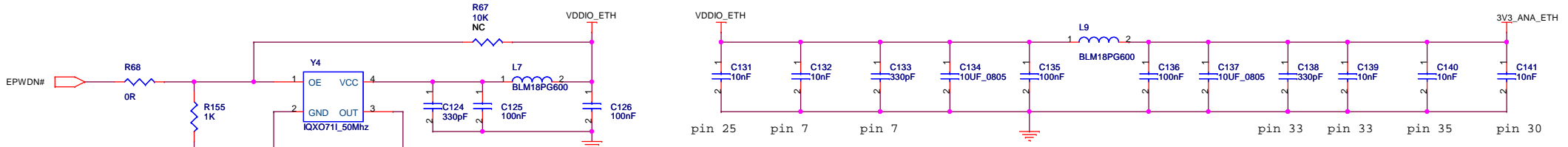
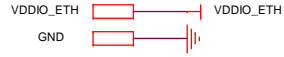


# Serial Debug Port



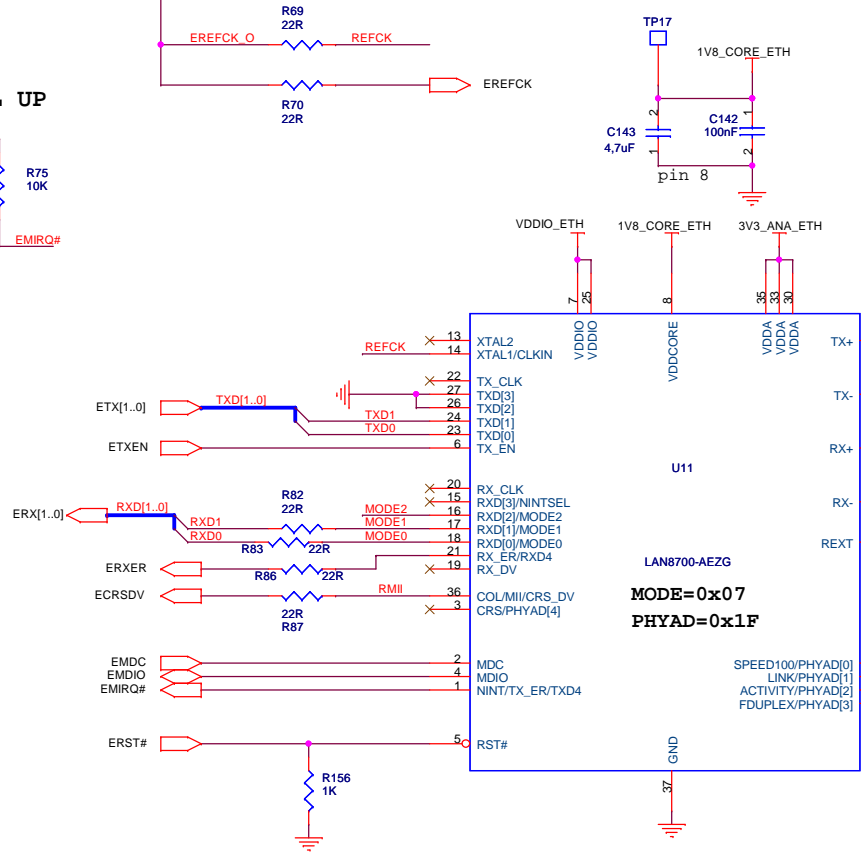
2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com				Projet / Project <b>CAP9-STK</b>	
Schéma électronique / Schematic <b>DEBUG</b>				Révision / Reference ADEC101389001	
Rév. C02	Date 21/05/08	Auteur OBO	Historique / Background history Création	Format A3	Dessinateur / Drawer O. Boitet
Date: Tuesday, May 20, 2008				Page 14 de / of 21	

# 10/100 RMII SMSC Ethernet



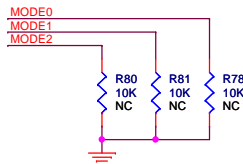
R72 Digital communication mode  
Empty = MII mode  
Populated = RMII mode

R73 (EMDC) and R74 (EMDIO)  
Pullup to 3V3 is normally  
pulled up by the MAC

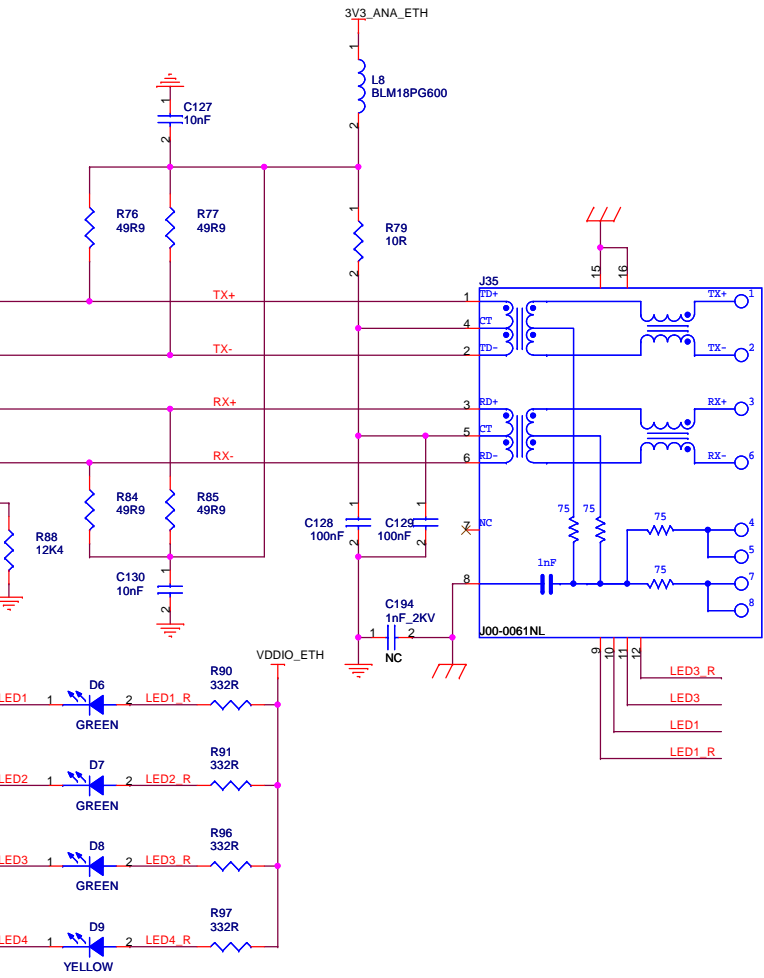


Internal Pull-up on PHYADx, MODEx, RST#, NINT  
Internal Pull-down on MDIO, MDC, RX\_ER, RX\_CLK, TX\_EN, COL/MI/CRS\_DV

## EXTERNAL PULL DOWN



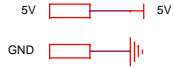
Mode 2 R32	Mode 1 R15	Mode 0 R16		
Empty	Empty	Empty	111	All Capable [Default]
Empty	Empty	Populated	110	Power Down Mode
Empty	Populated	Empty	101	Repeater Mode
Empty	Populated	Populated	100	100Base-TX Half duplex Advertised
Populated	Empty	Empty	011	100Base-TX Full Duplex Auto Negotiate
Populated	Populated	Empty	010	100Base-TX Half Duplex Auto Negotiate
Populated	Populated	Populated	001	10Base-T Full Duplex Auto Negotiate
Populated	Populated	Populated	000	10Base-T Half Duplex Auto Negotiate



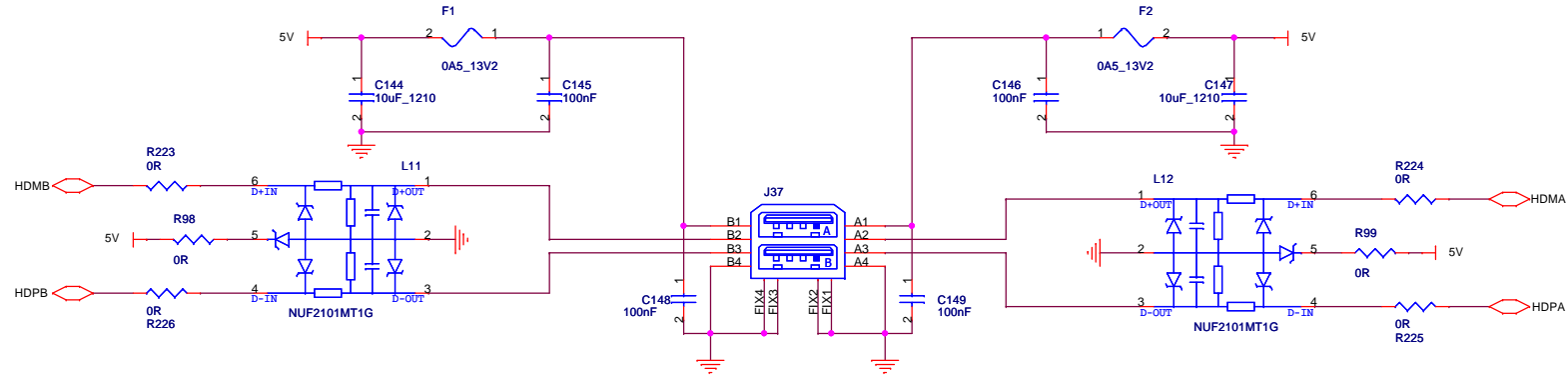
		2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com		Projet / Project <b>CAP9-STK</b>	
Rév. Date Auteur Historique / Background history C02/21/05/081 OBO 1 Création				Schéma électronique / Schematic <b>ETHERNET SMSC</b>	
Format A3		Dessinateur / Drawer O. Boitet		Référence / Reference ADEC101389001	
Date: Tuesday, May 20, 2008				Page 15 de / of 21	



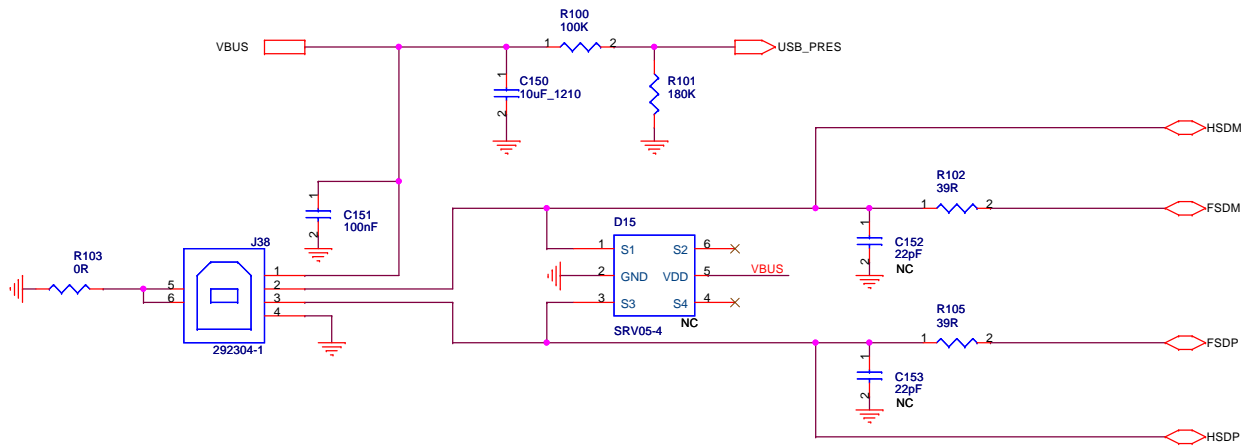
# USB Interfaces




## USB HOST INTERFACE



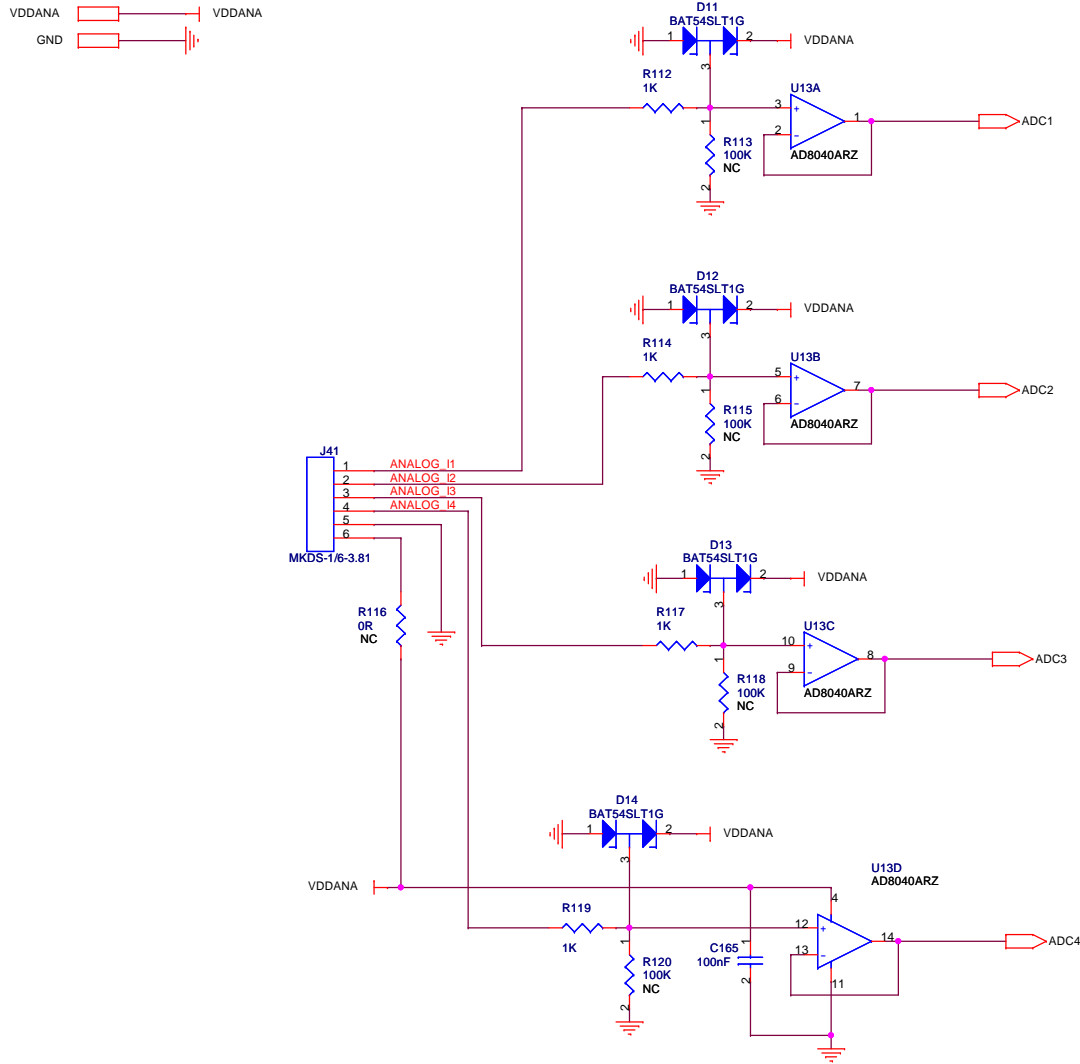
## USB DEVICE INTERFACE



		2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com		Projet / Project <b>CAP9-STK</b>	
Schéma électronique / Schematic <b>USB HOST &amp; DEVICE</b>				Révision / Reference ADEC101389001	
Rév. A3	Date 02/21/05/08	Auteur OBO	Historique / Background history 1 Création	Format A3	Dessinateur / Drawer O. Boitet
Date: Tuesday, May 20, 2008				Page 16 de / of 21	



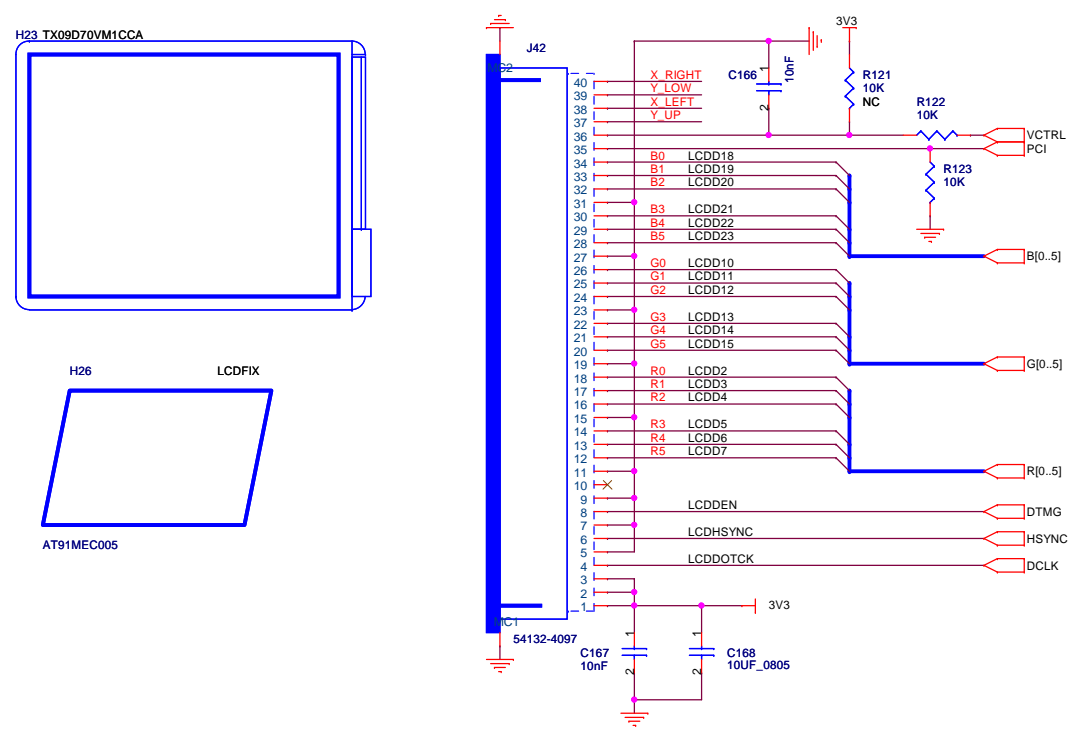
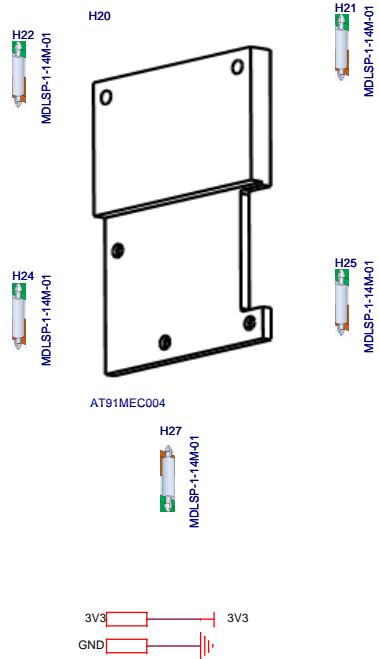
# Analog Inputs



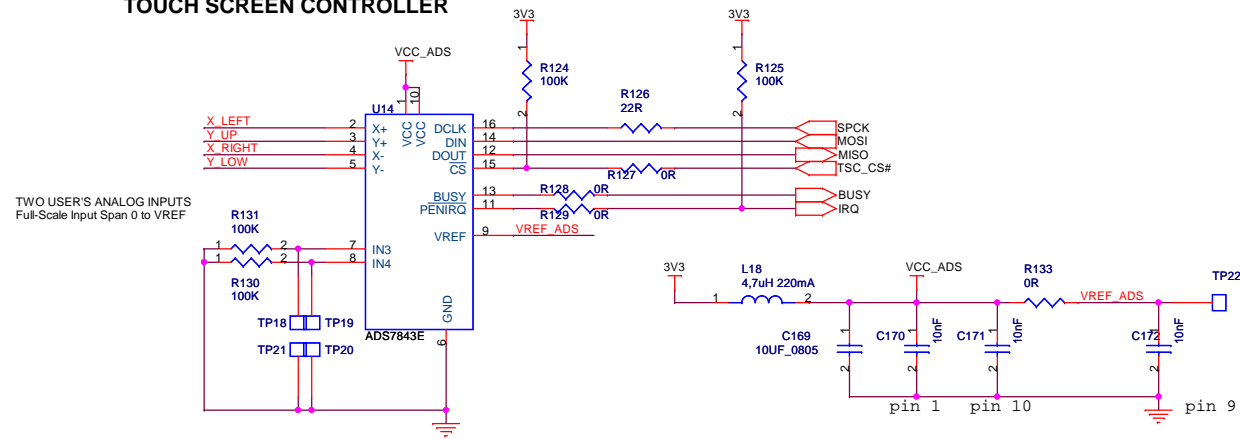
		2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com		Projet / Project <b>CAP9-STK</b>	
Rév. Date Auteur Historique / Background history C02/21/05/08 OBO 1 Création				Schéma électronique / Schematic <b>ANALOG</b>	
Format A3		Dessinateur / Drawer O. Boitet		Référence / Reference ADEC101389001	
Date: Tuesday, May 20, 2008		Page 18 de / of 21		Rév. C02	

# LCD Connector & Touch Screen Controller

## 3.5-inch 1/4 VGA TFT LCD DISPLAY

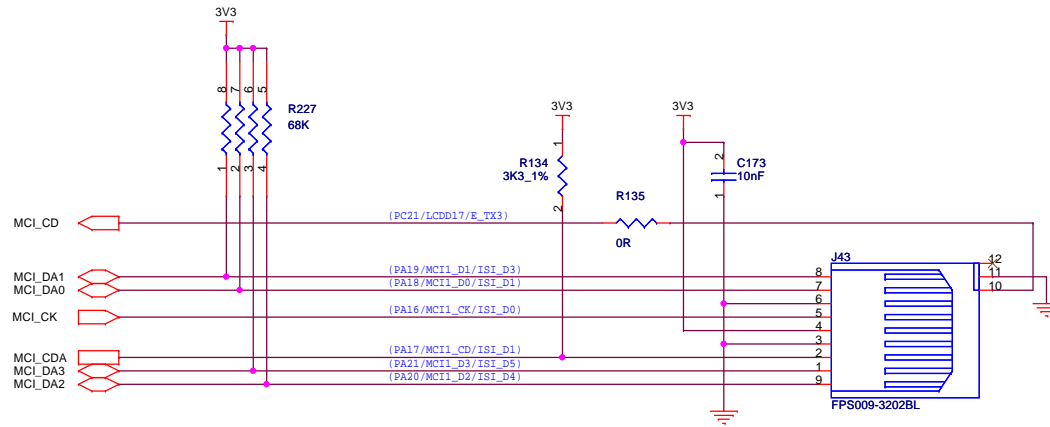
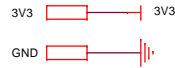


## TOUCH SCREEN CONTROLLER



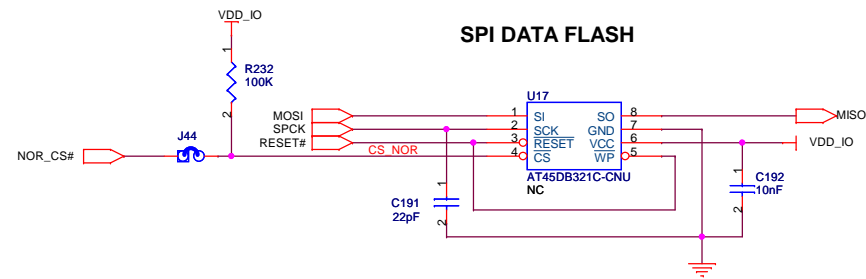
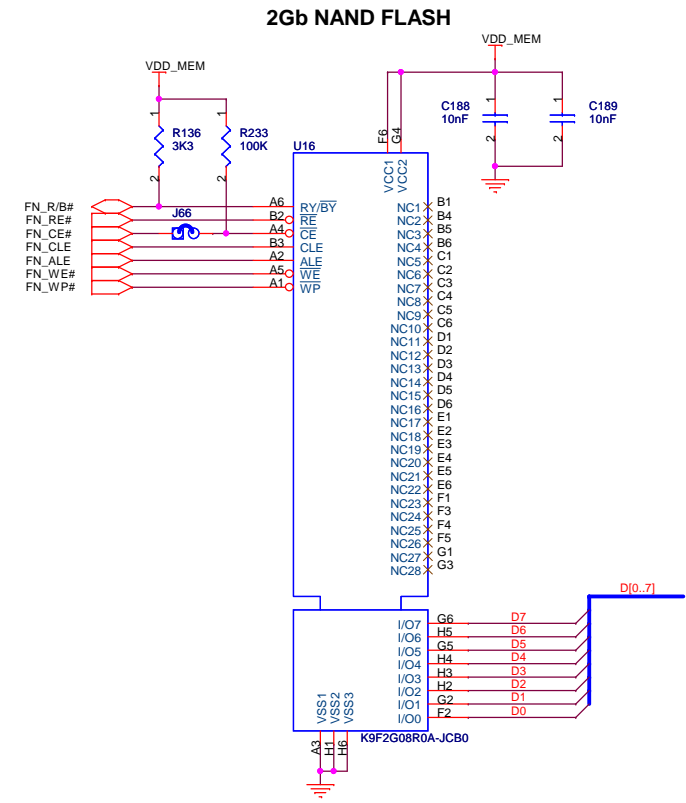
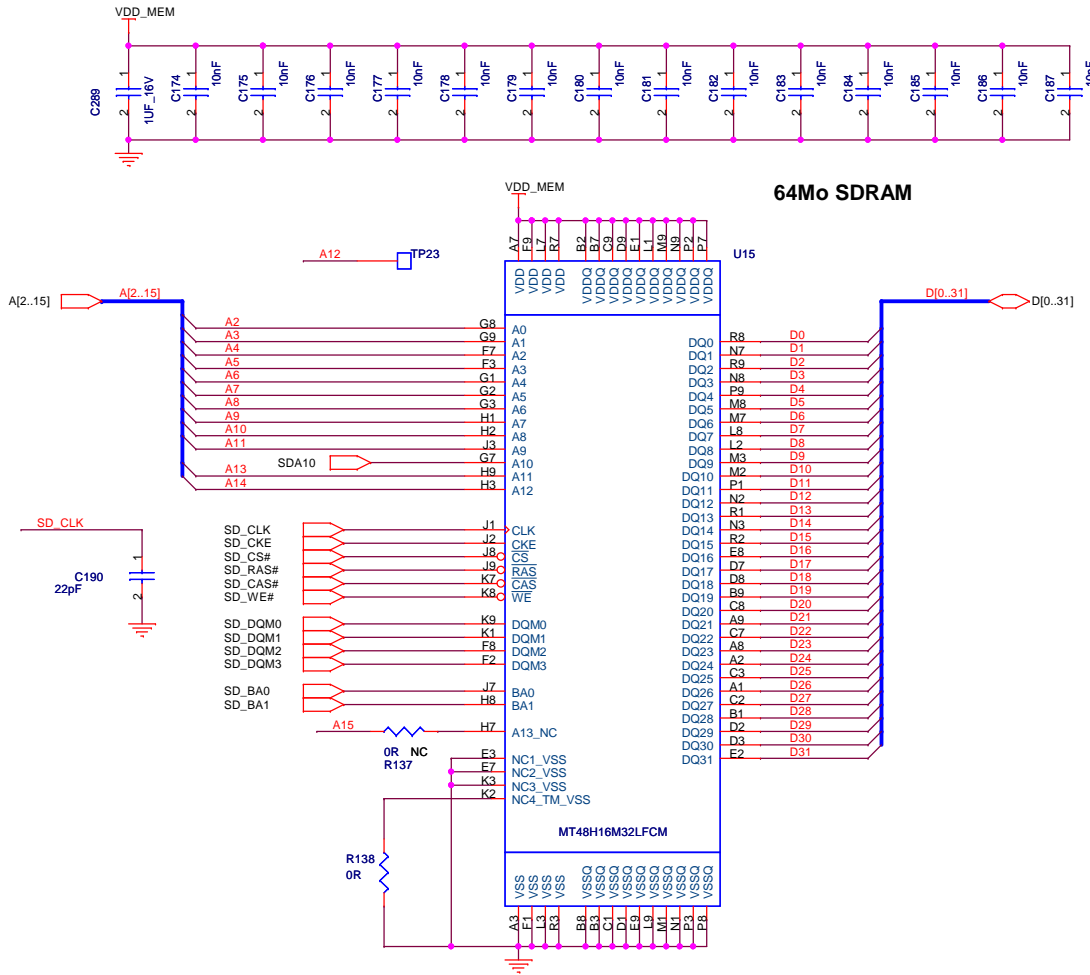
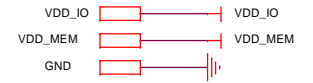
		2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com		Projet / Project <b>CAP9-STK</b>	
		Schéma électronique / Schematic <b>LCD &amp; TSC</b>			
Rév. A3 Date: 02/21/05/08	Auteur: OBO Historique / Background history: Création	Format: A3 Dessinateur / Drawer: O. Boitet	Référence / Reference: ADEC101389001	Rév. C02	Date: Tuesday, May 20, 2008
		Page 19 de / of 21			

# SDCARD Interface



2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com				Projet / Project <b>CAP9-STK</b>						
Schéma électronique / Schematic <b>SDCARD</b>				Format A3		Dessinateur / Drawer O. Boitet		Référence / Reference ADEC101389001		Rév. C02
Rév. C02	Date 21/05/08	Auteur OBO	Historique / Background history Création	Date Tuesday, May 20, 2008	Page 20	de / of 21	Rév. C02	Page 1	de / of 21	

# SDRAM & Flash Memories



2, Chemin du Ruisseau BP 121 69136 Ecully Tél : 04 72 18 08 40 Fax : 04 72 18 08 41 www.adeneo.adetelgroup.com		Projet / Project <b>CAP9-STK</b> Schéma électronique / Schematic <b>SDRAM, NAND &amp; DATAFLASH</b>	
Rév. Date Auteur Historique / Background history C02/21/05/08 OBO Création	Format A3 Dessinateur / Drawer O. Boitet Date: Tuesday, May 20, 2008	Référence / Reference ADEC101389001 Page 21 de / of 21	Rév. C02



## Section 5

# Revision History

### 5.1 Revision History

Document	Comments	Change Request Ref
6351A	First Issue	
6351B	<a href="#">Section "AT91CAP9-STK Schematics" on page 4-1</a> updated <a href="#">Section 1.2 on page 1-1</a> , removed "A" from AT91CAP9-STK	5606



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[www.atmel.com/AT91CAP](http://www.atmel.com/AT91CAP)

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