## Features

- **Read Access Time – 100 ns**
- **Word-wide or Byte-wide Configurable**
- **8-megabit Flash and Mask ROM Compatible**
- **Low-power CMOS Operation**
  - **– 100 µA Maximum Standby**
  - **– 50 mA Maximum Active at 5 MHz**
- **Wide Selection of JEDEC Standard Packages**
  - **– 42-pin 600 mil PDIP**
  - **– 44-lead PLCC**
  - **– 44-lead SOIC (SOP)**
  - **– 48-lead TSOP (12 mm x 20 mm)**
- **5V ± 10% Power Supply**
- **High-reliability CMOS Technology**
  - **– 2,000 ESD Protection**
  - **– 200 mA Latch-up Immunity**
- **Rapid™ Programming Algorithm – 50 µs/Word (Typical)**
- **CMOS- and TTL-compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

## Description

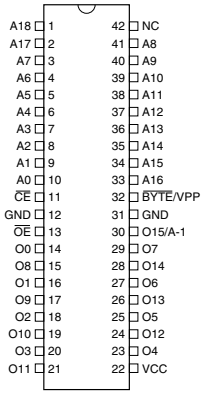
The AT27C800 is a low-power, high-performance, 8,388,608-bit, UV-erasable, programmable read-only memory (EPROM) organized as either 512K by 16 or 1024K by

*(continued)*

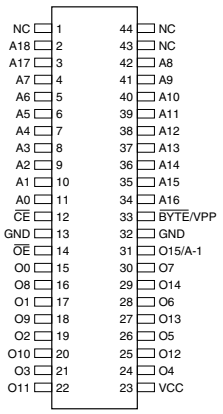
## Pin Configurations

| Pin Name | Function |
|---|---|
| A0 - A18 | Addresses |
| O0 - O15 | Outputs |
| O15/A-1 | Output/Address |
| $\overline{BYTE}$/VPP | Byte Mode/ Program Supply |
| CE | Chip Enable |
| OE | Output Enable |
| NC | No Connect |

PDIP Top View

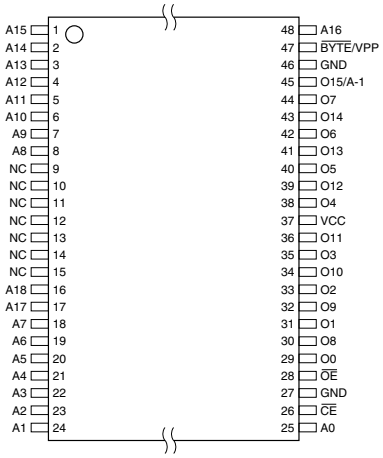



SOIC (SOP)

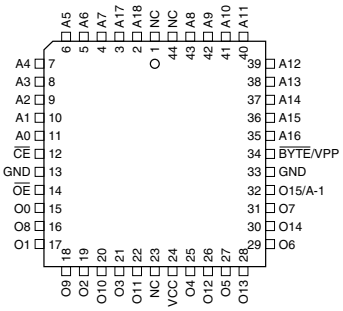



TSOP

**Type 1**




PLCC Top View




Note: PLCC Package Pin 23 is DON'T CONNECT.

# 8-megabit (512K x 16 or 1024K x 8) OTP EPROM

# AT27C800

**Not Recommended for New Designs**

Rev. 0801C–05/00

8 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 100 ns, eliminating the need for speed-reducing WAIT states. The x16 organization makes this part ideal for high-performance 16- and 32-bit microprocessor systems.

The AT27C800 can be organized as either word-wide or byte-wide. The organization is selected via the $\overline{BYTE}/V_{PP}$ pin. When $\overline{BYTE}/V_{PP}$ is asserted high ($V_{IH}$), the word-wide organization is selected and the O15/A-1 pin is used for O15 data output. When $\overline{BYTE}/V_{PP}$ is asserted low ($V_{IL}$), the byte-wide organization is selected and the O15/A-1 pin is used for the address pin A-1. When the AT27C800 is logically regarded as x16 (word-wide), but read in the byte-wide mode, then with A-1 = $V_{IL}$ the lower eight bits of the 16-bit word are selected; with A-1 = $V_{IH}$ the upper eight bits of the 16-bit word are selected.

In read mode, the AT27C800 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C800 is available in industry-standard, JEDEC-approved, one-time programmable (OTP) PLCC, PDIP, SOIC (SOP) and TSOP, as well as UV-erasable windowed Cerdip packages. The device features two-line control ($\overline{CE}$,$\overline{OE}$) to eliminate bus contention in high-speed systems.

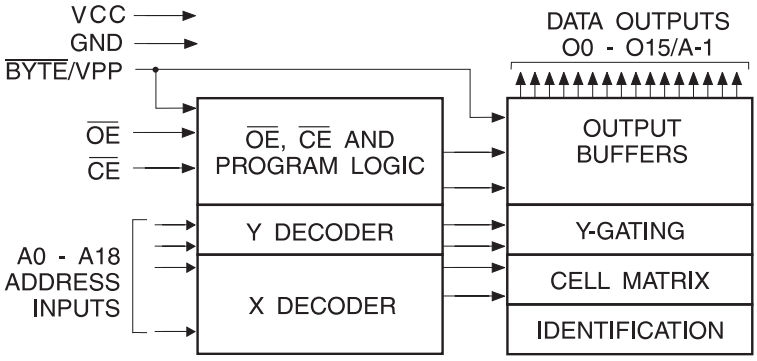
With high-density 512K-word or 1024K-bit storage capability, the AT27C800 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C800 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming equipment and voltages.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the $V_{CC}$ and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the $V_{CC}$ and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram



## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with with Respect to Ground | -2.0V to +7.0V(1) |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V(1) |
| $V_{PP}$ Supply Voltage with Respect to Ground | -2.0V to +14.0V(1) |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V DC, which may overshoot to + 7.0V for pulses of less than 20 ns.

## Operating Modes

| Mode\Pin | $\overline{CE}$ | $\overline{OE}$ | Ai | $\overline{BYTE}/V_{PP}$ | Outputs | | |
|---|---|---|---|---|---|---|---|
| | | | | | $O_0$ - $O_7$ | $O_8$ - $O_{14}$ | $O_{15}$/A-1 |
| Read Word-wide | $V_{IL}$ | $V_{IL}$ | X(1) | $V_{IH}$ | $D_{OUT}$ | $D_{OUT}$ | $D_{OUT}$ |
| Read Byte-wide Upper | $V_{IL}$ | $V_{IL}$ | X(1) | $V_{IL}$ | $D_{OUT}$ | High-Z | $V_{IH}$ |
| Read Byte-wide Lower | $V_{IL}$ | $V_{IL}$ | X(1) | $V_{IL}$ | $D_{OUT}$ | High-Z | $V_{IL}$ |
| Output Disable | X(1) | $V_{IH}$ | X(1) | X | | High-Z | |
| Standby | $V_{IH}$ | X(1) | X(1) | X(5) | | High-Z | |
| Rapid Program(2) | $V_{IL}$ | $V_{IH}$ | Ai | $V_{PP}$ | | $D_{IN}$ | |
| PGM Verify | X | $V_{IL}$ | Ai | $V_{PP}$ | | $D_{OUT}$ | |
| PGM Inhibit | $V_{IH}$ | $V_{IH}$ | X(1) | $V_{PP}$ | | High-Z | |
| Product Identification(4) | $V_{IL}$ | $V_{IL}$ | A9 = $V_H$(3)<br>A0 = $V_{IH}$ or $V_{IL}$<br>A1 - A18 = $V_{IL}$ | $V_{IH}$ | Identification Code | | |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to the programming characteristics tables in this datasheet.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier words may be selected. All Ai inputs are held low ($V_{IL}$) except A9, which is set to $V_H$, and A0, which is toggled low ($V_{IL}$) to select the Manufacturer's Identification word and high ($V_{IH}$) to select the Device Code word.
5. Standby $V_{CC}$ current ($I_{SB}$) is specified with $V_{PP} = V_{CC}$. $V_{CC} > V_{PP}$ will cause a slight increase in $I_{SB}$.

## DC and AC Operating Conditions for Read Operation

| | | AT27C800 | | |
|---|---|---|---|---|
| | | -10 | -12 | -15 |
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| $V_{CC}$ Power Supply | | 5V ± 10% | 5V ± 10% | 5V ± 10% |

## DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | | ±1.0 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | | ±5.0 | µA |
| $I_{PP1}$[2] | $V_{PP}$[1] Read/Standby Current | $V_{PP}$ = $V_{CC}$ | | ±10 | µA |
| $I_{SB}$ | $V_{CC}$[1] Standby Current | $I_{SB1}$ (CMOS), $\overline{CE}$ = $V_{CC}$ ± 0.3V | | 100 | µA |
| | | $I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | 1.0 | mA |
| | $V_{CC}$ Active Current | f = 5 MHz, $I_{OUT}$ = 0 mA, $\overline{CE}$ = $V_{IL}$ | | 50 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$= 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 mA | 2.4 | | V |

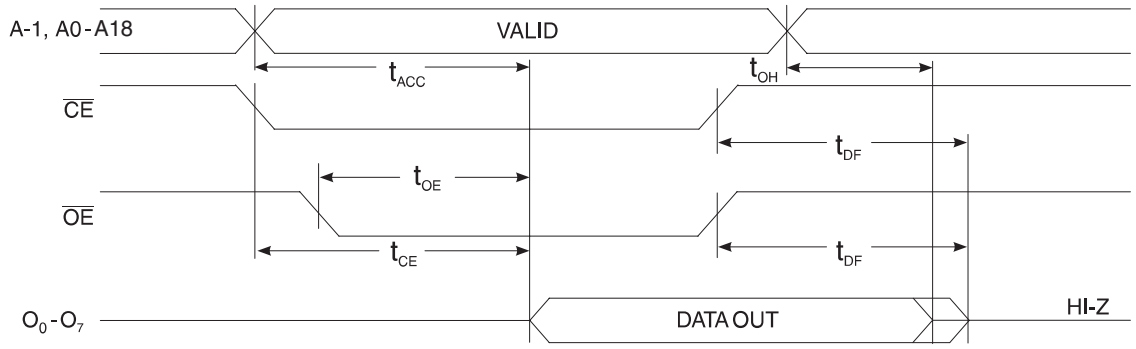
Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$, and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP}$.

## AC Characteristics for Read Operation

| | | | AT27C800 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | -10 | | -12 | | -15 | | |
| Symbol | Parameter | Condition | Min | Max | Min | Max | Min | Max | Units |
| $t_{ACC}$[3] | Address to Output Delay | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 100 | | 120 | | 150 | ns |
| $t_{CE}$[2] | $\overline{CE}$ to Output Delay | $\overline{OE}$ = $V_{IL}$ | | 100 | | 120 | | 150 | ns |
| $t_{OE}$[2,3] | $\overline{OE}$ to Output Delay | $\overline{CE}$ = $V_{IL}$ | | 40 | | 40 | | 50 | ns |
| $t_{DF}$[4,5] | $\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occured first | | | 30 | | 35 | | 40 | ns |
| $t_{OH}$[4] | Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occured first | | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_{ST}$ | $\overline{BYTE}$ High to Output Valid | | | 100 | | 120 | | 150 | ns |
| $t_{STD}$ | $\overline{BYTE}$ Low to Output Transition | | | 40 | | 50 | | 60 | ns |

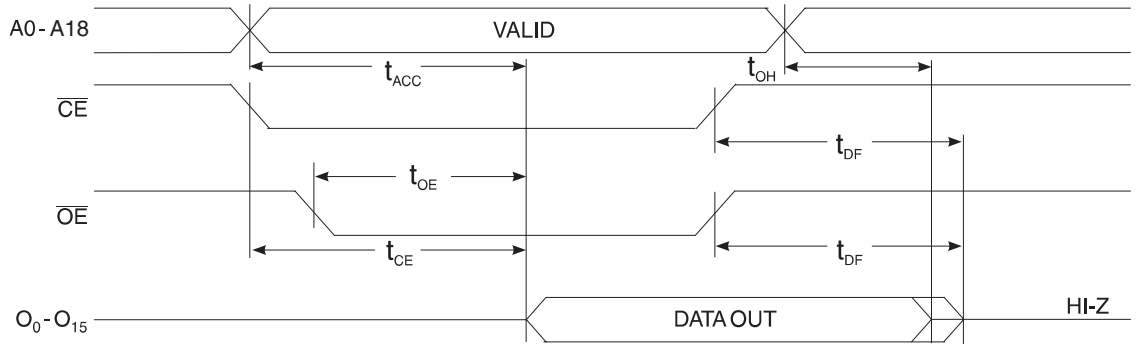
Note: 2,3,4,5. See the AC Waveforms for Read Operation diagram.

## Byte-wide Read Mode AC Waveforms(1)



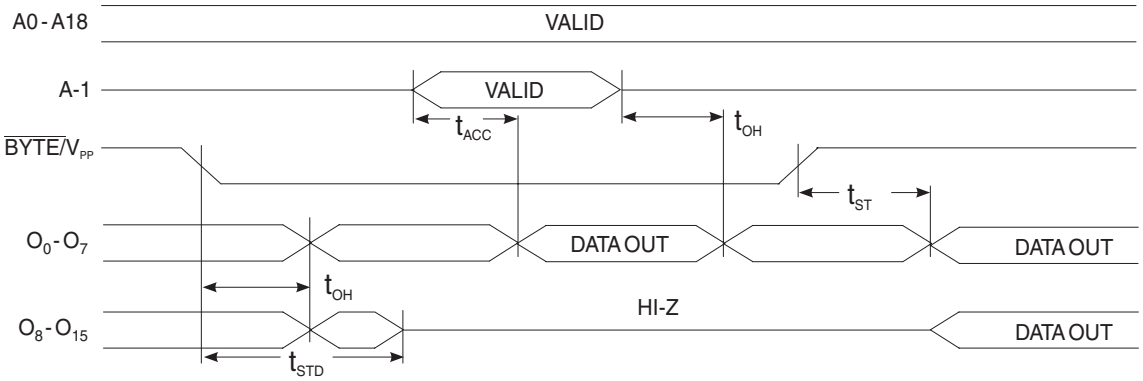

Note: 1. $\overline{BYTE}/V_{PP} = V_{IL}$

## Byte-wide Read Mode AC Waveforms(1)



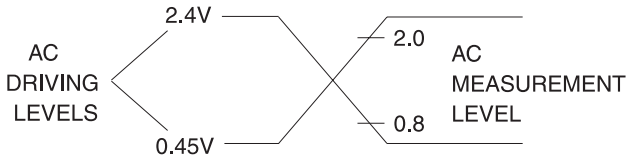

Note: 1. $\overline{BYTE}/V_{PP} = V_{IH}$

## $\overline{BYTE}$ Transition AC Waveforms



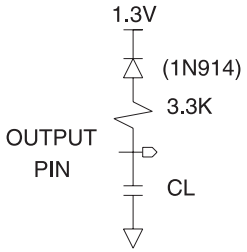

Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on $t_{ACC}$.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

## Input Test Waveforms and Measurement Levels




$t_R$, $t_F$ < 20 ns (10% to 90%)

## Output Test Load




Note: CL = 100 pF including jig capacitance.

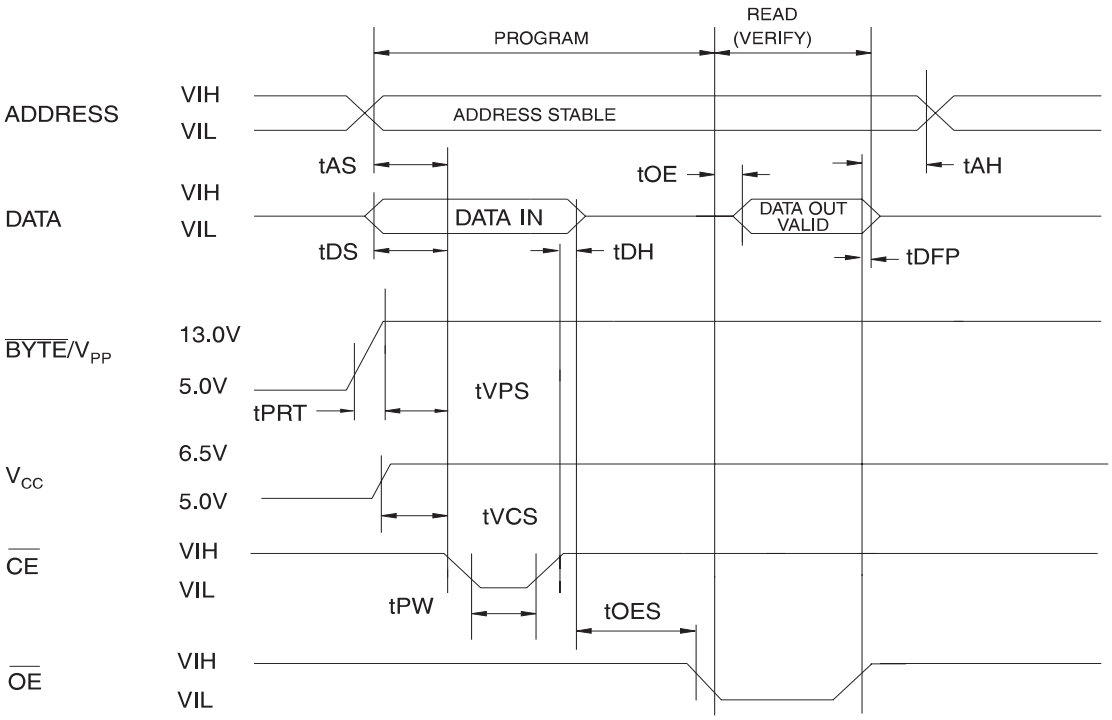
## Pin Capacitance

f = 1 MHz, T = 25°C[1]

| Symbol | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 10 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Programming Waveforms[1]




Notes: 1. The Input Timing reference is 0.8V for $V_{IL}$ and 2.0V for $V_{IH}$.

2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.

3. When programming the AT27C800, a 0.1 µF capacitor is required across $V_{PP}$ and ground to suppress voltage transients.

## DC Programming Characteristics

$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ± 0.25V

| Symbol | Parameter | Test Conditions | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ±10 | µA |
| $V_{IL}$ | Input Low Level | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | 50 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL}$ | | 30 | mA |
| $V_{ID}$ | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

## AC Programming Characteristics

$T_A$ = 25 ± 5°C, $V_{CC}$ = 6.5 ± 0.25V, $V_{PP}$ = 13.0 ± 0.25V

| Symbol | Parameter | Test Conditions[1] | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{AS}$ | Address Setup Time | Input Rise and Fall Times: (10% to 90%) 20 ns<br>Input Pulse Levels: 0.45V to 2.4V<br>Input Pulse Levels: 0.8V to 2.0V<br>Input Timing Reference Level: 0.8V to 2.0V<br>Output Timing Reference Level: 0.8V to 2.0V | 2 | | µs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | µs |
| $t_{DFP}$ | $\overline{OE}$ High to Output Float Delay[2] | | 0 | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | µs |
| $t_{PW}$ | $\overline{CE}$ Program Pulse Width[3] | | 47.5 | 52.5 | µs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | 150 | ns |
| $t_{PRT}$ | $\overline{BYTE}$ /$V_{PP}$ Pulse Rise Time During Programming | | 50 | | ns |

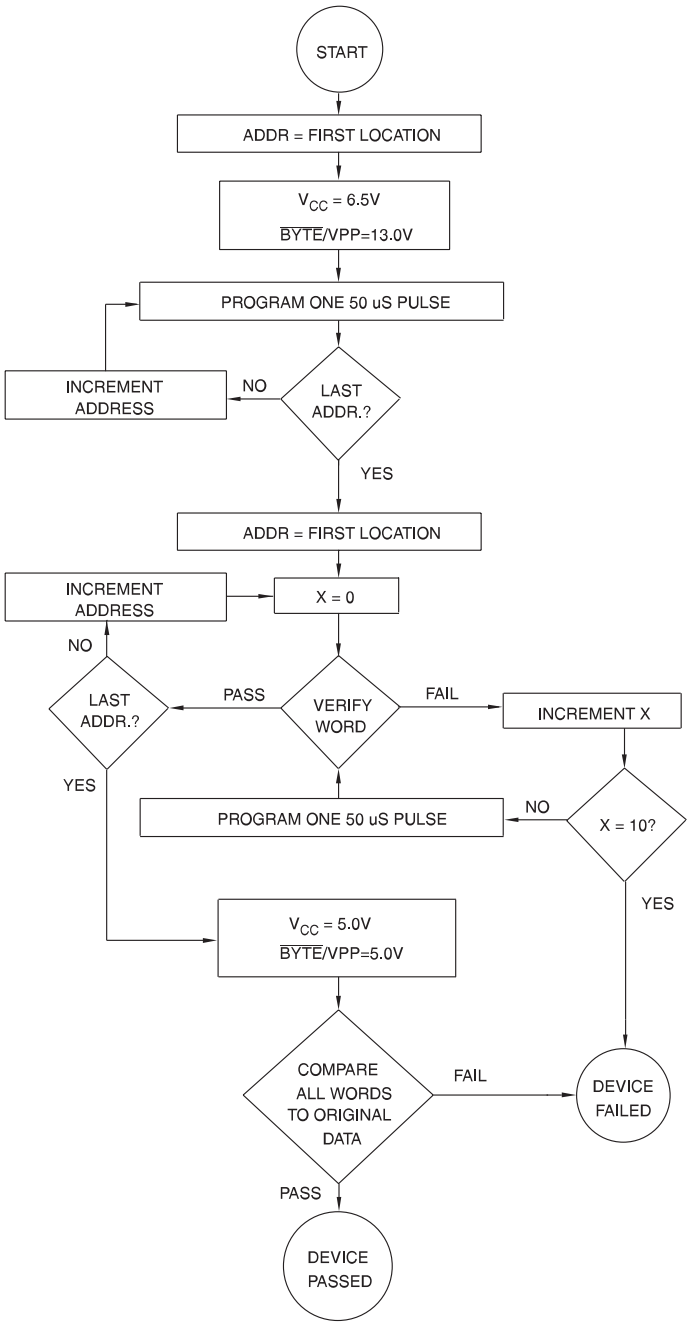
Notes:
1. $V_{cc}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Program Pulse width tolerance is 50 µs ± 5%.

## Atmel's 27C800 Integrated Product Identification Code

| | Pins | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 | |
| Codes | | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | Hex Data |
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E1E |
| Device Type | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F8F8 |

## Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. $V_{CC}$ is raised to 6.5V and $\overline{BYTE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. $V_{PP}$ is then lowered to 5.0V and $V_{CC}$ to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



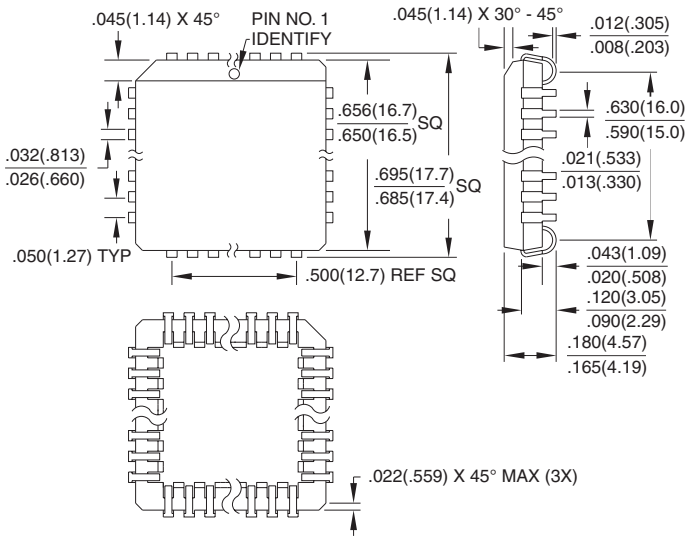
## Ordering Information

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 100 | 50 | 0.1 | AT27C800-10JC<br>AT27C800-10PC<br>AT27C800-10RC<br>AT27C800-10TC | 44J<br>42P6<br>44R<br>48T | Commercial<br>(0°C to 70°C) |
| | 50 | 0.1 | AT27C800-10JI<br>AT27C800-10PI<br>AT27C800-10RI<br>AT27C800-10TI | 44J<br>42P6<br>44R<br>48T | Industrial<br>(-40°C to 85°C) |
| 120 | 50 | 0.1 | AT27C800-12JC<br>AT27C800-12PC<br>AT27C800-12RC<br>AT27C800-12TC | 44J<br>42P6<br>44R<br>48T | Commercial<br>(0°C to 70°C) |
| | 50 | 0.1 | AT27C800-12JI<br>AT27C800-12PI<br>AT27C800-12RI<br>AT27C800-12TI | 44J<br>42P6<br>44R<br>48T | Industrial<br>(-40°C to 85°C) |
| 150 | 50 | 0.1 | AT27C800-15JC<br>AT27C800-15PC<br>AT27C800-15RC<br>AT27C800-15TC | 44J<br>42P6<br>44R<br>48T | Commercial<br>(0°C to 70°C) |
| | 50 | 0.1 | AT27C800-15JI<br>AT27C800-15PI<br>AT27C800-15RI<br>AT27C800-15TI | 44J<br>42P6<br>44R<br>48T | Industrial<br>(-40°C to 85°C) |

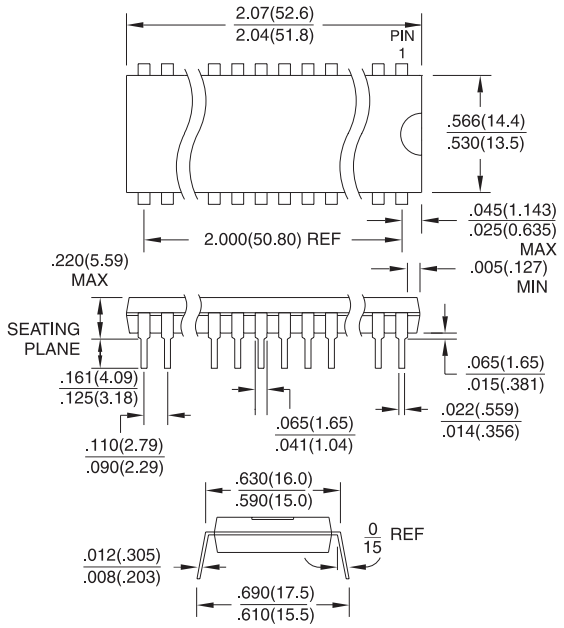
| Package Type | |
|---|---|
| **44J** | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **42P6** | 42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **44R** | 44-lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP) |
| **48T** | 48-lead, Plastic Thin Small Outline Package (TSOP) 12 x 20 mm |

## Packaging Information

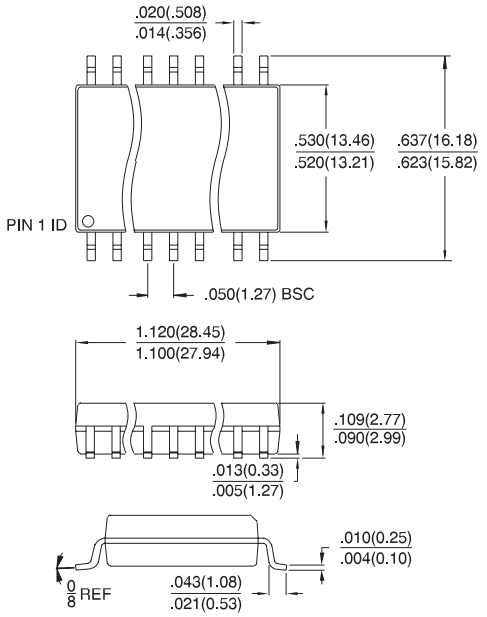
**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



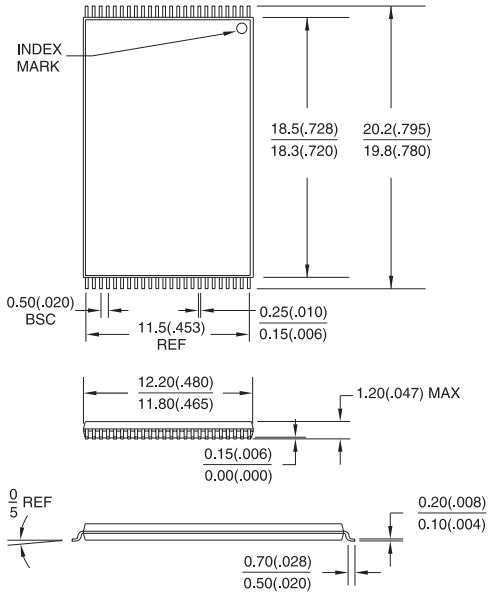

**42P6**, 42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)




**44R**, 44-lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)




**48T**, 48-lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 DD




*Controlling dimension: millimeters

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