

Features

- Fast Read Access Time – 90 ns
- Word-wide or Byte-wide Configurable
- 4-megabit Flash and Mask ROM Compatible
- Low-power CMOS Operation
 - 100 μ A Maximum Standby
 - 50 mA Maximum Active at 5 MHz
- Wide Selection of JEDEC Standard Packages
 - 40-lead 600 mil PDIP
 - 44-lead SOIC (SOP)
 - 48-lead TSOP (12 mm x 20 mm)
- 5V \pm 10% Power Supply
- High-reliability CMOS Technology
 - 2,000V ESD Protection
 - 200 mA Latch-up Immunity
- Rapid™ Programming Algorithm – 50 μ s/Word (Typical)
- CMOS- and TTL-compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C400 is a low-power, high-performance, 4,194,304-bit, one-time programmable read-only memory (OTP EPROM) organized as either 256K by 16 or 512K by 8 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 90 ns, eliminating the need for speed-reducing WAIT states. The by-16 organization makes this part ideal for high-performance 16- and 32-bit microprocessor systems.

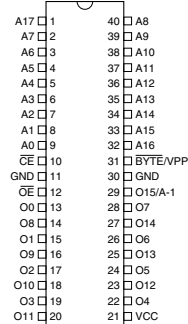
(continued)

Pin Configurations

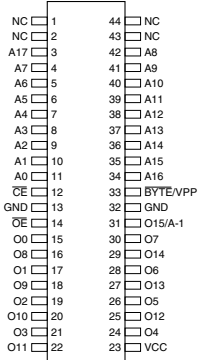
| Pin Name | Function |
|------------------------------|------------------------------|
| A0 - A17 | Addresses |
| O0 - O15 | Outputs |
| O15/A-1 | Output/Address |
| $\overline{\text{BYTE/VPP}}$ | Byte Mode/ Program Supply |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| NC | No Connect |

Note: Both GND pins must be connected.

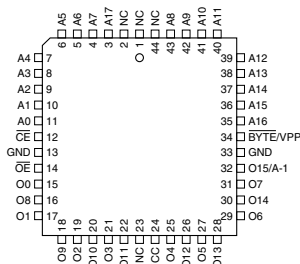
PDIP Top View



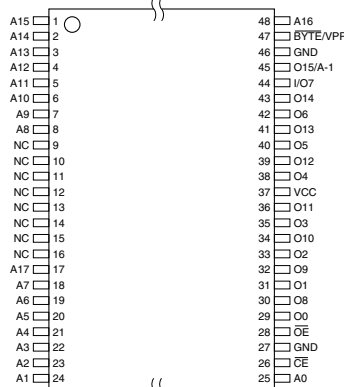
SOIC (SOP)



PLCC



TSOP
Type 1



4-megabit (256K x 16 or 512K x 8) OTP EPROM

AT27C400

**Not Recommended for
New Designs**



The AT27C400 can be organized as either word-wide or byte-wide. The organization is selected via the $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ pin. When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is asserted high (V_{IH}), the word-wide organization is selected and the O15/A-1 pin is used for O15 data output. When $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ is asserted low (V_{IL}), the byte-wide organization is selected and the O15/A-1 pin is used for the address pin A-1. When the AT27C400 is logically regarded as x16 (word-wide), but read in the byte-wide mode, then with A-1 = V_{IL} , the lower eight bits of the 16-bit word are selected and with A-1 = V_{IH} , the upper eight bits of the 16-bit word are selected.

In read mode, the AT27C400 typically consumes 15 mA. Standby mode supply current is typically less than 10 μA .

The AT27C400 is available in industry-standard, JEDEC-approved, one-time programmable (OTP) PDIP, SOIC (SOP) and TSOP packages. The device features two-line control ($\overline{\text{CE}}$, $\overline{\text{OE}}$) to eliminate bus contention in high-speed systems.

With high-density 256K word or 512K byte storage capability, the AT27C400 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

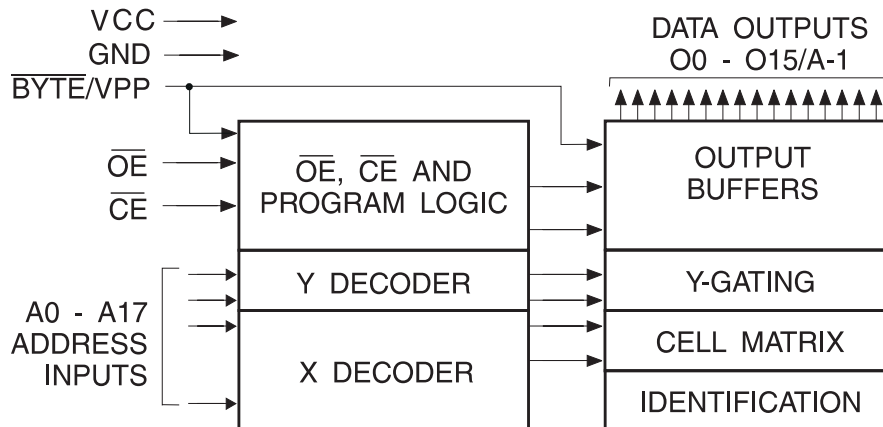
Atmel's AT27C400 has additional features that ensure high quality and efficient production use. The Rapid™

Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 μs /word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

| | |
|--|--------------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on A9 with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |
| V _{PP} Supply Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |
| Integrated UV Erase Dose..... | .7258 W •sec/cm ² |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which undershoots to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

| Mode/Pin | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | Ai | $\overline{\text{BYTE}}/\text{V}_{\text{PP}}$ | Outputs | | |
|---------------------------------------|------------------------|------------------------|---|---|---------------------------------|----------------------------------|----------------------|
| | | | | | O ₀ - O ₇ | O ₈ - O ₁₄ | O ₁₅ /A-1 |
| Read Word-wide | V _{IL} | V _{IL} | X ⁽¹⁾ | V _{IH} | D _{OUT} | D _{OUT} | D _{OUT} |
| Read Byte-wide Upper | V _{IL} | V _{IL} | X ⁽¹⁾ | V _{IL} | D _{OUT} | High-Z | V _{IH} |
| Read Byte-wide Lower | V _{IL} | V _{IL} | X ⁽¹⁾ | V _{IL} | D _{OUT} | High-Z | V _{IL} |
| Output Disable | X ⁽¹⁾ | V _{IH} | X ⁽¹⁾ | X | | High-Z | |
| Standby | V _{IH} | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽⁵⁾ | | High-Z | |
| Rapid Program ⁽²⁾ | V _{IL} | V _{IH} | Ai | V _{PP} | | D _{IN} | |
| PGM Verify | X | V _{IL} | Ai | V _{PP} | | D _{OUT} | |
| PGM Inhibit | V _{IH} | V _{IH} | X ⁽¹⁾ | V _{PP} | | High-Z | |
| Product Identification ⁽⁴⁾ | V _{IL} | V _{IL} | A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A17 = V _{IL} | V _{IH} | | Identification Code | |

- Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to the programming characteristics tables in this datasheet.
 3. V_H = 12.0 ± 0.5V.
 4. Two identifier words may be selected. All inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
 5. Standby V_{CC} current (ISB) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in ISB.

DC and AC Operating Conditions for Read Operation

| | | AT27C400 | | |
|------------------------------|------|--------------|--------------|--------------|
| | | -90 | -12 | -15 |
| Operating Temperature (Case) | Com. | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| V _{CC} Power Supply | | 5V ± 10% | 5V ± 10% | 5V ± 10% |

DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | Min | Max | Units |
|---------------------------------|---|---|------|-----------------------|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} | | ±1 | μA |
| I _{LO} | Output Leakage Current | V _{OUT} = 0V to V _{CC} | | ±5 | μA |
| I _{PP1} ⁽²⁾ | V _{PP} ⁽¹⁾ Read/Standby Current | V _{PP} = V _{CC} | | 10 | μA |
| I _{SB} | V _{CC} ⁽¹⁾ Standby Current | I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$ | | 100 | μA |
| | | I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V | | 1 | mA |
| | V _{CC} Active Current | f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$ | | 40 | mA |
| V _{IL} | Input Low Voltage | | -0.6 | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | V |

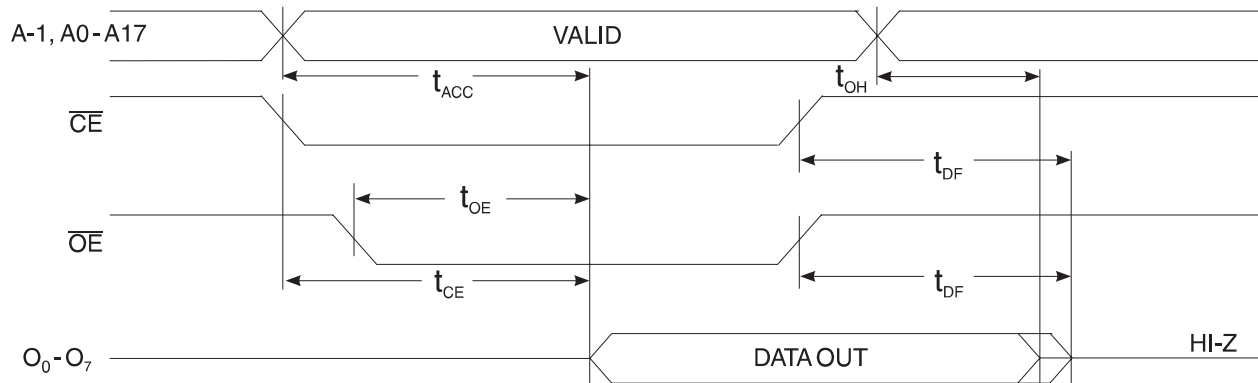
- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

| Symbol | Parameter | Condition | AT27C400 | | | | | | Units |
|-----------------------------------|---|--|----------|-----|-----|-----|-----|-----|-------|
| | | | -90 | | -12 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| t _{ACC} ⁽²⁾ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 90 | | 120 | | 150 | ns |
| t _{CE} ⁽²⁾ | \overline{CE} to Output Delay | $\overline{OE} = V_{IL}$ | | 90 | | 120 | | 150 | ns |
| t _{OE} ⁽²⁾⁽³⁾ | \overline{OE} to Output Delay | $\overline{CE} = V_{IL}$ | | 35 | | 40 | | 50 | ns |
| t _{DF} ⁽⁴⁾⁽⁵⁾ | \overline{OE} or \overline{CE} High to Output Float, whichever occurred first | | | 20 | | 30 | | 35 | ns |
| t _{OH} ⁽⁴⁾ | Output Hold from Address, \overline{CE} or \overline{OE} , whichever occurred first | | 5 | | 5 | | 5 | | ns |
| t _{ST} | \overline{BYTE} High to Output Valid | | | 90 | | 120 | | 150 | ns |
| t _{STD} | \overline{BYTE} Low to Output Transition | | | 40 | | 50 | | 60 | ns |

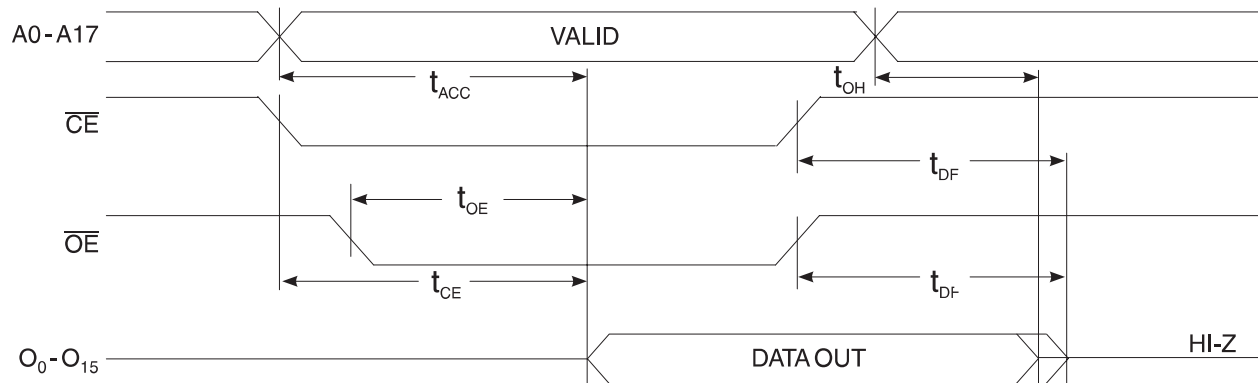
Note: 2, 3, 4, 5. See the AC Waveforms for Read Operation diagram.

Byte-wide Read Mode AC Waveforms



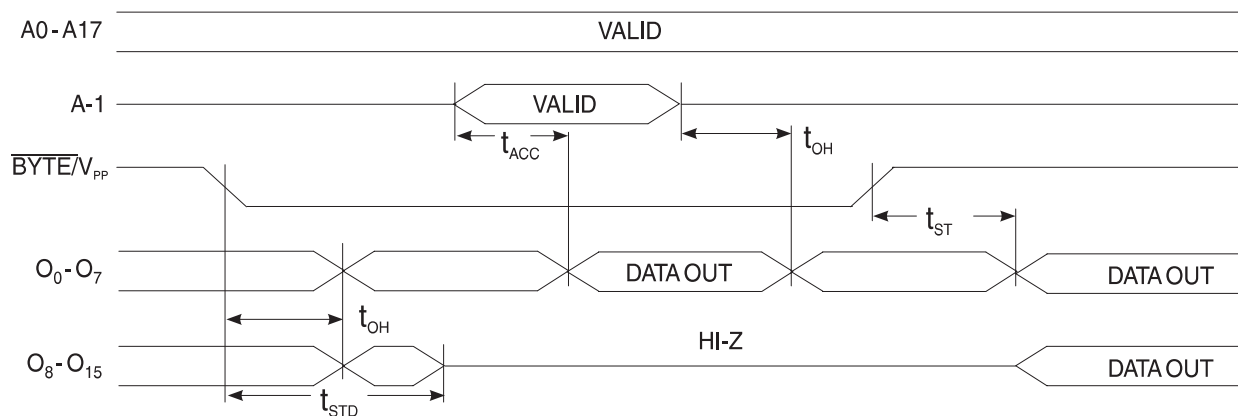
Note: $\overline{BYTE}/V_{PP} = V_{IL}$

Word-wide Read Mode AC Waveforms



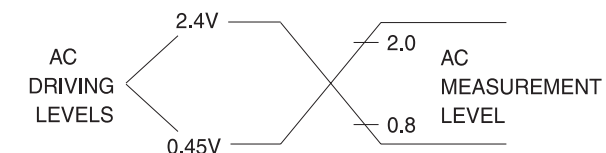
Note: $\overline{BYTE}/V_{PP} = V_{IH}$

BYTE Transition AC Waveforms



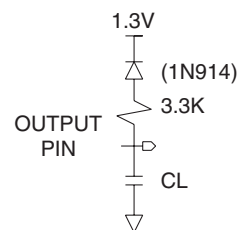
- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



$t_R, t_F < 20 \text{ ns}$ (10% to 90%)

Output Test Load



Note: $C_L = 100 \text{ pF}$ including jig capacitance.

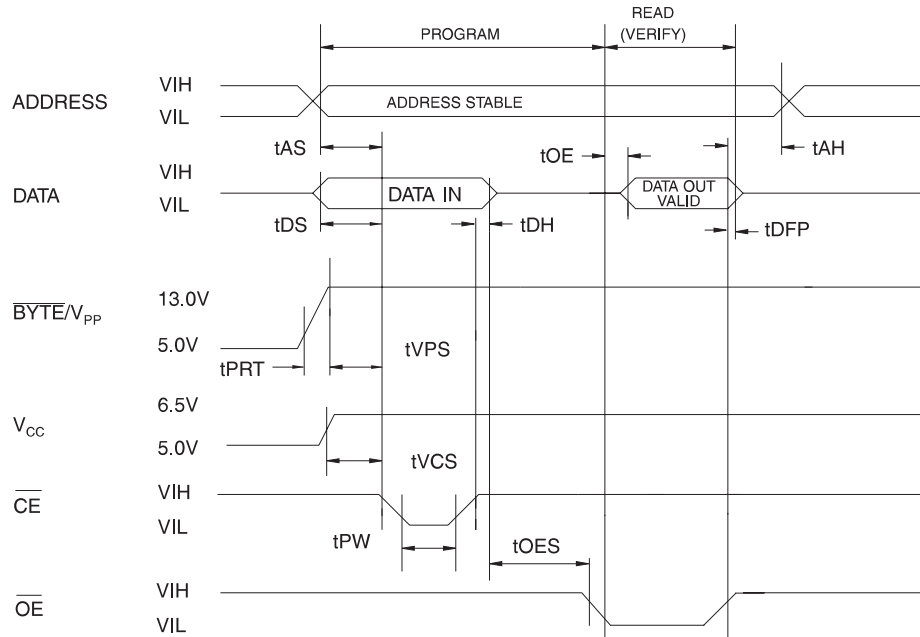
Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}^{(1)}$

| Symbol | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 4 | 10 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms⁽¹⁾



- Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
 3. When programming the AT27C400, a 0.1 μ F capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 \pm 5°C, V_{CC} = 6.5 \pm 0.25V, V_{PP} = 13.0 \pm 0.25V

| Symbol | Parameter | Test Conditions | Limits | | Units |
|------------------|---|---|--------|-----------------------|---------|
| | | | Min | Max | |
| I _{LI} | Input Load Current | V _{IN} = V _{IL} , V _{IH} | | \pm 10 | μ A |
| V _{IL} | Input Low Level | | -0.6 | 0.8 | V |
| V _{IH} | Input High Level | | 2.0 | V _{CC} + 0.5 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μ A | 2.4 | | V |
| I _{CC2} | V _{CC} Supply Current (Program and Verify) | | | 50 | mA |
| I _{PP2} | V _{PP} Supply Current | $\overline{\text{CE}}$ = V _{IL} | | 30 | mA |
| V _{ID} | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Limits | | Units |
|-----------|---|--|--------|------|---------------|
| | | | Min | Max | |
| t_{AS} | Address Setup Time | Input Rise and Fall Times: (10% to 90%) 20 ns | 2 | | μs |
| t_{OES} | \overline{OE} Setup Time | | 2 | | μs |
| t_{DS} | Data Setup Time | | 2 | | μs |
| t_{AH} | Address Hold Time | Input Pulse Levels: 0.45V to 2.4V | 0 | | μs |
| t_{DH} | Data Hold Time | | 2 | | μs |
| t_{DFP} | \overline{OE} High to Output Float Delay ⁽²⁾ | | 0 | 130 | ns |
| t_{VPS} | V_{PP} Setup Time | Input Timing Reference Level: 0.8V to 2.0V | 2 | | μs |
| t_{VCS} | V_{CC} Setup Time | | 2 | | μs |
| t_{PW} | \overline{CE} Program Pulse Width ⁽³⁾ | Output Timing Reference Level: 0.8V to 2.0V | 47.5 | 52.5 | μs |
| t_{OE} | Data Valid from \overline{OE} | | | 150 | ns |
| t_{PRT} | \overline{BYTE}/V_{PP} Pulse Rise Time During Programming | | 50 | | ns |

- Notes:
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
 - Program Pulse width tolerance is $50 \mu\text{sec} \pm 5\%$.

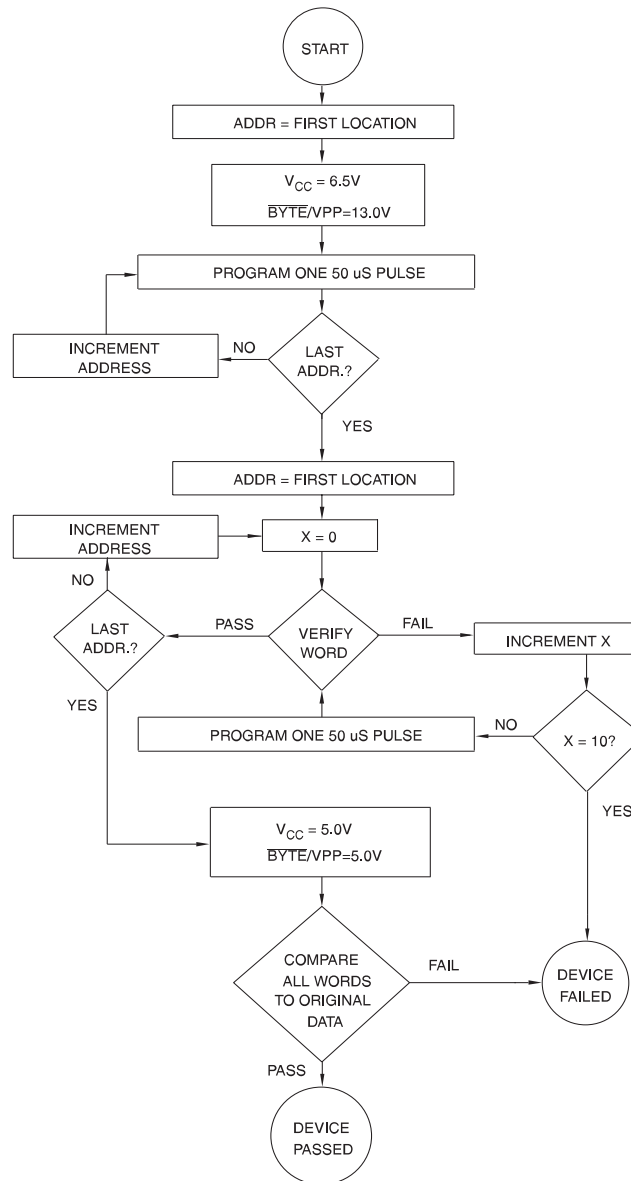
Atmel's 27C400 Integrated Product Identification Code

| Codes | Pins | | | | | | | | | Hex Data |
|--------------|------|-----|-----|-----|-----|-----|-----|----|----|----------|
| | A0 | O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 | |
| | | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | |
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E1E |
| Device Type | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | F4F4 |

Rapid Programming Algorithm

A 50 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{\text{BYTE}}/\text{VPP}$ is raised to 13.0V. Each address is first programmed with one 50 μs $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 μs pulses are applied with a verification after each

pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.





Ordering Information

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|--|---------------------------|-------------------------------|
| | Active | Standby | | | |
| 90 | 40 | 0.1 | AT27C400-90PC AT27C400-90RC AT27C400-90TC AT27C400-90JC | 40P6 44R 48T 44J | Commercial (0°C to 70°C) |
| | 40 | 0.1 | AT27C400-90PI AT27C400-90RI AT27C400-90TI AT27C400-90JI | 40P6 44R 48T 44J | Industrial (-40°C to 85°C) |
| 120 | 40 | 0.1 | AT27C400-12PC AT27C400-12RC AT27C400-12TC AT27C400-12JC | 40P6 44R 48T 44J | Commercial (0°C to 70°C) |
| | 40 | 0.1 | AT27C400-12PI AT27C400-12RI AT27C400-12TI AT27C400-12JI | 40P6 44R 48T 44J | Industrial (-40°C to 85°C) |
| 150 | 40 | 0.1 | AT27C400-15PC AT27C400-15RC AT27C400-15TC AT27C400-15JC | 40P6 44R 48T 44J | Commercial (0°C to 70°C) |
| | 40 | 0.1 | AT27C400-15PI AT27C400-15RI AT27C400-15TI AT27C400-15JI | 40P6 44R 48T 44J | Industrial (-40°C to 85°C) |

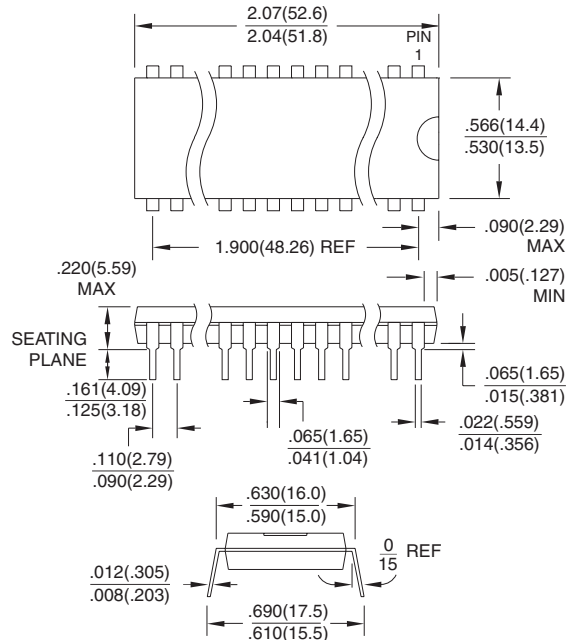
| Package Type | |
|--------------|--|
| 40P6 | 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 44R | 44-lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP) |
| 48T | 48-lead, Plastic Thin Small Outline Package (TSOP) 12 x 20 mm |
| 44J | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |

Packaging Information

40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

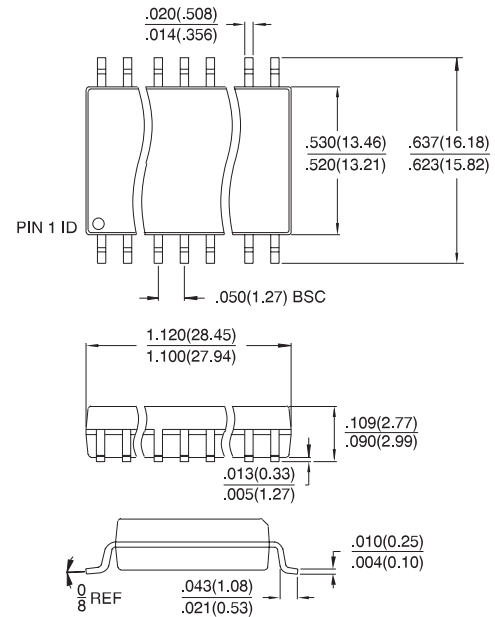
Dimensions in Inches and (Millimeters)

JEDEC STANDARD MS-011 AC



44R, 44-lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)

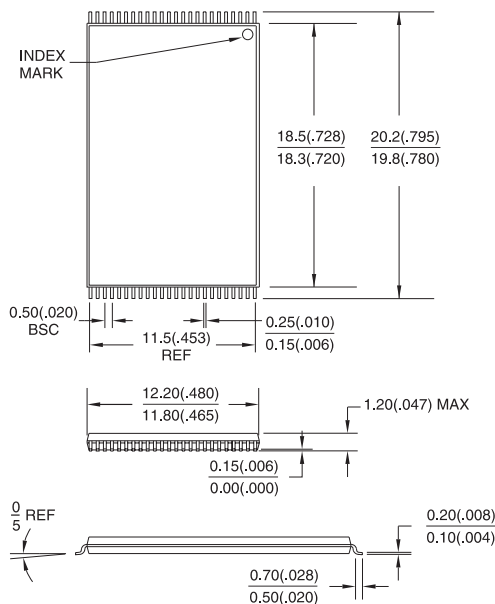
Dimensions in Inches and (Millimeters)



48T, 48-lead, Plastic Thin Small Outline Package (TSOP)

Dimensions in Millimeters and (Inches)*

JEDEC OUTLINE MO-142 DD

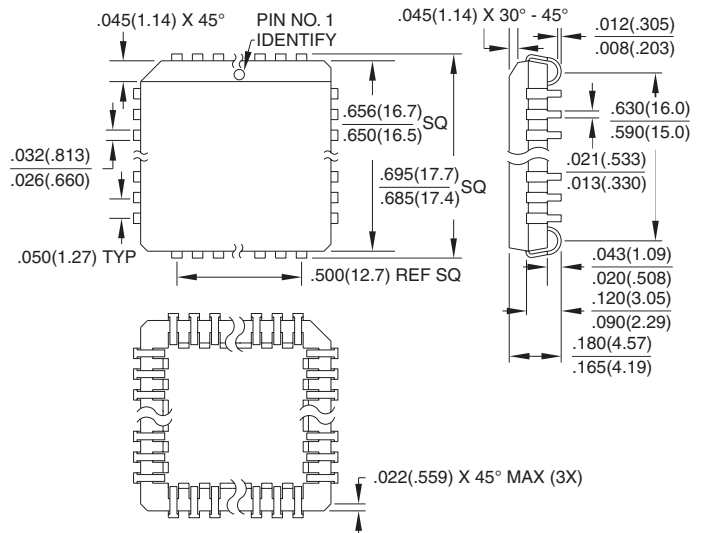


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)

Dimensions in Inches and (Millimeters)

JEDEC STANDARD MS-018 AC





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