Features

- **Serial EEPROM Family for Configuring Altera FLEX® Devices**
- **In-System Programmable via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **EE Programmable 64K, 128K and 256K Bits Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **Cascadable Read-back to Support Additional Configurations or Future Higher-density Arrays (128K and 256K only)**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in the Space-efficient Surface-mount PLCC Package (Compatible across Product Family)**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Available in 3.3V ± 10% LV and 5V ± 5% C Versions**

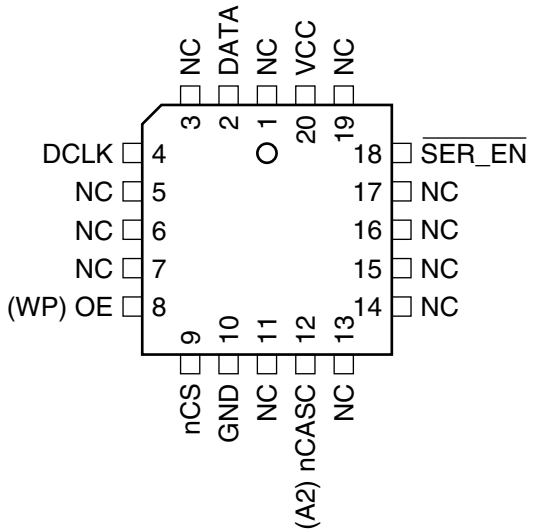
Description

The AT17C65A/128A/256A and AT17LV65A/128A/256A (low-density AT17A Series) FPGA Configuration EEPROMs (configurators) provide an easy-to-use, cost-effective configuration memory for programming Altera FLEX devices. The AT17A Series is packaged in the popular 20-lead PLCC. The AT17A Series family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17A Series organization supplies enough memory to configure one or multiple smaller FPGAs. Using a feature of the AT17A Series, the user can select the polarity of the reset function by programming a special EEPROM byte. These devices also support a write-protection mechanism within its programming mode.

The AT17A Series Configurators can be programmed with industry-standard programmers or Atmel's ATDH2200E Programming Kit.

Pin Configurations

20-lead PLCC



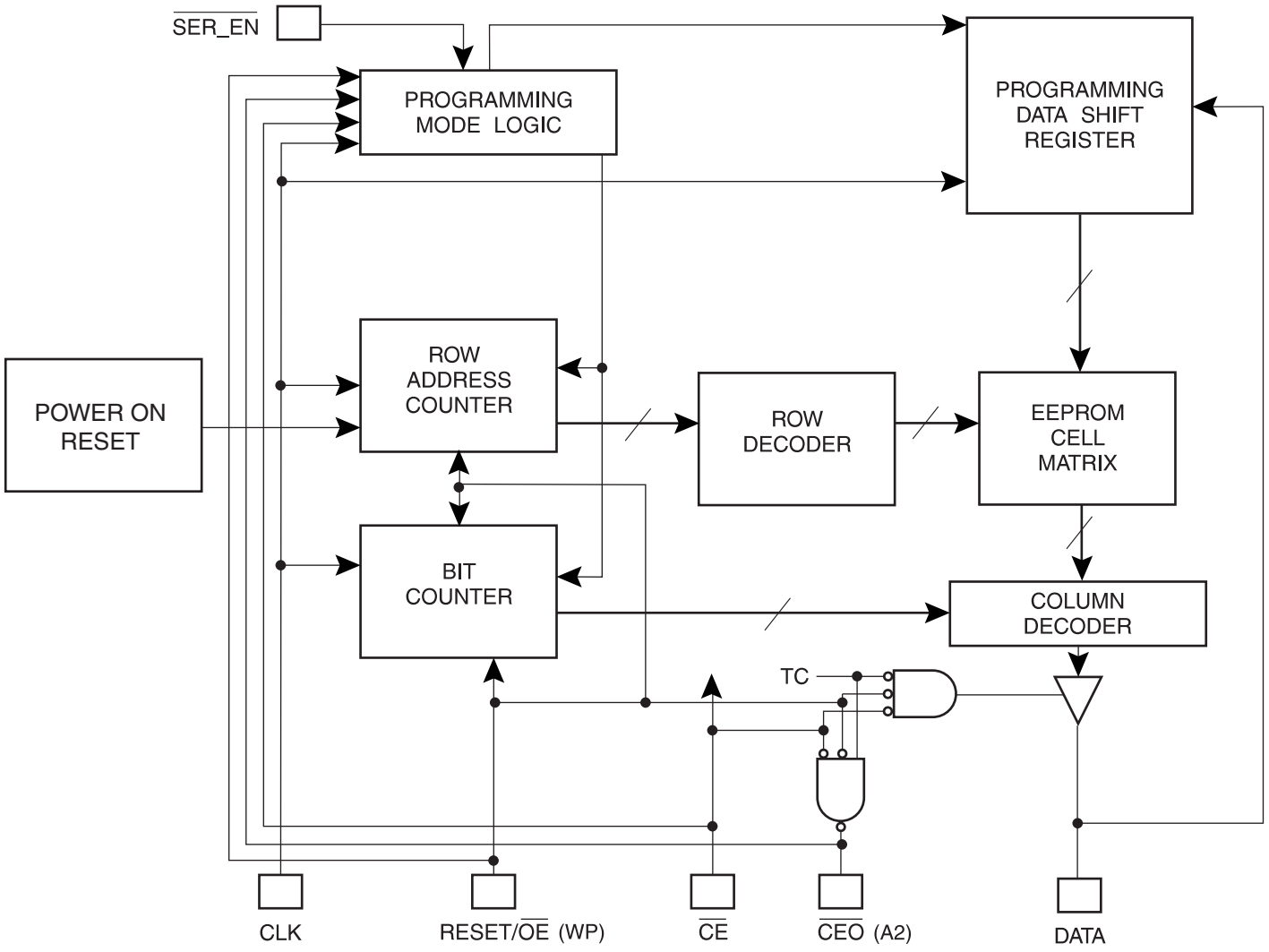
FPGA Configuration EEPROM Memory

64-kilobit, 128-kilobit and 256-kilobit Altera Pinout

AT17C65A
AT17LV65A
AT17C128A
AT17LV128A
AT17C256A
AT17LV256A

Rev. 0996D–08/01

Block Diagram



Device Configuration

The control signals for the configuration EEPROM – nCS, OE, and DCLK – interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM device's OE and nCS pins together control the tri-state buffer on the DATA output pin and enable the address counter. When OE is driven Low, the configuration EEPROM resets its address counter and tri-states its DATA pin. The nCS pin also controls the output of the AT17A Series Configurator. If nCS is held High after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is subsequently driven Low, the counter and the DATA output pin are enabled. When OE is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

When the configurator has driven out all of its data and nCASC is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This document discusses the EPF8K and EPF10K device interfaces. For more details or information on other Altera applications, please reference the “AT17A Series Conversions from Altera FPGA Serial Configuration Memories” application note.

FPGA Device Configuration

FPGA devices can be configured with a low-density AT17A Series EEPROM (see Figure 1 and Figure 2). The AT17A Series device stores configuration data in its EEPROM array and clocks the data out serially according to an external clock source. The OE, nCS and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The AT17A Series device sends a serial bitstream of configuration data to its DATA pin, which is connected to the DATA0 input pin on the FPGA device.

When configuration data for an FPGA device exceeds the capacity of a single AT17A Series device, multiple AT17A Series devices can be serially linked together (see Figure 2). When multiple AT17A Series devices are required, the nCASC and nCS pins provide handshaking between the cascaded EEPROMs.

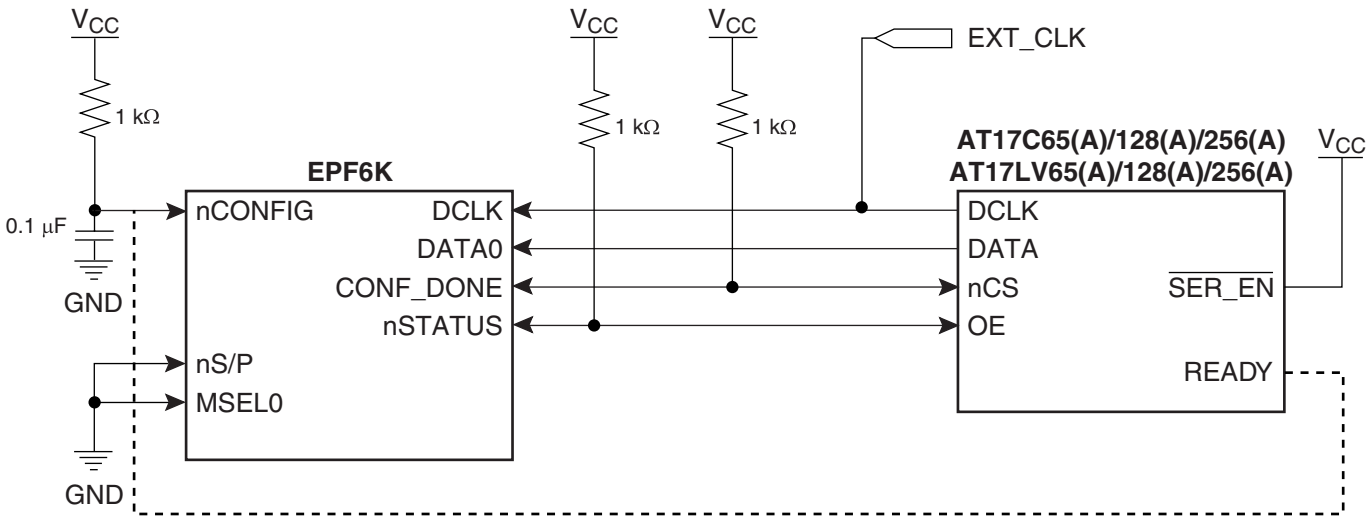
Note: A single AT17C/LV65A may only be used at the end of a cascade chain or as a stand-alone device.

The first AT17A Series Configurator (whose nCS input is directly driven by the FPGA) provides the first stream of data to the FPGA device during multi-device configuration. Once the first AT17A Series device finishes sending configuration data, it drives its nCASC pin Low, which drives the nCS pin of the second AT17A Series device Low. This allows the second AT17A Series device to send configuration data to the FPGA.

If the nCS pin on the first AT17A Series device is driven High before all configuration data is transferred, or if nCS is not driven High after all configuration data is transferred, nSTATUS is driven Low, indicating a configuration error.

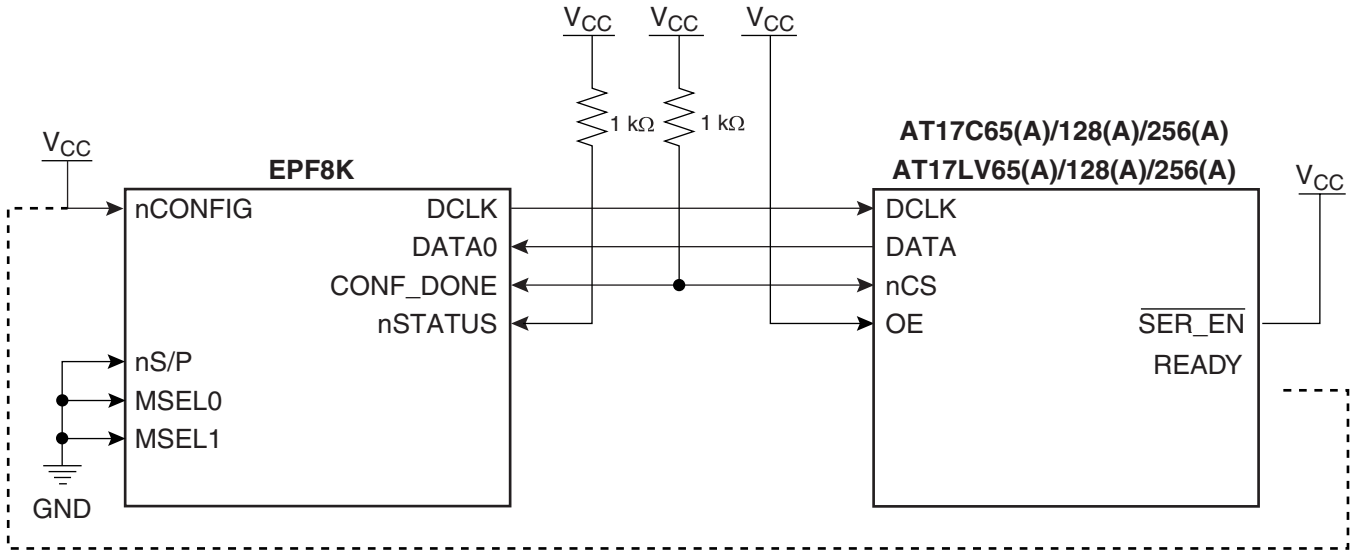
The low density AT17A Series Configuration EEPROMs are not designed to act as system masters (i.e., provide clock pulses on the serial bus to other devices). Clocking must be supplied by an FPGA device, a high-density AT17A Series device (see Figure 3), or an external oscillator.

Figure 1. FPGA Device Configured with a Single AT17A Series Configurator[1][2][3]



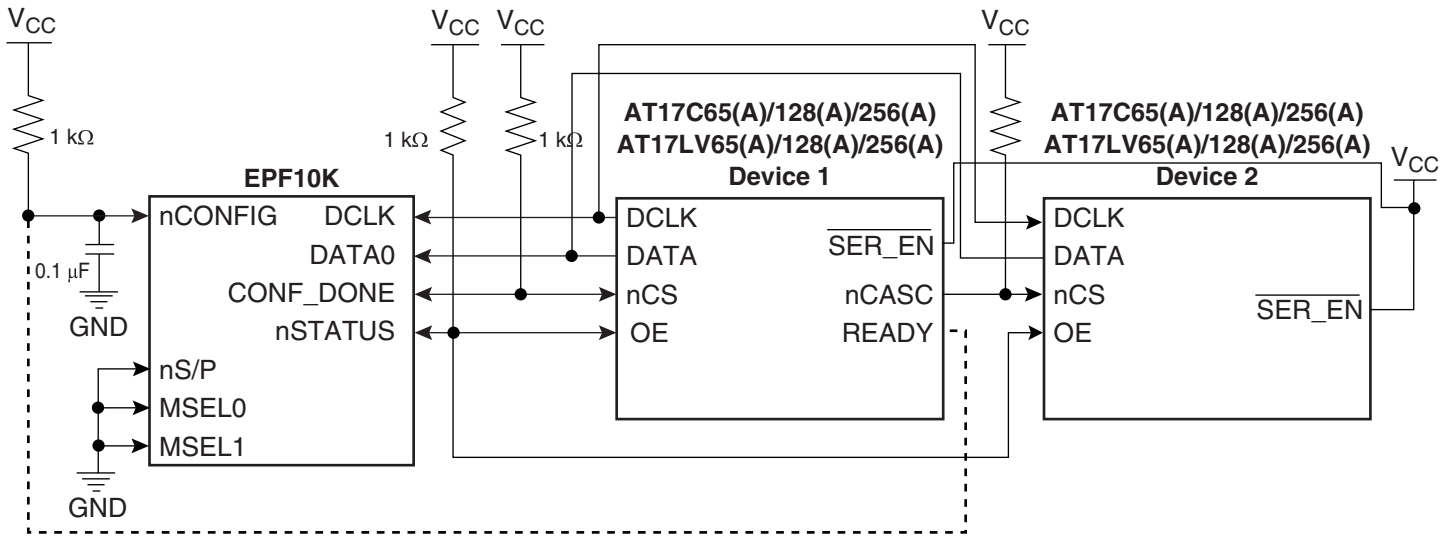
Notes: 1. Reset polarity must be set active Low.
2. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. (nCONFIG can instead be connected to an active Low system reset signal.)
3. The use of the READY pin is optional.

Figure 2. FPGA Device Configured with a Single AT17A Series Configurator[1][2][3]



Notes: 1. Reset polarity must be set active Low.
2. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. (nCONFIG can instead be connected to an active Low system reset signal.)
3. The use of the READY pin is optional.

Figure 3. FPGA Device Configured with Multiple AT17A Series Configurators[1][2][3]



Notes:
1. Reset polarity must be set active Low.
2. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable. (nCONFIG can instead be connected to an active Low system reset signal.)
3. The use of the READY pin is optional.

AT17A Series Reset Polarity

The AT17 Series Configurator allows the user to program the polarity of the OE pin as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This feature is supported by industry-standard programmer algorithms. For more details on programming the EEPROM's reset polarity, please reference the "Programming Specification for Atmel's FPGA Configuration EEPROMs" application note.

Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. See the "Programming Specification for Atmel's Configuration EEPROM" application note for further information. The AT17CXXXA parts are read/write at 5V nominal. The AT17LVXXXA parts are read/write at 3.3V nominal.

Standby Mode

The AT17C/LV65A/128A/256A enters a low-power standby mode whenever nCS is asserted High. In this mode, the configurator consumes less than 75 µA of current at 5.0V. The output remains in a high-impedance state regardless of the state of the OE input.

Pin Configurations

20 PLCC Pin	Name	I/O	Description
2	DATA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
4	DCLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
8	OE	I	Output enable (active High) and reset (active Low) when $\overline{\text{SER\_EN}}$ is High. A Low logic level resets the address counter. A High logic level (with nCS Low) enables DATA and permits the address counter to count. The logic polarity of OE is programmable and must be set active High (RESET active Low) by the user during programming for Altera applications.
	WP	I	Write Protect (WP) input (when nCS is Low) during programming only (i.e., when $\overline{\text{SER\_EN}}$ is Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This function is not available during FPGA loading operations. Please refer to the "Programming Specification for Atmel's Configuration EEPROM" application note for more details.
9	nCS	I	Chip select input (active Low). A Low input (with OE active) allows DCLK to increment the address counter and enables DATA to drive out. A High level on nCS disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the 2-wire Serial Programming Mode (i.e., when SER_EN is Low).
10	GND		Ground pin. A 0.2 µF decoupling capacitor should be placed between the VCC and GND pins.
12	nCASC	O	Cascade select output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy-chain of AT17A Series devices, the nCASC pin of one device must be connected to the nCS input pin of the next device in the chain. It will stay Low as long as nCS is Low and OE is High. It will then follow nCS until OE goes Low, thereafter, nCASC will stay High until the entire EEPROM is read again.
	A2	I	Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low; please refer to the "Programming Specification for Atmel's Configuration EEPROM" application note for more details).
18	$\overline{\text{SER\_EN}}$	I	Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-wire Serial Programming Mode.
20	VCC		+3.3V/+5V Power Supply Pin.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} + 0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		AT17CxxxA		AT17LVxxxA		Units
			Min	Max	Min	Max	
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	3.0	3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial; 5V ± 10% Industrial/Military

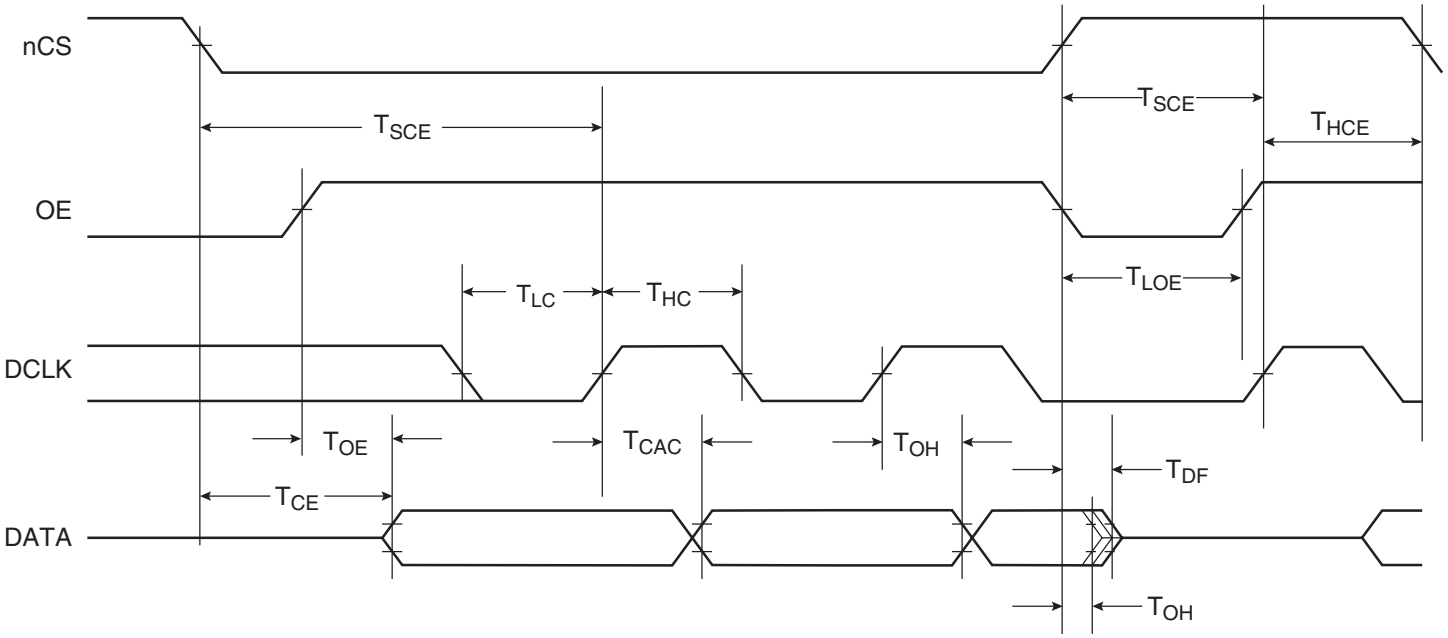
Symbol	Description		Min	Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0.0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Commercial	3.7		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Industrial	3.6		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Military	3.5		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply Current, Active Mode (at FMAX)			10	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply Current, Standby Mode AT17C512A/010A	Commercial		75	µA
		Industrial/Military		150	µA

DC Characteristics

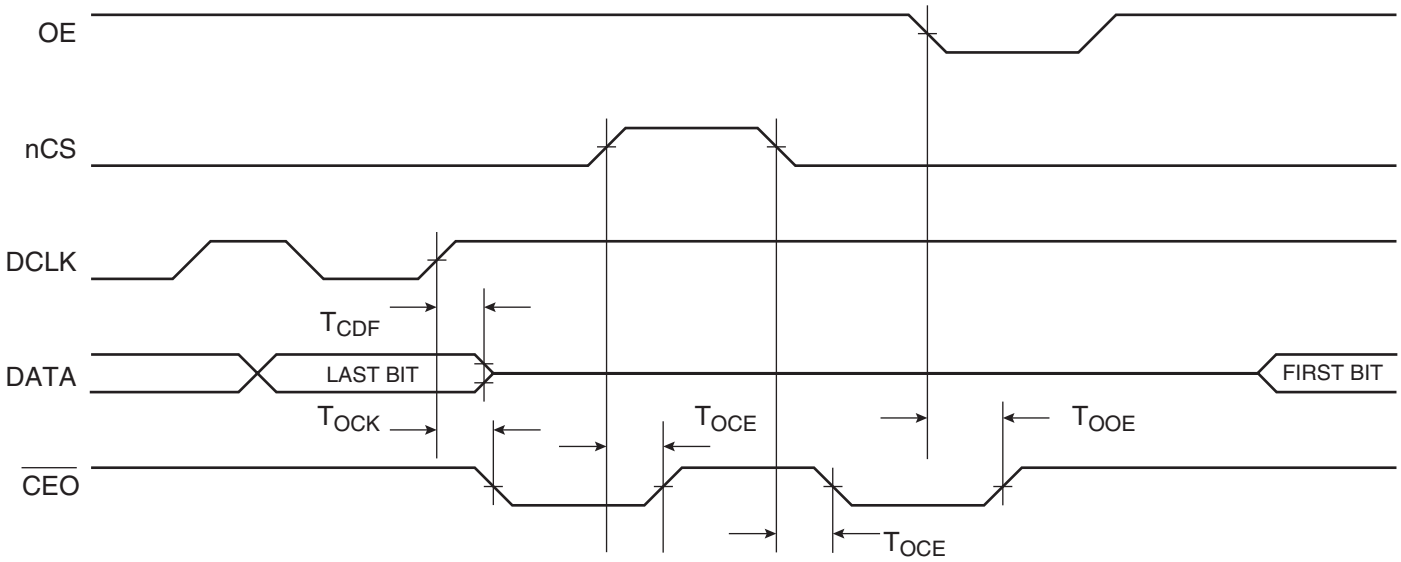
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0.0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply Current, Active Mode (at FMAX)			5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		50	µA
		Industrial/Military		100	µA

AC Characteristics



AC Characteristics when Cascading



AC Characteristics for AT17C65A/128A

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		30		35	ns
T_{CE}[2]	nCS to Data Delay		50		50	ns
T_{CAC}[2]	DCLK to Data Delay		50		55	ns
T_{OH}	Data Hold From nCS, OE, or DCLK	0		0		ns
T_{DF}[3]	nCS or OE to Data Float Delay		50		50	ns
T_{LC}	DCLK Low Time	30		35		ns
T_{HC}	DCLK High Time	30		35		ns
T_{SCE}	nCS Setup Time to DCLK (to guarantee proper counting)	45		50		ns
T_{HCE}	nCS Hold Time from DCLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE Low Time (guarantees counter is reset)	25		25		ns
F_{MAX}	Maximum Input Clock Frequency	12.5		12.5		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics for AT17C128A when Cascading

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	DCLK to Data Float Delay		50		50	ns
T_{OCK}[2]	DCLK to nCASC Delay		55		60	ns
T_{OCE}[2]	nCS to nCASC Delay		55		60	ns
T_{OE}[2]	OE to nCASC Delay		40		45	ns
F_{MAX}	Maximum Input Clock Frequency	8		8		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics for AT17C256A

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		30		35	ns
T_{CE}[2]	nCS to Data Delay		45		45	ns
T_{CAC}[2]	DCLK to Data Delay		50		55	ns
T_{OH}	Data Hold From nCS, OE, or DCLK	0		0		ns
T_{DF}[3]	nCS or OE to Data Float Delay		50		50	ns
T_{LC}	DCLK Low Time	20		20		ns
T_{HC}	DCLK High Time	20		20		ns
T_{SCE}	nCS Setup Time to DCLK (to guarantee proper counting)	35		40		ns
T_{HCE}	nCS Hold Time from DCLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE Low Time (guarantees counter is reset)	20		20		ns
F_{MAX}	Maximum Input Clock Frequency	12.5		12.5		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics for AT17C256A when Cascading

V_{CC} = 5V ± 5% Commercial; V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	DCLK to Data Float Delay		50.0		50.0	ns
T_{OCK}[2]	DCLK to nCASC Delay		35.0		40.0	ns
T_{OCE}[2]	nCS to nCASC Delay		35.0		35.0	ns
T_{OOE}[2]	OE to nCASC Delay		30.0		35.0	ns
F_{MAX}	Maximum Input Clock Frequency	10.0		10.0		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics for AT17LV65A/128A/256A

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		50		55	ns
T_{CE}[2]	nCS to Data Delay		60		60	ns
T_{CAC}[2]	DCLK to Data Delay		75		80	ns
T_{OH}	Data Hold from nCS, OE or DCLK	0		0		ns
T_{DF}[3]	nCS or OE to Data Float Delay		55		55	ns
T_{LC}	DCLK Low Time	25		25		ns
T_{HC}	DCLK High Time	25		25		ns
T_{SCE}	nCS Setup Time to DCLK (to guarantee proper counting)	35		60		ns
T_{HCE}	nCS Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE Low Time (guarantees counter is reset)	25		25		ns
F_{MAX}	Maximum Input Clock Frequency	10		10		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

AC Characteristics for AT17LV128A/256A when Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	DCLK to Data Float Delay		60		60	ns
T_{OCK}[2]	DCLK to nCASC Delay		55		60	ns
T_{OCE}[2]	nCS to nCASC Delay		55		60	ns
T_{OOE}[2]	OE to nCASC Delay		40		45	ns
F_{MAX}	Maximum Input Clock Frequency	8		8		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test lead = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady-state active levels.

Ordering Information – 5V Devices[1]

Memory Size	Ordering Code	Package	Operation Range
64-Kbit[2]	AT17C65A-10JC	20J	Commercial (0°C to 70°C)
	AT17C65A-10JI	20J	Industrial (-40°C to 85°C)
128-Kbit	AT17C128A-10JC	20J	Commercial (0°C to 70°C)
	AT17C128A-10JI	20J	Industrial (-40°C to 85°C)
256-Kbit[3]	AT17C256A-10JC	20J	Commercial (0°C to 70°C)
	AT17C256A-10JI	20J	Industrial (-40°C to 85°C)

Notes:
1. Currently, there are two types of low-density configurators. The new version will be identified by a “B” after the datacode. The “B” version is fully backward-compatible with the original devices so existing customers will not be affected. The new parts no longer require a MUX for ISP. See programming specification for more details.
2. Use 64-Kbit density parts to replace Altera EPC1064.
3. Use 256-Kbit density parts to replace Altera EPC1213.

Ordering Information – 3.3V Devices[1]

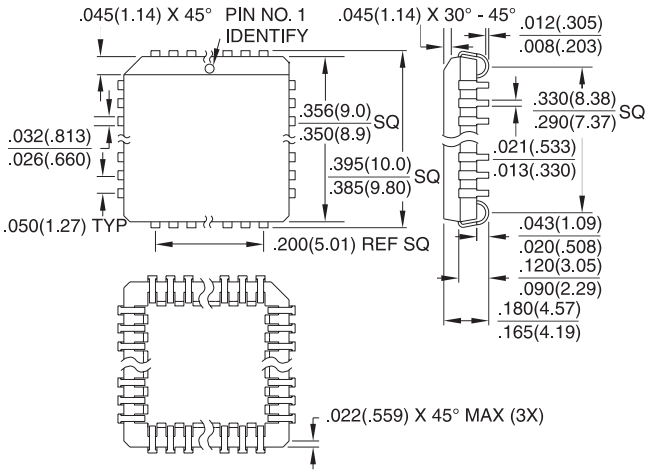
Memory Size	Ordering Code	Package	Operation Range
64-Kbit[2]	AT17LV65A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV65A-10JI	20J	Industrial (-40°C to 85°C)
128-Kbit	AT17LV128A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV128A-10JI	20J	Industrial (-40°C to 85°C)
256-Kbit[3]	AT17LV256A-10JC	20J	Commercial (0°C to 70°C)
	AT17LV256A-10JI	20J	Industrial (-40°C to 85°C)

Notes:
1. Currently, there are two types of low-density configurators. The new version will be identified by a “B” after the datacode. The “B” version is fully backward-compatible with the original devices so existing customers will not be affected. The new parts no longer require a MUX for ISP. See programming specification for more details.
2. Use 64-Kbit density parts to replace Altera EPC1064.
3. Use 256-Kbit density parts to replace Altera EPC1213.

Package Type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)

Packaging Information

20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



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