KL5BPLC200WMP

HD-PLC Data Processing IC

Datasheet

Rev. 0.7.2

Table of Contents

1 Product overview

1.1 Function Overview

The KL5BPLC200WMP is an HD-PLC LSI designed to connect a wide range of home network devices in a flexible manner using existing residential electrical wiring. Its capabilities include transmission of high-definition video and other broadband content. HD-PLC is the name of a high definition power line communication system put forth by Panasonic.

Thanks to compatibility with the ubiquitous Ethernet standard, the KL5BPLC200WMP can be easily connected to network-enabled products such as broadband networks, televisions, and computers anywhere there is an electrical outlet simply by supporting the Internet protocol (IP), which already enjoys widespread use.

The KL5BPLC200WMP incorporates a 32-bit RISC processor and provides a single-chip implementation of high-performance wavelet conversion OFDM functionality, MAC processing functionality with high-quality QoS support, and HD-PLC/Ethernet bridge functionality.

QoS functionality can be used to guarantee a fixed communication speed for a variety of communications ranging from data transmission and reception to video streaming and IP telephony.

The KL5BPLC200WMP also has highly integrated analog front-end chip so that no other analog front-end IC for PLC is necessary. An on-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source.

Following are the features of KL5BPLC200WMP.

- Single chip solution for HD-PLC application.
- Network construction and optimization, advanced network diagnostics and management.
- HD-PLC network bridge function compatible with Ethernet address system.
- Ensuring the security and easy connectivity by data encryption using AES.
- High-speed communications up to 432 carriers within 2-28MHz band(Maximum PHY Rate: 240Mbps without notch)
- Determine the optimal rate according to the power line channel characteristics with the multilevel modulation for each sub-carrier.
- Optional sub-carriers masking function to be adapted to individual country's regulations.
- Level-up function to achieve maximum speed under individual country's regulations.
- Error correction and selective transmission retry to achieve efficient frame transfer.
- Backward compatible with existing 1st, 2nd HD-PLC systems.
- IEEE1901 compliant(Wavelet MAC/PHY, ISP)

1.2 Block Diagram

Figure- 1 shows a block diagram of the KL5BPLC200WMP.

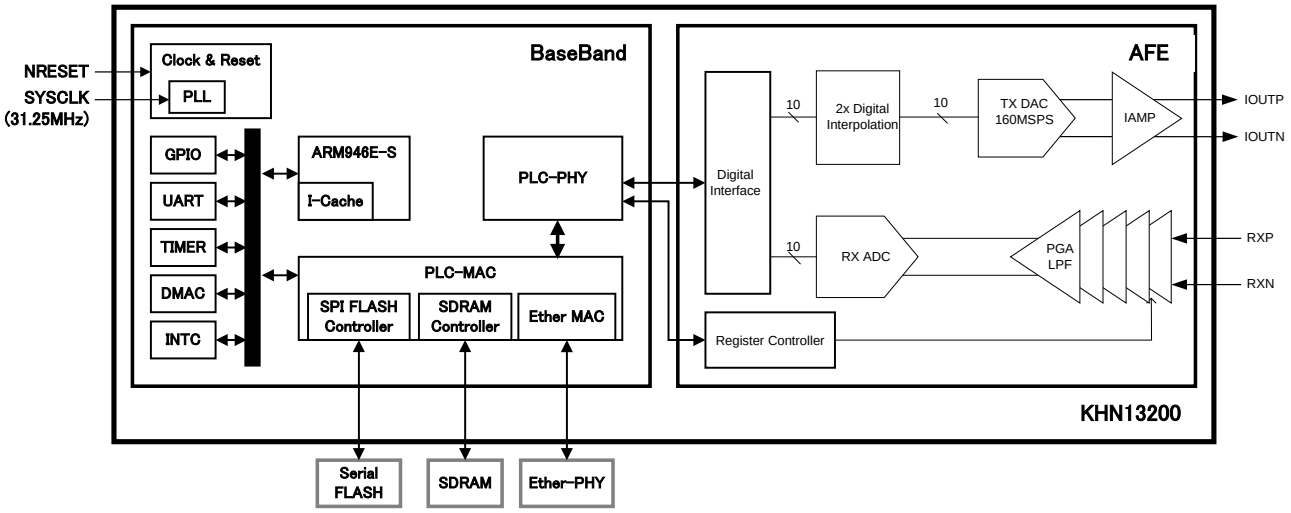

Figure- 1 KL5BPLC200WMP Block Diagram

2 Pins

2.1 Pin Assignments

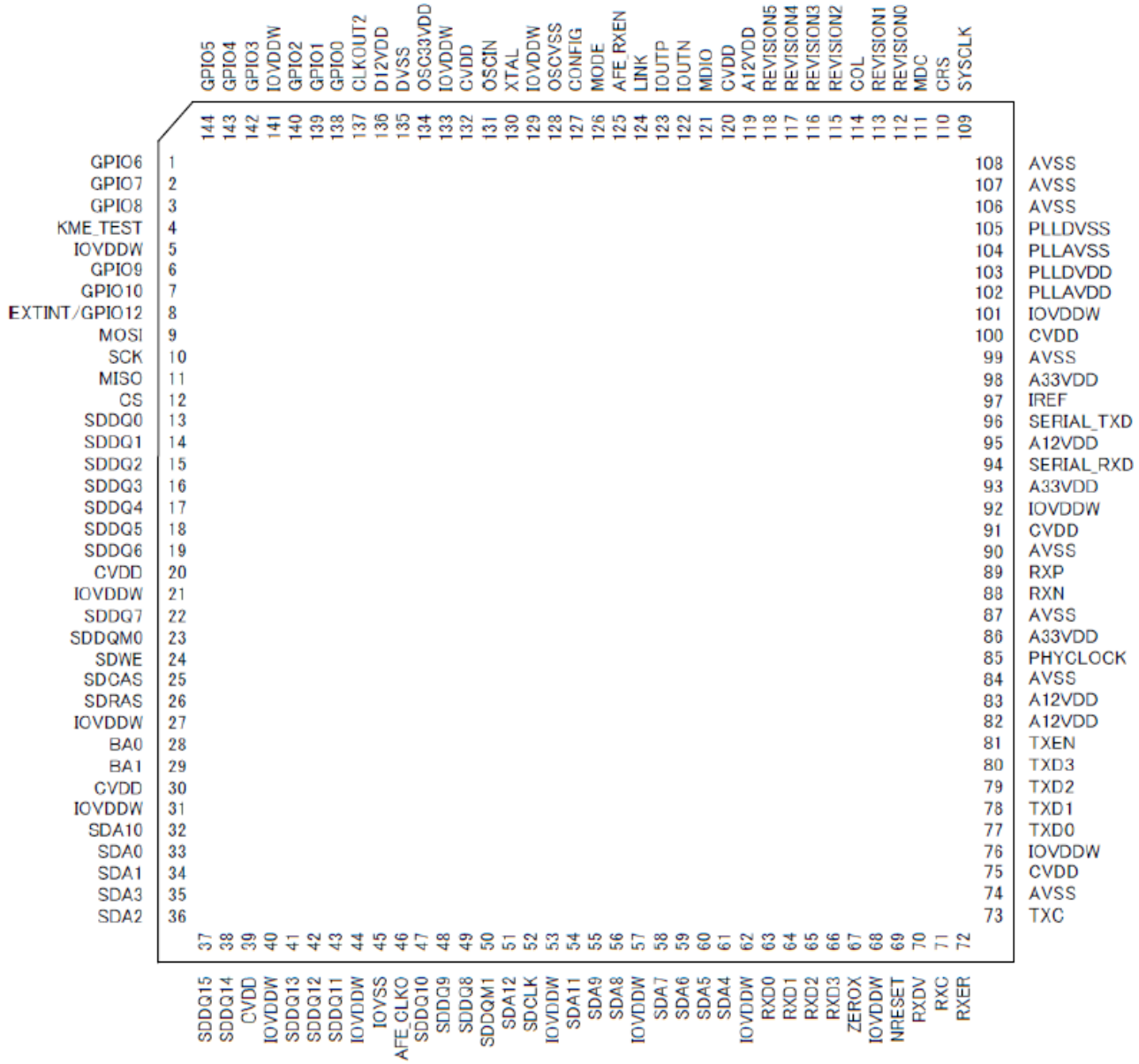

Figure- 2 Pin Assignment

2.2 Pin Descriptions

This section describes the KL5BPLC200WMP's pins. In the pin list, initial values for pins are given as “RST initial value”, and "---" means that initial values are undefined since those pins act as input in the initial state (following reset cancellation).

Pins whose names are followed by "(shared)" are treated as shared pins. Shared pins are not shown in Figure- 2.

2.2.1 Analog Front-end Connection Pins

Table- 1 shows a list of analog front-end connection pins.

Table- 1 List of Analog Front-end Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
46	AFE_CLKO	O	Low	A/D / D/A sampling clock output.(62.5MHz)
125	AFE_RXEN	O	Low	Active high receive enable output.

2.2.2 Ethernet Connection Pins

The KL5BPLC200WMP's Ethernet connection pins comply with MII and RMII specifications and also support Turbo-MII specification. Register settings can be used to select the desired specification set.

Table- 2 shows a list of Ethernet connection pins.

Table- 2 List of Ethernet Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
77	TXD0	O	Low	When MII/Turbo-MII is selected, act as 4-bit transmission data output. When RMII is selected, TXD0 and TXD1 act as 2-bit transmission data output pins. Do not connect anything to TXD2 or TXD3 in this configuration.
78	TXD1		Low	
79	TXD2		Low	
80	TXD3		Low	
81	TXEN	O	Low	Active high transmission data enable output.
73	TXC	I	---	Transmission clock input. Not used when RMII is selected. Requires pull-down.
63	RXD0	I	---	When MII/Turbo-MII is selected, act as 4-bit receive data input. When RMII is selected, RXD0 and RXD1 act as 2-bit receive data input. RXD2 and RXD3 act as monitor pins as described below: RXD2 : 10M/100M communications mode information RXD3 : LINK status
64	RXD1		---	
65	RXD2		---	
66	RXD3		---	
70	RXDV	I	---	Active high receive data valid input. When RMII is selected, connect to the EtherPHY LSI's CRS_DV pin.
71	RXC	I	---	Receive clock input Not used when RMII is selected. Requires pull-down.
72	RXER	I	---	Active high receive error indicator input.
114	COL	I	---	Active high collision detection input. Not used when RMII is selected. Requires pull-down.

110	CRS	I	---	Active high carrier sense input. Not used when RMII is selected. Requires pull-down.
121	MDIO	IO	---	Control data input/output.
111	MDC	O	Low	Control data clock output.
85	PHYCLOCK	O	Low	Acts as the Ethernet clock output. The clock precision is the same as for the clock input to the SYSCLK pin. When MII is selected, outputs 25MHz. When RMII, Turbo-MII are selected, outputs 50MHz.
124	LINK	I	---	Acts as the link state input. For more information about the pin level (indicating the presence of the link state), see the specifications for the EtherPHY LSI to which the pin will be connected. A toggle signal indicates that communications are in progress.

2.2.3 SDRAM Connection Pins

Table- 3 shows a list of SDRAM connection pins.

Table- 3 List of SDRAM Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
13	SDDQ0	IO	---	16-bit data bus input/output for external SDRAM.
14	SDDQ1		---	
15	SDDQ2		---	
16	SDDQ3		---	
17	SDDQ4		---	
18	SDDQ5		---	
19	SDDQ6		---	
22	SDDQ7		---	
49	SDDQ8		---	
48	SDDQ9		---	
47	SDDQ10		---	
43	SDDQ11		---	
42	SDDQ12		---	
41	SDDQ13		---	
38	SDDQ14		---	
37	SDDQ15		---	
33	SDA0	O	Low	13-bit address bus output for external SDRAM.
34	SDA1		Low	
36	SDA2		Low	
35	SDA3		Low	
61	SDA4		Low	
60	SDA5		Low	
59	SDA6		Low	
58	SDA7		Low	
56	SDA8		Low	
55	SDA9		Low	
32	SDA10		Low	
54	SDA11		Low	
51	SDA12		Low	
28	BA0	O	Low	Bank address output for external SDRAM.
29	BA1		Low	
52	SDCLK	O	Low	SDRAM transfer clock output.
26	SDRAS	O	High	Bank select / row address strobe output.
25	SDCAS	O	High	Command select / column address strobe output.
24	SDWE	O	High	Write enable output.
23	SDDQM0	O	Low	Data mask control output.
50	SDDQM1	O	Low	

2.2.4 Serial Flash Connection Pins

Table- 4 shows a list of serial flash connection pins.

Table- 4 List of Serial Flash Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
12	CS	O	High	Chip select output.
11	MISO	I	---	Serial data input.
10	SCK	O	Low	Serial clock output. (50MHz)
9	MOSI	O	Low	Serial data output

2.2.5 Serial Communication Connection Pins

Table- 5 shows a list of serial communication connection pins.

Table- 5 List of Serial Communication Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
94	SERIAL_RXD	I	---	Serial data input.
96	SERIAL_TXD	O	Low	Serial data output.

2.2.6 General-purpose Ports

Table- 6 shows a list of general-purpose ports.

Table- 6 List of General-purpose ports

No.	Pin Name	I/O	RST Initial Value	Description
138	GPIO0	IO	---	General-purpose port.
139	GPIO1	IO	---	General-purpose port.
140	GPIO2	IO	---	General-purpose port.
142	GPIO3	IO	---	General-purpose port.
143	GPIO4	IO	---	General-purpose port. (*1) Shared with AJTRSTN pin.
144	GPIO5	IO	---	General-purpose port. (*1) Shared with AJTDI pin.
1	GPIO6	IO	---	General-purpose port. (*1) Shared with AJTMS pin.
2	GPIO7	IO	---	General-purpose port. (*1) Shared with AJTCK pin.
3	GPIO8	IO	---	General-purpose port. (*1) Shared with AJRTCK pin.
6	GPIO9	IO	---	General-purpose port. (*1) Shared with AJTDO pin.
7	GPIO10	IO	---	General-purpose port. (*1) Shared with AJSRSTN pin.
8	GPIO12	IO	---	General-purpose port. (*2) Shared with EXTINT pin.

Note:

- *In normal mode, all ports are configured as input ports.*
- **1 : When ICE mode is selected, acts as the ICE JTAG pin.*
- **2 : Enabled by register settings.*

2.2.7 CPU Peripheral Connection Pin

Table- 7 shows a list of CPU peripheral connection pin.

Table- 7 List of CPU Peripheral Connection Pin

No.	Pin Name	I/O	RST Initial Value	Description
8	EXTINT	I	---	Active Low external interrupt input. * Shared with GPIO12.

2.2.8 AC Synchronous Detection Pin

Table- 8 shows a list of AC synchronous detection pin.

Table- 8 List of AC Synchronous Detection Pin

No.	Pin Name	I/O	RST Initial Value	Description
67	ZEROX	I	---	AC synchronous detection input.

2.2.9 Clock and Reset Pins

Table- 9 shows a list of clock and reset connection pins.

Table- 9 List of Clock and Reset Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
109	SYSCLK	I	---	System clock input. (31.25MHz)
130	XTAL	O	---	Crystal Oscillator Inverter Output
131	OSCIN	I	---	Crystal Oscillator Inverter Input
137	CLKOUT2	O	---	f_{osc}/L Clock Output (L=1,2,4,8)
69	NRESET	I	---	Active low asynchronous reset input.

2.2.10 DAC Pins

Table- 10 shows a list of DAC connection pins.

Table- 10 List of DAC Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
123	IOUTP	O	---	IAMP+ Current Output Sink
122	IOUTN	O	---	IAMP- Current Output Sink
97	IREF	I	---	Reference Current DAC, connect to 8.2kOhm resistor

2.2.11 ADC Pins

Table- 11 shows a list of ADC connection pins.

Table- 11 List of ADC Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
89	RXP	I	---	Receive Path Analog Input pin
88	RXN	I	---	Receive Path Analog Input pin

2.2.12 Test Setting Pin

Table- 12 shows a list of test pins.

Table- 12 List of Test Setting Pin

No.	Pin Name	I/O	RST Initial Value	Description
4	KME_TEST	I	---	Production test mode setting input. In normal operation, this input should be tied to low.
126	MODE	I	---	Vendor test purpose only, Fixed to “Low”
127	CONFIG	I	---	Vendor test purpose only, Fixed to “Low”

2.2.13 Debugger Connection Pins

Table- 13 shows a list of debugger connection pins.

Table- 13 List of Debugger Connection Pins

No.	Pin Name	I/O	RST Initial Value	Description
143	AJTRSTN(Shared)	I	---	JTAG reset signal. * Shared with GPIO4.
144	AJTDI(Shared)	I	---	JTAG test data input. * Shared with GPIO5.
1	AJTMS(Shared)	I	---	JTAG TAP controller mode selection signal. * Shared with GPIO6.
2	AJTCK(Shared)	I	---	JTAG test clock. * Shared with GPIO7.
3	AJRTCK(Shared)	O	Low	JTAG Return TCK output to ICE. * Shared with GPIO8.
6	AJTDO(Shared)	O	Hi-Z	JTAG test data output. * Shared with GPIO9.
7	AJSRSTN(Shared)	I	---	JTAG system reset signal. * Shared with GPIO10.

Note:

- *GPIO10 to GPIO4 cannot be used as general-purpose ports during ICE mode operation.*

2.2.14 Hardware Revision Setting Pins

Table- 14 shows a list of hardware revision setting pins. For more information, see Section 4.9.1 Special Pin Settings.

Table- 14 List of Hardware Revision Setting Pins

No.	Pin Name	I/O	RST Initial Value	Description
112	REVISION0	I	---	Revision setting
113	REVISION1	I	---	Revision setting
115	REVISION2	I	---	Revision setting
116	REVISION3	I	---	Revision setting
117	REVISION4	I	---	Used as ICEMODE setting pin
118	REVISION5	I	---	Reserved. Fixed to “Low”

Note:

- *Always mount a pull-up resistor or pull-down resistor outside the LSI for these pins.*

2.2.15 Power Supply and VSS Pins

Table- 15 shows a list of power supply and VSS pins.

Table- 15 List of Power Supply and VSS Pins

No.	Pin Name	Description
5,21,27,31,40,44,53,57,62,68,76,92, 101,129,133,141	IOVDDW	3.3-V I/O Buffer power supply pins
45	IOVSS	Digital I/O Buffer Ground for AFE chip
20,30,39,75,91,100,120,132	CVDD	1.2-V (core) power supply pins for BaseBand
136	D12VDD	1.2-V (core) power supply pins for AFE
135	DVSS	Digital Ground for AFE
86,93,98	A33VDD	3.3V Analog Power Supply pins for AFE
82,83,95,119	A12VDD	1.2V Analog Power Supply pins
74,84,87,90,99,106,107,108	AVSS	Analog Ground for AFE
102	PLLAVDD	1.2V Analog VDD pin for BaseBand PLL
104	PLLAVSS	Analog Ground pin for BaseBand PLL
103	PLLDVDD	1.2V Digital VDD pin for BaseBand PLL
105	PLLDVSS	Digital Ground for BaseBand PLL
134	OSC33VDD	Crystal Oscillator Buffer 3.3V Power Supply pin
128	OSCVSS	Crystal Oscillator Buffer Ground
Exposed Pad	VSS	Digital Ground

2.2.16 Shared Pins

Table- 16 shows a list of shared pins.

Table- 16 List of Shared Pins

No.	Pin Name	Shared Pin Name	Description
143	GPIO4	AJTRSTN	Switchable with normal mode/ICE mode settings.
144	GPIO5	AJTDI	Switchable with normal mode/ICE mode settings.
1	GPIO6	AJTMS	Switchable with normal mode/ICE mode settings.
2	GPIO7	AJTCK	Switchable with normal mode/ICE mode settings.
3	GPIO8	AJRTCK	Switchable with normal mode/ICE mode settings.
6	GPIO9	AJTDO	Switchable with normal mode/ICE mode settings.
7	GPIO10	AJSRSTN	Switchable with normal mode/ICE mode settings.
8	GPIO12	EXTINT	Can be switched with GPIO selection register settings.

3 Operating Conditions

3.1 Absolute Maximum Ratings

Table- 17 shows absolute maximum ratings.

Table- 17 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
External supply IO voltage	V_{IOVDDW}	-0.3 to 4.0	V
External supply Analog voltage	V_{A33VDD}	-0.3 to 4.0	V
External supply Analog voltage	$V_{OSC33VDD}$	-0.3 to 4.0	V
Internal supply voltage for BaseBand	V_{CVDD}	-0.3 to 1.32	V
Internal supply voltage for AFE (Analog Part)	V_{A12VDD}	-0.3 to 1.6	V
Internal supply voltage for AFE (Digital Part)	V_{D12VDD}	-0.3 to 1.6	V
Input pin voltage	V_I	-0.3 to V_{IOVDDW} +0.3	V
Analog Input/Output Voltage RXP,RXN,IREF IOUTP, IOUTN OSCIN, XTAL	 V_{A1} V_{A2} V_{A3}	 -0.3 to V_{A33VDD} +0.3 -0.3 to 6.0 -0.3 to $V_{OSC33VDD}$ +0.3	 V V V
Output current (2mA)	I_O	-5.2/+15.9	mA
Output current (4mA)	I_O	-10.6/+31.7	mA
Output current (8mA)	I_O	-21.2/+63.4	mA
Power dissipation	P_D	700	mW
Storage temperature	T_{stg}	-55 to 125	°C

Note:

- *The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.*
- *Directly connect all VDD pins to external power supplies and ground all VSS pins.*
- *Ensure that the junction temperature (Tj) is 125°C or less during use.*

3.2 Recommended Operating Conditions

Table- 18 shows recommended operating conditions.

Table- 18 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
External supply voltage	V_{IOVDDW} V_{A33VDD} $V_{OSC33VDD}$	---	3.1	3.3	3.5	V
Internal supply voltage	V_{CVDD} V_{A12VDD} V_{D12VDD}	---	1.1	1.2	1.3	V
Operating package surface temperature	T_C	Tj = 125°C	-40	---	85	°C

4 Package

Figure- 24 shows the package outline of KL5BPLC200WMP (Exposed TQFP-144 pins).

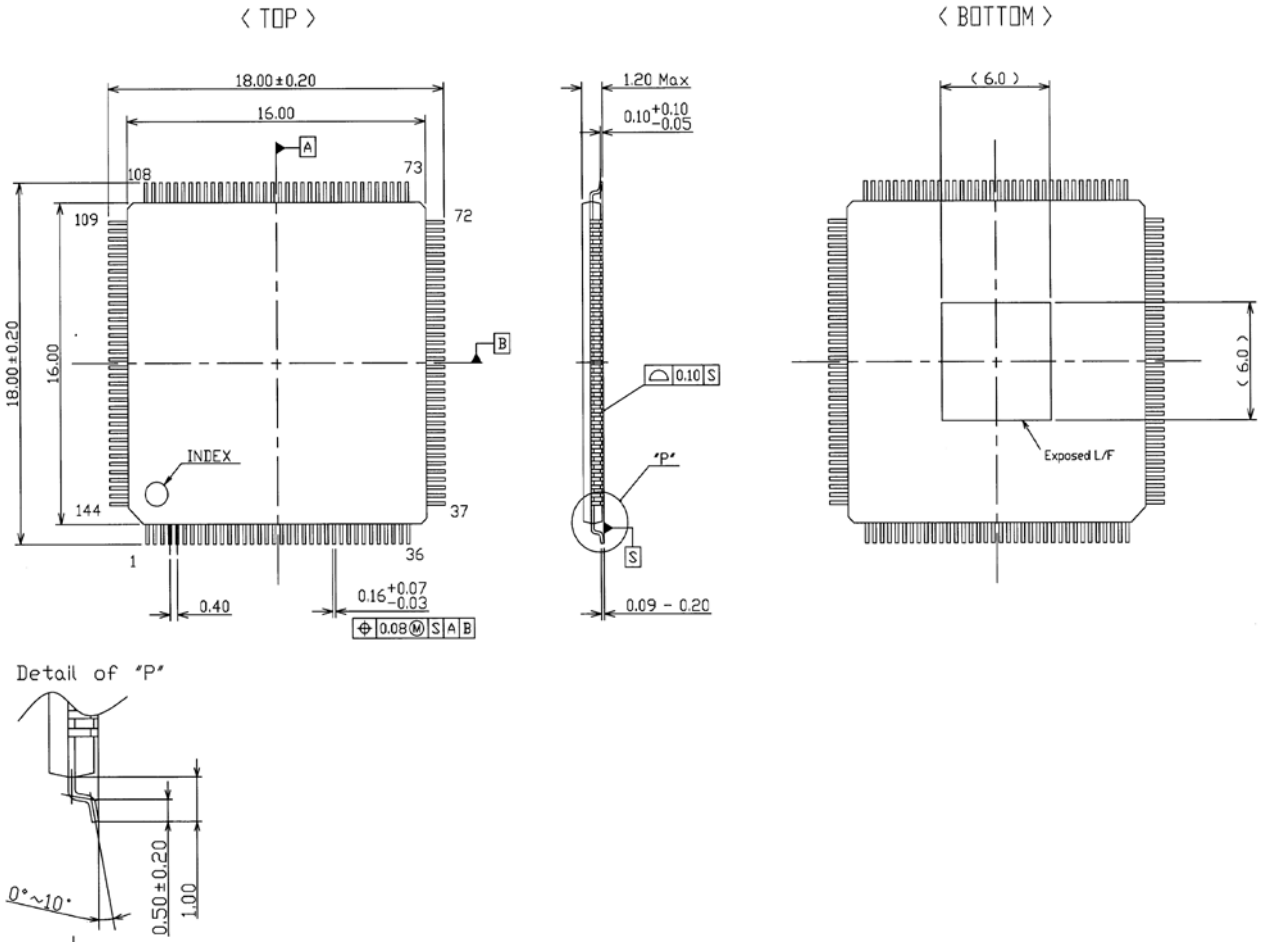

Figure- 3 KL5BPLC200WMP package outline (Exposed TQFP-144 pins)

5 Ordering Information

Part Number: KL5BPLC200WMP

Notice

- Semiconductor products may possibly experience breakdown or malfunction. Adequate care should be taken with respect to the safety design of equipment in order to prevent the occurrence of human injury, fire or social loss in the event of breakdown or malfunction of semiconductor products
- The overview of operations and illustration of applications described in this document indicate the conceptual method of use of the semiconductor product and do not guarantee operability in equipment in which the product is actually used.
- The names of companies and trademarks stated in this document are registered trademarks of the relevant companies.
- MegaChips Corporation provides no guarantees nor grants any implementation rights with respect to industrial property rights, intellectual property rights and other such rights belonging to third parties or/and MegaChips Corporation in the use of products and of technical information including information on the overview of operations and the circuit diagrams that are described in this document.
- The product described in this document may possibly be considered goods or technology regulated by the Foreign Currency and Foreign Trade Control Law. In the event such law applies, export license will be required under said law when exporting the product. This regulation shall be valid in Japan domestic.
- In the event the intention is to use the product described in this document in applications that require an extremely high standard of reliability such as nuclear systems, aerospace equipment or medical equipment for life support, please contact the sales department of MegaChips Corporation in advance.
- All information contained in this document is subject to change without notice.