Rev 0; 6/07

EVALUATION KIT AVAILABLE

Mixed-Signal Microcontroller with Analog Comparators, LCD, and RTC

MAXQ3100

General Description

The MAXQ3100 microcontroller is a low-power, 16-bit RISC device that incorporates an integrated liquid-crystal display (LCD) interface that can drive up to 160 segments, two analog comparators with precision internal 1.25V reference voltage, and a real-time clock (RTC) module with a dedicated battery-backup supply. An internal temperature sensor allows software to monitor device temperature and optionally interrupt to alert when a temperature conversion is complete. The MAXQ3100 is uniquely suited for single-phase electricity metering applications that require an external analog front-end, but can be used in any application that requires high-performance operation. The device operates at a fixed 4.194MHz, generated from the 32.76kHz RTC crystal. The device has 8kWords of EEPROM, 512 words of RAM, three 16-bit timers, and two universal synchronous/asynchronous receiver/transmitters (USARTs). The microcontroller core and I/O are powered by a single 3.3V supply, and an additional battery supply keeps the RTC running during power outages.

Applications

- Utility Meters
- Battery-Powered and Portable Devices
- Electrochemical and Optical Sensors
- Industrial Control
- Data-Acquisition Systems and Data Loggers
- Home Appliances
- Consumer Electronics
- Thermostats/Humidity Sensors
- Security Sensors
- Gas and Chemical Sensors
- HVAC
- Smart Transmitters

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXQ3100-EMN+	-40°C to +85°C	80 MQFP

+Denotes a Pb-free/RoHS-compliant device.

Typical Application Circuits and Pin Configuration appear at end of data sheet.

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* **www.maxim-ic.com/errata**.

Features

- **High-Performance, Low-Power, 16-Bit RISC Core**
  - 4.194MHz Operation, Approaching 1MIPS per MHz
  - 3.3V Core and I/O
  - 33 Instructions, Most Single-Cycle
  - Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement
  - 16-Level Hardware Stack
  - 16-Bit Instruction Word, 16-Bit Data Bus
  - 16 x 16-Bit, General-Purpose Working Registers
  - Optimized for C-Compiler (High-Speed/Density Code)
- **Program and Data Memory**
  - 8kWords EEPROM
  - 200,000 EEPROM Write/Erase Cycles
  - 512 Words of Internal Data RAM
  - JTAG-Compatible Debug Port Bootloader for Programming
- **Peripheral Features**
  - Up to 27 General-Purpose I/O Pins, Most 5V Tolerant
  - 160-Segment LCD Driver
    - Up to 4 COM and 40 Segments
    - Static, 1/2, and 1/3 LCD Bias Supported
    - No External Resistors Required
  - Two Analog Comparators with Internal +1.25V Precision Reference
  - Two Serial USARTs, One with Infrared PWM Support
  - Digital Temperature Sensor
  - Three 16-Bit Programmable Timers/Counters
  - 8-Bit, Subsecond, System Timer/Alarm
  - Battery-Backed, 32-Bit RTC with Time-of-Day Alarm and Digital Trim
  - Programmable Watchdog Timer
- **Flexible Programming Interface**
  - Bootloader Simplifies Programming
  - In-System Programming Through Debug Port
  - Supports In-Application Programming of EEPROM
- **Power Consumption**
  - 1.9mA at 4.194MHz, 3.6V Operation
  - 1.9µA Standby Current in Sleep Mode
  - Low-Power Divide-by-256 Mode

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on DV_{DD} Relative to DGND .....-0.5V to +6.0V
Voltage Range on Any Pin Relative to DGND
(3V Tolerant) .....-0.5V to (DV_{DD} + 0.5V)
Continuous Output Current
(Any Single I/O Pin).....25mA
(All I/O Pins Combined) 25mA

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DV_{DD} = V_{RST} to 3.6V, f_{32KIN} = 32.768kHz, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	DV_{DD}		V_{RST}	3.3	3.6	V
Digital Power-Fail Reset	V_{RST}		2.34	2.5	2.71	V
Battery Supply Voltage	V_{BAT}		2.0		3.8	V
Active Current (Note 2)	I_{DD1}	/1 mode		1.9	2.6	mA
	I_{DD2}	/2 mode		1.3	1.8	
	I_{DD3}	/4 mode		1.0	1.4	
	I_{DD4}	/8 mode		0.8	1.2	
	I_{DD5}	PMM1 mode		0.7	1.0	
Stop-Mode Current	I_{STOP1}	Brownout detector disabled (Note 3), T_A = +25°C		1.9	5.0	µA
		Brownout detector disabled (Note 3), T_A = +60°C		2.1	10.0	
		Brownout detector disabled (Note 3), T_A = +85°C		3.3	35.0	
	I_{STOP2}	Brownout detector enabled (Note 3)		16.3	63.0	
	I_{STOP3}	Brownout detector enabled, RTC enabled (Note 3)		16.4	64.0	
ANALOG VOLTAGE COMPARATOR						
Comparator Input-Voltage Range	V_{INPUT}		GND		DV_{DD}	V
Internal Voltage Reference	V_{REF}		1.15	1.25	1.35	V
Input Offset Voltage	V_{OS}	(Note 4)	-10		+10	mV
Input Common-Mode Voltage	V_{CMR}	(Note 4)	1		DV_{DD}	V
Common-Mode Rejection Ratio	CMMR	(Note 4)	55			dB
DC Input-Leakage Current		T_A = +25°C, CMPx pin in tri-state mode	-50		+50	nA
Comparator Setup Time	t_{CMP_SETUP}	f_{SYS} = 4.194MHz, ΔV = 20mV (Note 4)		0.8	1.6	µs
Response Time (CMPx Change to CMO Valid)	t_{CMP_RESP}	f_{SYS} = 4.194MHz, transition CMPx from DGND to DV_{DD} in ~2ns, t_{SYS} = 1/f_{SYS} (Note 4)		140 + (2 x t_{SYS})	600 + (2 x t_{SYS})	ns
Current Consumed By Comparator	I_{DD_CMP}	Per enabled comparator, CMONx = 1, brownout detector enabled, CMPx pins in tri-state mode		18.0	39.0	µA

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = V_{RST} to 3.6V, f_{32KIN} = 32.768kHz, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O						
Input High Voltage (Port 0, 1, 3, $\overline{RESET}$)	V_{IH1}		0.8 x DV_{DD}		5.5	V
Input High Voltage (Port 2)	V_{IH2}		0.8 x DV_{DD}		DV_{DD} + 0.3	V
Input Low Voltage	V_{IL}				0.2 x DV_{DD}	V
Output High Voltage (All Ports)	V_{OH}	I_{SOURCE} = 3mA	DV_{DD} - 0.4		DV_{DD}	V
Output Low Voltage (All Ports, $\overline{RESET}$)	V_{OL}	I_{SINK} = 4mA			0.4	V
Input Pullup Current	I_{PULLUP}	DV_{DD} = 3.6V, input mode with weak pullup enabled	40	120	250	µA
Input Leakage (All Ports)	I_L	Input mode with weak pullup disabled	-50		+50	nA
TEMPERATURE SENSOR						
Temperature Conversion Time	T_{CONV}	10-bit resolution, f_{SYS} = 4.194MHz		12.5		ms
		11-bit resolution, f_{SYS} = 4.194MHz		25		
		12-bit resolution, f_{SYS} = 4.194MHz		50		
		13-bit resolution, f_{SYS} = 4.194MHz		100		
Temperature Sensor Accuracy				±2		°C
RTC						
Battery Supply Current, Battery-Backed Mode	I_{BAT}	Measured on V_{BAT} pin, V_{BAT} = 3.6V, DV_{DD} = 0V, RTC enabled		1.76	3.1	µA
Battery Supply Leakage Current	I_{BATL}	Measured on V_{BAT} pin, V_{BAT} = 3.6V, DV_{DD} = 3.6V, RTC enabled		4	200	nA
Trimming Resolution		One 32.768kHz clock per 10s (Note 4)	3.05			ppm
LCD						
LCD Supply Voltage	V_{LCD}		2.4		DV_{DD}	V
LCD Bias Voltage 1	V_{LCD1}	(Note 4)	V_{ADJ} + 2/3 (V_{LCD} - V_{ADJ})			V
LCD Bias Voltage 2	V_{LCD2}	(Note 4)	V_{ADJ} + 1/3 (V_{LCD} - V_{ADJ})			V
LCD Adjustment Voltage	V_{ADJ}	(Note 4)	0		0.4 x V_{LCD}	V
LCD Digital Operating Current	I_{LCD}	Measured on DV_{DD} pin; LCFG = 0xF7, LCRA = 0x1B20, LCDx = 0xFF; LCD pins are unconnected		0.1		µA
LCD Bias Resistor	R_{LCD}			40		kΩ
LCD Adjust Resistor	R_{LADJ}	LRA3:LRA0 = 1111		80		kΩ

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ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = V_{RST} to 3.6V, f_{32KIN} = 32.768kHz, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LCD Segment Voltage	V_{SEGxx}	Segment is driven at V_{LCD}; V_{LCD} = 3V, I_{SEGxx} = -3µA, guaranteed by design	V_{LCD} - 0.06		V_{LCD}	V
		Segment is driven at V_{LCD1}; V_{LCD1} = 2V, I_{SEGxx} = -3µA, guaranteed by design	V_{LCD1} - 0.04		V_{LCD1}	
		Segment is driven at V_{LCD2}; V_{LCD2} = 1V, I_{SEGxx} = -3µA, guaranteed by design	V_{LCD2} - 0.02		V_{LCD2}	
		Segment is driven at V_{ADJ}; V_{ADJ} = 0V, I_{SEGxx} = +3µA, guaranteed by design	V_{ADJ}		0.1	
CLOCK SOURCES						
External Crystal Frequency	f_{32KIN}			32.768		kHz
Internal Clock Frequency	f_{CLK}	f_{32KIN} = 32.768kHz, DV_{DD} = 3.6V	4.110	4.194	4.278	MHz
System Clock Frequency	f_{SYS}	f_{SYS} = f_{CLK} / system clock divisor	f_{CLK} / 256		f_{CLK}	
JTAG-COMPATIBLE PROGRAMMING						
TCK Frequency	f_{TCK}	JTAG programming (Note 4)	0		f_{SYS} / 8	MHz
MEMORY CHARACTERISTICS						
EEPROM Write/Erase Cycles		Theta-JA = +25°C	200,000			Cycles
		Theta-JA = +85°C	50,000			
EEPROM Data Retention		Theta-JA = +85°C	50			Years

Note 1: Specifications to -40°C are guaranteed by design and are not production tested.
Note 2: Measured on the DV_{DD} pin with DV_{DD} = 3.6V, V_{BAT} = 3.8V, f_{32KIN} = 32.768kHz, executing from EEPROM.
Note 3: Measured on the DV_{DD} pin with DV_{DD} = 3.6V, V_{BAT} = 3.8V, f_{32KIN} = 32.768kHz, all I/O pins disconnected, and not in reset.
Note 4: Specification guaranteed by design but not production tested.

Mixed-Signal Microcontroller with Analog Comparators, LCD, and RTC

Pin Description

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>1, 11, 52, 58, 75</td><td>DGND</td><td>Digital Ground</td></tr>
<tr><td>6, 53, 59, 76</td><td>DV_{DD}</td><td>Digital Supply Voltage (+3.3V)</td></tr>
<tr><td rowspan="10">2–5, 77–80</td><td rowspan="10">P0.0–P0.7; INT0–INT7; TXD0, RXD0, T0G, T0, T1, EX</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins only. All port pins default to input mode with weak pullups enabled after a reset. All port pins can be configured as external interrupt inputs. All alternate functions must be enabled from software.
<table>
<tr><th rowspan="2">PIN</th><th colspan="2" rowspan="2">NAME</th><th colspan="2">SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>77</td><td>P0.0</td><td>INT0</td><td>TXD0</td><td>Serial Port 0 Transmit</td></tr>
<tr><td>78</td><td>P0.1</td><td>INT1</td><td>RXD0</td><td>Serial Port 0 Receive</td></tr>
<tr><td>79</td><td>P0.2</td><td>INT2</td><td>T0G</td><td>Timer 0 Gate Input</td></tr>
<tr><td>80</td><td>P0.3</td><td>INT3</td><td>T0</td><td>Timer 0 Input</td></tr>
<tr><td>2</td><td>P0.4</td><td>INT4</td><td>T1</td><td>Timer 1 Input/Output</td></tr>
<tr><td>3</td><td>P0.5</td><td>INT5</td><td>T1EX</td><td>Timer 1 External Capture/Reload Input</td></tr>
<tr><td>4</td><td>P0.6</td><td>INT6</td><td>—</td><td>—</td></tr>
<tr><td>5</td><td>P0.7</td><td>INT7</td><td>—</td><td>—</td></tr>
</table></td></tr>
<tr><td>7–10</td><td>COM0–COM3</td><td>Dedicated LCD Common-Voltage Outputs</td></tr>
<tr><td>12–43</td><td>SEG1–SEG31</td><td>Dedicated LCD Drive Outputs</td></tr>
<tr><td rowspan="10">44–51</td><td rowspan="10">P2.0–P2.7; SEG32–SEG39</td><td>General-Purpose, Digital, I/O, Type C Port; LCD Segment-Driver Output. These port pins function as bidirectional I/O pins and LCD segment-driver outputs. All alternate functions must be enabled from software.
<table>
<tr><th rowspan="2">PIN</th><th rowspan="2">NAME</th><th colspan="2">SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>44</td><td>P2.0</td><td>SEG32</td><td>LCD Segment 32</td></tr>
<tr><td>45</td><td>P2.1</td><td>SEG33</td><td>LCD Segment 33</td></tr>
<tr><td>46</td><td>P2.2</td><td>SEG34</td><td>LCD Segment 34</td></tr>
<tr><td>47</td><td>P2.3</td><td>SEG35</td><td>LCD Segment 35</td></tr>
<tr><td>48</td><td>P2.4</td><td>SEG36</td><td>LCD Segment 36</td></tr>
<tr><td>49</td><td>P2.5</td><td>SEG37</td><td>LCD Segment 37</td></tr>
<tr><td>50</td><td>P2.6</td><td>SEG38</td><td>LCD Segment 38</td></tr>
<tr><td>51</td><td>P2.7</td><td>SEG39</td><td>LCD Segment 39</td></tr>
</table></td></tr>
<tr><td>54</td><td>V_{LCD}</td><td>LCD Bias-Control Voltage. Highest LCD drive voltage used in all bias modes. This pin must be connected to an external supply when using the LCD display controller.</td></tr>
<tr><td>55</td><td>V_{LCD1}</td><td>LCD Bias, Voltage 1. Next highest LCD drive voltage, used in 1/2 and 1/3 LCD bias modes. An internal resistor-divider sets the voltage at this pin. External resistors and capacitors can be used to change LCD voltage or drive capability at this pin. This pin must be shunted externally to V_{LCD2} when using 1/2 bias mode.</td></tr>
</table>

Mixed-Signal Microcontroller with Analog Comparators, LCD, and RTC

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>56</td><td>V_{LCD2}</td><td>LCD Bias, Voltage 2. Third highest LCD drive voltage, used in 1/3 LCD bias mode only. An internal resistor-divider sets the voltage at this pin. External resistors and capacitors can be used to change LCD voltage or drive capability at this pin. This pin must be shunted externally to V_{LCD1} when using 1/2 bias mode.</td></tr>
<tr><td>57</td><td>V_{ADJ}</td><td>LCD Adjustment Voltage. Lowest LCD drive voltage, used in all bias modes. Connect to DGND through an external resistor to provide external control of the LCD contrast. Leave disconnected for internal contrast adjustment.</td></tr>
<tr><td>60–63</td><td>P1.0–P1.3; INT8–INT11; T2B, T2A, TXD1, RXD1</td><td>General-Purpose, Digital, I/O, Type D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins only. All port pins default to input mode with weak pullups enabled after a reset. Port pins P1.0–P1.3 can be configured as external interrupt inputs. All alternate functions must be enabled from software.
<table>
<tr><th rowspan="2">PIN</th><th colspan="2" rowspan="2">NAME</th><th colspan="2">SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>60</td><td>P1.0</td><td>INT8</td><td>T2B</td><td>Timer 2 Secondary I/O</td></tr>
<tr><td>61</td><td>P1.1</td><td>INT9</td><td>T2A</td><td>Timer 2 Primary I/O</td></tr>
<tr><td>62</td><td>P1.2</td><td>INT10</td><td>TXD1</td><td>Serial Port 1 Transmit</td></tr>
<tr><td>63</td><td>P1.3</td><td>INT11</td><td>RXD1</td><td>Serial Port 1 Receive</td></tr>
</table></td></tr>
<tr><td>64–70</td><td>P3.0–P3.6; TDI, TDO, TCK, TMS, SWQ, CMP0, CMP1</td><td>General-Purpose, Digital, I/O, Type C Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins only. All port pins default to input mode with weak pullups enabled after a reset. All alternate functions must be enabled from software, except for the JTAG-compatible functions that are enabled by default following reset.
<table>
<tr><th rowspan="2">PIN</th><th rowspan="2">NAME</th><th colspan="2">SPECIAL/ALTERNATE FUNCTION</th></tr>
<tr><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>64</td><td>P3.0</td><td>TDI</td><td>JTAG TAP Data Input</td></tr>
<tr><td>65</td><td>P3.1</td><td>TDO</td><td>JTAG TAP Data Output</td></tr>
<tr><td>66</td><td>P3.2</td><td>TCK</td><td>JTAG TAP Clock Input</td></tr>
<tr><td>67</td><td>P3.3</td><td>TMS</td><td>JTAG TAP Mode-Select Input</td></tr>
<tr><td>68</td><td>P3.4</td><td>SQW</td><td>RTC Square-Wave Output</td></tr>
<tr><td>69</td><td>P3.5</td><td>CMP0</td><td>Analog Comparator Input 0</td></tr>
<tr><td>70</td><td>P3.6</td><td>CMP1</td><td>Analog Comarator Input 1</td></tr>
</table></td></tr>
<tr><td>71</td><td>$\overline{RESET}$</td><td>Active-Low, Digital Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin must be pulled high by an external 50kΩ resistor. This pin is driven low as an output when an internal reset condition occurs.</td></tr>
<tr><td>72</td><td>V_{BAT}</td><td>Digital Battery-Backup Supply. This supply provides an optional battery backup for the RTC when DV_{DD} power is removed. If this pin is connected to a nominal 3.3V battery then the RTC will operate and battery-backed register contents will be preserved when DV_{DD} is removed. If battery backup is not required this pin should be connected directly to DV_{DD}.</td></tr>
<tr><td>73</td><td>32KIN</td><td rowspan="2">32kHz Crystal Input/Output. Connect an external, 6pF 32kHz watch crystal between 32KIN and 32KOUT to generate the system clock.</td></tr>
<tr><td>74</td><td>32KOUT</td></tr>
</table>

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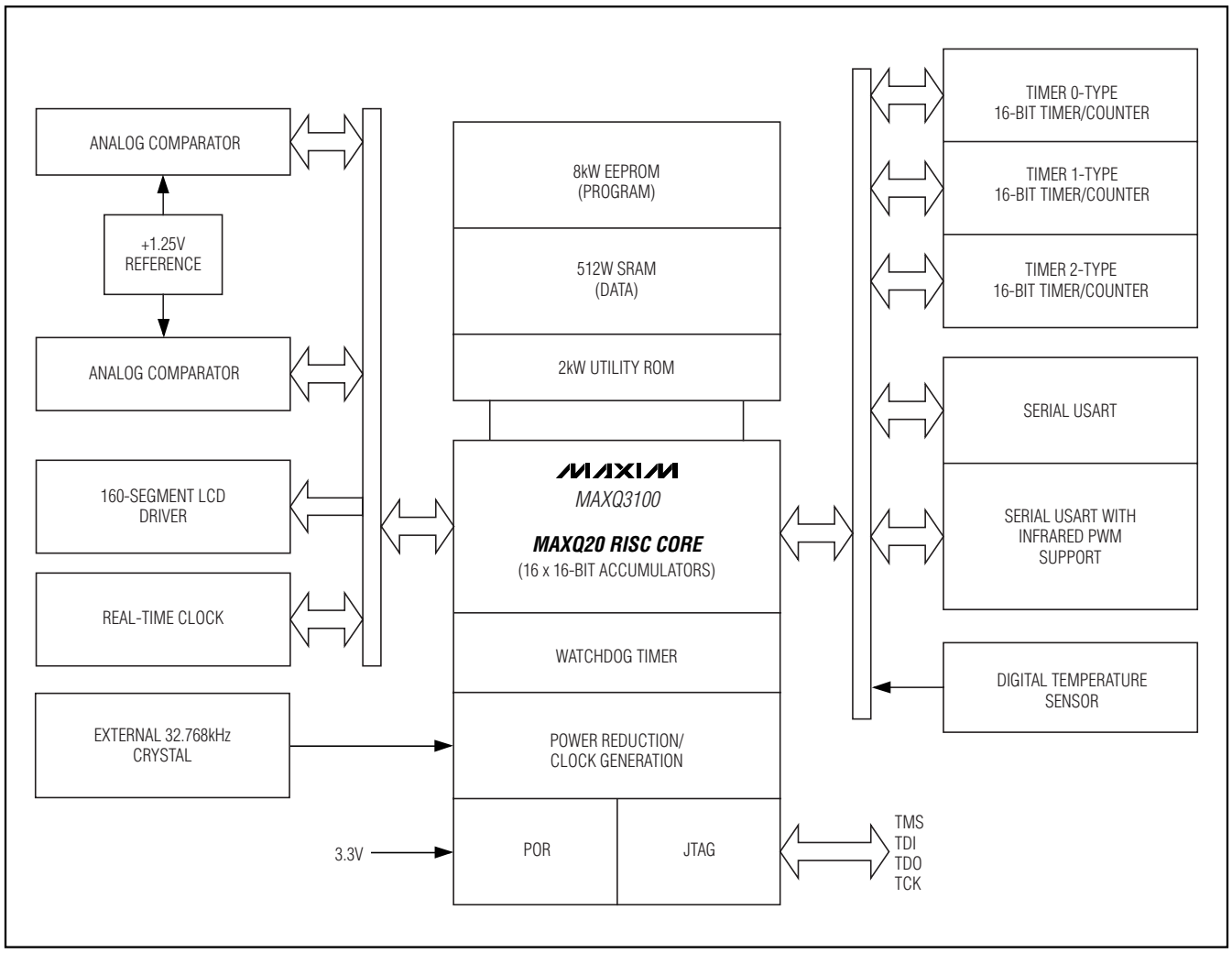
Functional Diagram



Detailed Description

The following is an introduction to the primary features of the microcontroller. More detailed descriptions of the device features can be found in the data sheets, errata sheets, and user's guides described later in the *Additional Documentation* section.

MAXQ Core Architecture

The MAXQ3100 is a high-performance, CMOS, 16-bit RISC microcontroller with EEPROM and an integrated 160-segment LCD controller. It is structured on a highly advanced, accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining, because the instruction contains both the op code and data. The result is a streamlined 4.194 million instructions-per-second (MIPS) microcontroller.

The highly efficient core is supported by a 16-level hardware stack, enabling fast subroutine calling and task switching. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement following an operation, eliminating the need for software intervention. As a result, the application speed is greatly increased.

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Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers control the peripherals and are subdivided into register modules. The family architecture is modular, so that new devices and modules can reuse code developed for existing products.

The architecture is transport-triggered. This means that writes or reads from certain register locations can also cause side effects to occur. These side effects form the basis for the higher-level op codes defined by the assembler, such as ADDC, OR, JUMP, etc. The op codes are actually implemented as MOVE instructions between certain system register locations, while the assembler handles the encoding, which need not be a concern to the programmer.

The 16-bit instruction word is designed for efficient execution. Bit 15 indicates the format for the source field of the instruction. Bits 0 to 7 of the instruction represent the source for the transfer. Depending on the value of the format field, this can either be an immediate value or a source register. If this field represents a register, the lower four bits contain the module specifier and the upper four bits contain the register index in that module.

Bits 8 to 14 represent the destination for the transfer. This value always represents a destination register, with the lower four bits containing the module specifier and the upper three bits containing the register subindex within that module.

Anytime that it is necessary to directly select one of the upper 24 index locations in a destination module, the prefix register PFX is needed to supply the extra destination bits. This prefix register write is inserted automatically by the assembler and requires only one additional execution cycle.

Memory Organization

The device incorporates several memory areas:

- 2kWords utility ROM
- 8kWords of EEPROM for program storage
- 512 words of SRAM for storage of temporary variables
- 16-level, 16-bit-wide stack memory for storage of program return addresses and general-purpose use

The memory is arranged by default in a Harvard architecture, with separate address spaces for program and data memory. The configuration of program and data space depends on the current execution location.

- When executing code from EEPROM memory, the SRAM and utility ROM are accessible in data space.
- When executing code from SRAM, the EEPROM and utility ROM are accessible in data space.
- When executing code from the utility ROM, the EEPROM memory and SRAM are accessible in data space.

Refer to the *MAXQ Family User's Guide: MAXQ3100 Supplement* for more details.

In all cases, whichever memory segment is currently being executed from cannot be accessed in data space. To allow the use of lookup tables and similar constructs in the memory, the utility ROM contains a set of lookup and block copy routines (refer to the user's guide supplement for more details).

The incorporation of EEPROM allows the device to be reprogrammed, eliminating the expense of throwing away one-time programmable devices during development and field upgrades. Program memory can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the stack location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at the stack location pointed to by SP, and then decrement SP.

Utility ROM

The utility ROM is a 2kWord block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include:

- In-system programming (bootloader) over the JTAG-compatible debug port
- In-circuit debug routines
- User-callable routines for in-application flash programming and code space table lookup

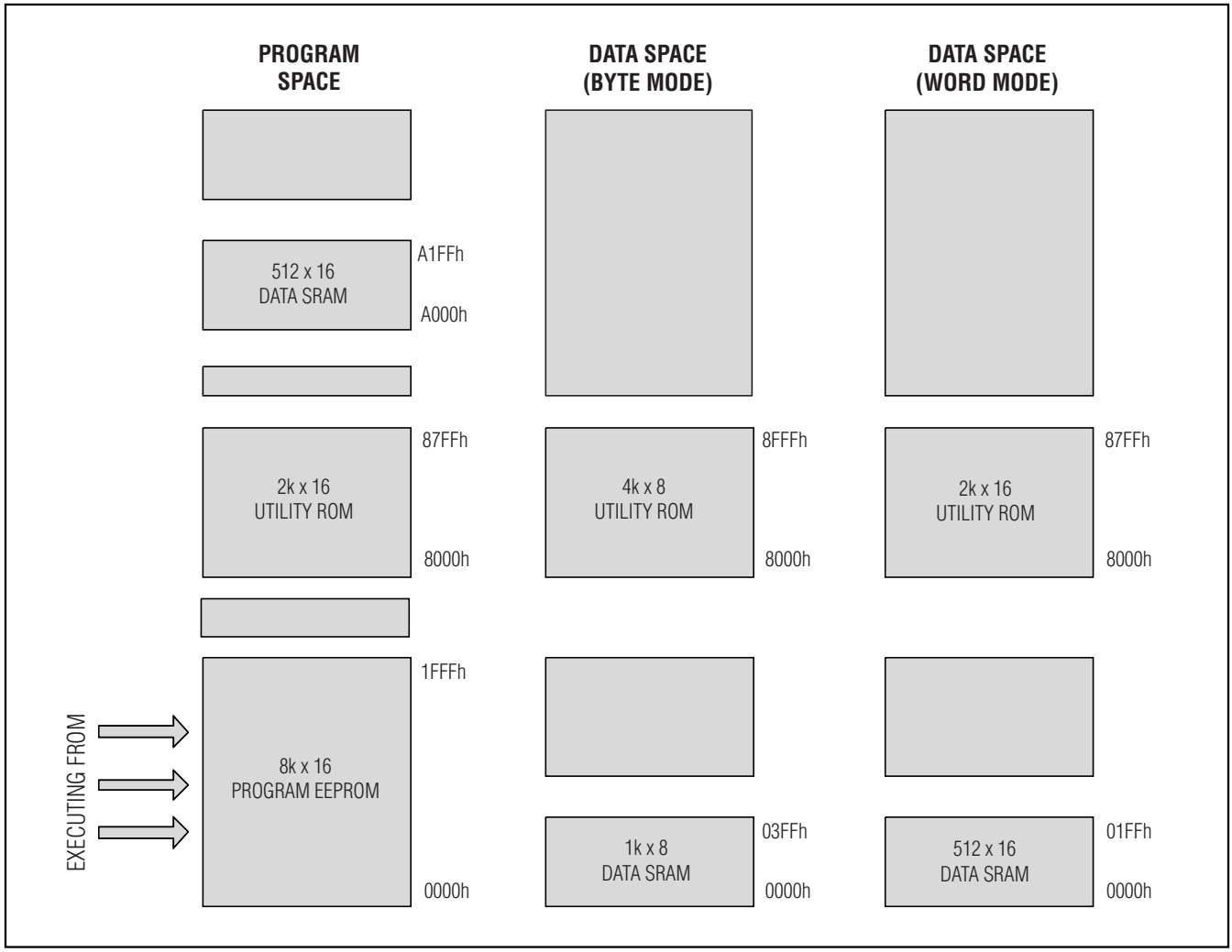

Figure 1. Memory Map When Executing from EEPROM

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Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to the start of user-application code (located at address 0000h), or to the bootloader. Routines within the utility ROM are user-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the user's guide supplement for this device.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied.

A single password-lock (PWL) bit is implemented in the SC register. When the PWL is set to one (power-on reset default), the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to zero, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase.

Programming

The microcontroller's EEPROM can be programmed by two different methods: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the life-cycle cost of the embedded system. In-system programming can be password protected to prevent unauthorized access to code memory.

In-System Programming

An internal bootloader allows the device to be reloaded over a simple JTAG-compatible debug port. As a result, system software can be upgraded in-system, eliminating the need for a costly hardware retrofit when software updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a serial-to-JTAG converter such as the one included in the MAXQ3100 evaluation kit. If in-system programmability is not required, a commercial gang programmer can be used for mass programming.

Activating the debug port and loading the test access port (TAP) with the system programming instruction invokes the bootloader. Setting the SPE bit to 1 during reset through the debug port executes the bootloader-mode program that resides in the utility ROM. When programming is complete, the bootloader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

The following bootloader functions are supported:

- Load
- Dump
- CRC
- Verify
- Erase

In-Application Programming

The in-application programming feature allows the microcontroller to modify its own program memory from its application software. This allows on-the-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible programming functions that erase and program memory. These functions are described in detail in the user's guide supplement for this device.

Register Set

Most functions of the device are controlled by sets of registers. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers and peripheral registers. The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality that may be included by different products based on the MAXQ architecture. This functionality is broken up into discrete modules so that only the features required for a given product need to be included. Tables 1 and 4 show the MAXQ3100 register set.

Table 1. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	**A (9h)**	**PFX (Bh)**	**IP (Ch)**	**SP (Dh)**	**DPC (Eh)**	**DP (Fh)**
0h	AP	A[0]	**PFX**	**IP**	—	—	—
1h	APC	A[1]	—	—	**SP**	—	—
2h	—	A[2]	—	—	**IV**	—	—
3h	—	A[3]	—	—	—	Offs	**DP[0]**
4h	PSF	A[4]	—	—	—	**DPC**	—
5h	IC	A[5]	—	—	—	**GR**	—
6h	IMR	A[6]	—	—	**LC[0]**	GRL	—
7h	—	A[7]	—	—	**LC[1]**	**BP**	**DP[1]**
8h	SC	A[8]	—	—	—	***GRS***	—
9h	—	A[9]	—	—	—	GRH	—
Ah	—	A[10]	—	—	—	***GRXL***	—
Bh	*IIR*	A[11]	—	—	—	***BP[offs]***	—
Ch	—	A[12]	—	—	—	—	—
Dh	—	A[13]	—	—	—	—	—
Eh	CKCN	A[14]	—	—	—	—	—
Fh	WDCN	A[15]	—	—	—	—	—

Note: *Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide. Registers in module AP are bit addressable.*

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Table 2. System Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									—	—	—	—	AP (4 bits)			
APC									CLR	IDS	—	—	—	MOD2	MOD1	MOD0
PSF									Z	S	—	GPF1	GPF0	OV	C	E
IC									—	—	CGDS	—	—	—	INS	IGE
IMR									IMS	—	—	—	IM3	—	IM1	IM0
SC									TAP	—	—	—	—	—	PWL	—
IIR									IIS	—	—	—	II3	—	II1	II0
CKCN									—	—	—	STOP	SWB	PMME	CD1	CD0
WDCN									POR	EWDI	WD1	WD0	WDIF	WTRF	EWT	RWT
A[0..15]	A[n] (16 bits)															
PFX	PFX (16 bits)															
IP	IP (16 bits)															
SP	—	—	—	—	—	—	—	—	—	—	—	—	SP (4 bits)			
IV	IV (16 bits)															
LC[0]	LC[0] (16 bits)															
LC[1]	LC[1] (16 bits)															
Offs									Offs (8 bits)							
DPC	—	—	—	—	—	—	—	—	—	—	—	WBS2	WBS1	WBS0	SDPS1	SDPS0
GR	GR (16 bits)															
GRL									GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
BP	BP (16 bits)															
GRS	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
GRH									GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
GRXL	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
BP[offs]	BP[offs] (16 bits)															
DP[0]	DP[0] (16 bits)															
DP[1]	DP[1] (16 bits)															

Table 3. System Register Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									0	0	0	0	0	0	0	0
APC									0	0	0	0	0	0	0	0
PSF									1	0	0	0	0	0	0	0
IC									0	0	0	0	0	0	0	0
IMR									0	0	0	0	0	0	0	0
SC									1	0	0	0	0	0	*s*	0
IIR									0	0	0	0	0	0	0	0
CKCN									1	0	0	0	0	0	0	0
WDCN									*s*	*s*	0	0	0	*s*	*s*	0
A[0..15]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PFX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
IV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Offs									0	0	0	0	0	0	0	0
DPC	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
GR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									0	0	0	0	0	0	0	0
BP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									0	0	0	0	0	0	0	0
GRXL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BP[offs]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: *Bits marked with an "s" have special behavior upon reset. Refer to the user's guide supplement for this device for more details.*

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Table 4. Peripheral Register Map

REGISTER INDEX	M0 (0h)	M1 (1h)	M2 (2h)	M3 (3h)
0h	PO0	PO1	PO2	PO3
1h	SCON0	SCON1	LCFG	RTRM
2h	SBUF0	SBUF1	**LCRA**	RCNT
3h	T0CN	T2CNB	LCD0	CCN0
4h	T0L	T2H	LCD1	CCN1
5h	T1CN	T2RH	LCD2	—
6h	T1MD	T2CH	LCD3	**TEMPR**
7h	EIF0	EIF1	LCD4	TPCFG
8h	*PI0*	*PI1*	*PI2*	*PI3*
9h	SMD0	SMD1	LCD5	RTSS
Ah	**PR0**	**PR1**	LCD6	**RTSH**
Bh	T0H	T2CNA	LCD7	**RTSL**
Ch	T1L	T2CFG	LCD8	**RSSA**
Dh	T1H	**T2V**	LCD9	RASH
Eh	T1CL	**T2C**	LCD10	**RASL**
Fh	T1CH	IRCN	LCD11	PWCN
10h	PD0	PD1	PD2	PD3
11h	—	**T2R**	LCD12	—
12h	—	—	LCD13	—
13h	—	—	LCD14	—
14h	—	—	LCD15	—
15h	—	—	LCD16	—
16h	—	—	LCD17	—
17h	—	—	LCD18	—
18h	—	—	LCD19	—
19h	—	—	—	—
1Ah	—	—	—	—
1Bh	—	—	—	—
1Ch	—	—	—	—
1Dh	—	—	—	—
1Eh	EIE0	EIE1	—	—
1Fh	EIES0	EIES1	—	—

Note: *Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide.*

Table 5. Peripheral Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									PO0.7	PO0.6	PO0.5	PO0.4	PO0.3	PO0.2	PO0.1	PO0.0
SCON0									SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF0									SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0
T0CN									ET0	T0M	TF0	TR0	GATE	C/$\overline{T}$	M1	M0
T0L									T0L.7	T0L.6	T0L.5	T0L.4	T0L.3	T0L.2	T0L.1	T0L.0
T1CN									TF1	EXF1	T1OE	DCEN	EXEN1	TR1	C/$\overline{T1}$	CP/$\overline{RL1}$
T1MD									—	—	—	—	—	—	ET1	T1M
EIF0									IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
PI0									PI0.7	PI0.6	PI0.5	PI0.4	PI0.3	PI0.2	PI0.1	PI0.0
SMD0									EIR	OFS	—	—	—	ESI	SMOD	FEDE
PR0	PR0.15	PR0.14	PR0.13	PR0.12	PR0.11	PR0.10	PR0.9	PR0.8	PR0.7	PR0.6	PR0.5	PR0.4	PR0.3	PR0.2	PR0.1	PR0.0
T0H									T0H.7	T0H.6	T0H.5	T0H.4	T0H.3	T0H.2	T0H.1	T0H.0
T1L									T1L.7	T1L.6	T1L.5	T1L.4	T1L.3	T1L.2	T1L.1	T1L.0
T1H									T1H.7	T1H.6	T1H.5	T1H.4	T1H.3	T1H.2	T1H.1	T1H.0
T1CL									T1CL.7	T1CL.6	T1CL.5	T1CL.4	T1CL.3	T1CL.2	T1CL.1	T1CL.0
PD0									PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
EIE0									EX7	EX6	EX5	EX4	EX3	EX2	EX1	EX0
EIES0									IT7	IT6	IT5	IT4	IT3	IT2	IT1	IT0
PO1									—	—	—	—	PO1.3	PO1.2	PO1.1	PO1.0
SCON1									SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF1									SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
T2CNB									ET2L	T2OE1	T2POL1	—	TF2	TF2L	TCC2	TC2L
T2H									T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8
T2RH									T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8
T2CH									T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8
EIF1									—	—	—	—	IE11	IE10	IE9	IE8
PI1									—	—	—	—	PI1.3	PI1.2	PI1.1	PI1.0
SMD1									—	—	—	—	—	ESI	SMOD	FEDE
PR1	PR1.15	PR1.14	PR1.13	PR1.12	PR1.11	PR1.10	PR1.9	PR1.8	PR1.7	PR1.6	PR1.5	PR1.4	PR1.3	PR1.2	PR1.1	PR1.0

Table 5. Peripheral Register Bit Functions (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T2CNA									ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
T2CFG									T2CI	DIV2	DIV1	DIV0	T2MD	CCF1	CCF0	C/$\overline{T2}$
T2V	T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8	T2V.7	T2V.6	T2V.5	T2V.4	T2V.3	T2V.2	T2V.1	T2V.0
T2C	T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8	T2C.7	T2C.6	TCV.5	TCV.4	TCV.3	TCV.2	TCV.1	TCV.0
IRCN									—	—	—	—	—	IREN	IRTX	IRBB
PD1									—	—	—	—	PD1.3	PD1.2	PD1.1	PD1.0
T2R	T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8	T2R.7	T2R.6	T2R.5	T2R.4	T2R.3	T2R.2	T2R.1	T2R.0
EIE1									—	—	—	—	EX11	EX10	EX9	EX8
EIES1									—	—	—	—	IT11	IT10	IT9	IT8
PO2									PO2.7	PO2.6	PO2.5	PO2.4	PO2.3	PO2.2	PO2.1	PO2.0
LCFG									PCF3	PCF2	PCF1	PCF0	—	SMO	OPM	DPE
LCRA	—	—	—	DUTY1	DUTY0	FRM3	FRM2	FRM1	FRM0	—	LRIG	—	LRA3	LRA2	LRA1	LRA0
LCD0									LCD0.7	LCD0.6	LCD0.5	LCD0.4	LCD0.3	LCD0.2	LCD0.1	LCD0.0
LCD1									LCD1.7	LCD1.6	LCD1.5	LCD1.4	LCD1.3	LCD1.2	LCD1.1	LCD1.0
LCD2									LCD2.7	LCD2.6	LCD2.5	LCD2.4	LCD2.3	LCD2.2	LCD2.1	LCD2.0
LCD3									LCD3.7	LCD3.6	LCD3.5	LCD3.4	LCD3.3	LCD3.2	LCD3.1	LCD3.0
LCD4									LCD4.7	LCD4.6	LCD4.5	LCD4.4	LCD4.3	LCD4.2	LCD4.1	LCD4.0
PI2									PI2.7	PI2.6	PI2.5	PI2.4	PI2.3	PI2.2	PI2.1	PI2.0
LCD5									LCD5.7	LCD5.6	LCD5.5	LCD5.4	LCD5.3	LCD5.2	LCD5.1	LCD5.0
LCD6									LCD6.7	LCD6.6	LCD6.5	LCD6.4	LCD6.3	LCD6.2	LCD6.1	LCD6.0
LCD7									LCD7.7	LCD7.6	LCD7.5	LCD7.4	LCD7.3	LCD7.2	LCD7.1	LCD7.0
LCD8									LCD8.7	LCD8.6	LCD8.5	LCD8.4	LCD8.3	LCD8.2	LCD8.1	LCD8.0
LCD9									LCD9.7	LCD9.6	LCD9.5	LCD9.4	LCD9.3	LCD9.2	LCD9.1	LCD9.0
LCD10									LCD10.7	LCD10.6	LCD10.5	LCD10.4	LCD10.3	LCD10.2	LCD10.1	LCD10.0
LCD11									LCD11.7	LCD11.6	LCD11.5	LCD11.4	LCD11.3	LCD11.2	LCD11.1	LCD11.0
PD2									PD2.7	PD2.6	PD2.5	PD2.4	PD2.3	PD2.2	PD2.1	PD2.0
LCD12									LCD12.7	LCD12.6	LCD12.5	LCD12.4	LCD12.3	LCD12.2	LCD12.1	LCD12.0

Table 5. Peripheral Register Bit Functions (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCD13									LCD13.7	LCD13.6	LCD13.5	LCD13.4	LCD13.3	LCD13.2	LCD13.1	LCD13.0
LCD14									LCD14.7	LCD14.6	LCD14.5	LCD14.4	LCD14.3	LCD14.2	LCD14.1	LCD14.0
LCD15									LCD15.7	LCD15.6	LCD15.5	LCD15.4	LCD15.3	LCD15.2	LCD15.1	LCD15.0
LCD16									LCD16.7	LCD16.6	LCD16.5	LCD16.4	LCD16.3	LCD16.2	LCD16.1	LCD16.0
LCD17									LCD17.7	LCD17.6	LCD17.5	LCD17.4	LCD17.3	LCD17.2	LCD17.1	LCD17.0
LCD18									LCD18.7	LCD18.6	LCD18.5	LCD18.4	LCD18.3	LCD18.2	LCD18.1	LCD18.0
LCD19									LCD19.7	LCD19.6	LCD19.5	LCD19.4	LCD19.3	LCD19.2	LCD19.1	LCD19.0
PO3									—	PO3.6	PO3.5	PO3.4	PO3.3	PO3.2	PO3.1	PO3.0
RTRM									TSGN	TRM6	TRM5	TRM4	TRM3	TRM2	TRM1	TRM0
RCNT	WE	—	—	—	—	—	FT	SQE	ALSF	ALDF	RDYE	RDY	BUSY	ASE	ADE	RTCE
CCN0									CMON	CMIE	CMF	CMM	—	CMO	CMPOL	—
CCN1									CMON	CMIE	CMF	CMM	—	CMO	CMPOL	—
TEMPR	TEMPR .15	TEMPR .14	TEMPR .13	TEMPR .12	TEMPR .11	TEMPR .10	TEMPR .9	TEMPR .8	TEMPR.7	TEMPR.5	TEMPR.5	TEMPR.4	TEMPR.3	TEMPR.2	TEMPR.1	TEMPR.0
TPCFG									TPIF	TPIE	—	—	—	RES1	RES0	START
PI3									—	PI3.6	PI3.5	PI3.4	PI3.3	PI3.2	PI3.1	PI3.0
RTSS									RTSS.7	RTSS.6	RTSS.5	RTSS.4	RTSS.3	RTSS.2	RTSS.1	RTSS.0
RTSH	RTSH. 15	RTSH. 14	RTSH. 13	RTSH. 12	RTSH. 11	RTSH. 10	RTSH. 9	RTSH. 8	RTSH.7	RTSH.6	RTSH.5	RTSH.4	RTSH.3	RTSH.2	RTSH.1	RTSH.0
RTSL	RTSL. 15	RSTL. 14	RTSL. 13	RTSL. 12	RTSL. 11	RTSL. 10	RTSL. 9	RTSL. 8	RSTL.7	RTSL.6	RTSL.5	RTSL.4	RTSL.3	RTSL.2	RTSL.1	RTSL.0
RSSA	RSSA. 15	RSSA. 14	RSSA. 13	RSSA. 12	RSSA. 11	RSSA. 10	RSSA. 9	RSSA. 8	RSSA.7	RSSA.6	RSSA.5	RSSA.4	RSSA.3	RSSA.2	RSSA.1	RSSA.0
RASH									—	—	—	—	RASH.3	RASH.2	RASH.1	RASH.0
RASL	RASL. 15	RASL. 14	RASL. 13	RASL. 12	RASL. 11	RASL. 10	RASL. 9	RASL. 8	RASL.7	RASL.6	RASL.5	RASL.4	RASL.3	RASL.2	RASL.1	RASL.0
PWCN									—	—	—	—	—	—	—	BOD
PD3									—	PD3.6	PD3.5	PD3.4	PD3.3	PD3.2	PD3.1	PD3.0

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Table 6. Peripheral Register Bit Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									1	1	1	1	1	1	1	1
SCON0									0	0	0	0	0	0	0	0
SBUF0									0	0	0	0	0	0	0	0
T0CN									0	0	0	0	0	0	0	0
T0L									0	0	0	0	0	0	0	0
T1CN									0	0	0	0	0	0	0	0
T1MD									0	0	0	0	0	0	0	0
EIF0									0	0	0	0	0	0	0	0
PI0									s	s	s	s	s	s	s	s
SMD0									0	0	0	0	0	0	0	0
PR0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T0H									0	0	0	0	0	0	0	0
T1L									0	0	0	0	0	0	0	0
T1H									0	0	0	0	0	0	0	0
T1CL									0	0	0	0	0	0	0	0
T1CH									0	0	0	0	0	0	0	0
PD0									0	0	0	0	0	0	0	0
EIE0									0	0	0	0	0	0	0	0
EIES0									0	0	0	0	0	0	0	0
PO1									0	0	0	0	1	1	1	1
SCON1									0	0	0	0	0	0	0	0
SBUF1									0	0	0	0	0	0	0	0
T2CNB									0	0	0	0	0	0	0	0
T2H									0	0	0	0	0	0	0	0
T2RH									0	0	0	0	0	0	0	0
T2CH									0	0	0	0	0	0	0	0
EIF1									0	0	0	0	0	0	0	0
PI1									0	0	0	0	s	s	s	s
SMD1									0	0	0	0	0	0	0	0
PR1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA									0	0	0	0	0	0	0	0
T2CFG									0	0	0	0	0	0	0	0
T2V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRCN									0	0	0	0	0	0	0	0
PD1									0	0	0	0	0	0	0	0
T2R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EIE1									0	0	0	0	0	0	0	0
EIES1									0	0	0	0	0	0	0	0
PO2									1	1	1	1	1	1	1	1
LCFG									0	0	0	0	0	0	0	0

Note: *Bits marked with an "s" have special behavior upon reset. Refer to the user's guide supplement for this device for more details.*

Table 6. Peripheral Register Bit Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LCRA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LCD0									0	0	0	0	0	0	0	0
LCD1									0	0	0	0	0	0	0	0
LCD2									0	0	0	0	0	0	0	0
LCD3									0	0	0	0	0	0	0	0
LCD4									0	0	0	0	0	0	0	0
PI2									s	s	s	s	s	s	s	s
LCD5									0	0	0	0	0	0	0	0
LCD6									0	0	0	0	0	0	0	0
LCD7									0	0	0	0	0	0	0	0
LCD8									0	0	0	0	0	0	0	0
LCD9									0	0	0	0	0	0	0	0
LCD10									0	0	0	0	0	0	0	0
LCD11									0	0	0	0	0	0	0	0
PD2									0	0	0	0	0	0	0	0
LCD12									0	0	0	0	0	0	0	0
LCD13									0	0	0	0	0	0	0	0
LCD14									0	0	0	0	0	0	0	0
LCD15									0	0	0	0	0	0	0	0
LCD16									0	0	0	0	0	0	0	0
LCD17									0	0	0	0	0	0	0	0
LCD18									0	0	0	0	0	0	0	0
LCD19									0	0	0	0	0	0	0	0
PO3									0	1	1	1	1	1	1	1
RTRM									0	0	s	s	s	s	s	s
RCNT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	s
CCN0									0	0	0	0	0	0	0	0
CCN1									0	0	0	0	0	0	0	0
TEMPR	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s
TPCFG									0	0	0	0	0	0	0	0
PI3									0	s	s	s	s	s	s	s
RTSS									s	s	s	s	s	s	s	s
RTSH	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s
RTSL	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s
RSSA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RASH									0	0	0	0	0	0	0	0
RASL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PWCN									0	0	0	0	0	0	0	s
PD3									0	0	0	0	0	0	0	0

Note: *Bits marked with an "s" have special behavior upon reset. Refer to the user's guide supplement for this device for more details.*

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System Timing

The MAXQ3100 generates its internal system clock from the external 32.768kHz crystal. This serves as the timebase for the RTC and is multiplied internally by a frequency-locked loop (FLL) to provide a system clock of 4.194MHz. Best performance is achieved when mated with a 32.768kHz crystal rated for a 6pF load. No external load capacitors are required. The frequency accuracy of a crystal-based oscillator circuit is dependent upon crystal accuracy, the match between the crystal and the oscillator capacitor load, ambient temperature, etc.

A crystal warmup counter enhances operational reliability. Each time the external crystal oscillation must restart, including a power-on reset, the device initiates a crystal warmup period of approximately 2 seconds. This warmup period allows time for the crystal amplitude and frequency to stabilize before using it as a clock source.

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. This means device operation can be slowed and power consumption minimized during periods of reduced activity. When more processing power is required, the microcontroller can increase its operating frequency. Software-selectable clock-divide operations allow flexibility, selecting whether a system clock cycle (SYSCLK) is 1, 2, 4, or 8 of the 4.194MHz oscillator cycles. By performing this function in software, a lower power state can be entered without the cost of additional hardware.

For extremely power-sensitive applications, two additional low-power modes are available.

- Divide-by-256 power-management mode (PMM1) (PMME = 1, CD1:0 = 00b)
- Stop mode (STOP = 1)

In PMM1, one system clock is 256 oscillator cycles, significantly reducing power consumption while the microcontroller functions at reduced speed. The optional switchback feature allows enabled interrupt sources, such as the external interrupts, to cause the processor to quickly exit PMM1 mode and return to a faster internal clock rate.

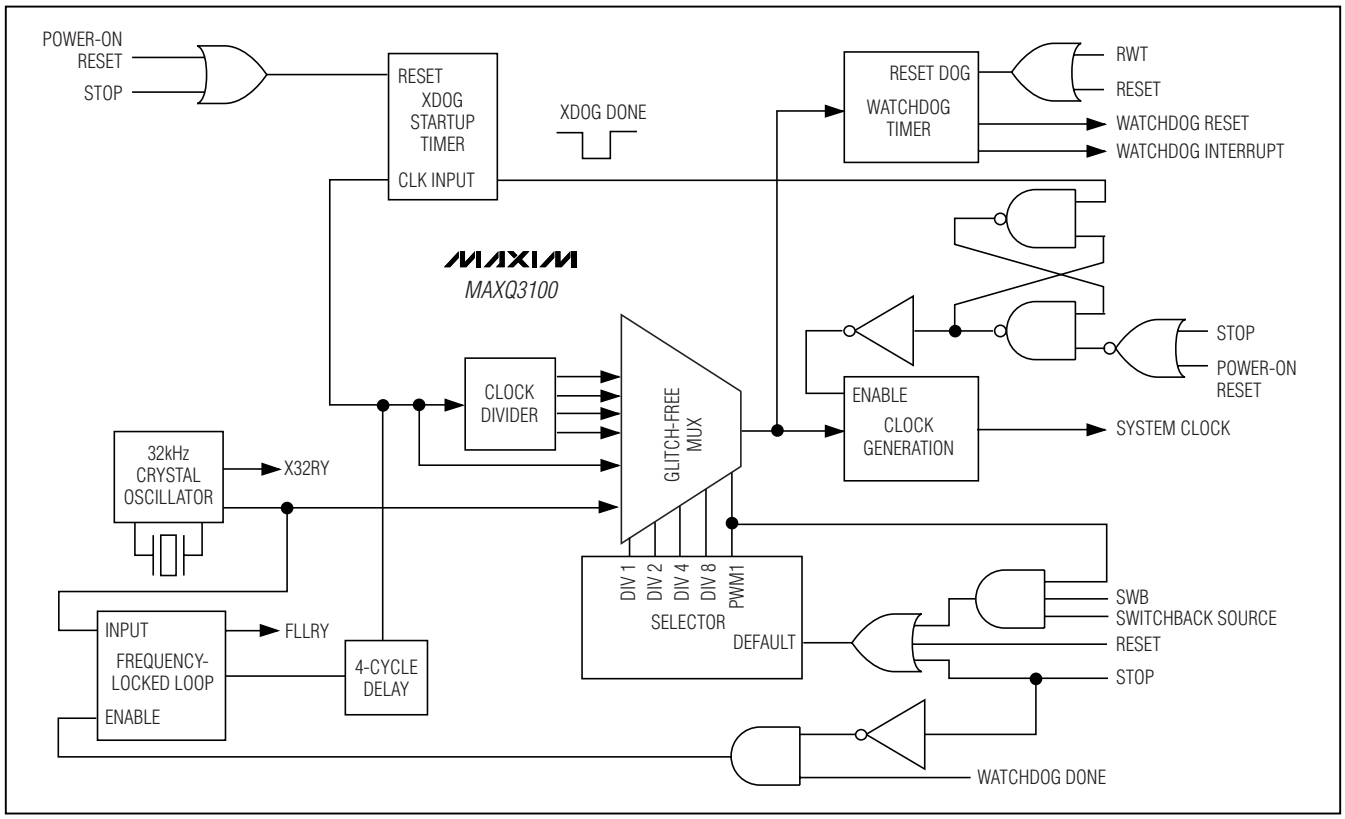

Figure 2. Clock Sources

Power consumption reaches its minimum in stop mode. In this mode, the system clock and all code execution is halted. Upon receiving one of the following enabled events, the device executes a 250ms warmup delay and then begins normal operation from the point in the code following the setting of the STOP bit:

- An enabled external interrupt pin is triggered.
- An enabled comparator interrupt is triggered.
- An external reset signal is applied to the $\overline{\text{RESET}}$ pin.
- The RTC time-of-day or subsecond alarms are activated.

The following peripherals can be enabled during stop mode:

- Analog comparators
- RTC
- LCD controller

Interrupts

Multiple interrupt sources are available for quick response to internal and external events. The MAXQ architecture uses a single interrupt vector (IV), single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the user-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay, and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, the user program must determine whether a jump to 0000h came from a reset or interrupt source.

Once software control has been transferred to the ISR, the interrupt identification register (IIR) can determine if a system register or peripheral register was the source of the interrupt. The specified module can then be interrogated for the specific interrupt source and software can take appropriate action. Because the interrupts are evaluated by user software, the user can define a unique interrupt priority scheme for each application. The following interrupt sources are available.

- Watchdog Interrupt
- External Interrupts 0 to 11
- Analog Comparator 0 and 1 Interrupts
- Temperature Sensor Interrupt
- RTC Time-of-Day and Subsecond Alarms
- Serial Port 0 Receive and Transmit Interrupts
- Serial Port 1 Receive and Transmit Interrupts
- Timer 0 Overflow Interrupt
- Timer 1 Overflow and External Trigger Interrupts
- Timer 2 Low Compare, Low Overflow, Capture/Compare, and Overflow Interrupts

Reset Sources

Several reset sources are provided for microcontroller control. Although code execution is halted in the reset state, the high-frequency oscillator continues to oscillate.

Power-On Reset/Brownout Reset

An internal power-on reset circuit enhances system reliability. This circuit forces the device to perform a power-on reset whenever a rising voltage on DV_{DD} climbs above approximately V_{RST}. Additionally, the device performs a brownout reset whenever DV_{DD} drops below V_{RST}, a feature that can be optionally disabled in stop mode. The following events occur during a power-on reset:

- All registers and circuits enter their power-on reset state.
- I/O pins revert to their reset state, with logic one states tracking DV_{DD}.
- The power-on reset flag is set to indicate the source of the reset.
- Code execution begins at location 8000h following a 2-second 32.768kHz warmup.

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ Family User's Guide*. Software can determine if a reset was caused by a watchdog timeout by checking the watchdog timer reset flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Asserting the external $\overline{\text{RESET}}$ pin low causes the device to enter the reset state. The external reset functions as described in the *MAXQ Family User's Guide*. Execution resumes at location 8000h after the $\overline{\text{RESET}}$ pin is released.

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I/O Ports

The microcontroller uses the Type C and Type D bidirectional I/O ports described in the *MAXQ Family User's Guide*. The use of two port types allows for maximum flexibility when interfacing to external peripherals. Each port has independent, general-purpose I/O pins and three configure/control registers. Many pins support alternate functions such as timers or interrupts, which are enabled, controlled, and monitored by dedicated peripheral registers. Using the alternate function automatically converts the pin to that function.

Type C port pins have Schmitt Trigger receivers and full CMOS output drivers, and can support alternate functions. The pin is either tri-stated or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register.

Type D port pins have Schmitt Trigger receivers and full CMOS output drivers, and can support alternate functions. The pin is either tri-stated or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. All Type D pins also have interrupt capability.

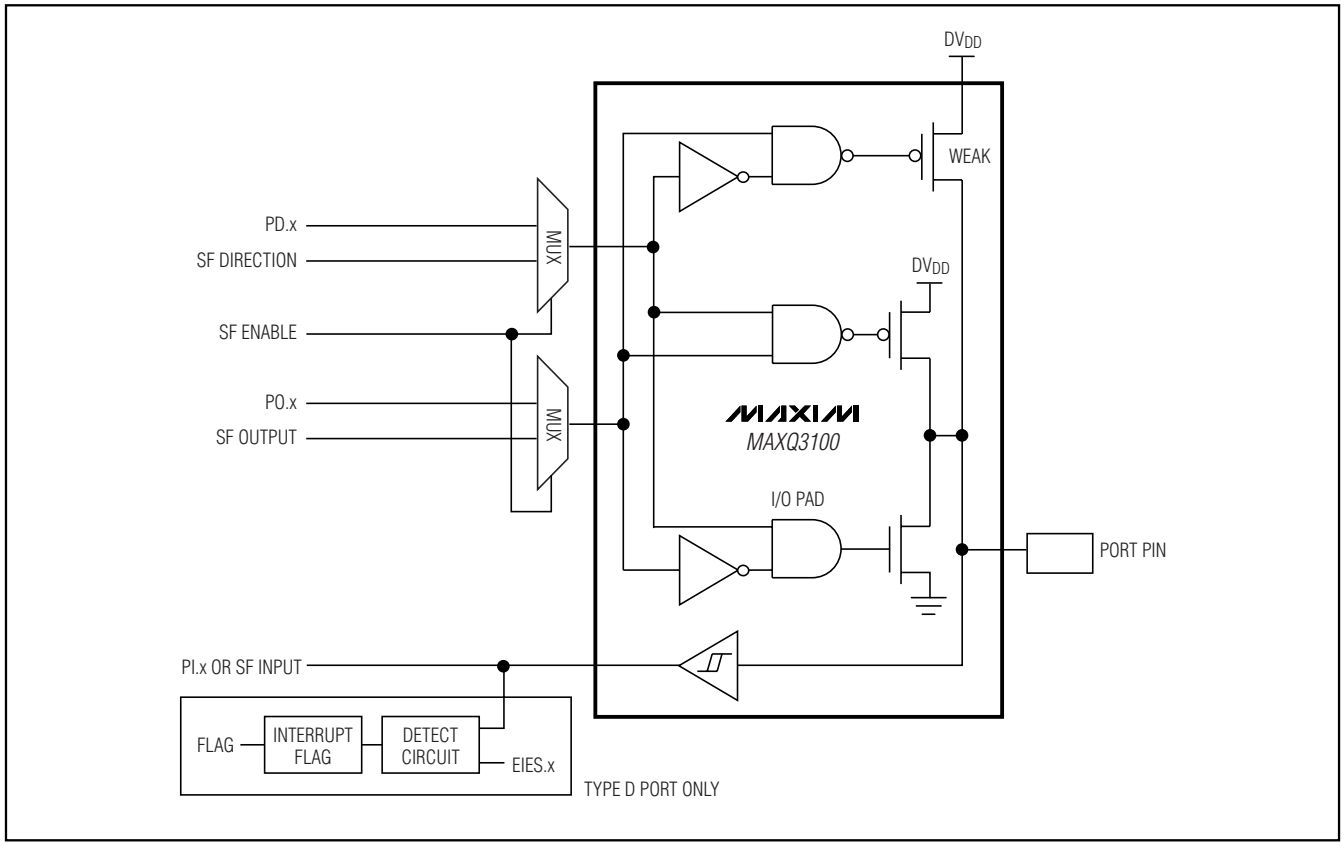

Figure 3. Type C/D Port Pin Schematic

Real-Time Clock

A binary real-time clock keeps the time of day in absolute seconds with 1/256-second resolution. The 32-bit second counter can count up to approximately 136 years and be translated to calendar format by the application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode.

The independent subsecond alarm runs from the same RTC, and allows the application to perform periodic interrupts up to 8 seconds with a granularity of approximately 3.9ms. This creates an additional timer that can be used to measure long periods without performance degradations. Traditionally, long time periods have been measured using multiple interrupts from shorter programmable timers. Each timer interrupt required servicing, with each accompanying interruption slowing system operation. By using the RTC subsecond timer as a long-period timer, only one interrupt is needed, eliminating the performance hit associated with using a shorter timer.

Higher accuracy can be obtained by using the user-accessible digital RTC trim function. This feature allows the designer to fine tune the RTC timing to compensate for crystal inaccuracies and any unintended board-level effects that could cause crystal-frequency drift. The user can enable a 1Hz or 512Hz square-wave output on P3.4. Frequency measurements of these signals can show if there is any deviation from the expected frequency, and writes to the RTC trim register can compensate in increments of 1 to 127 steps, with each step approximately 3.05ppm (30.5µs).

If the V_{BAT} pin is not directly tied to the DV_{DD} pin, then there may be a short increase in I_{DD} while the device is switching between V_{BAT} and DV_{DD} as the RTC power source. I_{DD} can temporarily increase up to 300µA while DV_{DD} is rising and in the range $1.05 \times V_{BAT} < DV_{DD} < [(1.05 \times V_{BAT}) + 200mV]$. A similar effect may be observed while V_{BAT} is falling and in the range $[(0.95 \times DV_{DD}) - 200mV] < V_{BAT} < 0.95 \times DV_{DD}$.

Programmable Timers

The MAXQ3100 incorporates one instance each of the timer 0, timer 1, and timer 2 peripherals. These timers can be used in counter/timer/capture/compare/PWM functions, allowing precise control of internal and external events. Timer 2 supports optional single-shot, external gating, and polarity control options as well as carrier generation support for infrared transmit/receive functions using serial port 0.

Timer 0

The timer 0 peripheral includes the following:

- 8-bit autoreload timer/counter
- 13-bit or 16-bit timer/counter
- Dual 8-bit timer/counter
- External pulse counter

Timer 1

The timer 1 peripheral includes the following:

- 16-bit autoreload timer/counter
- 16-bit capture
- 16-bit counter
- Clock generation output

Timer 2

The timer 2 peripheral includes the following:

- 16-bit autoreload timer/counter
- 16-bit capture
- 16-bit counter
- 8-bit capture and 8-bit timer
- 8-bit counter and 8-bit timer
- Infrared carrier generation support

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the processor if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer is controlled through bits in the WDCN register. Its timeout period can be set to one of four programmable intervals ranging from 2^{12} to 2^{21} system clocks in its default mode, allowing flexibility to support different types of applications. The interrupt occurs 512 system clocks before the reset, allowing the system to execute an interrupt and place the system in a known, safe state before the device performs a total system reset. At 4.194MHz, watchdog timeout periods can be programmed from 976µs to 128s, depending on the system clock mode.

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In-Circuit Debug

Embedded debugging capability is available through the debug port TAP. Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. Figure 4 shows a block diagram of the in-circuit debugger. The in-circuit debug features include:

- Hardware debug engine
- Set of registers able to set breakpoints on register, code, or data accesses
- Set of debug service routines stored in the utility ROM

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

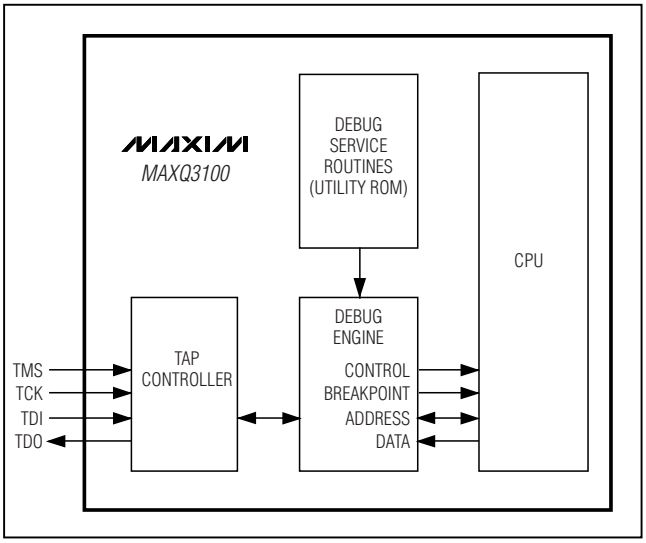

Figure 4. In-Circuit Debugger

Serial Peripherals

The MAXQ3100 incorporates two 8051-style universal synchronous/asynchronous receiver/transmitters. The USARTs allow the device to conveniently communicate with other RS-232 interface-enabled devices, as well as PCs and serial modems when paired with an external RS-232 line driver/receiver. The dual independent USARTs can communicate simultaneously at different baud rates with two separate peripherals. The USART can detect framing errors and indicate the condition through a user-accessible software bit.

The time base of the serial ports is derived from either a division of the system clock or the dedicated baud clock generator. The following table summarizes the operating characteristics as well as the maximum baud rate of each mode.

Serial port 0 contains additional functionality to support low-speed infrared transmission in combination with the PWM function of timer 2. When enabled in this mode, the serial port automatically outputs a waveform generated by combining the normal serial port output waveform with the PWM carrier waveform output by timer 2, using a logical OR or logical NOR function. The output of serial port 0 in this mode can be used to drive an infrared LED to communicate using a fixed-frequency carrier modulated signal. Depending on the drive strength required, the output may require a buffer when used for this purpose.

MODE	TYPE	START BITS	DATA BITS	STOP BIT	MAX BAUD RATE AT 4.194MHz
Mode 0	Synchronous	—	8	—	1.05Mbps
Mode 1	Asynchronous	1	8	1	131kbps
Mode 2	Asynchronous	1	8 + 1	1	131kbps
Mode 3	Asynchronous	1	8 + 1	1	131kbps

Analog Comparators

The MAXQ3100 incorporates a pair of 1-bit analog-to-digital comparators. The comparator inputs can be connected to a wide range of peripherals, including chemical, motion, or proximity detectors; voltage-supply monitoring; or any other appropriate analog input. The comparator measures the analog inputs against the internal +1.25V reference. The polarity of the internal comparator-output signal can be selected to indicate a value above or below the internal reference. The comparators can be configured to generate an optional interrupt in addition to setting an internal flag when the input is out of range. A combination of the two comparators along with appropriate biasing of an input allows the two comparators to be used as a window comparator. When not in use, the pins associated with the comparator are usable as general-purpose I/O. A useful feature of the comparators is that they can be used to wake the device from stop mode, allowing the device to monitor external voltages while in an ultra-low-power mode and only wake when necessary.

Temperature Sensor

The internal temperature sensor has a user-selectable resolution of 10 (0.5°C), 11 (0.25°C), 12 (0.125°C), or 13 (0.0625°C) bits. Higher resolutions require longer conversion times.

Setting the START bit initiates the temperature conversion, and the temperature sensor hardware clears the bit when the conversion is complete. This bit can be polled by software, or, optionally, the temperature conversion complete interrupt can be used to alert the system that the results are ready to be read from the temperature results register (TEMPR).

Applications Information

Grounds and Bypassing

Careful PC-board layout significantly minimizes crosstalk among the comparator inputs and other digital signals. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Bypass DV_{DD} with a capacitor as low as 1µF and keep bypass capacitor leads short for best noise rejection.

This device incorporates both analog and digital components, straddling both the analog and digital ground planes. For increased accuracy, an LC filter can be used to isolate pin 59. This pin powers the analog circuitry, and the additional filtering reduces the noise entering the analog block.

Device Applications

The low-power, high-performance RISC architecture of the MAXQ3100 makes it an excellent fit for many applications that require analog measurements combined with the intelligence of a full-featured microcontroller. Simple voltage-dividers can be used to scale any input into a value in the range of the +1.25V reference. The dual comparators allow the device to function as a simple limit comparator or window comparator in a wide range of analog applications.

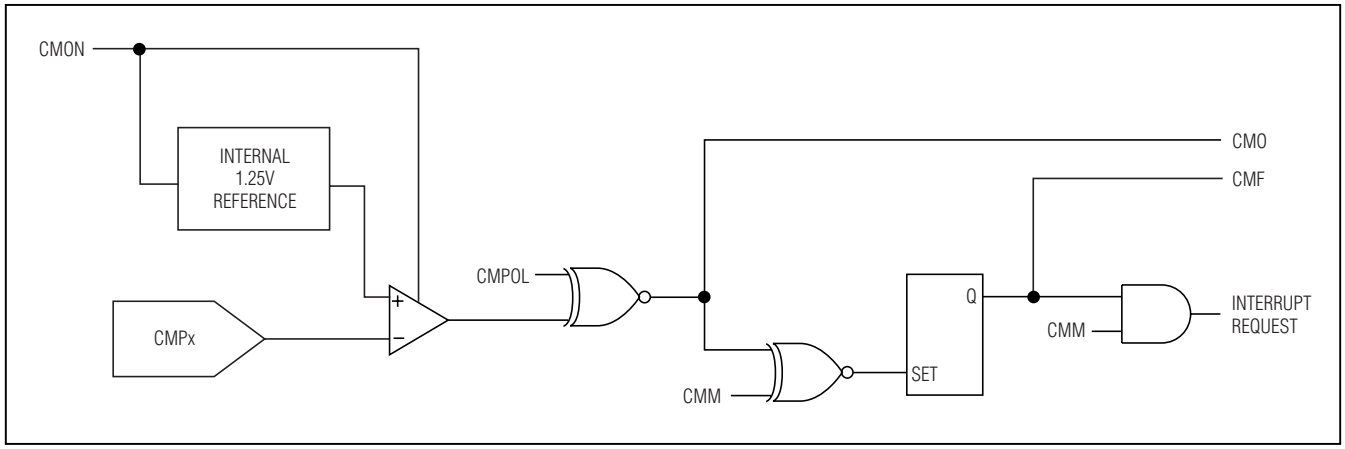

Figure 5. Analog Comparator Functional Diagram

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Additional Documentation

Designers must have four documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about programming, device features, and operation. The following documents can be downloaded from www.maxim-ic.com/microcontrollers.

- The MAXQ3100 data sheet, which contains electrical/timing specifications and pin descriptions, available at www.maxim-ic.com/MAXQ3100.
- The MAXQ3100 errata sheet, available at www.maxim-ic.com/errata.
- The *MAXQ Family User's Guide*, which contains detailed information on core features and operation, including programming, avaliable at www.maxim-ic.com/MAXQUG.
- The *MAXQ Family User's Guide: MAXQ3100 Supplement*, which contains detailed information on features specific to the MAXQ3100, available at www.maxim-ic.com/MAXQ3100UG.

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this microcontroller are available from Maxim/Dallas Semiconductor and third-party suppliers, including:

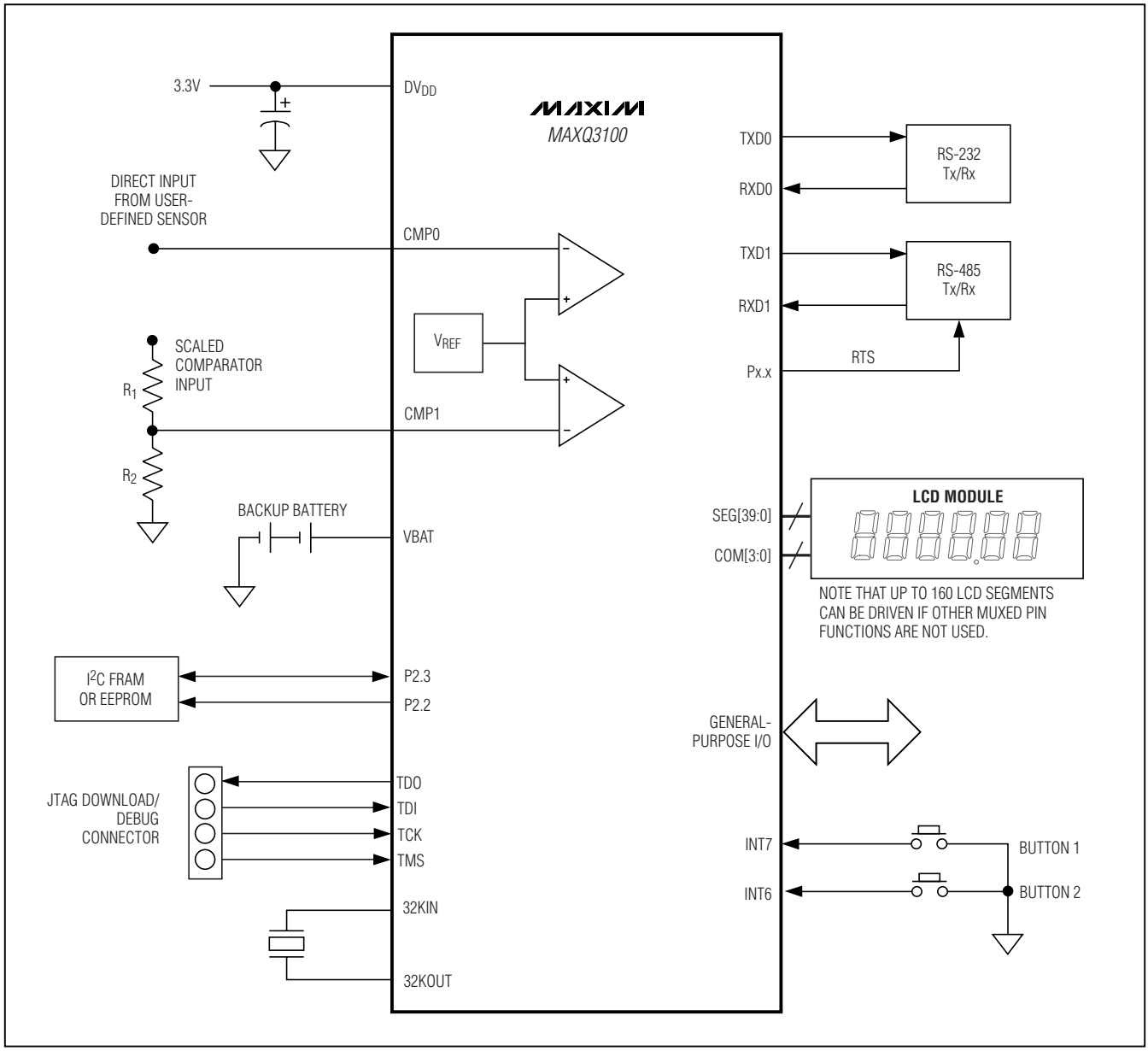
- Compilers
- In-circuit emulators
- Integrated development environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found on our website at www.maxim-ic.com/microcontrollers. Technical support is available through email at maxq.support@dalsemi.com.

Typical Application Circuits

Typical Application Circuit #1

Typical Application Circuit #1 shows a general-purpose implementation using a MAXQ3100 that reads two sensor inputs, displays result and status information on an LCD display, and also interfaces simultaneously with an RS-232 and RS-485 networks. I/O pins that are not dedicated to special functions are available to control other system functions.



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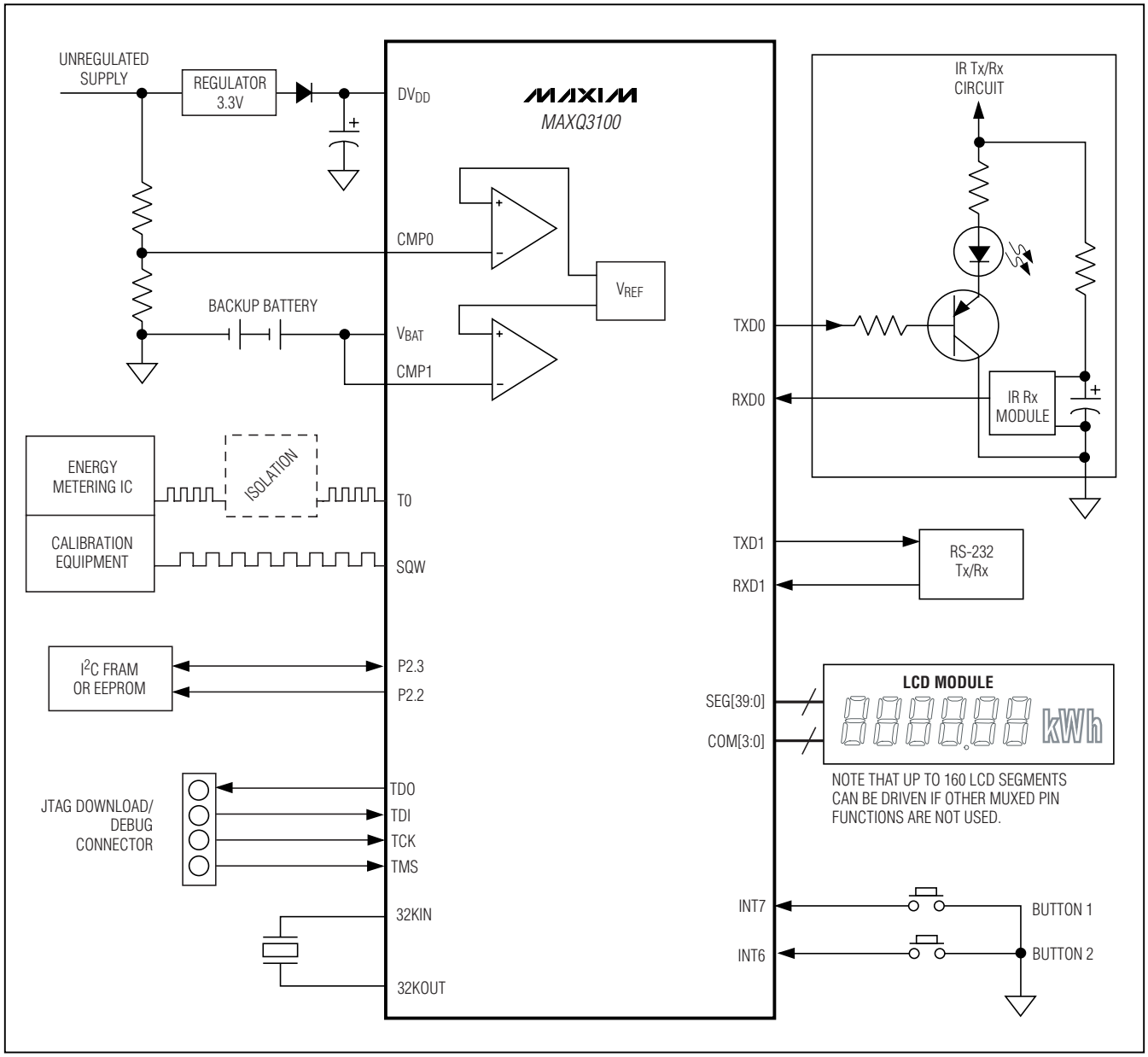
Typical Application Circuits (continued)

Typical Application Circuit #2

Another target application of the MAXQ3100 is in the electricity metering market. When coupled with an analog front-end, the microcontroller becomes the core of an affordable electricity metering solution. Such an application can accurately keep time, incorporate a versatile display, and allow for multiple modes of communication. See *Typical Application Circuit #2*.



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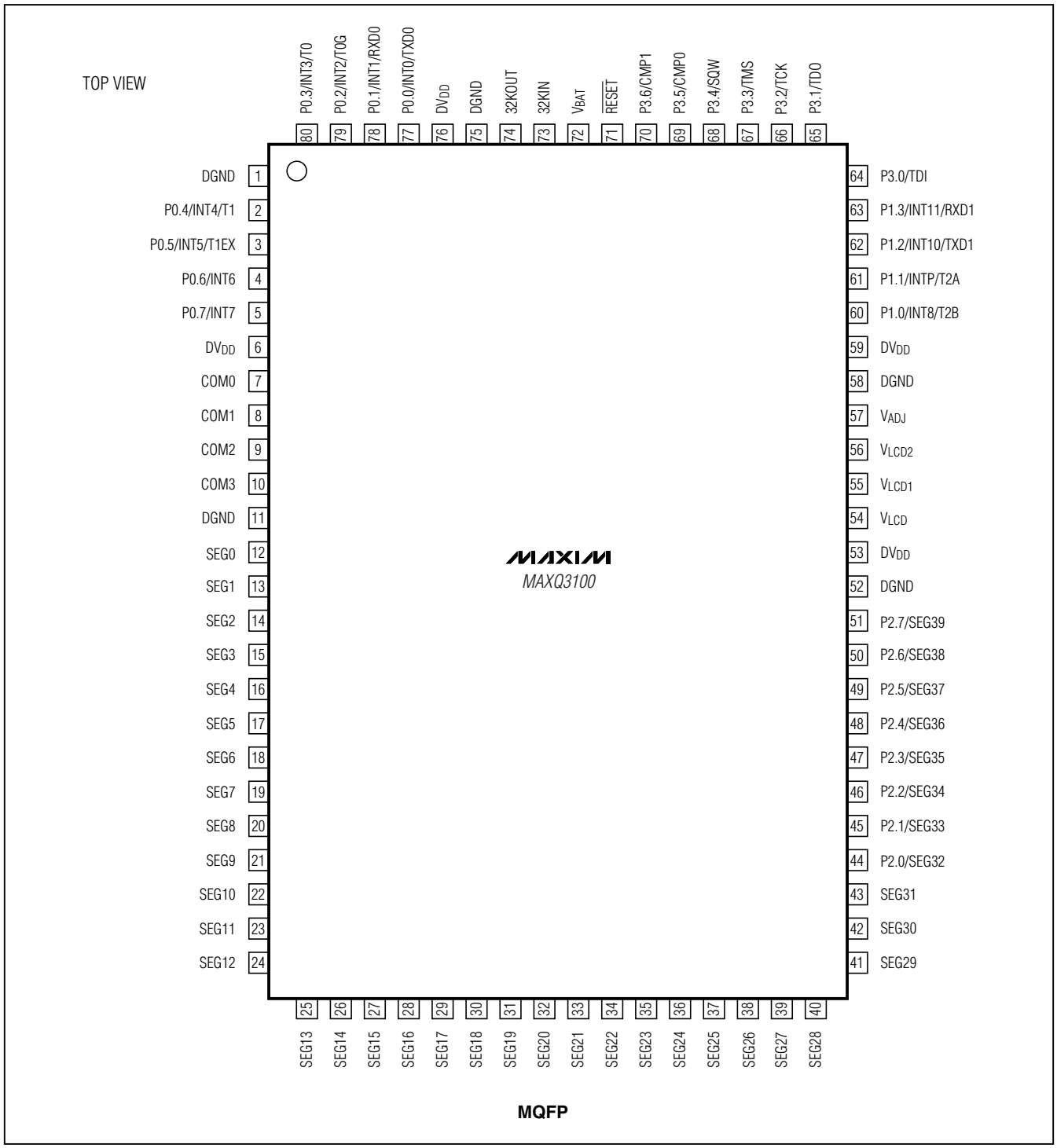
Pin Configuration



MQFP

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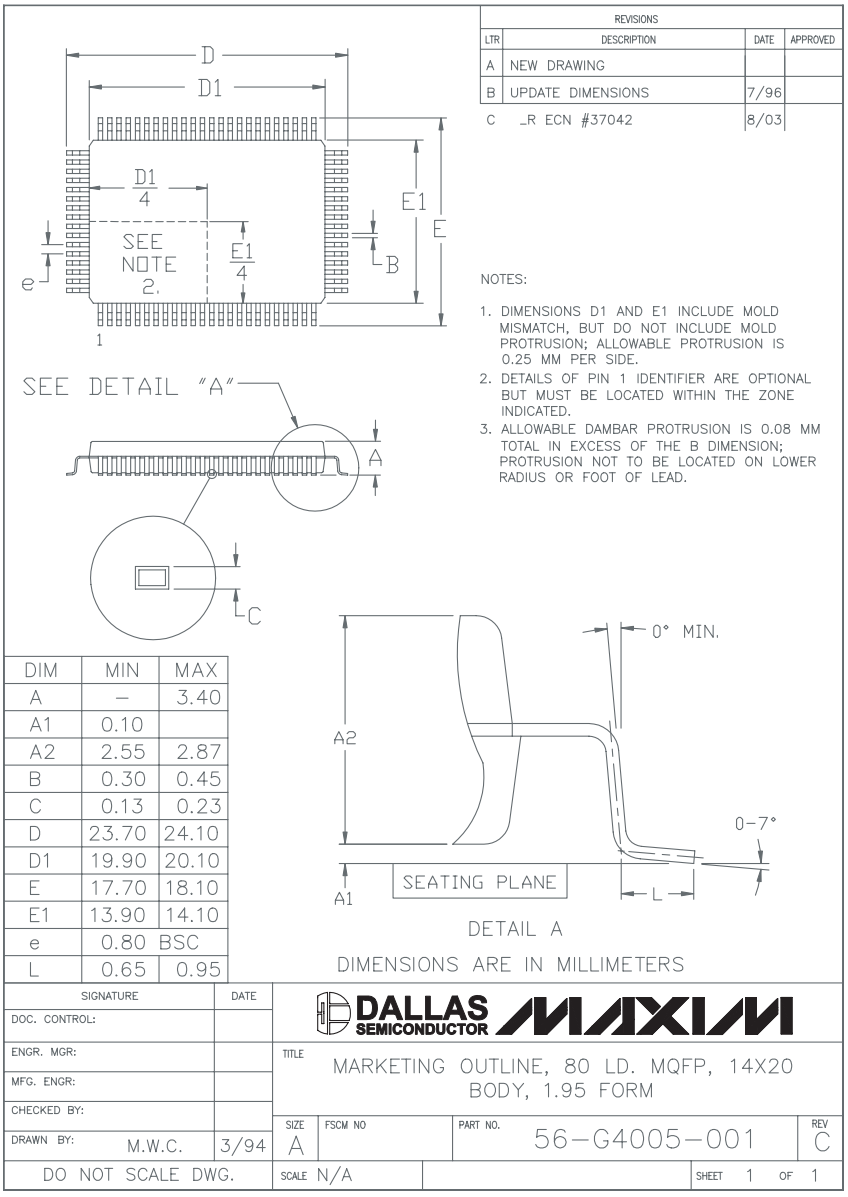
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**).



Revision History

Rev 0; 6/07: Original release.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.