19-5470; Rev 0; 7/10

EVALUATION KIT AVAILABLE

Multiband Digital Television Tuner

General Description

The MAX3544 broadband single-conversion television tuner is designed for use in digital (DVB-T, DVB-C, GB20600) television sets and terrestrial receivers. It receives all television bands from 47MHz to 862MHz and converts the selected channel to an industry-standard 36MHz IF.

The MAX3544 includes a variable-gain low-noise input amplifier; an RF tracking filter; an image rejection mixer; a peak detector; an optional internal, self-contained RF gain-control loop (RFAGC); a VCO with fractional-N PLL; an IF bandpass filter; an IF variable-gain amplifier; and a crystal oscillator.

The MAX3544 is available in a small, 6mm x 6mm, thin QFN package, and the application circuit fits in 20mm x 25mm on a two-layer board with single-sided component mounting.

Applications

DVB-T/DVB-T2	DTMB/GB20600
DVB-C	ATSC

Features

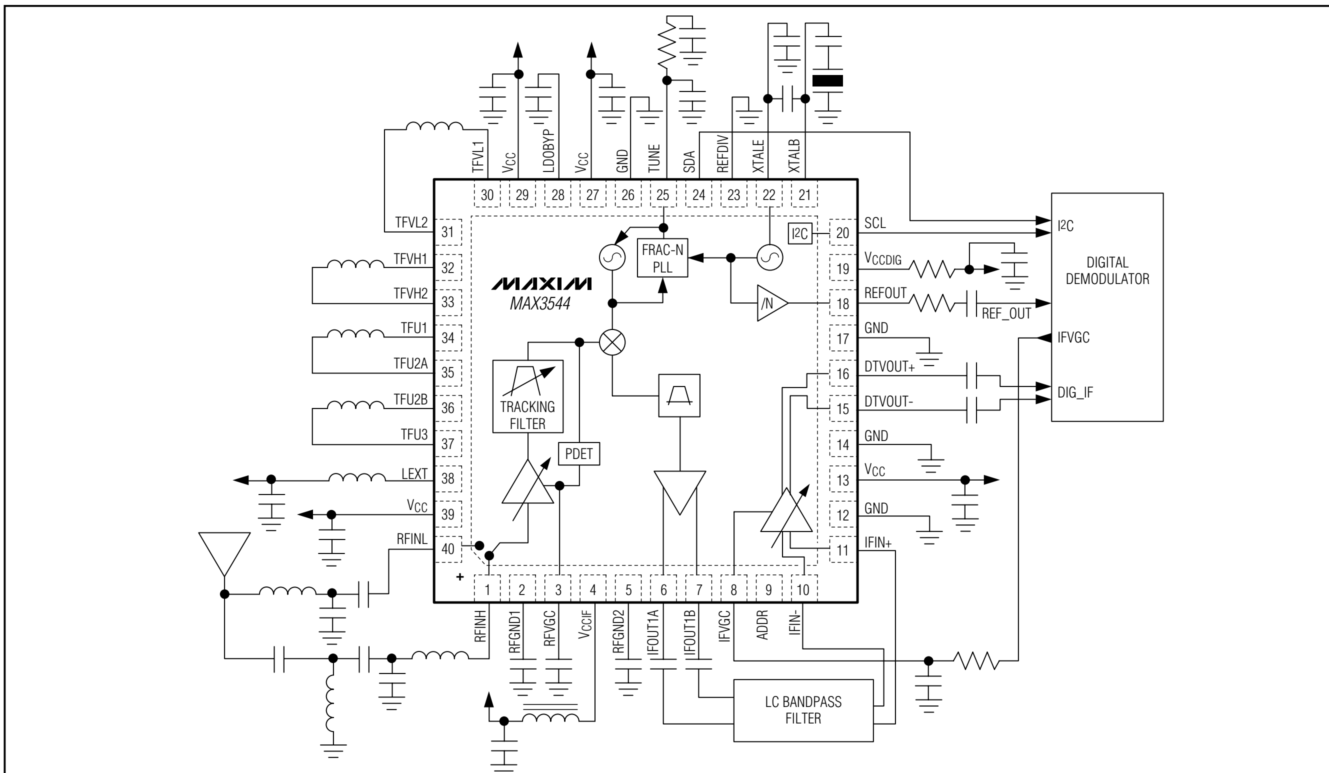
- ♦ **Standard IF Architecture Ensures < -70dBc Spurs**
- ♦ **Integrated RF Tracking Filter**
- ♦ **Integrated IF Bandpass Filter**
- ♦ **Full-Band Coverage (47MHz to 862MHz)**
- ♦ **70dB Image Rejection**
- ♦ **4dB Noise Figure**
- ♦ **Fast-Locking, Low Phase-Noise PLL Supports 256QAM**
- ♦ **Crystal Oscillator and Buffer/Divider to Drive Baseband IC**
- ♦ **745mW Power Dissipation**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3544CTL+	0°C to +70°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

Block Diagram/Typical Application Circuit/Pin Configuration



NOTE: LAYOUT FITS 25mm x 20mm ON 2-LAYER BOARD WITH DEVICE PLACEMENT ON TOP SIDE ONLY.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND...-0.3V to +3.6V
RFINL, RFINH, IFIN+, IFIN-, DTVOUT+, DTVOUT-,
IFOUT1A, IFOUT1B............................. -0.3V to (V_{CC} + 0.3V)
SDA, SCLK, IFAGC, RFVGA ....-0.3V to +3.6V
Short-Circuit Protection: DTVOUT+, DTVOUT-,
IFOUT1A, IFOUT1B .... Indefinite
RF Input Power... +10dBm
Continuous Power Dissipation (T_A = +70°C)
(derate 35.7mW/°C above +70°C)............................2857mW
Operating Temperature Range............................ 0°C to +70°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +165°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX3544 Evaluation Kit, V_{CC} = 3.1V to 3.5V, T_A = 0°C to +70°C, registers set according to Table 1. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT					
Supply Voltage		3.1		3.5	V
Supply Current	IF VGA enabled		225	270	mA
	Standby (REF oscillator on) R08[7] = 1		5		
RF and IF VGC Input Bias Current	At 0.5V to 3.0V DC		-100 to +100		µA
RF and IF VGC Control Voltage	Maximum gain	3.0			V
RF and IF VGC Control Voltage	Minimum gain			0.5	V
SERIAL INTERFACE					
Input Logic-Level Low				0.3 x V_{CC}	V
Input Logic-Level High		0.7 x V_{CC}			V
Output Logic-Level Low	3mA sink current			0.4	V
Output Logic-Level High		V_{CC} - 0.5V			V
Maximum Clock Rate		400			kHz

AC ELECTRICAL CHARACTERISTICS

(MAX3544 Evaluation Kit, RF center frequency = 666MHz, IF center frequency = 36.15MHz, registers set according to Table 1, f_{REF} = 16MHz, V_{RFVGC} = V_{IFVGC} = 3.0V, V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL REQUIREMENTS (RF INPUT TO IF OUTPUT)					
RFINL Operating Frequency Range	Tunable frequency range	47		345	MHz
RFINH Operating Frequency Range	Tunable frequency range	345		862	MHz
Maximum Voltage Gain to IFOUT1	DVB-T mode (see Table 1)		50		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX3544 Evaluation Kit, RF center frequency = 666MHz, IF center frequency = 36.15MHz, registers set according to Table 1, f_{REF} = 16MHz, V_{RFVGC} = V_{IFVGC} = 3.0V, V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Gain Control Range	(gain at V_{RFVGC} = 3.0V) - (gain at V_{RFVGC} = 0.5V)			53		dB
Noise Figure				4		dB
Image Rejection	Image applied at 77.8MHz above desired channel's center frequency	47MHz to 470MHz		> 70		dB
		470MHz to 862MHz		> 65		
IF VARIABLE-GAIN AMPLIFIER						
Maximum Voltage Gain	Output load impedance > 2kΩll3pF, differential load			60		dB
Minimum Voltage Gain	Output load impedance > 2kΩll3pF, differential load, V_{IFVGC} = 0.5V			19		dB
In-Channel Output V1dB	36.15MHz CW output signal			> 2.5		V_{P-P}
DETECTOR						
Wideband Detector Input-Referred Attack Point	Programmable, R0B[6:4] = 100, CW input signal			-36		dBm
Narrowband Detector Input-Referred Attack Point	Programmable, R0B[2:0] = 011, CW input signal			-47		dBm
SIGMA-DELTA FRAC-N SYNTHESIZER						
N-Divider Value			19		251	
Fractional-N Resolution				20		Bits
Phase-Detector Frequency	f_{XTAL}/2		8		10.5	MHz
Phase-Detector Frequency	f_{XTAL}/1		16		21	MHz
REFERENCE OSCILLATOR						
Frequency	(Note 2)		16		32	MHz
External Overdrive Level	AC-coupled sine-wave input		0.5		1.5	V_{P-P}
REFERENCE OSCILLATOR OUTPUT BUFFER						
Output Frequency	/1, /4 modes		4	4	f_{XTAL}	MHz
Output Level	Load Impedance > 20kΩll3pF			1.1		V_{P-P}

Note 1: Guaranteed by production test at +25°C. 0°C and +70°C are guaranteed by design and characterization.
Note 2: Guaranteed by design and characterization.

Typical Register Summary

Table 1 shows register settings to configure the MAX3544 for operation with a 16MHz crystal frequency and 666MHz RF frequency with a differential LC bandpass filter.

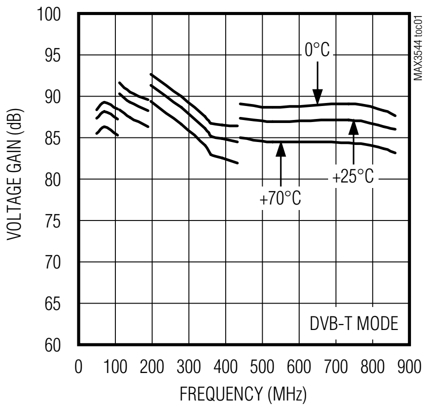
Table 1. Typical Register Settings

REGISTER NAME	REGISTER ADDRESS	REGISTER FUNCTION	DVB-T MODE, 8MHz DIFFERENTIAL IF (hex)
R00	0x00	VCO	4C
R01	0x01	NDIV INT	2B
R02	0x02	NDIV FRAC2	8E
R03	0x03	NDIV FRAC1	26
R04	0x04	NDIV FRAC0 (VAS Trigger)	66
R05	0x05	MODE CTRL	D8
R06	0x06	TFS	Calculated from ROM values
R07	0x07	TFP	Calculated from ROM values
R08	0x08	SHUTDOWN	00
R09	0x09	REF CONFIG	0A
R0A	0x0A	VAS CONFIG	16
R0B	0x0B	PWRDET CFG1	43
R0C	0x0C	PWRDET CFG2	01
R0D	0x0D	FILT CF ADJ	Read from ROM
R0E	0x0E	ROM ADDR	00
R0F	0x0F	IRHR	Read from ROM
R10	0x10	ROM READBACK	Read only
R11	0x11	VAS STATUS	Read only
R12	0x12	GEN STATUS	Read only
R13	0x13	BIAS ADJ	56
R14	0x14	TEST1	40
R15	0x15	ROM WRITE DATA	Maxim use only

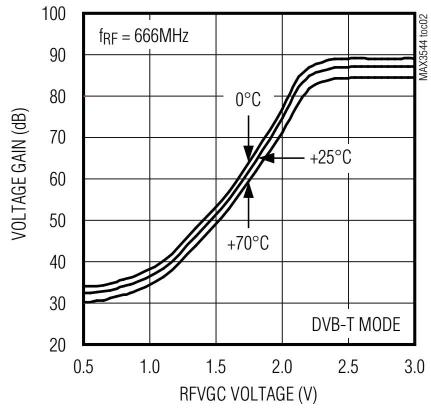
Typical Operating Characteristics

(MAX3544 Evaluation Kit, V_{CC} = 3.3V, T_A = +25°C, registers set according to Table 1, unless otherwise noted.)

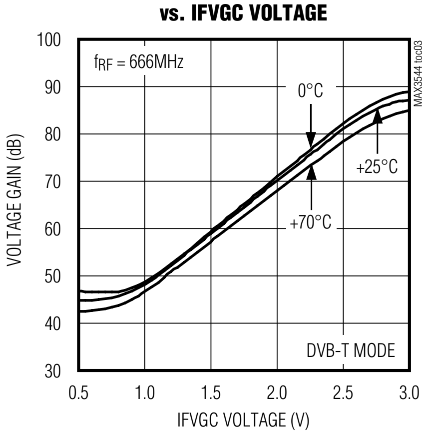
CASCADED VOLTAGE GAIN vs. FREQUENCY



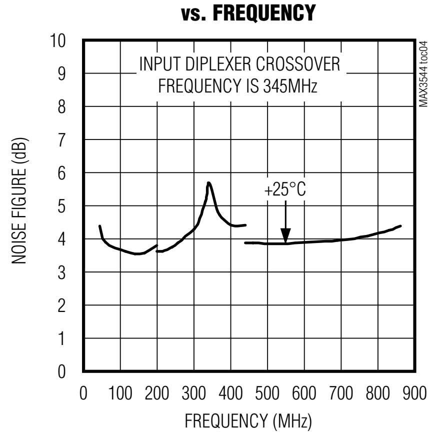
CASCADED VOLTAGE GAIN vs. RFVGC VOLTAGE



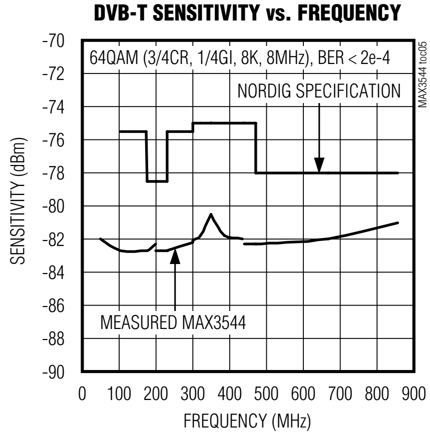
CASCADED VOLTAGE GAIN vs. IFVGC VOLTAGE



NOISE FIGURE vs. FREQUENCY



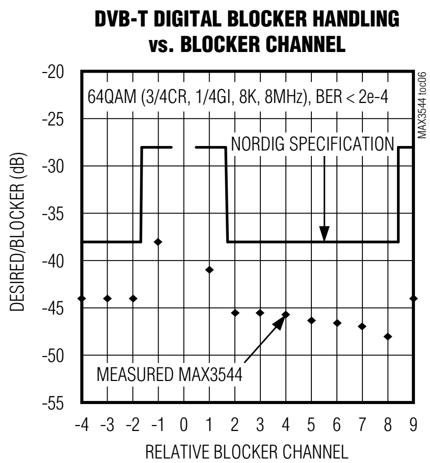
DVB-T SENSITIVITY vs. FREQUENCY

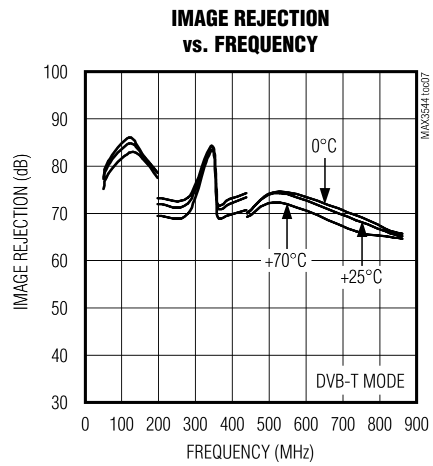


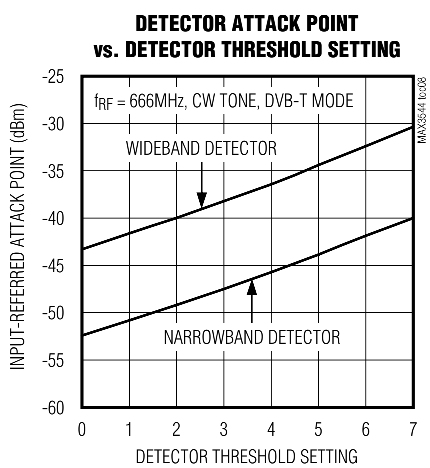
Multiband Digital Television Tuner

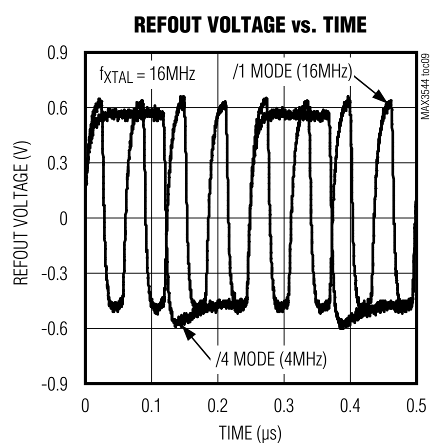
Typical Operating Characteristics (continued)

(MAX3544 Evaluation Kit, V_{CC} = 3.3V, T_A = +25°C, registers set according to Table 1, unless otherwise noted.)









Pin Description

PIN	NAME	FUNCTION
1	RFINH	High-Frequency RF Input. Matched to 75Ω over the operating band. Requires a DC-blocking capacitor.
2	RFGND1	RF Ground. Bypass to the PCB's ground plane with a 1000pF capacitor. Keep traces as short as possible to minimize inductance to ground plane. **Do not connect RFGND1 and RFGND2 together.**
3	RFVGC	RF VGA Gain Control Voltage. Accepts a DC voltage from 0.5V to 3V.
4	V_{CCIF}	IF Power Supply. Requires a 600Ω series ferrite bead to a bypass capacitor to ground.
5	RFGND2	RF Ground. Bypass to the PCB's ground plane with a 1000pF capacitor. Keep traces as short as possible to minimize inductance to ground plane. **Do not connect RFGND1 and RFGND2 together.**
6	IFOUT1A	Dual-Mode IF Output. In single-ended mode, this pin is the IF signal output. In differential mode, this pin is the positive terminal of the differential IF output.
7	IFOUT1B	Dual-Mode IF Output. In single-ended mode, this pin is the SAW filter bandwidth switch. In differential mode, this pin is the negative terminal of the differential IF output.
8	IFVGC	IF VGA Gain Control Voltage. Accepts a DC voltage from 0.5V to 3V.
9	ADDR	2-Wire Serial-Interface Address Line. This pin sets the device address for the I^2C-compatible serial interface. There are three selectable addresses based on the state of this pin: logic-low, logic-high, or unconnected.
10, 11	IFIN-, IFIN+	Differential IF VGA Input. Connect to the IF filter output.
12, 14, 17, 26	GND	Ground. Connect pin to paddle ground to minimize trace inductance.
13, 27, 29, 39	V_{CC}	Power-Supply Connections. Bypass each supply pin with a separate 1000pF capacitor to ground.
15, 16	DTVOUT-, DTVOUT+	Differential IF VGA Output. Connect to the demodulator input. Requires a 1000pF DC-blocking capacitor.
18	REFOUT	Crystal Output to Drive Baseband IC. Output frequency is f_{XTAL} or $f_{XTAL}/4$.
19	V_{CCDIG}	Digital Supply. Requires a 15Ω series resistor to a 1µF bypass capacitor.
20	SCL	2-Wire Serial Clock Interface. Connect to the serial bus and ensure the bus includes an approximately 5kΩ pullup resistor.
21	XTALB	Crystal Oscillator Base. Connect to the crystal through a DC-blocking capacitor and connect a capacitor to XTALE.
22	XTALE	Crystal Oscillator Emitter. Connect a capacitor to ground and a capacitor to XTALB.
23	REFDIV	Reference Frequency Divider Control. Three modes are available depending on the state of this pin: high = $f_{XTAL}/1$, low = $f_{XTAL}/4$, unconnected = state determined by register. **Note: Power-up state of register is not guaranteed; therefore, unconnected mode should only be used if the controller can reprogram I^2C in any of the divider settings.**
24	SDA	2-Wire Serial Data Interface. Connect to serial bus and ensure the bus includes an approximately 5kΩ pullup resistor.
25	TUNE	PLL Charge-Pump Output and TUNE Input. Connect to the PLL loop filter.
28	LDOBYP	Bypass for On-Chip VCO LDO. Bypass to ground with a 0.47µF capacitor.

Multiband Digital Television Tuner

Pin Description (continued)

PIN	NAME	FUNCTION
30	TFVL1*	VHF Low Tracking Filter 1
31	TFVL2*	VHF Low Tracking Filter 2
32	TFVH1*	VHF High Tracking Filter 1
33	TFVH2*	VHF High Tracking Filter 2
34	TFU1*	UHF Tracking Filter 1
35	TFU2A*	UHF Tracking Filter 2A
36	TFU2B*	UHF Tracking Filter 2B
37	TFU3*	UHF Tracking Filter 3
38	LEXT*	RF VGA Supply Voltage. Connect through a 270nH pullup inductor to V_{CC}.
40	RFINL	Low-Frequency RF Input. Matched to 75Ω over the operating band. Requires a DC-blocking capacitor.
—	EP (GND)	Exposed Paddle Ground. Solder evenly to the PCB ground plane for proper operation.

**Improper placement of these inductors degrades image rejection, gain, and noise figure. Copy Maxim reference design layout exactly in this area.*

Detailed Description

I²C-Compatible Serial Interface

The MAX3544 uses a 2-wire I²C-compatible serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX3544 and the master at clock frequencies up to 400kHz. The master initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX3544 behaves as a slave device that transfers and receives data to and from the master. Pull SDA and SCL high with external pullup resistors for proper bus operation.

One bit is transferred during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte in or out of the MAX3544 (8 data bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX3544 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX3544 has a 7-bit slave address plus one $R/\overline{W}$ bit. These 8 bits must be sent to the device following a START condition to initiate communication. The slave address is determined by the state of the ADDR pin as shown in Table 2.

Table 2. Address Configurations

ADDR PIN	ADDR2	ADDR1	WRITE ADDRESS	READ ADDRESS
0	0	0	0xC0	0xC1
Unconnected	0	1	0xC2	0xC3
1	1	0	0xC4	0xC5

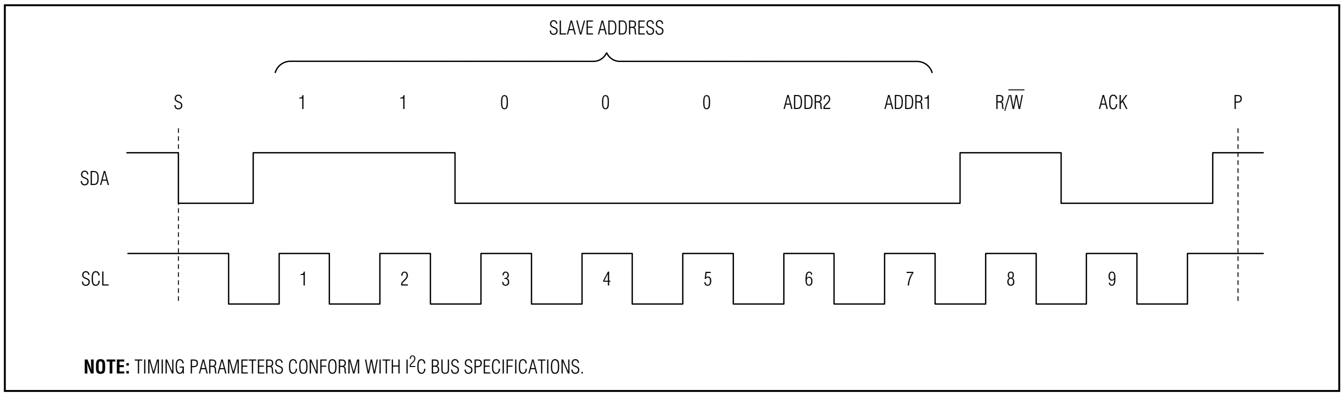


Figure 1. MAX3544 Slave Address Byte. Example shows read address 0x0C1 (ADDR pin grounded).

The MAX3544 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/$\overline{W}$ bit (Figure 1).

Write Cycle

When addressed with a write command, the MAX3544 allows the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition followed by the 7 slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX3544 issues an ACK if the slave address byte is successfully received. The bus master must then send to the slave the address of the first register it wishes to write to. If the slave acknowledges the address, the master can then write 1 byte to the register at the specified address. Data is written beginning with the most significant bit. The MAX3544 again issues an ACK if the data is successfully written to the register. The master can continue to write data to the successive internal registers with the MAX3544 acknowledging each successful transfer, or it can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

Figure 2 illustrates an example in which registers 0, 1, and 2 are written with 0x0E, 0xD8, and 0xE1, respectively.

Read Cycle

A read cycle begins with the bus master issuing a START condition followed by the 7 slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX3544 issues an ACK if the slave address byte is successfully received. The master then sends the 8-bit address of the first register that it wishes to read. The MAX3544 then issues another ACK. Next, the master must issue a START condition followed by the 7 slave address bits and a read bit (R/$\overline{W}$ = 1). The MAX3544 issues an ACK if it successfully recognizes its address and begins sending data from the specified register address starting with the most significant bit (MSB). Data is clocked out of the MAX3544 on the rising edge of SCL. On the ninth rising edge of SCL, the master can issue an ACK and continue reading successive registers or it can issue a NACK followed by a STOP condition to terminate transmission. The read cycle does not terminate until the master issues a STOP condition. Figure 3 illustrates an example in which registers 0 and 1 are read back.

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	11000[ADDR2][ADDR1]	0	—	0x00	—	0x0E	—	0xD8	—	0xE1	—	

Figure 2. Example: Write registers 0, 1, and 2 with 0x0E, 0xD8, and 0xE1, respectively.

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE 1ST REGISTER ADDRESS	ACK	START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	READ DATA REG 0	ACK	READ DATA REG 1	NACK	STOP
	110000[ADDR2][ADDR1]	0	—	0x00	—		110000[ADDR2][ADDR1]	1	—	D7–D0	—	D7–D0	—	

Figure 3. Example: Read data from registers 0 and 1.

Control Register Description

The MAX3544 includes 18 programmable registers, two status registers (read only), one register for ROM readback (read only), and one for Maxim use only. The programmable registers configure the VCO settings, PLL settings, detector and AGC settings, state control, bias adjustments, individual block shutdown, and the tracking filter frequency. These programmable registers are also readable. The read-only registers include two status registers and a ROM table data register.

Typical bit settings are provided only for user convenience and are not guaranteed at power-up. All registers must be written no earlier than 100µs after power-up or recovery from a brownout event (i.e., when V_{CC} drops below 1V) to initialize the registers. Then follow up by rewriting the registers needed for channel/frequency programming (i.e., registers R00–R04). The typical values listed in Table 3 configure the MAX3544 for DVB-T reception with 16MHz crystal, 8MHz channel BW, 36.15MHz IF center frequency, differential LC bandpass filter, and 666MHz RF center frequency.

Table 3. Register Configuration

REG ADDR	REG NAME	REGISTER FUNCTION	TYPICAL SETTING	MSB			BIT LOCATION				LSB
				7	6	5	4	3	2	1	0
0x00	R00	VCO	4C	VCO[1:0]		VSUB[3:0]				VDIV[1:0]	
0x01	R01	NDIV INT	2B	NINT[7:0]							
0x02	R02	NDIV FRAC2	8E	CPS	CP	RDIV[1:0]		F[19:16]			
0x03	R03	NDIV FRAC1	26	F[15:8]							
0x04	R04	NDIV FRAC0 (VAS Trigger)	66	F[7:0]							
0x05	R05	MODE CTRL	D8	LNA2G	RFIN	RFLPF	CHBW	TFB[1:0]		IFSEL[1:0]	
0x06	R06	TFS	30	TFS[7:0]							
0x07	R07	TFP	12	—	—	TFP[5:0]					
0x08	R08	SHUTDOWN	00	STBY	SDRF	SDMIX	SDIF	SDIFVG	SDPD	SDSYN	SDVCO
0x09	R09	REF CONFIG	0A	—	—	—	CPLIN[1:0]		ALC[1:0]		XODIV
0x0A	R0A	VAS CONFIG	17	LFDIV[1:0]		VASS	VAS	ADL	ADE	LTC[1:0]	
0x0B	R0B	PWRDET CFG1	43	DWPD	WPDA[2:0]			DNPD	NPDA[2:0]		
0x0C	R0C	PWRDET CFG2	01	—	—	—	—	—	PULLUP	RFIFD[1:0]	
0x0D	R0D	FILT CF ADJ	ROM	—	—	CFSET[5:0]					
0x0E	R0E	ROM ADDR	00	—	—	—	—	ROMA[3:0]			
0x0F	R0F	IRHR	ROM	IRHR[7:0]							
0x10	R10	ROM READBACK	RO	ROMR[7:0]							
0x11	R11	VAS STATUS	RO	VVCO[1:0]		VVSB[3:0]				VASA	VASE
0x12	R12	GEN STATUS	RO	—	—	VCP	TRIM	POR	VCOADC[2:0]		
0x13	R13	BIAS ADJ	56	—	MIXGM	LNA2B[1:0]		MIXB[1:0]		FILTB	IFVGAB
0x14	R14	TEST1	40	RESERVED							
0x15	R15	ROM WRITE DATA	00	ROMW[7:0]							

Note: *Registers should be written in the order of ascending addresses. When changing frequency, write R00 to R07 in order of ascending addresses to ensure proper VCO setup.*

Register and Bit Descriptions

Table 4. R00: VCO Register—VCO and LO Divider Control (Address: 00h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
VCO[1:0]	7:6	01	VCO select. Selects one of three VCOs when VAS = 0, or selects the VCO starting band when VASS = 0. 00 = Selects VCO1 (approximately 2200MHz to 2800MHz) 01 = Selects VCO2 (approximately 2800MHz to 3500MHz) 10 = Selects VCO3 (approximately 3500MHz to 4400MHz) 11 = VCO shutdown
VSUB[3:0]	5:2	0011	VCO sub-band select. Selects one of 16 possible VCO sub-bands when VAS = 0, or selects the VCO starting sub-band when VASS = 0. 0000 = Selects SB0 … 1111 = Selects SB15
VDIV[1:0]	1:0	00	VCO divider ratio select. 00 = Sets VCO divider to 4 (use when f_{LO} > 550MHz) 01 = Sets VCO divider to 8 (use when 275MHz < f_{LO} < 550MHz) 10 = Sets VCO divider to 16 (use when 137.5MHz < f_{LO} < 275MHz) 11 = Sets VCO divider to 32 (use when f_{LO} < 137.5MHz)

Table 5. R01: NDIV INT Register—Integer Part of N-Divider (Address: 01h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
NINT[7:0]	7:0	0010 1011	Sets the PLL integer divide number (N)

Table 6. R02: NDIV FRAC2 Register—N-Divider Fractional Part [19:16] and R-Divider (Address: 02h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
CPS	7	1	Sets the charge-pump current-selection mode between automatic and manual. Must set to 1 for proper operation.
CP	6	0	For Maxim use only
RDIV[1:0]	5:4	00	Reference divider. 00 = /1 01 = /2 1X = Maxim use only
F[19:16]	3:0	1110	N-divider fractional part bits 19:16 (out of 19:0)

Multiband Digital Television Tuner

Table 7. R03: NDIV FRAC1 Register—N-Divider Fractional Part [15:8] (Address: 03h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
F[15:8]	7:0	0010 0110	N-divider fractional part bits 15:8 (out of 19:0)

Table 8. R04: NDIV FRAC0 Register—N-Divider Fractional Part [7:0] (Address: 04h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
F[7:0]	7:0	0110 0110	N-divider fractional part bits 7:0 (out of 19:0). Writing this register also triggers VCO autoselect (VAS).

Table 9. R05: MODE CTRL Register—Mode Control (Address: 05h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
LNA2G	7	1	Premixer gain configuration. Set to 1 for nominal gain. Set to 0 for approximately 2.5dB reduced gain.
RFIN	6	1	0 = Selects RFINL input (for f_{RF} < 345MHz) 1 = Selects RFINH input (for f_{RF} > 345MHz)
RFLPF	5	0	0 = Disables RF LPF (for f_{RF} > 110MHz) 1 = Enables RF LPF (for f_{RF} < 110MHz)
CHBW	4	1	0 = Sets IF BW to 7MHz mode 1 = Sets IF BW to 8MHz mode
TFB[1:0]	3:2	10	Selects the tracking filter band of operation. 00 = VHFL (for f_{RF} < 196MHz) 01 = VHFH (for 196MHz < f_{RF} < 440MHz 10 = UHF (for f_{RF} > 440MHz) 11 = Unused
IFSEL[1:0]	1:0	00	IF output selection. 00 = IFOUT1 differential mode (for driving a differential bandpass filter) 01 = IFOUT1 single-ended (for driving a switched BW single-ended SAW filter) 10 = Unused 11 = Unused

Table 10. R06: TFS Register—Tracking Filter Series Capacitor (Address: 06h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
TFS[7:0]	7:0	N/A	Programs series capacitor values in the tracking filter. The value is determined from the values in the ROM table applied to an equation executed in the Maxim-provided device driver code.

Table 11. R07: TFP Register—Tracking Filter Parallel Capacitor (Address: 07h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7:6	00	Empty
TFP[5:0]	5:0	N/A	Programs parallel capacitor values in the tracking filter. The value is determined from the values in the ROM table applied to an equation executed in the Maxim-provided device driver code.

Table 12. R08: SHUTDOWN Register—Shutdown Control (Address: 08h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
STBY	7	0	Standby. 1 = All circuits shut down except crystal oscillator and REFOUT
SDRF	6	0	RF shutdown. Must set to 0 for proper operation.
SDMIX	5	0	Mixer shutdown. Must set to 0 for proper operation.
SDIF	4	0	IF shutdown. Must set to 0 for proper operation.
SDIFVG	3	0	IF VGA shutdown. 0 = IF VGA enabled 1 = IF VGA disabled
SDPD	2	0	Power-detector shutdown. Must set to 0 for proper operation.
SDSYN	1	0	Frequency synthesizer shutdown. Must set to 0 for proper operation.
SDVCO	0	0	VCO shutdown. Must set to 0 for proper operation.

Table 13. R09: REF CONFIG Register—Reference Oscillator Configuration (Address: 09h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7:5	000	Empty
CPLIN[1:0]	4:3	01	Must set to 01 for proper operation
ALC[1:0]	2:1	01	Must set to 01 for proper operation
XODIV	0	0	Sets crystal oscillator divider for REFOUT signal when REFDIV pin is unconnected. 0: $f_{REFOUT} = f_{XTAL}/4$ 1: $f_{REFOUT} = f_{XTAL}$

Multiband Digital Television Tuner

Table 14. R0A: VAS CONFIG Register—VCO Autoselect Configuration (Address: 0Ah)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
LFDIV[1:0]	7:6	00	Sets the low-frequency clock-divider. 00 = Use for 16MHz ≤ f_{REF} < 20MHz 01 = Use for 20MHz ≤ f_{REF} < 28MHz 10 = Use for 28MHz ≤ f_{REF} ≤ 32MHz 11 = Unused
VASS	5	0	Controls the VCO autoselect (VAS) start conditions function. 0 = VAS starts from the current VCO/VCOSB loaded in the VCO[1:0] and VSUB[3:0] bits (in R00) 1 = VAS starts from the currently used VCO and VCOSB
VAS	4	1	Controls the VCO autoselect (VAS) function. Must set to 1 for proper operation.
ADL	3	0	Enables or disables the VCO tuning voltage ADC latch when the VCO autoselect (VAS) mode is disabled. 0 = Disables the ADC latch 1 = Latches the ADC value
ADE	2	0	Enables or disables VCO tuning voltage ADC read when the VCO autoselect (VAS) mode is disabled. 0 = Disables ADC read 1 = Enables ADC read
LTC[1:0]	1:0	10	Sets the VCO autoselect wait time. Must set to 10 for proper operation.

Note: *Only production tested and guaranteed functional in states 0001 0010, 0101 0010, and 1001 0010. All other states are untested and may not function correctly. Contact Maxim if untested settings will be used in production.*

Table 15. R0B: PWRDET CFG1 Register—Power-Detector Configuration 1 of 2 (Address: 0Bh)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
DWPD	7	0	Enables or disables wideband power detector. Use this state for autonomous RFAGC. 0 = Enables wideband power detector 1 = Disables wideband power detector
WPDA[2:0]	6:4	100	Sets the wideband power-detector attack point (takeover point). 000 = Min 100 = Nom (see the *Typical Operating Characteristics*) 111 = Max
DNPD	3	0	Enables or disables narrowband power detector. Use this state for autonomous RFAGC. 0 = Enables narrowband detector 1 = Disables narrowband detector
NPDA[2:0]	2:0	011	Sets the narrowband power-detector attack point (takeover point). 000 = Min 011 = Nom (see the *Typical Operating Characteristics*) 111 = Max

Note: *Only production tested and guaranteed functional in state X100 X011, where X can be either 0 or 1. All other states are untested and may not function correctly. Contact Maxim if untested settings will be used in production.*

Table 16. R0C: PWRDET CFG2 Register—Power-Detector Configuration 2 of 2 (Address: 0Ch)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7:3	0000 0	Empty
PULLUP	2	0	Must set to 0 for proper operation
RFIFD[1:0]	1:0	01	RF IF AGC diode voltage. 00 = Approximately 0.6V 01 = Approximately 0.95V 10 = Approximately 1.3V 11 = Off

Table 17. R0D: FILT CF ADJ Register—IF Filter Center Frequency and BW Adjustment (Address: 0Dh)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7:6	00	Empty
CFSET[5:0]	5:0	ROM	Sets the IF filter center frequency and bandwidth. For proper operation, must read value from ROM address A[5:0] and write that value to this register.

Note: *Only production tested and guaranteed functional in factory-trimmed state from ROM table. All other states are untested and may not function correctly. Contact Maxim if untested settings will be used in production.*

Table 18. R0E: ROM ADDR Register—ROM Address (Address: 0Eh)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7:4	00	Empty
ROMA[3:0]	3:0	0000	Address bits of the ROM register to be read or written. Must set to 0000 when not reading the ROM table.

Table 19. R0F: IRHR Register (Address: 0Fh)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
IRHR[7:0]	7:0	ROM	For proper operation, must read value from ROM address B[7:0] and write that value to this register.

Note: *Only production tested and guaranteed functional in factory-trimmed state from ROM table. All other states are untested and may not function correctly.*

Table 20. R10: ROM READBACK Register—ROM Readback (Address: 10h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
ROMR[7:0]	7:0	N/A	Data bits read from the ROM table address as specified by R0E[3:0]

Multiband Digital Television Tuner

Table 21. R11: VAS STATUS Register—VCO Autoselect Status (Address: 11h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
VVCO[1:0]	7:6	N/A	Indicates which VCO has been selected by either the autoselect state machine or by manual selection when the VSA state machine is disabled. See the R00 description for the VCO[1:0] definition.
VVSB[3:0]	5:2	N/A	Indicates which sub-band of a particular VCO has been selected by either the autoselect state machine or by manual selection when the VSA state machine is disabled. See the R00 description for the VSUB[3:0] definition.
VASA	1	N/A	Indicates whether VCO autoselection was successful. 0 = Indicates the autoselect function is disabled or unsuccessful VCO selection 1 = Indicates successful VCO autoselection
VASE	0	N/A	Status indicator for the autoselect function. 0 = Indicates the autoselect function is active 1 = Indicates the autoselect process is inactive

Note: *Not production tested or guaranteed functional.*

Table 22. R12: GEN STATUS Register—General Status (Address: 12h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7:6	N/A	Empty
VCP	5	N/A	Maxim use only
TRIM	4	N/A	Maxim use only
POR	3	N/A	Maxim use only
VCOADC [2:0]	2:0	N/A	VCO tuning voltage indicators. 000 = PLL not in lock, tune to the next lowest sub-band 001 to 110 = PLL in lock 111 = PLL not in lock, tune to the next higher sub-band

Note: *Not production tested or guaranteed functional.*

Table 23. R13: BIAS ADJ Register—Bias Adjustments (Address: 13h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
EMPTY	7	0	Empty
MIXGM	6	1	Mixer gain setting. Set to 1 for nominal gain. Set to 0 for approximately 2dB reduced gain.
LNA2B[1:0]	5:4	01	LNA bias. 00 = Unused 01 = Nominal setting 10 = Unused 11 = Highest linearity setting

Table 23. R13: BIAS ADJ Register—Bias Adjustments (Address: 13h) (continued)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
MIXB[1:0]	3:2	01	Mixer bias. 00 = Unused 01 = Nominal setting 10 = Unused 11 = Highest linearity setting
FILTB	1	1	Must set to 1 for proper operation
IFVGAB	0	0	IF VGA bias. 0 = Default 1 = Highest current (approximately nominal + 6mA)

Note: *Only production tested and guaranteed functional in state 0XX1 X11X, where X can be either 1 or 0. All other states are untested and may not function correctly. Contact Maxim if untested settings will be used in production.*

Table 24. R14: TEST1 Register (Address: 14h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
RESERVED	7:0	0100 0000	Must set to 0100 0000 for proper operation

Note: *This register is not available to the end user.*

Table 25. R15: ROM WRITE DATA Register (Address: 15h)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTING	FUNCTION
ROMW[7:0]	7:0	N/A	Maxim use only

Note: *This register is not available to the end user.*

Applications Information

RF Inputs and Filters

The MAX3544 features separate low- and high-frequency inputs. These two inputs are combined to a single input by an off-chip diplexer circuit as shown in the *Typical Application Circuit*. When the desired channel is less than 345MHz, use RFINL. When the desired input is greater than 345MHz, use RFINH. Further, when the desired input is less than 110MHz, an internal lowpass filter should be enabled to limit high-frequency interference incident at the mixer input. The lowpass filter is enabled by the RFLPF bit in R05[5].

Besides selecting the appropriate input port and setting RFLPF appropriately, one of three tracking filters must be chosen based on the desired frequency. Set TFB (R05[3:2]) to select VHFL, VHFH, or UHF tracking filter bands. Use VHFL when the desired frequency is less than 196MHz, use VHFH when the desired frequency is between 196MHz and 440MHz, or use UHF when the desired frequency is greater than 440MHz.

RF Gain Control

The MAX3544 is designed to control its own RF gain based on internally measured signal and blocker levels. The user can adjust the AGC attack points (takeover points) by setting WDPA and NDPA in register R0B. Alternatively, the user can control the RF gain by driving the RFVGC input pin.

Multiband Digital Television Tuner

Table 26. ROM Table

DESCRIPTION	ADDR	MSB			DATA BYTE				LSB
BIAS	0x0	Unused			BIAS[3:0]				
VHF-Low Tracking Filter. VLS0, VLS1, VLP0, VLP1	0x1	VLS0[5]	VLS0[4]	VLS0[3]	VLS0[2]	VLS0[1]	VLS0[0]	VLS1[5]	VLS1[4]
	0x2	VLS1[3]	VLS1[2]	VLS1[1]	VLS1[0]	VLP0[5]	VLP0[4]	VLP0[3]	VLP0[2]
	0x3	VLP0[1]	VLP0[0]	VLP1[5]	VLP1[4]	VLP1[3]	VLP1[2]	VLP1[1]	VLP1[0]
VHF-High Tracking Filter. VHS0, VHS1, VHP0, VHP1	0x4	VHS0[5]	VHS0[4]	VHS0[3]	VHS0[2]	VHS0[1]	VHS0[0]	VHS1[5]	VHS1[4]
	0x5	VHS1[3]	VHS1[2]	VHS1[1]	VHS1[0]	VHP0[5]	VHP0[4]	VHP0[3]	VHP0[2]
	0x6	VHP0[1]	VHP0[0]	VHP1[5]	VHP1[4]	VHP1[3]	VHP1[2]	VHP1[1]	VHP1[0]
UHF Tracking Filter. US0, US1, UP0, UP1	0x7	US0[5]	US0[4]	US0[3]	US0[2]	US0[1]	US0[0]	US1[5]	US1[4]
	0x8	US1[3]	US1[2]	US1[1]	US1[0]	UP0[5]	UP0[4]	UP0[3]	UP0[2]
	0x9	UP0[1]	UP0[0]	UP1[5]	UP1[4]	UP1[3]	UP1[2]	UP1[1]	UP1[0]
IF Filter	0xA	Unused	Unused	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]
IRHR	0xB	IRHR[7]	IRHR[6]	IRHR[5]	IRHR[4]	IRHR[3]	IRHR[2]	IRHR[1]	IRHR[0]
Reserved	0xC	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

VCO and VCO Divider Selection

The MAX3544 frequency synthesizer includes three VCOs with 16 sub-bands for each VCO. These VCOs and sub-bands are selected to best center the VCO near the operating frequency. This selection process is performed automatically by the VAS circuitry. The Maxim driver software seeds the VCO starting band for fastest selection time.

In addition to VCO selection, a VCO divider value of 32, 16, 8, or 4 must be selected to provide the desired mixer LO drive frequency. The divider is selected by VDIV in register R00[1:0].

Reading the ROM Table

The MAX3544 includes 13 ROM registers to store factory calibration data (see Table 26). Each ROM table entry must be read using a two-step process. First, the address of the ROM bits to be read must be programmed into the ROM ADDR register (R0E[3:0]).

Once the address has been programmed, the data stored in that address is automatically transferred to the ROM READBACK register (R10[7:0]). The ROM data at the specified address can then be read from the ROM READBACK register and stored in the microprocessor's local memory. After all ROM registers have been read and stored in the microprocessor's local memory, ROM ADDR must be programmed to 00 for proper operation.

Setting RF Tracking Filter Codes

The MAX3544 includes a programmable tracking filter for each band of operation to optimize rejection of out-of-band interference while minimizing insertion loss for the desired received signal. The center frequency of each tracking filter is selected by a switched-capacitor array that is programmed by the TFS[7:0] bits in the R06 register and the TFP[5:0] bits in the R07 register.

Optimal tracking filter settings for each channel vary from part to part due to process variations. To accommodate part-to-part variations, each part is factory calibrated by Maxim. During calibration the correction factors for the series and parallel tracking capacitor arrays are calculated and written into an internal ROM table. The user must read the ROM table upon power-up and store the data in local memory (8 bytes total) to calculate the optimal TFS and TFP settings for each channel. The equation for setting TFS and TFP at each channel is available in the device driver code provided by Maxim. Table 26 shows the address and bits for each ROM table entry.

Layout Recommendations

IMPORTANT: The MAX3544 includes on-chip tracking filters that utilize external inductors placed on the PCB at pins 30 through 37. Because the tracking filters operate at frequencies up to 862MHz, they are sensitive to the inductor and PCB trace parasitics. To achieve the optimal RF performance (gain, noise figure, and image rejection), the MAX3544 is production tested and trimmed with the exact inductors, their relative location and orientation, and the trace parasitics present on the MAX3544 Reference Design. To avoid performance degradation, PCB designs should exactly copy the RF section of the Reference Design layout and use the inductors specified in the Reference Design bill of materials. Contact Maxim to obtain the Reference Design layout to use as a starting point for PCB designs.

In addition to the aforementioned requirements, follow general good RF layout practices. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. The exposed paddle must be soldered evenly to the board's ground plane for proper operation. Use abundant vias beneath the exposed paddle and maximize the area of continuous ground plane around the paddle on the bottom layer for maximum heat dissipation. Use abundant ground vias between RF traces to minimize undesired coupling.

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at the central V_{CC} node. The V_{CC} traces branch out from this node, with each trace going to separate V_{CC} pins of the MAX3544. Each V_{CC} pin must have a bypass capacitor with a low impedance to ground at the frequency of interest. Do not share ground vias among multiple connections to the PCB ground plane.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4066+2	21-0141	90-0053

Multiband Digital Television Tuner

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—