

M21260

4x4 Crosspoint Switch with Integrated CDR/Reclockers

The M21260 is a high-performance 4x4 crosspoint switch with an integrated independent multi-rate quad channel CDR/reclocker array, optimized for telecom, datacom, and digital video applications. Each channel has an independent multi-rate reclocker capable of operating at data-rates between 42 Mbps and 3.2 Gbps. Signal conditioning features include input equalization and output pre-emphasis, allowing robust reception and transmission of signals to other devices up to 60" away. The built-in frequency synthesizer allows multi-rate operation, while operating from a single reference clock.

The device can be controlled either through hardwired pins or a 2-wire or 4-wire serial programming interface. The hardwired mode eliminates the need for an external micro-controller, while allowing control of the key features of the device. The serial programming interface is available as a two wire or four wire and allows complete control of the device features.

The M21260 supports JTAG external boundary scan, which includes all of the high-speed I/O as well as the traditional digital I/O.

Features

- 4x4 Crosspoint Switch with four independent Reclockers (RCLKs) SMPTE, DVB-ASI compliant
- Integrated loop filter and terminations
- Serial control or hardwired control, JTAG boundary scan
- Low power consumption of 405 mW (1 channel active)
- Built-in pattern generator and receiver for module and system testing (PRBS, 8b/10b, Fibre Channel, User Programmable patterns)
- Broadcast and Multicast crosspoint modes
- User Selectable Input Equalization and Pre-Emphasis for backplane ISI reduction

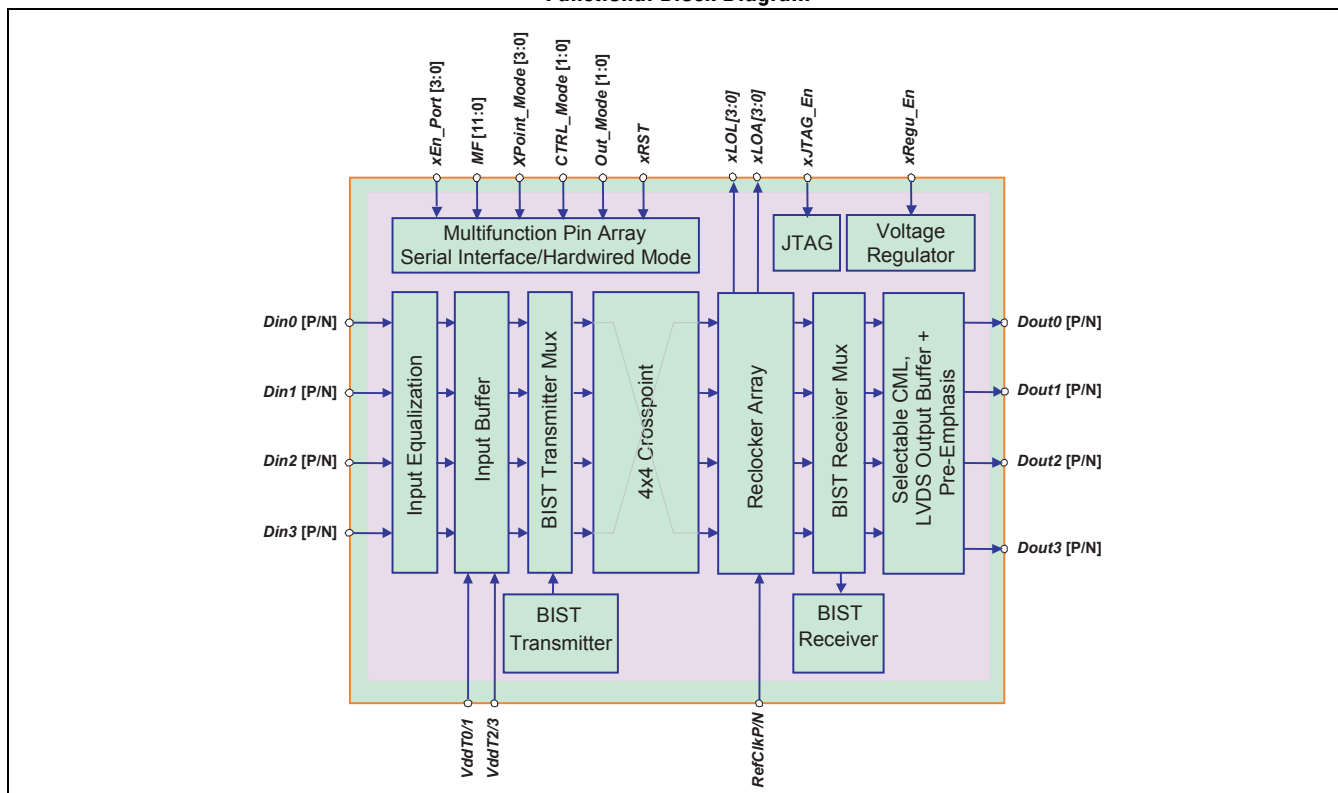
Applications

- 3G/HD/SD-SDI Routing Switchers, Distribution amplifiers, and transport systems¹
- SONET systems and modules
- 10 GBASE-CX4 systems
- Gigabit Ethernet systems
- PCI-Express
- SAS/S-ATA/S-ATA2 systems

Standards Compliance

- SMPTE 292M
- SMPTE 259M
- SMPTE 344M
- SMPTE 424M

Functional Block Diagram



Ordering Information

Part Number	Number of Channels	Package	Operating Temperature
M21260-12	4	72-terminal, 10 mm, QFN	-40°C to +85°C
M21260G-12*	4	72-terminal, 10 mm, QFN, RoHS compliant package	-40°C to +85°C

* The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information. The RoHS compliant devices are backwards compatible with 225°C reflow profiles.

Not Recommended for New Designs

Revision History

Revision	Date	Description
H	December 2010	- Removed video support in hardware mode (Table 3-5 and Table 3-6). - Update table reference in Section 3.2.18. - Updated LOS Section 3.2.20 and added Figure 3-12. - J_{TRF} replaced with J_{TRAN} - t_{PLL} replaced with t_{LOCK} - t_{PD, CLOCK} replaced with t_{SKEW, CLK-DATA} - DCD replaced with DCD_{DATA} - DR and DR replaced with DR - idd_core replaced with DI_{DCCORE} - idd_io replaced with DI_{DDIO} - V_{ID} replaced with V_{IN} - CV_{OD} replaced with V_{OD} - N_{NARROW} replaced with N_{NARROW} - N_{WIDE} replaced with N_{WIDE} - Added register M8h, CDR#N LOA Window Control (trim) (Section 2.2.8).
G	March 2009	- Added 3G support. - Revised xCS timing in Figure 3-6 and Figure 3-7. - Added SD HD, and 3G parameters to Table 3-13 and Pin 24 default in Table 3-21. - Added Note 4 in Table 1-2. - Revised Bit 5 description in Table 2-35. - Added 820Ω resistor in Figure 3-4.
F	May 2008	- Added SMPTE 424M in standards compliance list. - Revised Section 1.8. - Added 3G-SDI data in Table 1-6, and Table 1-14. - Updated Section 2.0.
E	January 2007	- Added support for Telecom and Datacom applications. - Updated specification tables. - Reformatted register tables.
D	October 2005	- Changed temperature range as follows: from “–40°C to 85°C” to “0°C to 70°C.” - Removed reference to LVPECL output mode. Inputs can be AC-coupled to LVPECL signals. - Changed ESD rating for high speed pins to 350V with HBM testing. - Removed references to FDA operation. FDA is not supported with this device.
C	February 2005	Modified ARD description, added misc. figures, tables, updated device description as necessary.
B	May 2004	Changed ordering information from M21260-11P to M21260-12P.
A	March 2004	Initial release.

Not Recommended for New Designs



Table of Contents

Ordering Information	2
Revision History	3
Table of Contents	4
List of Figures	6
List of Tables	7
1.0 Product Specifications	10
1.1 Absolute Maximum Ratings	10
1.2 Recommended Operating Conditions	11
1.3 Power Dissipation	11
1.4 Input/Output Specifications	12
1.5 High-Speed Performance Specifications	17
1.6 Package Drawings and Surface Mount Assembly Details	22
1.7 PCB High-Speed Design and Layout Guidelines	28
1.8 Auto Rate Detect (ARD)	30
2.0 Registers	31
2.1 Global Control Registers	32
2.1.1 Global Control	32
2.1.2 Crosspoint Switch-State Setting	33
2.1.3 04h: External Reference Frequency Divider Control (RFD)	33
2.1.4 Master IC Reset	34
2.1.5 IC Electronic Identification	34
2.1.6 IC Revision Code	34
2.1.7 Built In Self-Test (BIST) Receiver Channel Select	34
2.1.8 Built In Self-Test (BIST) Receiver Main Control Register	35
2.1.9 Built In Self-Test (BIST) Receiver Bit Error Counter	35
2.1.10 Built In Self-Test (BIST) Transmitter Channel Select	36
2.1.11 Built In Self-Test (BIST) Transmitter Main Control Register	37
2.1.12 Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register	38
2.1.13 Built In Self-Test (BIST) Transmitter PLL Control Register A	39
2.1.14 Built In Self-Test (BIST) Transmitter PLL Control Register B	40
2.1.15 Built In Self-Test (BIST) Transmitter PLL Control Register C	40
2.1.16 Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern	41
2.1.17 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern	41
2.1.18 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern	41
2.1.19 Built In Self-Test (BIST) Transmitter Alarm	42

2.1.20	Internal Junction Temperature Monitor	42
2.1.21	Internal Junction Temperature Value	43
2.1.22	CDR/RCLK Loss of Lock Register Alarm Status	43
2.1.23	CDR/RCLK Loss of Activity Register Alarm Status	44
2.1.24	32h:VCO Trim Alarm Window	44
2.2	Individual Channel/CDR/RCLK Control	45
2.2.1	M0h:CDR N Control Register A	45
2.2.2	M1h:CDR/RCLK N Control Register B	46
2.2.3	CDR/RCLK N Control Register C	46
2.2.4	Output Buffer Control for CDR/RCLK N	47
2.2.5	Output Buffer Pre-Emphasis Control for Output N	48
2.2.6	Input Equalization Control for Output N	48
2.2.7	CDR/RCLK N Loop Bandwidth and Data Sampling Point Adjust.	49
2.2.8	CDR#N LOA Window Control (trim)	50
2.2.9	CDR/RCLK N LOL Window Control	51
2.2.10	MAh: Jitter Reduction Control	53
3.0	Functional Description	54
3.1	Applications	54
3.2	Detailed Feature Descriptions	57
3.2.1	Conventions	57
3.2.2	Reset	57
3.2.3	Internal Voltage Regulator	57
3.2.4	High-Speed Input/Output Pins	57
3.2.5	Switch-State Settings	58
3.2.6	CDR/Reclocker Reference Frequency	59
3.2.7	Multifunction Pins Overview	59
3.2.8	Multifunction Pins Defined for Hardwired Mode	60
3.2.9	Multi-function Pins: Four-Wire Serial Interface	61
3.2.10	Two-Wire Serial Interface	64
3.2.11	JTAG	64
3.2.12	Input Deterministic Jitter Attenuators	64
3.2.13	Output Pre-Emphasis	66
3.2.14	CDR/RCLK Overview	67
3.2.15	General CDR/RCLK Features	68
3.2.16	Multi-Rate CDR Data-Rate Selection	68
3.2.17	Frequency Acquisition	69
3.2.18	CDR/Reclocker Data Rate Programming (3G/HD/SD-SDI data rates only)	72
3.2.19	Ambient Temperature Range Limitations	73
3.2.20	Loss of Activity	73
3.2.21	Built-In Self Test (BIST) Overview	74
3.2.22	BIST Test Patterns	74
3.2.23	BIST Receiver (BIST Rx) Operation	75
3.2.24	BIST Transmitter (BIST Tx) Operation	75
3.2.25	Junction Temperature Monitor	76
3.2.26	IC Identification / Revision Code	76
3.3	Pin Definitions	77

Appendix 80

 A.1 Glossary of Terms/Acronyms80

 A.2 Reference Documents80

 A.2.1 External80

 A.2.2 Mindspeed81



List of Figures

Figure 1-1.	Data Input Internal Circuitry	13
Figure 1-2.	Definitions of Eye Parameters.	15
Figure 1-3.	Reference Clock Input Internal Circuitry	17
Figure 1-4.	SMPTE Jitter Tolerance Specification Mask	20
Figure 1-5.	SONET Jitter Tolerance Specification Mask	20
Figure 1-6.	SONET/SMPTE Jitter Transfer Specification Mask	21
Figure 1-7.	Cross-Section of QFN Package	22
Figure 1-8.	Package Drawing (1 of 2)	23
Figure 1-9.	Package Drawing (2 of 2)	24
Figure 1-10.	72-Pin Package Dimensions	25
Figure 1-11.	PCB Footprint for 72-Pin 10 mm QFN Package.	26
Figure 1-12.	PCB Pad Extensions	27
Figure 1-13.	Recommended Via Array for Thermal Pad	27
Figure 1-14.	Trace-Length Matching Using Serpentine Pattern	29
Figure 1-15.	Loop Length Matching for Differential Traces.	29
Figure 3-1.	M21260 Application - Small Routing Switcher	54
Figure 3-2.	Module Application.	55
Figure 3-3.	Backplane Application.	55
Figure 3-4.	Recommended Data and Reference Clock Input Coupling Circuitry	56
Figure 3-5.	Serial Word Format.	62
Figure 3-6.	Serial WRITE Mode.	62
Figure 3-7.	Serial READ Mode	63
Figure 3-8.	STS-48 waveform after transmission through 76" of PCB traces (input to M21260)	65
Figure 3-9.	STS-48 waveform at M21260 output with input shown in Figure 3-7.	66
Figure 3-10.	Definition of Pre-Emphasis Levels	67
Figure 3-11.	Block Diagram of Frequency Acquisition Circuits	70
Figure 3-12.		74
Figure 3-13.	M21260 Pinout Diagram (Top View)	79



List of Tables

Table 1-1.	Absolute Maximum Ratings	10
Table 1-2.	Recommended Operating Conditions	11
Table 1-3.	DC Power Electrical Specifications	11
Table 1-4.	Serial Interface (2-wire and 4-wire) CMOS I/O Electrical Specifications	12
Table 1-5.	Input Electrical Specifications	13
Table 1-6.	PCML (Positive Current Mode Logic) Output Electrical Specifications	14
Table 1-7.	LVDS (Low Voltage Differential Signal) Output Electrical Specifications.	14
Table 1-8.	Input Equalization Performance Specifications	15
Table 1-9.	Output Pre-Emphasis Performance Specifications	16
Table 1-10.	Reference Clock Input.	16
Table 1-11.	Crosspoint Switching Performance	17
Table 1-12.	CDR/RCLK High-Speed Performance	18
Table 1-13.	RCLK Alarm Performance.	19
Table 1-14.	SMPTE Jitter Tolerance Mask.	20
Table 1-15.	Loop Bandwidths for Typical Video Data Rates	21
Table 2-1.	Register Table Summary	31
Table 2-2.	Global Control (Globctrl: Address 00h).	32
Table 2-3.	Crosspoint Switch-State Setting (XPoint_ctrl: Address 01h)	33
Table 2-4.	External Reference Frequency Divider Control (RFD) (Refclk_ctrl: Address 04h)	33
Table 2-5.	Master IC Reset (Mastreset: Address 05h)	34
Table 2-6.	IC Electronic ID (Chipcode: Address 06h).	34
Table 2-7.	IC Revision Code (Revcode: Address 07h)	34
Table 2-8.	Built In Self-Test (BIST) Receiver Channel Select (BISTrx_chsel: Address 10h).	34
Table 2-9.	Built In Self-Test (BIST) Receiver Main Control Register (BISTrx_ctrl: Address 11h).	35
Table 2-10.	Built In Self-Test (BIST) Receiver Bit Error Counter (BISTrx_error: Address 12h)	35
Table 2-11.	Built In Self-Test (BIST) Transmitter Channel Select (BISTtx_chsel: Address 14h)	36
Table 2-12.	Built In Self-Test (BIST) Transmitter Main Control Register (BISTtx_ctrl: Address 15h)	37
Table 2-13.	Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (BISTtx_LOLctrl: Address 17h).	38
Table 2-14.	Built In Self-Test (BIST) Transmitter PLL Control Register A (BISTtx_PLL_ctrlA: Address 18h)	39
Table 2-15.	Built In Self-Test (BIST) Transmitter PLL Control Register B (BISTtx_PLL_ctrlB: Address 19h)	40
Table 2-16.	Built In Self-Test (BIST) Transmitter PLL Control Register C (BISTtx_PLL_ctrlC: Address 1Ah)	40
Table 2-17.	Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern (BIST_pattern0: Address 1Bh)41	

Table 2-18.	Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern (BIST_pattern1: Address 1Ch)41	
Table 2-19.	Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern (BIST_pattern2: Address 1Dh)41	
Table 2-20.	Built In Self-Test (BIST) Transmitter Alarm (BISTtx_alarm: Address 1Fh)	42
Table 2-21.	Internal Junction Temperature Monitor (Temp_mon: Address 20h)	42
Table 2-22.	Internal Junction Temperature Value (Temp_value: Address 21h)	43
Table 2-23.	CDR/RCLK Loss of Lock Register Alarm Status (Alarm_LOL: Address 30h)	43
Table 2-24.	CDR/RCLK Loss of Activity Register Alarm Status (Alarm_LOA: Address 31h)	44
Table 2-25.	VCO Trim Alarm Window Trim (Alarm_trim: Address 32h)	44
Table 2-26.	CDR N Control Register A (RCLK_ctrlA_N: Address M0h)	45
Table 2-27.	CDR N Control Register B (RCLK_ctrlB_N: Address M1h)	46
Table 2-28.	CDR/RCLK N Control Register C (RCLK_ctrlC_N: Address M2h)	46
Table 2-29.	Output Buffer Control for CDR/RCLK N (Out_ctrl_N: Address M3h)	47
Table 2-30.	Output Buffer Pre-Emphasis Control for Output N (Preemp_ctrl_N: Address M4h)	48
Table 2-31.	Input Equalization Control for Output N (Ineq_ctrl_N: Address M5h)	48
Table 2-32.	CDR/RCLK N Loop Bandwidth and Data Sampling Point Adjust (Phadj_ctrl_N: Address M6h)	49
Table 2-33.	CDR#N LOA Window Control (trim) (LOA_ctrl_N: Address M8h)	50
Table 2-34.	CDR/RCLK N LOL Window Control (LOL_ctrl_N: Address M9h)	51
Table 2-35.	Jitter Reduction Control (Jitter_reduc_N: Address MAh)	53
Table 3-1.	Output Interface and Level Mapping (For both hardwired and software modes)	58
Table 3-2.	Output Interface and Recommended AVDDIO Range	58
Table 3-3.	Crosspoint Switch-State in Hardwired Mode	59
Table 3-4.	Mode Select Pins	60
Table 3-5.	Multifunction Pins for Hardwired Mode	60
Table 3-6.	Hardwired Data-Rates and Associated Reference Clock Frequencies	61
Table 3-7.	Multi-function Pins for Four-Wire Interface	61
Table 3-8.	Serial Interface Timing – Specified at Recommended Operating Conditions	63
Table 3-9.	Multifunction Pins for Two-Wire Interface	64
Table 3-10.	Multifunction Pins for JTAG	64
Table 3-11.	Valid Input Data Ranges	69
Table 3-12.	Reference Clock Frequency Ranges	70
Table 3-13.	DRD/RFD/VCD Settings for Different Data-Rates and Reference Frequencies.	71
Table 3-14.	LOL Window Size and Decision Time Examples	72
Table 3-15.	Supported Ambient Temperature Range by Data-Rate	73
Table 3-16.	BIST PRBS Patterns	75
Table 3-17.	BIST 8b/10b Patterns	75
Table 3-18.	Junction Temperature Monitor	76
Table 3-19.	Power Pins	77
Table 3-20.	High-Speed Signal Pins	77

Table 3-21. Control, Interface, and Alarm Pins78

Table A-1. Acronyms80



1.0 Product Specifications

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the device can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DV _{DDIO}	Digital I/O power	—	0	1.8/2.5/3.3	3.6	V
AV _{DDIO}	Analog I/O power	—	0	1.8/2.5/3.3	3.6	V
AV _{DDCORE}	Analog core power	2	0	1.2	1.5	V
DV _{DDCORE}	Digital core power	2	0	1.2	1.5	V
—	High-speed signal pins	1, 4	V _{SS} - 0.5	—	AV _{DD} - I/O + 0.5	
—	Control, interface, and alarm pins	1, 5	V _{SS} - 0.5	—	AV _{DD} - I/O + 0.5	
T _{STORE}	Storage temperature	—	-65	—	+150	°C
V _{ESD, HBM}	Human body model (low-speed)	—	2000	—	—	V
V _{ESD, HBM}	Human body model (high-speed)	—	350	—	—	V
V _{ESD, CDM}	Charged device model	—	100	—	—	V
—	Maximum DC input current	1, 3	—	—	25	mA

NOTES:

1. No damage under these conditions.
2. Apply voltage to core pin if internal regulator is disabled. If enabled, pins should be floating with by-pass to V_{SS}.
3. Computed as the current through 50Ω from the voltage difference between the input voltage common mode and V_{DDT}.
4. High-speed signal pins are shown in [Table 3-16](#).
5. Control, interface, and alarm pins are shown in [Table 3-17](#).

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DV _{DDIO}	Digital I/O power	2	—	1.8/2.5/3.3	—	V
AV _{DDIO}	Analog I/O power	2	—	1.8/2.5/3.3	—	V
AV _{DDCORE}	Analog core power	1, 2	—	1.2	—	V
DV _{DDCORE}	Digital core power	1, 2	—	1.2	—	V
T _{AMB}	Ambient temperature	4	-40	—	85	°C
θ _{JA}	Junction to ambient thermal resistance	3	—	24	—	°C/W

NOTES:

1. Needed only if **AV_{DDCORE}** or **DV_{DDCORE}** are provided from external source (internal regulator disabled **xRegu_En** = H).
2. Typical value +/- 5% is acceptable.
3. With forced convection of 1 m/s and 2.5 m/s, θ_{JA} is decreased to 18°C/W and 16°C/W respectively.
4. See [Section 3.2.19, “Ambient Temperature Range Limitations,” on page 73.](#)

1.3 Power Dissipation

Table 1-3. DC Power Electrical Specifications (1 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
I _{DD}	Case 1: current consumption for output swing = 550 mV CML, internal regulator = on	1	—	310	365	mA
P _{TOTAL}	Power dissipation at 1.8V	—	—	560	660	mW
P _{TOTAL}	Power dissipation at 3.3V	2	—	1.02	1.2	W
I _{DD}	Case 2: current consumption for output swing = 900 mV CML, internal regulator = on	1	—	340	400	mA
P _{TOTAL}	Power dissipation at 1.8V	—	—	610	720	mW
P _{TOTAL}	Power dissipation at 3.3V	2	—	1.12	1.32	W
	Case 3: output swing = 550 mV CML, internal regulator = off	1				
DI _{DDCORE}	Core current consumption	—	—	260	300	mA
DI _{DDIO}	Input/Output buffers current consumption	—		50	70	mA
P _{TOTAL}	Power dissipation at 1.2V core, 1.8V I/O	—	—	400	490	mW
P _{TOTAL}	Power dissipation at 1.2V core, 3.3V I/O	—	—	480	590	mW
I _{DD}	Case 4: current consumption for output swing = 450 mV LVDS, internal regulator = on	1	—	320	380	mA
P _{TOTAL}	Power dissipation at 1.8V	—	—	580	680	mW
P _{TOTAL}	Power dissipation at 3.3V	2	—	1.06	1.25	W

Table 1-3. DC Power Electrical Specifications (2 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
I_{DD}	Case 5: current consumption for output swing = 1.5V PCML+, internal regulator = on	1	—	410	470	mA
P_{TOTAL}	Power dissipation at 1.8V	—	—	740	850	mW
P_{TOTAL}	Power dissipation at 3.3V	2	—	1.35	1.55	W
NOTES: 1. Specified at recommended operating conditions – see Table 1-2 . 2. Thermal design such as thermal pad vias on PCB must be considered for this case.						

1.4 Input/Output Specifications

Table 1-4. Serial Interface (2-wire and 4-wire) CMOS I/O Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output logic high $I_{OH} = -3$ mA	2	$0.8 \times DV_{DDIO}$	DV_{DDIO}	—	V
V_{OL}	Output logic low $I_{OL} = 24$ mA	2	—	0.0	$0.2 \times DV_{DDIO}$	V
I_{OH}	Output current (logic high)	—	-10	—	0	mA
I_{OL}	Output current (logic low)	—	0	—	10	mA
V_{IH}	Input logic high	—	$0.75 \times DV_{DDIO}$	—	$DV_{DDIO} + 0.3$	V
V_{IL}	Input logic low	—	0	—	$0.25 \times DV_{DDIO}$	V
I_{IH}	Input current (logic high)	—	-100	—	100	μA
I_{IL}	Input current (logic low)	—	-100	—	100	μA
t_R	Output rise time (20-80%)	—	—	—	250	ns
t_F	Output fall time (20-80%)	—	—	—	250	ns
C2wire	Input capacitance of MF10 and MF11 in 2-wire serial interface mode.	3	—	—	10	pF
NOTES: 1. Entire table specified at recommended operating conditions – see Table 1-2 . 2. DV_{DDIO} can be chosen independently from AV_{DDIO} . 3. 2-wire serial output mode can drive 500 pF.						

Table 1-5. Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input signal data-rate	—	42	—	3200	Mbps
V_{IN}	Input differential voltage (P-P)	2, 3	100	—	2000	mV
V_{ICM}	Input common-mode voltage	—	700	—	1200	mV
V_{IH}	Maximum input high voltage	—	—	—	$AV_{DDCORE} + 400$	mV
V_{IL}	Minimum input low voltage	—	400	—	—	mV
R_{IN}	Input termination to V_{ddT}	4	45	50	65	Ω
S_{11}	Input return loss (40 MHz to 2.5 GHz)	—	—	-15.0	—	dB

NOTES:

- Entire table specified at recommended operating conditions – see [Table 1-2](#).
- Example 1200 mV_{PP} differential = 600 mV_{PP} for each single-ended terminal.
- Minimum input level defined as error free operation at 10^{-12} BER.
- See [Figure 1-1](#) for input termination circuit.

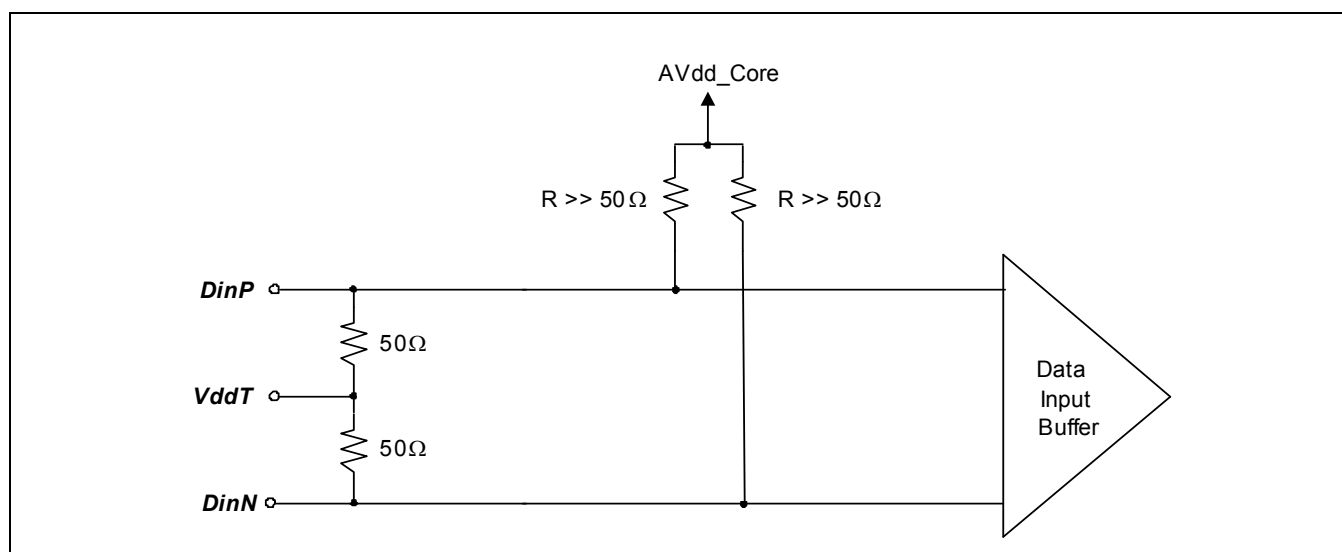
Figure 1-1. Data Input Internal Circuitry

Table 1-6. PCML (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Output signal data-rate (Reclockers enabled)	—	42	—	3200	Mbps
t_R/t_F	Rise/Fall time (20-80%) for all levels	—	—	75	130	ps
V_{OH}	Low swing: output logic high (single-ended)	—	$AV_{DDIO} - 25$	—	AV_{DDIO}	mV
V_{OL}	Low swing: output logic low (single-ended)	—	$AV_{DDIO} - 370$	—	$AV_{DDIO} - 250$	mV
V_{OD}	Low swing: differential swing	2	400	550	750	mV
V_{OH}	Medium swing: output logic high (single-ended)	—	$AV_{DDIO} - 80$	—	AV_{DDIO}	mV
V_{OL}	Medium swing: output logic low (single-ended)	—	$AV_{DDIO} - 600$	—	$AV_{DDIO} - 420$	mV
V_{OD}	Medium swing: differential swing	2	700	900	1150	mV
V_{OH}	High swing: output logic high (single-ended)	—	$AV_{DDIO} - 95$	—	AV_{DDIO}	mV
V_{OL}	High swing: output logic low (single-ended)	—	$AV_{DDIO} - 770$	—	$AV_{DDIO} - 535$	mV
V_{OD}	High swing: differential swing	2	900	1200	1500	mV
V_{OH}	PCML+ swing: output logic high (single-ended)	—	$AV_{DDIO} - 115$	—	AV_{DDIO}	mV
V_{OL}	PCML+ swing: output logic low (single-ended)	—	$AV_{DDIO} - 1000$	—	$AV_{DDIO} - 680$	mV
V_{OD}	PCML+ swing: differential swing	2	1150	1500	1900	mV
R_{OUT}	Output termination to AV_{DDCORE}	—	45	50	65	Ω
S_{22}	Output return loss (40 MHz to 2.5 GHz)	—	—	-15.0	—	dB

NOTES:

1. Specified at recommended operating conditions – see [Table 1-2](#).
2. Example 1200 mV_{P-P} differential = 600 mV_{P-P} for each single-ended terminal.
3. All output swings defined with pre-emphasis off.

Table 1-7. LVDS (Low Voltage Differential Signal) Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Output Signal Data Rate (reclockers enabled)	—	42	—	3200	Mbps
V_{OCM}	Output average common mode range	2	—	1200	—	mV
t_R/t_F	GPL: rise/fall time (20-80%)	—	—	75	130	ps
V_{OD}	GPL: differential output (P-P)	3	500	650	800	mV
V_{OD}	RRL: differential output (P-P)	—	300	450	550	mV
R_{OUT}	Output termination (differential)	—	90	100	130	Ω
S_{22}	Output return loss (40 MHz to 2.5 GHz)	—	—	-15.0	—	dB

NOTES:

1. Specified at recommended operating conditions - see [Table 1-2](#).
2. Computed as average (average positive output and average negative output).
3. Conforms to IEEE Std 1596.3-1996 for GPL. All values specified for 50 Ω single-ended back-match, 100 Ω differential load.
4. All output swings defined with pre-emphasis off.
5. See [Figure 1-2](#) for definitions of eye parameters.

Figure 1-2. Definitions of Eye Parameters

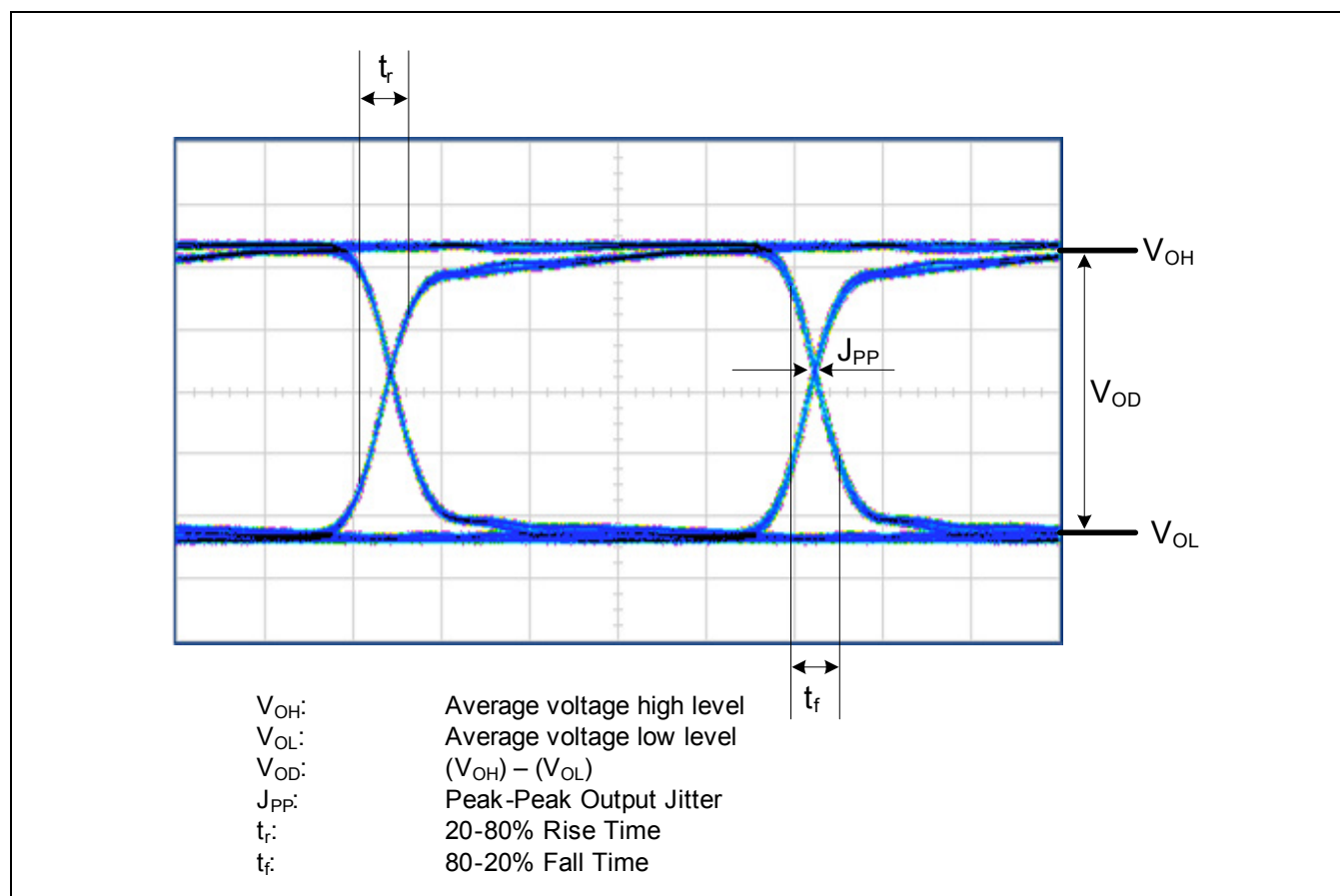


Table 1-8. Input Equalization Performance Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input signal data-rate	—	42	—	3200	Mbps
—	Maximum error-free distance at 3.2 Gbps	2, 3, 6, 7	—	—	60	in
—	Maximum error-free distance at 1.6 Gbps	2, 3, 6, 7	—	—	72	in

NOTES:

- Specified at recommended operating conditions – see Table 1-2.
- Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
- Measured with PCML driver without output pre-emphasis at a minimum launch voltage of 900 mV_{PP} output swing at beginning of line.
- Combined input equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
- Input equalization has greatest effect for data-rates higher than 1 Gbps.
- Default setting optimized for driving 10 - 46 in of PCB trace length. Equalizer can be configured for longer reach using serial interface.
- Test setup: Pattern generator -> test backplane -> DUT -> error detector

Table 1-9. Output Pre-Emphasis Performance Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Output signal data-rate	—	42	—	1600	Mbps
—	Maximum error-free distance at 3.2 Gbps	2, 3, 6	—	—	40	in
—	Maximum error-free distance at 1.6 Gbps	2, 3, 6	—	—	60	in

NOTES:

1. Specified at recommended operating conditions – see [Table 1-2](#).
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML receiver without input equalization, using PCML output driver at 1200 mV_{PP} output swing at beginning of line.
4. Combined adaptive equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
5. Output pre-emphasis has greatest effect for data-rates higher than 1 Gbps.
6. Test setup: Pattern generator -> DUT -> test backplane -> error detector

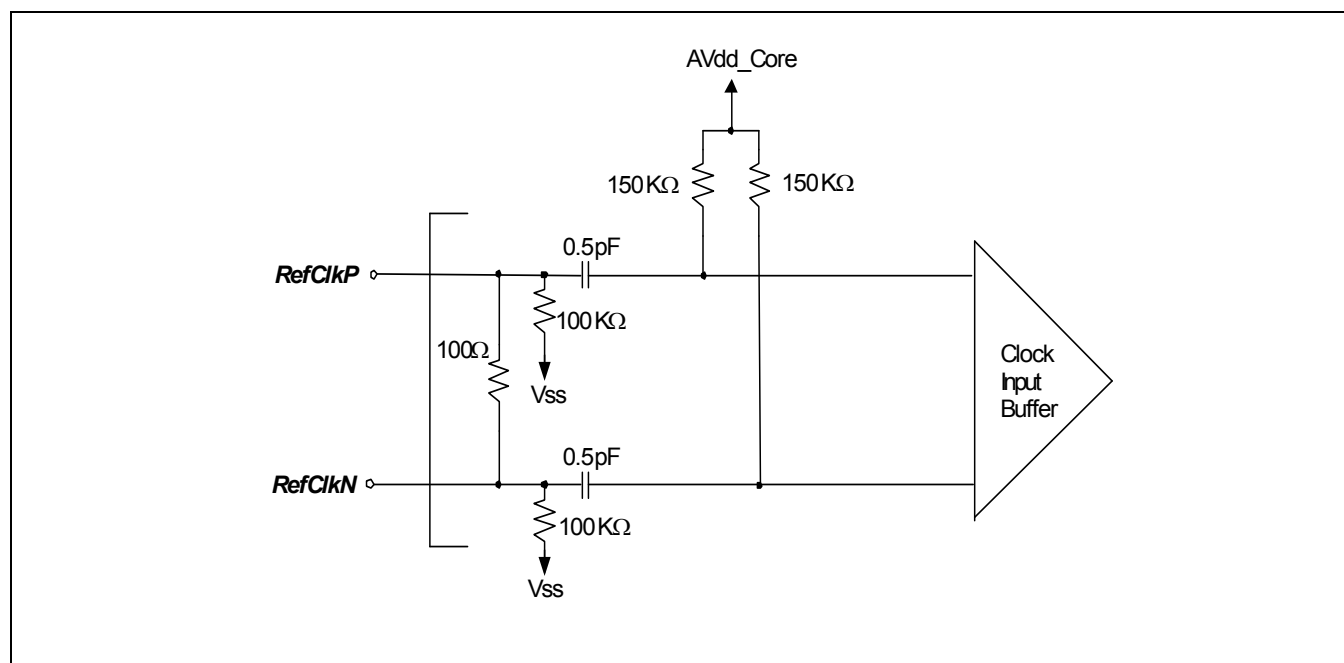
Table 1-10. Reference Clock Input

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 000b)	2,3	10	19.44	25	MHz
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 001b)	2,3	20	38.88	50	MHz
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 010b)	2,3	40	77.76	100	MHz
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 011b)	2,3	80	155.52	200	MHz
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 100b)	2	120	250	300	MHz
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 101b)	2,3	160	311.04	400	MHz
F _{REF}	Input frequency (<i>Refclk_ctrl</i> [3:1] = 110b)	2,3	320	622.08	800	MHz
V _{IN}	Input differential voltage (P-P)	4,5	100	—	1600	mV
V _{ICM}	Input common-mode voltage	2,5	250	—	AV_{DDIO}	mV
—	Input duty cycle	—	40	50	60	%
—	Frequency stability	2	—	—	100	ppm
R _{IN}	Differential termination	5	—	100	—	Ω
—	Internal pull-down to V_{SS}	—	—	100	—	kΩ
—	Maximum DC input current	—	—	—	15	mA

NOTES:

1. Specified at recommended operation conditions – see [Table 1-2](#).
2. Used for frequency acquisition.
3. Typical values are exact integer ratios for SONET applications.
4. Example 1200 mV_{PP} differential = 600 mV_{PP} for each single-ended terminal.
5. Input can accept a CMOS single-ended clock on differential P terminal when differential N terminal is decoupled to ground with a large enough capacitor. CMOS input will then see an effective 100Ω load.
6. See [Figure 1-3](#) for input termination circuit.

Figure 1-3. Reference Clock Input Internal Circuitry



1.5 High-Speed Performance Specifications

Table 1-11. Crosspoint Switching Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
—	Switch command to start of high-speed signal switching (hardwired mode)	2, 4	—	1	1.5	ns
t_{SW}	Switching time	3, 4	—	1	2	ns
t_{PD}	Input/Output latency (CDR/reclocker disabled or bypassed)	—	—	—	500	ps
t_{PD}	Input/Output latency (utilizing CDR/reclocker)	—	—	—	2	ns
$t_{SKEW, CH}$	Channel to channel output data skew (CDR/reclocker disabled or bypassed)	—	—	—	55	ps
$t_{SKEW, CH}$	Channel to channel output data skew (utilizing CDR/reclocker)	5	—	—	65	ps

NOTES:

- Specified at recommended operating conditions – see Table 1-2.
- Defined as 50% point in switch state pins, to when high-speed data amplitude changes by 10%.
- Defined as when the terminated high-speed signal drops 10% in amplitude, and the new high-speed signal is 90% settled.
- Specified with CDR/reclocker disabled or bypassed.
- Does not include variation in static phase offset between CDR/reclockers.

Table 1-12. CDR/RCLK High-Speed Performance (1 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR	Input signal data-rate (NRZ data) divider ratio = 1	—	2	—	3.2	Gbps
DR	Input signal data-rate (NRZ data) divider ratio = 2	—	1	—	1.6	Gbps
DR	Input signal data-rate (NRZ data) divider ratio = 4	—	500	—	800	Mbps
DR	Input signal data-rate (NRZ data) divider ratio = 8	—	250	—	400	Mbps
DR	Input signal data-rate (NRZ data) divider ratio = 12	—	167	—	267	Mbps
DR	Input signal data-rate (NRZ data) divider ratio = 16	—	125	—	200	Mbps
DR	Input signal data-rate (NRZ data) divider ratio = 24	—	83	—	133	Mbps
DR	Input signal data-rate (NRZ data) divider ratio = 32	—	62.5	—	100	Mbps
DR	Input signal data-rate (NRZ data) divider ratio = 48	—	42	—	67	Mbps
J _{TOL}	Jitter tolerance (Figure 1-5)	2	—	0.625	—	UI
J _{TRAN}	Jitter transfer (Figure 1-6)	2, 16	—	—	—	—
J _{GEN}	Jitter generation (rms) at STS-N (N = 1, 3, 12, 48)	2, 12	—	4.5	6.5	mUI
J _{GEN}	Jitter generation (pp) at STS-N (N = 1, 3, 12, 48)	2, 12	—	30	55	mUI
F _{LBW}	Default loop bandwidth: divider ratio = 1	3,4,5	—	—	2	MHz
F _{LBW}	Default loop bandwidth: divider ratio = 2	3,4,5	—	—	1	MHz
F _{LBW}	Default loop bandwidth: divider ratio = 4	3,4,5	—	—	500	kHz
F _{LBW}	Default loop bandwidth: divider ratio = 8	3,4,5	—	—	250	kHz
F _{LBW}	Default loop bandwidth: divider ratio = 12	3,4,5	—	—	167	kHz
F _{LBW}	Default loop bandwidth: divider ratio = 16	3,4,5	—	—	125	kHz
F _{LBW}	Default loop bandwidth: divider ratio = 24	3,4,5	—	—	83	kHz
F _{LBW}	Default loop bandwidth: divider ratio = 32	3,4,5	—	—	62.5	kHz
F _{LBW}	Default loop bandwidth: divider ratio = 48	3,4,5	—	—	41.6	kHz
t _{RJ}	Output data random jitter (pp)	13	—	—	100	mUI
t _{DJ}	Output data deterministic jitter (pp)	13	—	—	110	mUI
T _{JUNC}	Output data total jitter (pp)	13	—	—	210	mUI
t _{PD}	Latency from input to output (utilizing CDR)	—	—	1.75	2	ns
t _{SKEW, CH}	Channel to channel output data skew (utilizing CDR)	—	—	10	65	ps
—	Initialization time	6,7,10	—	2	—	ms
t _{FRA}	Frequency acquisition time	6,8	—	0.4	—	ms

Table 1-12. CDR/RCLK High-Speed Performance (2 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_{LOCK}	Phase lock time with 100 ppm delta F	9,11			100	ns
t_{LOCK}	Phase lock time with 0 ppm delta F	9,11			50	ns

NOTES:

- Specified at recommended operating conditions – see [Table 1-2](#).
- Jitter tolerance, jitter transfer, and jitter generation specified with input equalization and output pre-emphasis disabled, utilizing PRBS 2²³-1, per GR-253 test methodologies.
- Nominal loop bandwidth for 2.48832 GHz/ DRD.
- Bandwidth is proportional to frequency.
- For SONET data-rates, default meets SONET specifications.
- Assume that reference is within +/-100 ppm of desired data-rate.
- Time after power up, reset, or data-rate change.
- Time from application of valid data to lock within +/-20% of lock phase.
- Defined as when phase settles to within 20% of lock phase.
- After reset (master or soft), initialization takes place, then frequency acquisition.
- Based on nominal SONET bandwidth (bandwidth can be increased for lower phase lock time).
- Jitter generation specified per GR-253, utilizing bandpass filter with passband 12 kHz to 20 MHz for STS-48.
- t_{RJ} , t_{DJ} , T_{JUNC} represent jitter measured to BER of 10⁻¹² per FC-P1-2 specifications.
- Broadband jitter defined as jitter measured on sampling oscilloscope without the use of filters.
- Maximum value specified incorporates asynchronous aggressors.
- Jitter transfer of CDR meets the SONET STS-48 mask if loop bandwidth is set to 80% of nominal by writing *Phadj_ctrl_N[5:4] = 00b*. Jitter transfer at STS-12 (STS-3) exceeds mask by 0.1 dB in frequency range 10 - 25.1 kHz (1.5 - 10 kHz).

Table 1-13. RCLK Alarm Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DT _{LOA}	xLOA decision time	5	—	26	—	μs
—	xLOA assertion transition density threshold (xLOA = H to L)	5, 6	—	12.5	—	%
—	xLOA de-assertion transition density threshold (xLOA = L to H)	5, 6	—	12.5	—	%
DT _{LOL}	xLOL decision time (measurement time)	2	10	420	3275	μs
N _{WIDE}	xLOL assertion frequency threshold (xLOL = H to L)	2,3	±185	±2930	±250000	ppm
N _{NARROW}	xLOL de-assertion frequency threshold (xLOL = L to H)	2,3	±120	±1955	±250000	ppm

NOTES:

- Specified at recommended operating conditions – see [Table 1-2](#).
- Actual time is set with LOL window. Typical is the default value. Minimum and maximum indicate dynamic range.
- Assume that reference is +/-50 ppm of operating frequency.
- Computed for 1.4835 Gbps data-rate. Will scale with data-rate.
- Fixed values.
- Specification shown represents deviation from 50% transition density.

Figure 1-4. SMPTE Jitter Tolerance Specification Mask

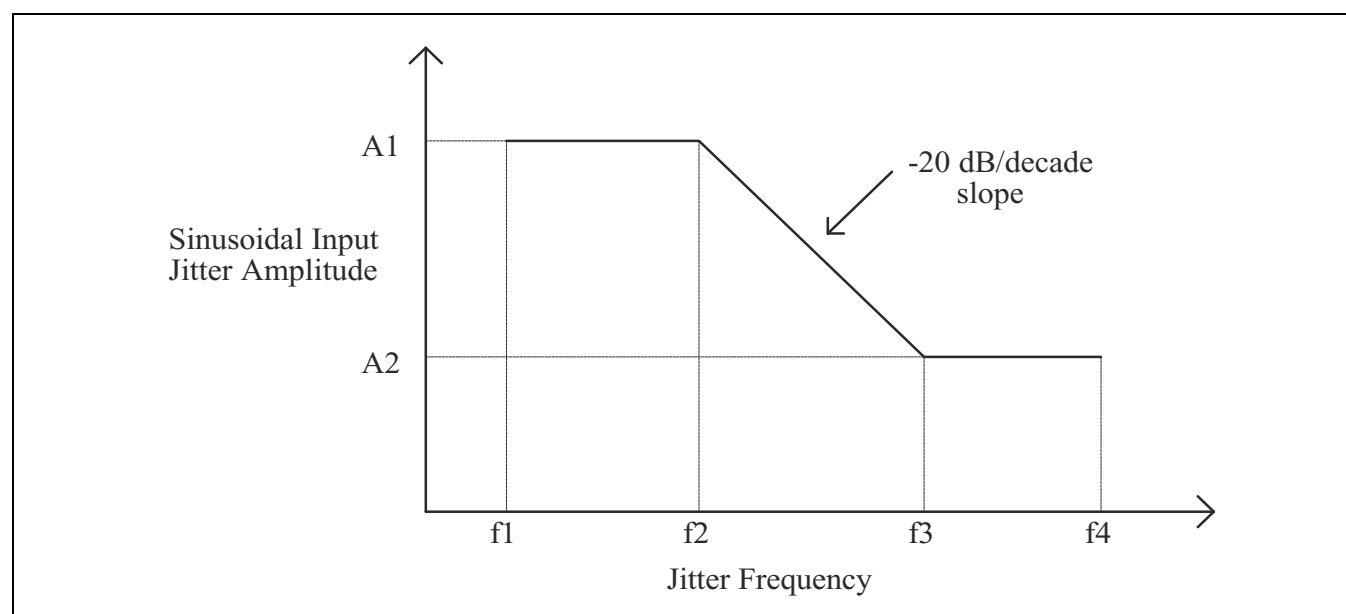


Table 1-14. SMPTE Jitter Tolerance Mask

Jitter Parameter	SMPTE 259M	SMPTE 292M
f1	10 Hz	10 Hz
f2	200 Hz	20 kHz
f3	1 kHz	100 kHz
f4	27 MHz	148.5 MHz
A1	1.0 UI	1.0 UI
A2	0.2 UI	0.2 UI

Figure 1-5. SONET Jitter Tolerance Specification Mask

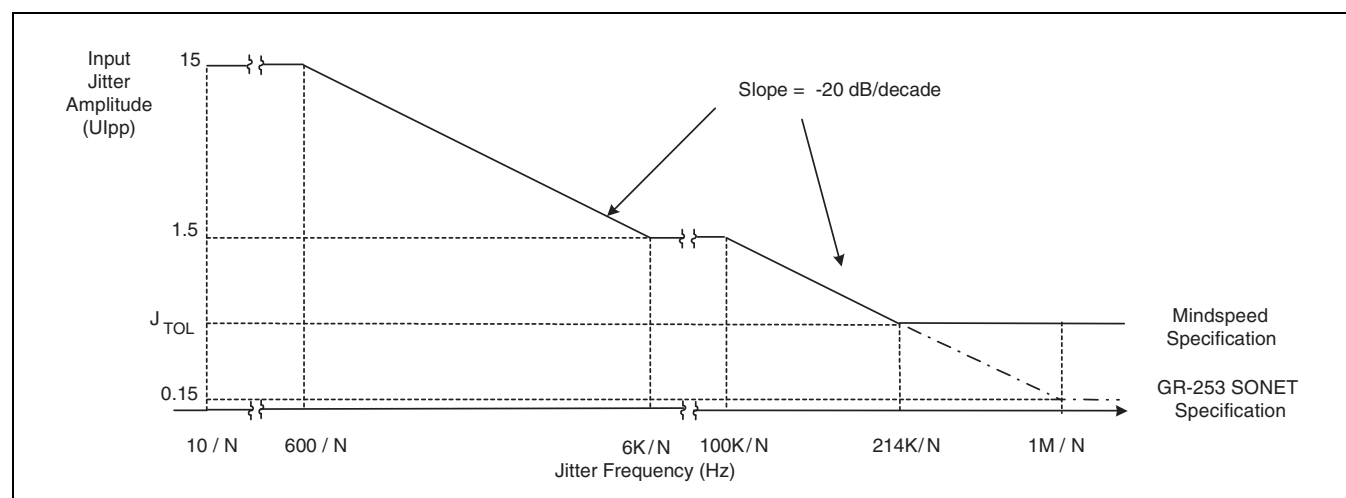


Figure 1-6. SONET/SMPTE Jitter Transfer Specification Mask

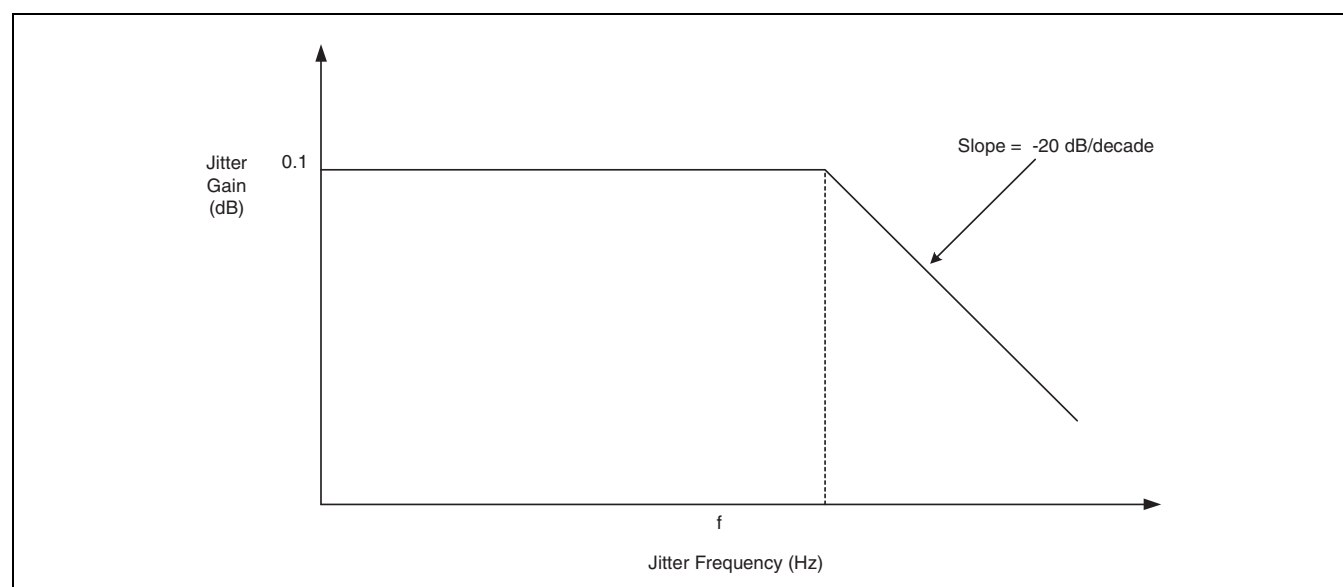


Table 1-15. Loop Bandwidths for Typical Video Data Rates

Application	Bit Rate (Mbps)	Value of N	Approximate Loop BW (f)
3G-SDI	2967/2970	0.84	2.38 MHz
HD-SDI	1485/1483.5	1.68	1.19 MHz
2xSD-SDI	540	4.6	435 MHz
Progressive Scan	360	6.9	290 kHz
SD-SDI	270	9.2	217 kHz
Legacy Comp Video	177	14.1	142 kHz
Legacy Comp Video	143	17.4	115 kHz

* See [Table 1-11](#) for jitter transfer at SONET data rates.

1.6 Package Drawings and Surface Mount Assembly Details

The M21260 is assembled in 72-pin 10 mm x 10 mm QFN packages. This is a plastic encapsulated package with a copper leadframe. The QFN is a leadless package with lands on the bottom surface of the package.

The exposed die paddle serves as the IC ground (V_{SS}), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the QFN package can be found in [Figure 1-7](#).

Figure 1-7. Cross-Section of QFN Package

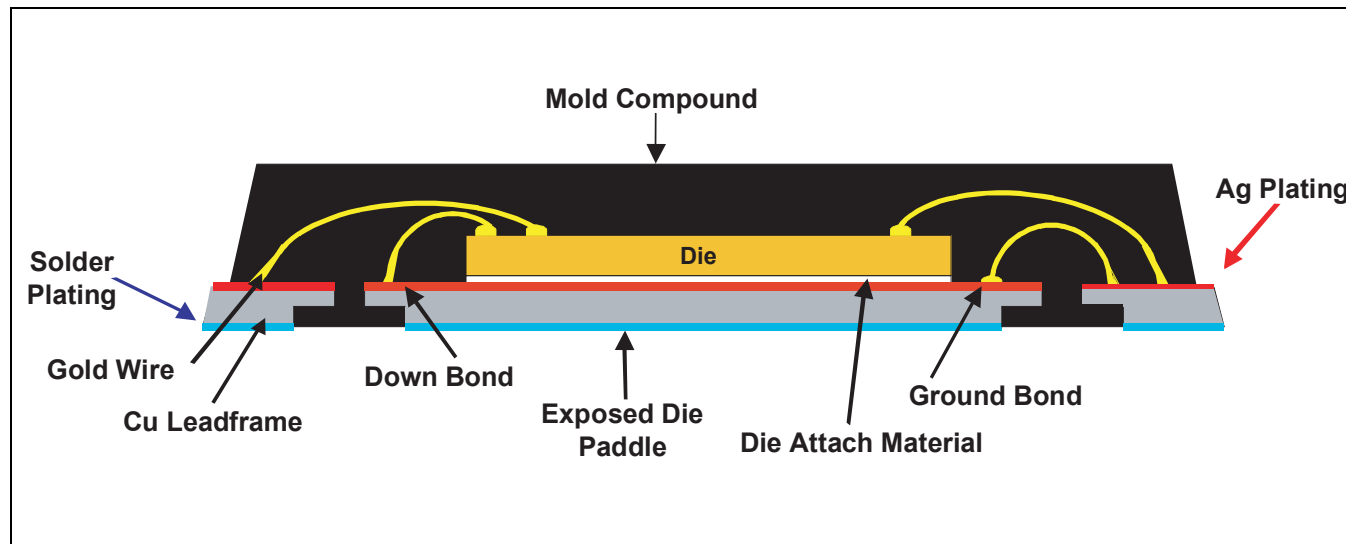
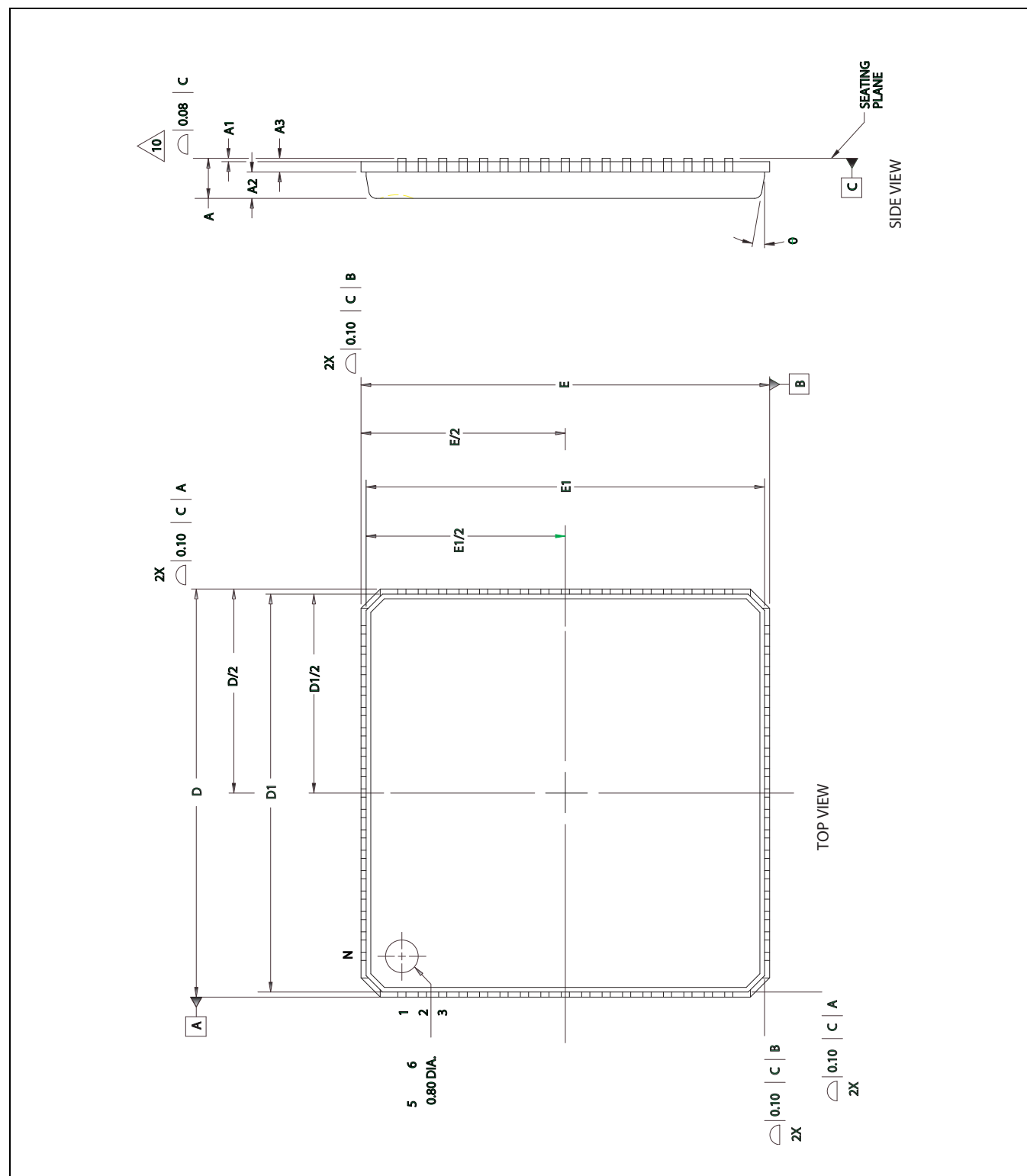


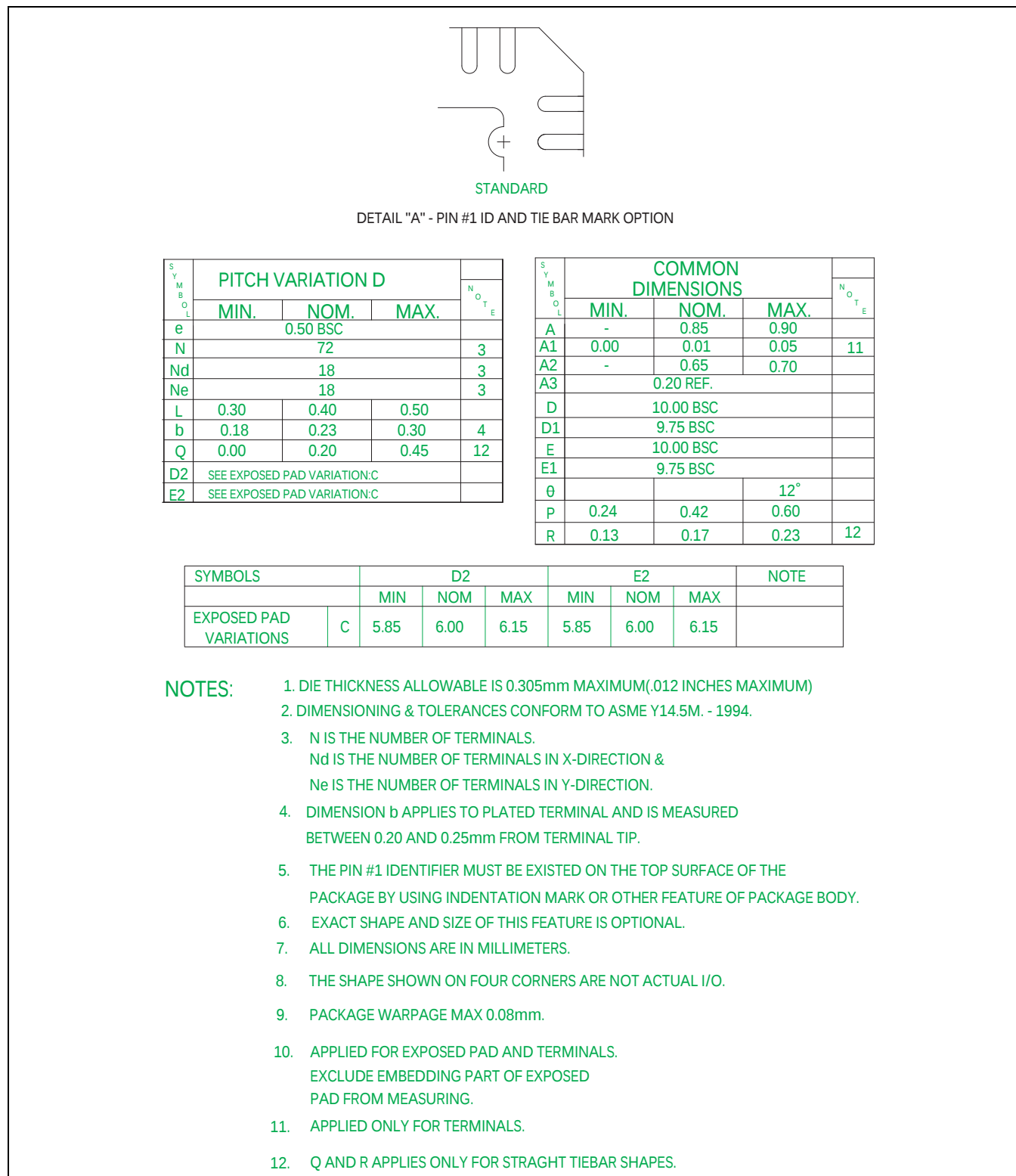
Figure 1-8. Package Drawing (1 of 2)



[illegible]

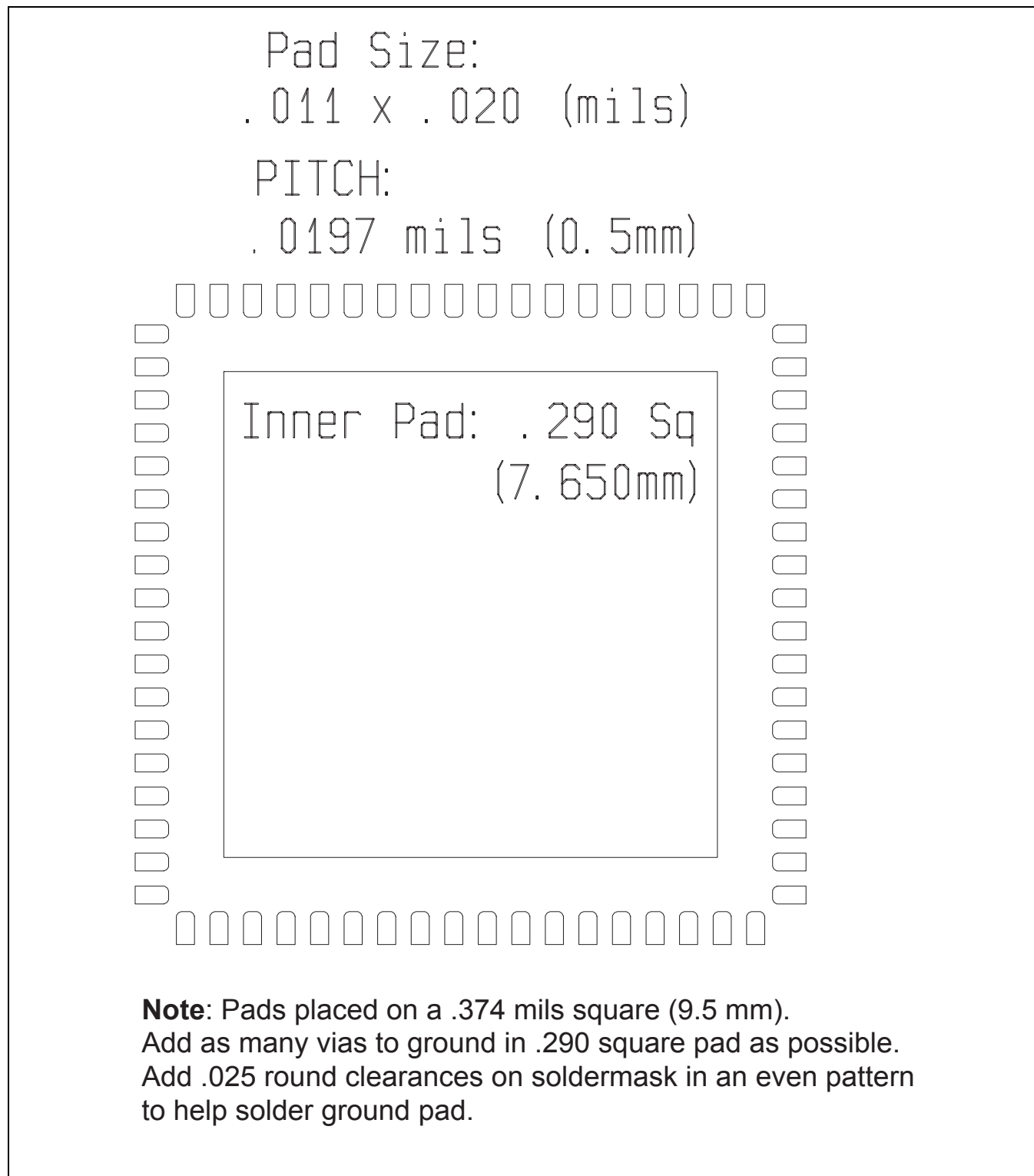
The relevant dimensions for the 72-pin version of the package can be found in [Figure 1-10](#).

Figure 1-10. 72-Pin Package Dimensions



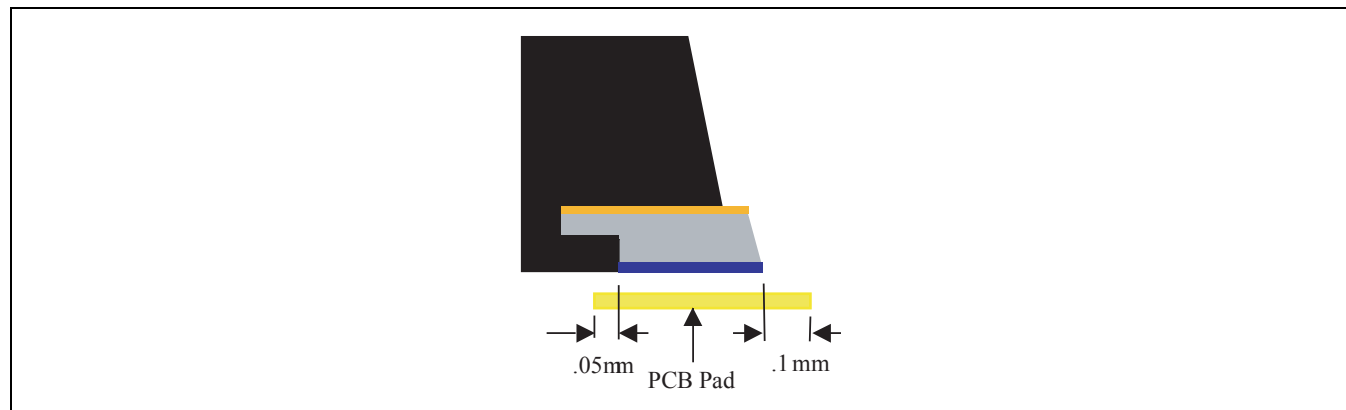
The M21260 evaluation module (EVM) uses the PCB footprint shown in [Figure 1-11](#).

Figure 1-11. PCB Footprint for 72-Pin 10 mm QFN Package



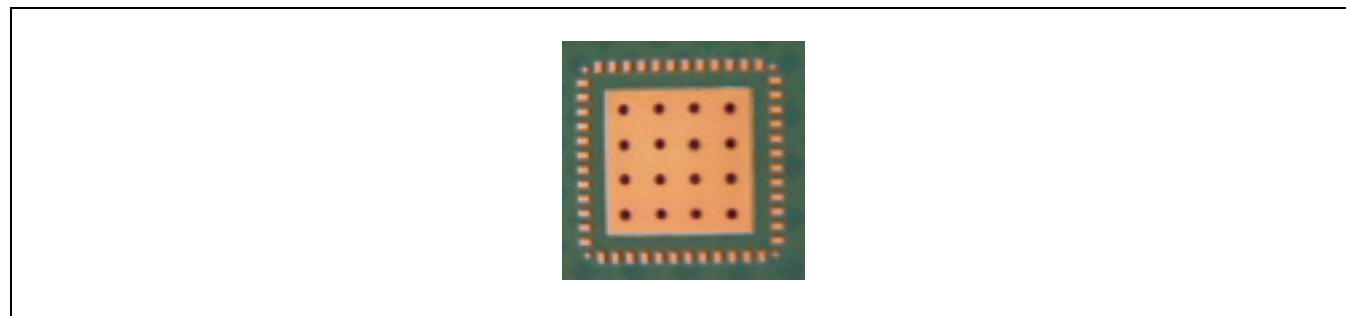
The pad length dimensions should account for component tolerances, PCB tolerances, and placement tolerances. At a minimum, the pad should extend at least 0.1 mm on the outside and 0.05 mm on the inside, as shown in [Figure 1-12](#).

Figure 1-12. PCB Pad Extensions



To efficiently dissipate heat from the M21260, a thermal pad with thermal vias should be used on the PCB. An example of a thermal pad with a 4x4 via array is shown in [Figure 1-13](#). The thermal vias provide a heat conduction path to inner and/or bottom layers of the PCB. The larger the via array, the lower the thermal resistance (θ_{JA}). It is recommended to use thermal vias with 1.0 to 1.2 mm pitch with 0.3 to 0.33 mm via diameter.

Figure 1-13. Recommended Via Array for Thermal Pad



For further details please refer to the relevant application note from package vendor Amkor (see list of references at the end of this document). Much of the material in this section has been adopted from the Amkor SMT application note.

1.7 PCB High-Speed Design and Layout Guidelines

A single power plane for the **AV_{DDIO}** and **AV_{DDCORE}** power supplies with bulk capacitors (typically 10 μF) distributed throughout the board will mitigate most power-rail related voltage transients. A bulk capacitor should also be placed where the power enters the board. It is recommended that decoupling capacitors only be routed directly to the power pin if they can be placed within 1/8 of an inch of the pin. Decoupling capacitors should be dispersed around the outside of the device on the top side and underneath the IC on the bottom side of the board. It is recommended that 0.1 μF and 0.01 μF decoupling capacitors be used. All three capacitor values are not required on each pin, but should be dispersed uniformly to filter different frequencies of noise.

A continuous ground plane is the best way to minimize ground impedance. Return currents and power supply transients produce most ground noise during switching. Reducing ground plane impedance minimizes this effect. There is a high frequency decoupling effect from the capacitive effect of power/ground planes and this can be used to help minimize the amount of high frequency decoupling capacitors.

High-speed PCML signals should be routed with 50 Ω equal length traces for P and N signals within each differential pair. Buried strip line is recommended for internal layers while microstrip line is used for signals routed on surface layers. There should be no discontinuity in the ground planes during the path of the signal traces.

Impedance discontinuities occur when a signal passes through vias and travels between layers. It is recommended to minimize the number of vias and layers that the transmit/receive signals travel through in the design. The system PCB should be designed so that high-speed signals pass through a minimal number of vias and remain on a single internal high-speed routing layer.

When vias need to be used, the via design should match the transmission line impedance by observing the following:

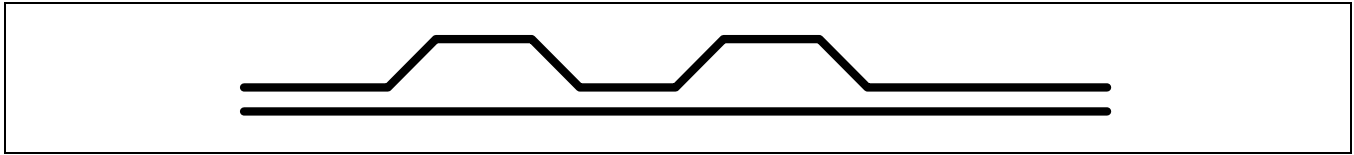
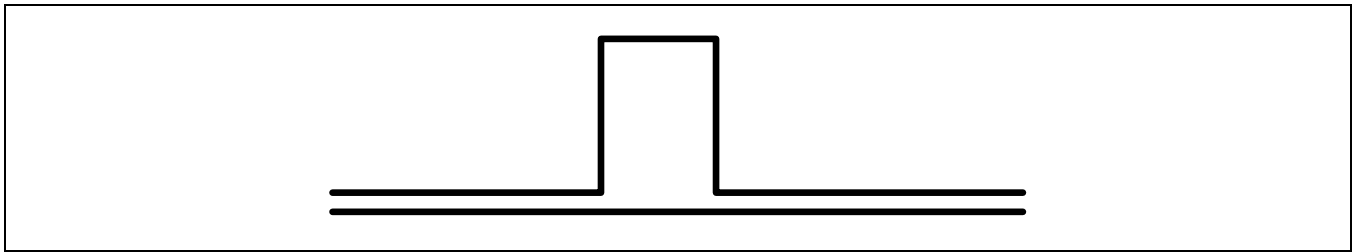
- Avoid through-hole vias; they cause stubs by extending the full cross-section of the PCB despite the fact that the layer change requires only a small length via (as in the case of adjacent layers). Use short blind vias.
- Avoid layer changes in general as the characteristic impedance of the transmission line changes as a result.

In general, some rules of thumb for PCB design for high data-rates are:

- PCB trace width for high-speed signals should closely match the SMT component width, so as to prevent stub effects from a sudden change in stripline width. A gradual increase in trace width is recommended as it meets the SMT pad.
- The PCB ground/power planes should be removed from under the I/O pins so as to reduce parasitic capacitance.
- High-speed traces should avoid sharp changes in direction. Using large radii will minimize impedance changes. Avoid bending traces by more than 45 degrees; otherwise, provide a circular bend so as to prevent the trace width from widening at the bend.
- Avoid trace stubs by minimizing components (resistors, capacitors) on the board. For instance, a termination resistor at the input of a receiver will inflict a stub effect at high frequency. Termination resistors integrated on chip will eliminate the stub. Components designed to DC couple to one another avoid the need for coupling capacitors and the inherent stubs created from them.

For high-speed differential signals, the trace lengths of each side of the differential pair should be matched to each other as much as possible. The skew between the P and N signals in a differential pair should be tightly controlled in order for the differential receiver to detect a valid data transition. When matching trace-lengths within a differential pair, care should be taken to avoid introducing large impedance discontinuities. The figures below show two methods of matching the trace-lengths for a differential pair.

Typically, the preferred solution for trace-length matching in differential pairs is to use a serpentine pattern for the shorter signal as shown in [Figure 1-14](#). Using a serpentine pattern for length matching will minimize the differential impedance discontinuity while making both trace-lengths equal.

Figure 1-14. Trace-Length Matching Using Serpentine Pattern**Figure 1-15. Loop Length Matching for Differential Traces**

The loop length matching method shown in [Figure 1-15](#) will match the trace lengths of a differential pair, but will create a large impedance discontinuity in the transmission line, which could result in higher jitter on the signal and/or a greater sensitivity to noise for the differential pair.

When using capacitors to AC-couple the input, care should be taken to minimize the pattern-dependant jitter (PD_J) associated with the low-frequency cutoff of the coupling network. When NRZ data containing long strings of 1s or 0s is applied to a high-pass filter, a voltage droop occurs. This voltage droop causes PD_J in much the same fashion as inter-symbol interference (ISI) is generated from dispersion effects of long trace-lengths in backplane material.

If needed, use 0.1 μF capacitors to AC-couple the high-speed output signals, and the reference clock inputs. The high-speed data input signals can be DC-coupled.

On the Evaluation Module (EVM), we have tied DV_{DDIO} and AV_{DDIO} together to minimize the number of power supply jacks. They are kept separate on-chip to give the flexibility to the system designers to supply a different voltage level for each. For instance, an FPGA can be used to supply power to DV_{DDIO} , while a lower voltage can be used to power AV_{DDIO} to minimize power dissipation. On the EVM, we have also tied DV_{DDCORE} and AV_{DDCORE} together to minimize the number of power supply jacks. They are kept separate on-chip to provide more isolation, however, if the system board plane is properly decoupled, they can be tied together.

No inductive filtering on the system board is necessary between different power supplies of the IC. It is up to the system designer to determine if this needs to be considered for supplies that are coming from other parts of the system board (such as switching regulators or ASICs).

An inductor should not be used at the V_{ddT} pins. These pins were made available to create a low AC impedance, such that the 50 Ω on-chip termination impedances see a common AC ground. This assures both common-mode and differential termination. If common-mode termination is not important (such as in LVDS applications), simply leave the V_{ddT} pins floating. Note that a low AC impedance can also be created by tying the V_{ddT} pins to the AV_{DDIO} plane, thus saving on the number of external capacitors. This, however, implies a CML-like data interface (unless the data is AC-coupled). V_{ddT} is not really a supply plane on-chip, it is simply the point to which the 50 Ω input impedances are tied.

Power planes should be decoupled to ground planes using thin dielectric layers, to increase capacitance (preferably 2-4 mils). Reference ground layers should be used on both sides of inner layer routing planes, with controlled impedance. The total board thickness should meet the standard drill holes to board thickness ratio of 1:12 or 1:14.

Use 1/2 ounce copper clad on all layers, which is approximately 0.7 mils. Avoid placing solder mask and silk-screen on top of transmission lines; solder mask will add 1 - 2Ω to the overall impedance of the transmission line. Dielectric core material should be used wherever possible, as it will maintain its thickness and geometry during processing, better than pliable prepreg.

The microwave ground should follow the transmission line from end to end, or from signal input to output. It is best to designate layers as dedicated microwave/circuit ground planes, and properly isolate them from other ground planes by providing adequate distance. All microwave ground planes should be tied together.

Uncoupled microstrip transmission lines should be placed at a distance from each other of at least three times the transmission line width. Coupled microstrip transmission lines, such as differential signal pairs, must be placed close to each other and maintain the same separation distance throughout the board (separation distance of at most twice the trace-width). For buried stripline transmission lines, it is good design practice to maintain equal distance between the conductor and the ground plane on both sides.

During PCB manufacturing, over- and under-etching of traces used for transmission lines results in impedance discontinuities. Use of wide traces for transmission lines will reduce the impact of etching issues. Wide traces also help compensate for skin-effect losses in transmission lines. It should be noted, however, that the wider the traces in a differential pair, the thicker the underlying dielectric layer needs to be.

Surface mount connectors are preferred over through-mount connectors. Connectors should be selected that have controlled characteristic impedances that match the characteristic impedances of the transmission lines.

1.8 Auto Rate Detect (ARD)

For many video applications, CDR/reclockers are required to auto rate detect (ARD) the incoming data rate. Mindspeed has developed a reference design for an ARD implementation. The reference design includes binary files for the ARD software and a hardware reference design based on the ATMEL AT89C51Rx2 series of micro controllers. The ARD automatically configures the device for nine possible fixed data rates of 143, 177, 270, 360, 540, 1483.5, 1485, 2967, or 2970 Mbps for the M21260. If desired, customers can expand the ARD code to include operation at other data rates.

Please refer to the M2125X and M2126X ARD software description documents for details on Mindspeed's implementation of Auto Rate Detect for this device.



2.0 Registers

Table 2-1. Register Table Summary

Addr	Register Name	d7: MSB	d6	d5	d4	d3	d2	d1	d0: LSB
Common Registers									
00h	<i>Globctrl</i>	powerup	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int	reserved	clear_alm
01h	<i>XPoint_ctrl</i>	port3[1]	port3[0]	port2[1]	port2[0]	port1[1]	port1[0]	port0[1]	port0[0]
04h	<i>Refclk_ctrl</i>	reserved	reserved	reserved	reserved	ref_divr[2]	ref_divr[1]	ref_divr[0]	MSPD int
05h	<i>Mastreset</i>	rst	rst	rst	rst	rst	rst	rst	rst
06h	<i>Chipcode</i>	chipcode[7]	chipcode[6]	chipcode[5]	chipcode[4]	chipcode[3]	chipcode[2]	chipcode[1]	chipcode[0]
07h	<i>Revcode</i>	revcode[7]	revcode[6]	revcode[5]	revcode[4]	revcode[3]	revcode[2]	revcode[1]	revcode[0]
10h	<i>BISTrx_chsel</i>					reserved	chan[2]	chan[1]	chan[0]
11h	<i>BISTrx_ctrl</i>	MSPD int	rx_ctrlr	rx_patt[3]	rx_patt[2]	rx_patt[1]	rx_patt[0]	en_rx	rx_rst
12h	<i>BISTrx_error</i>	err[7]	err[6]	err[5]	err[4]	err[3]	err[2]	err[1]	err[0]
14h	<i>BISTtx_chsel</i>	reserved	reserved	reserved	reserved	reserved	reserved	tx_chan_1	tx_chan_0
15h	<i>BISTtx_ctrl</i>	err_insert	rx2bclk	tx_patt[3]	tx_patt[2]	tx_patt[1]	tx_patt[0]	en_tx	tx_rst
17h	<i>BISTtx_LOLctrl</i>	tacq_LOL[2]	tacq_LOL[1]	tacq_LOL[0]	narwin_LOL[3]	narwin_LOL[2]	narwin_LOL[1]	narwin_LOL[0]	widwin_LOL[0]
18h	<i>BISTtx_PLL_ctrlA</i>	softreset	MSPD int	reserved	MSPD int	reserved	MSPD int	reserved	MSPD int
19h	<i>BISTtx_PLL_ctrlB</i>	PLLmode[1]	PLLmode[0]	MSPD int	MSPD int	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
1Ah	<i>BISTtx_PLL_ctrlC</i>	VCO_divr[7]	VCO_divr[6]	VCO_divr[5]	VCO_divr[4]	VCO_divr[3]	VCO_divr[2]	VCO_divr[1]	VCO_divr[0]
1Bh	<i>BIST_pattern0</i>					pattern[19]	pattern[18]	pattern[17]	pattern[16]
1Ch	<i>BIST_pattern1</i>	pattern[15]	pattern[14]	pattern[13]	pattern[12]	pattern[11]	pattern[10]	pattern[9]	pattern[8]
1Dh	<i>BIST_pattern2</i>	pattern[7]	pattern[6]	pattern[5]	pattern[4]	pattern[3]	pattern[2]	pattern[1]	pattern[0]
1Fh	<i>BISTtx_alarm</i>	tx_LOL	reserved	reserved	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int
20h	<i>Temp_mon</i>					reserved	reserved	en_temp_mon	strobe_temp
21h	<i>Temp_value</i>					temp[3]	temp[2]	temp[1]	temp[0]
30h	<i>Alarm_LOL</i>	MSPD int	MSPD int	MSPD int	MSPD int	LOL_3	LOL_2	LOL_1	LOL_0
31h	<i>Alarm_LOA</i>	MSPD int	MSPD int	MSPD int	MSPD int	LOA_3	LOA_2	LOA_1	LOA_0
32h	<i>Alarm_trim</i>	reserved	reserved	reserved	reserved	trim_alarm_3	trim_alarm_2	trim_alarm_1	trim_alarm_0
Per channel registers (N = channel/RCLK#, M = N+4)									
M0h	<i>cdr_ctrlA_N</i>	softreset	force_filter_rst	inh_force	lol_force	autoinh_en	freqwin_en	los_en	trim_en
M1h	<i>cdr_ctrlB_N</i>	CDRmode[1]	CDRmode[0]	test_1010pa t	reserved	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
M2h	<i>RCLK_ctrlC_N</i>	VCO_divr[7]	VCO_divr[6]	VCO_divr[5]	VCO_divr[4]	VCO_divr[3]	VCO_divr[2]	VCO_divr[1]	VCO_divr[0]
M3h	<i>Out_ctrl_N</i>	outlv[1]	outlv[0]	reserved	reserved	data_pol_flip	dataout_en	MSPD int	MSPD int
M4h	<i>Preemp_ctrl_N</i>	reserved	MSPD int	MSPD int	MSPD int	MSPD int	preemph[2]	preemph[1]	preemph[0]
M5h	<i>Ineq_ctrl_N</i>	reserved	MSPD int	MSPD int	en_DCservo	MSPD int	in_eq[2]	in_eq[1]	in_eq[0]
M6h	<i>Phadj_ctrl_N</i>	i_trim[1]	i_trim[0]	r_sel[1]	r_sel[0]	phase_adj[3]	phase_adj[2]	phase_adj[1]	phase_adj[0]
M8h	<i>LOA_ctrl_N</i>	tacq_LOA[2]	tacq_LOA[1]	tacq_LOA[0]	narwin_LOA[3]	narwin_LOA[2]	narwin_LOA[1]	narwin_LOA[0]	widwin_LOA[0]
M9h	<i>LOL_ctrl_N</i>	tacq_LOL[2]	tacq_LOL[1]	tacq_LOL[0]	narwin_LOL[3]	narwin_LOL[2]	narwin_LOL[1]	narwin_LOL[0]	widwin_LOL[0]
MAh	<i>trim_force_N</i>	force_FDAdiv	en_LOT	force_trimms b	trim_force[4]	trim_force[3]	trim_force[2]	trim_force[1]	trim_force[0]
MBh	<i>trim_value_N</i>	reserved	reserved	reserved	trim_val[4]	trim_val[3]	trim_val[2]	trim_val[1]	trim_val[0]
Notes:									
1. N = 0 for channel/RCLK 0, N = 1 for channel/RCLK 1,, N = 3 for channel/RCLK 3.									
2. M = 4 for channel/RCLK 0, M = 5 for channel/RCLK 1,, M = 7 for channel/RCLK 3. For example channel/RCLK 0 starts at address 40h, channel/RCLK 1 at 50h, channel/RCLK 2 at 60h, channel/RCLK 3 at 70h.									

2.1 Global Control Registers

Nomenclature:

1. Reserved bits: bits that exist and are reserved for future use by Mindspeed.
2. Bits not defined and not reserved do not exist.
3. Do not write to reserved or undefined bits – operation not guaranteed.
4. MSPD internal: defines an internal function. Must always write the default value to MSPD internal bits. When in doubt, read back default value after reset.

2.1.1 Global Control

Table 2-2. Global Control (Globctrl: Address 00h)

Bits	Type	Default	Label	Description
7	R/W	1b	powerup	Powers up the IC by enabling the current references 1b: Power up the IC (chip powerup, default) 0b: Power down the IC
6:2	R/W	00000b	MSPD internal	N/A
1	R/W	0b	Reserved	N/A
0	R/W	0b	clear_alm	Clears <i>Alarm_LOL</i> , <i>Alarm_LOA</i> alarm registers (write only) 1b: Clear alarms 0b: Normal operation - latch alarm bits (default) Note: Upon writing a 1b to this bit, it clears the registers, and user needs to write a 0b to enable the normal state.

2.1.2 Crosspoint Switch-State Setting

Table 2-3. Crosspoint Switch-State Setting (XPoint_ctrl: Address 01h)

Bits	Type	Default	Label	Description
7:6	R/W	11b	port 3	Determines input channel for output 3 00b: Selects input 0 01b: Selects input 1 10b: Selects input 2 11b: Selects input 3 (default)
5:4	R/W	10b	port 2	Determines input channel for output 2 00b: Selects input 0 01b: Selects input 1 10b: Selects input 2 (default) 11b: Selects input 3
3:2	R/W	01b	port 1	Determines input channel for output 1 00b: Selects input 0 01b: Selects input 1 (default) 10b: Selects input 2 11b: Selects input 3
1:0	R/W	00b	port 0	Determines input channel for output 0 00b: Selects input 0 (default) 01b: Selects input 1 10b: Selects input 2 11b: Selects input 3

2.1.3 04h: External Reference Frequency Divider Control (RFD)

Table 2-4. External Reference Frequency Divider Control (RFD) (Refclk_ctrl: Address 04h)

Bits	Type	Default	Label	Description
7:4	R/W	0b	Reserved	N/A (0 default)
3:1	R/W	000b	ref_divr	Sets the divider ratio to scale down RefClk to the internal rate for FRA/LOA 000b: RFD = 1 (default) 001b: RFD = 2 010b: RFD = 4 011b: RFD = 8 100b: RFD = 12 101b: RFD = 16 110b: RFD = 32
0	R/W	0b	MSPD internal	N/A (0 default)

2.1.4 Master IC Reset

Table 2-5. Master IC Reset (Mastreset: Address 05h)

Bits	Type	Default	Label	Description
7:0	R/W	0b	rst	Same feature as hardware xRST . Resets the entire IC AAh: Reset upon write to this register with AAh 00h: Normal operation [Default] Note: All other values are ignored.

2.1.5 IC Electronic Identification

Table 2-6. IC Electronic ID (Chipcode: Address 06h)

Bits	Type	Default	Label	Description
7:0	R	26h	chipcode	This register contains the identification of this IC.

2.1.6 IC Revision Code

Table 2-7. IC Revision Code (Revcode: Address 07h)

Bits	Type	Default	Label	Description
7:0	R	23h	revcode	This register contains the revision of the IC.

2.1.7 Built In Self-Test (BIST) Receiver Channel Select

Table 2-8. Built In Self-Test (BIST) Receiver Channel Select (BISTrx_chsel: Address 10h)

Bits	Type	Default	Label	Description
7:3	R/W	0b	Reserved	N/A
2:0	R/W	000b	chan	Selects which RCLK to route into the BIST receiver (active when <i>BISTrx_ctrl</i> [1]=1) 000b: Output RCLK 0 to BIST (default) 001b: Output RCLK 1 to BIST 010b: Output RCLK 2 to BIST 011b: Output RCLK 3 to BIST

2.1.8 Built In Self-Test (BIST) Receiver Main Control Register

Table 2-9. Built In Self-Test (BIST) Receiver Main Control Register (*BISTrx_ctrl*: Address 11h)

Bits	Type	Default	Label	Description
7	R/W	0b	MSPD internal	N/A
6	R/W	0b	rx_ctrlr	Clear the BIST Rx error count register, <i>BISTrx_error</i> (active when <i>BISTrx_ctrl</i> [1] = 1) 0b: Normal operation (default) 1b: Clear register
5:2	R/W	0000b	rx_patt	Selects the BIST Rx test pattern (active when <i>BISTrx_ctrl</i> [1] = 1) 0000b: PRBS 2 ⁷ -1 (default) 0001b: PRBS 2 ¹⁵ -1 0010b: PRBS 2 ²³ -1 0011b: PRBS 2 ³¹ -1 0100b: Fibre channel CJTPAT 0101b: Fibre channel CRPAT 0110b: 8b/10b countdown pattern 0111b: 16 bit user programmable pattern 1000b: 20 bit user programmable pattern
1	R/W	0b	en_rx	Powers up the BIST Rx 0b: Power down (default) 1b: Power up and enable
0	R/W	1b	rx_rst	Resets the BIST Rx (recommended after powerup/enable, active when <i>BISTrx_ctrl</i> [1] = 1) 0b: Normal BIST Rx operation 1b: Reset of BIST Rx (default)

2.1.9 Built In Self-Test (BIST) Receiver Bit Error Counter

Table 2-10. Built In Self-Test (BIST) Receiver Bit Error Counter (*BISTrx_error*: Address 12h)

Bits	Type	Default	Label	Description
7:0	R/W	00h	err	Bit error count (active when <i>BISTrx_ctrl</i> [1] = 1) This register is set to 00h upon reset, and is incremented for every bit error the BIST Rx receives, up to FFh. At FFh, the register will stay at this level until cleared.

2.1.10 Built In Self-Test (BIST) Transmitter Channel Select

Table 2-11. Built In Self-Test (BIST) Transmitter Channel Select (BISTtx_chsel: Address 14h)

Bits	Type	Default	Label	Description
7:4	R/W	0000b	Reserved	N/A
3:0	R/W	0000b	tx_chan	Selects which output channel the BIST Tx outputs the test pattern on (active when <i>BISTtx_ctrl</i> [1] = 1) Bit map: 1b = BIST Tx on, 0b = BIST Tx off [3]: N/A, set to "0" [2]: N/A, set to "0" [1]: Output channel 1 [0]: Output channel 0 Note: Registers are set up to allow for multicasting BIST Tx output.

2.1.11 Built In Self-Test (BIST) Transmitter Main Control Register

Table 2-12. Built In Self-Test (BIST) Transmitter Main Control Register (*BISTtx_ctrl*: Address 15h)

Bits	Type	Default	Label	Description
7	R/W	0b	err_insert	Inserts a single bit error into the PRBS Tx 1b: Insert error 0b: Normal operation (default) Note: Setting the register high allows one error to be inserted into the data stream. To insert another error, the user needs to clear, then set this register bit.
6	R/W	0b	rx2txclk	Selects the source of the clock for the BIST Tx PLL (active when <i>BISTtx_ctrl</i>[1] = 1) 0b: External reference frequency (default) 1b: Recovered clock from BIST Rx Note: For the recovered clock option, the BIST Rx must be enabled with <i>BISTrx_ctrl</i>[1] = 1, and use the recovered clock from the same RCLK selected by BIST Rx. This option only works for the full-rate case.
5:2	R/W	0000b	tx_patt	Selects the BIST Tx test pattern (active when <i>BISTtx_ctrl</i>[1] = 1) 0000b: PRBS 2⁷-1 (default) 0001b: PRBS 2¹⁵-1 0010b: PRBS 2²³-1 0011b: PRBS 2³¹-1 0100b: Fibre channel CJTPAT 0101b: Fibre channel CRPAT 0110b: 8b/10b countdown pattern 0111b: 16 bit user programmable pattern 1000b: 20 bit user programmable pattern
1	R/W	0b	en_tx	Powers up the BIST Tx and PLL 0b: Power down (default) 1b: Power up and enable
0	R/W	1b	tx_rst	Resets the BIST Tx (recommended after powerup/enable; active when <i>BISTtx_ctrl</i>[1] = 1) 0b: Normal BIST Tx operation 1b: Reset of BIST Tx (default)

2.1.12 Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register

Table 2-13. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (BISTtx_LOLctrl: Address 17h)

Bits	Type	Default	Label	Description																																		
7:5	R/W	101b	tacq_LOL	Sets the value for the LOL reference window <table><tr><td>Code</td><td>Value</td></tr><tr><td>000b</td><td>128</td></tr><tr><td>001b</td><td>256</td></tr><tr><td>010b</td><td>512</td></tr><tr><td>011b</td><td>1024</td></tr><tr><td>100b</td><td>2048</td></tr><tr><td>101b</td><td>4096 (default)</td></tr><tr><td>110b</td><td>8192</td></tr><tr><td>111b</td><td>16384</td></tr></table>	Code	Value	000b	128	001b	256	010b	512	011b	1024	100b	2048	101b	4096 (default)	110b	8192	111b	16384																
Code	Value																																					
000b	128																																					
001b	256																																					
010b	512																																					
011b	1024																																					
100b	2048																																					
101b	4096 (default)																																					
110b	8192																																					
111b	16384																																					
4:1	R/W	0100b	narwin_LOL	Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold) <table><tr><td>Code</td><td>Value</td></tr><tr><td>0000b</td><td>2</td></tr><tr><td>0001b</td><td>3</td></tr><tr><td>0010b</td><td>4</td></tr><tr><td>0011b</td><td>6</td></tr><tr><td>0100b</td><td>8 (default)</td></tr><tr><td>0101b</td><td>12</td></tr><tr><td>0110b</td><td>16</td></tr><tr><td>0111b</td><td>24</td></tr><tr><td>1000b</td><td>9</td></tr><tr><td>1001b</td><td>10</td></tr><tr><td>1010b</td><td>11</td></tr><tr><td>1011b</td><td>12</td></tr><tr><td>1100b</td><td>13</td></tr><tr><td>1101b</td><td>14</td></tr><tr><td>1110b</td><td>15</td></tr><tr><td>1111b</td><td>32</td></tr></table>	Code	Value	0000b	2	0001b	3	0010b	4	0011b	6	0100b	8 (default)	0101b	12	0110b	16	0111b	24	1000b	9	1001b	10	1010b	11	1011b	12	1100b	13	1101b	14	1110b	15	1111b	32
Code	Value																																					
0000b	2																																					
0001b	3																																					
0010b	4																																					
0011b	6																																					
0100b	8 (default)																																					
0101b	12																																					
0110b	16																																					
0111b	24																																					
1000b	9																																					
1001b	10																																					
1010b	11																																					
1011b	12																																					
1100b	13																																					
1101b	14																																					
1110b	15																																					
1111b	32																																					

Table 2-13. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (BISTtx_LOLctrl: Address 17h)

Bits	Type	Default	Label	Description		
0	R/W	0b	widwin_LOL	Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold)		
				Narrow	Wide	Wide
				Code	Code 0b (default)	Code 1b
				0000b	3	8
				0001b	4	12
				0010b	6	16
				0011b	8	24
				0100b	12	32
				0101b	16	32
				0110b	24	32
				0111b	32	32
				1000b	12	32
				1001b	12	32
				1010b	12	32
				1011b	16	32
				1100b	16	32
				1101b	16	32
				1110b	16	32
				1111b	32	32

2.1.13 Built In Self-Test (BIST) Transmitter PLL Control Register A

Table 2-14. Built In Self-Test (BIST) Transmitter PLL Control Register A (BISTtx_PLL_ctrlA: Address 18h)

Bits	Type	Default	Label	Description
7	R/W	0b	softreset	Resets the BIST transmitter PLL (assuming BISTtx_ctrl[1] = 1b) 0b: Normal operation (default) 1b: Reset PLL only
6	R/W	0b	MSPD internal	N/A
5	R/W	0b	Reserved	N/A
4	R/W	0b	MSPD internal	N/A
3	R/W	0b	Reserved	N/A
2	R/W	1b	MSPD internal	N/A
1	R/W	0b	Reserved	N/A
0	R/W	1b	MSPD internal	N/A

2.1.14 Built In Self-Test (BIST) Transmitter PLL Control Register B

Table 2-15. Built In Self-Test (BIST) Transmitter PLL Control Register B (BISTtx_PLL_ctrlB: Address 19h)

Bits	Type	Default	Label	Description
7:6	R/W	00b	PLLmode	Determines state of the PLL. Must be enabled in addition to the BIST Tx (BISTtx_ctrl[1] = 1b) 00b: Channel active, PLL powered up (default) 11b: Channel active, PLL powered down
5:4	R/W	01b	MSPD internal	N/A
3:0	R/W	0000b	data_rate	Data-rate divider (DRD): this divides down the VCO frequency to the desired data-rate 0000b = DRD = 1 (default) 0001b = DRD = 2 0010b = DRD = 4 0011b = DRD = 8 0100b = DRD = 12 0101b = DRD = 16 0110b = DRD = 24 0111b = DRD = 32 1000b = DRD = 48 Note: Consult F_{VCO_MAX} and F_{VCO_MIN} to determine the frequency range for each DRD ratio.

2.1.15 Built In Self-Test (BIST) Transmitter PLL Control Register C

Table 2-16. Built In Self-Test (BIST) Transmitter PLL Control Register C (BISTtx_PLL_ctrlC: Address 1Ah)

Bits	Type	Default	Label	Description
7:0	R/W	10000000b	VCO_divr	VCO comparison divider (VCD): Binary value reflects the divider ratio 01h: Minimum value (VCO /1) . . . FFh: Maximum value (VCO / 255) Note: Refer to Table 3-13 for recommended values of VCD for video data rates.

2.1.16 Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern

Table 2-17. Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern
(BIST_pattern0: Address 1Bh)

Bits	Type	Default	Label	Description
3:0	R/W	1100b	pattern	Sets the 20 bit user programmable pattern used in the BIST [3] MSB: Pattern bit#19 [2]: Pattern bit#18 [1]: Pattern bit#17 [0] LSB: Pattern bit#16

2.1.17 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern

Table 2-18. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern
(BIST_pattern1: Address 1Ch)

Bits	Type	Default	Label	Description
7:0	R/W	11001100b	pattern	Sets the 16/20 bit user programmable pattern used in the BIST [7] MSB: Pattern bit#15 [6]: Pattern bit#14 [5]: Pattern bit#13 [4]: Pattern bit#12 [3]: Pattern bit#11 [2]: Pattern bit#10 [1]: Pattern bit#9 [0] LSB: Pattern bit#8

2.1.18 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern

Table 2-19. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern
(BIST_pattern2: Address 1Dh)

Bits	Type	Default	Label	Description
7:0	R/W	11001100b	pattern	Sets the 16/20 bit user programmable pattern used in the BIST [7] MSB: Pattern bit#7 [6]: Pattern bit#6 [5]: Pattern bit#5 [4]: Pattern bit#4 [3]: Pattern bit#3 [2]: Pattern bit#2 [1]: Pattern bit#1 [0] LSB: Pattern bit#0

2.1.19 Built In Self-Test (BIST) Transmitter Alarm

Table 2-20. Built In Self-Test (BIST) Transmitter Alarm (*BISTtx_alarm*: Address 1Fh)

Bits	Type	Default	Label	Description
7	R	N/A	tx_LOL	Loss of lock for the BIST Tx PLL (active when <i>BISTtx_ctrl</i> [1] = 1) 0b: Normal operation 1b: Loss of lock
6:5	R/W	00b	Reserved	N/A
4:0	R/W	00000b	MSPD internal	N/A

2.1.20 Internal Junction Temperature Monitor

Table 2-21. Internal Junction Temperature Monitor (*Temp_mon*: Address 20h)

Bits	Type	Default	Label	Description
3:2	R/W	00b	Reserved	N/A
1	R/W	0b	en_temp_mon	Power up and enable the temperature monitor 1b: Enable and power up temperature monitor 0b: Disable temperature monitor (default)
0	R/W	0b	strobe_temp	Strobes ADC for temperature measurement 1b: Read temperature 0b: Ok to read temperature (default) Note: To strobe ADC, a rising edge should be provided by writing 1b, then writing 0b to return to default state.

2.1.21 Internal Junction Temperature Value

Table 2-22. Internal Junction Temperature Value (Temp_value: Address 21h)

Bits	Type	Default	Label	Description																																										
3:0	R	N/A	temp	A read of these bits returns the temperature from the last write cycle (to strobe_temp) <table><tr><td>Case Temperature</td><td>temp</td><td>Condition</td></tr><tr><td>To ≥ 130°C</td><td>1100b</td><td>High-alarm</td></tr><tr><td>130°C > T_{CASE} ≥ 120°C</td><td>1011b</td><td>High-alarm</td></tr><tr><td>120°C > T_{CASE} ≥ 110°C</td><td>1010b</td><td>High-warning</td></tr><tr><td>110°C > T_{CASE} ≥ 100°C</td><td>1001b</td><td>Normal</td></tr><tr><td>100°C > T_{CASE} ≥ 90°C</td><td>1000b</td><td>Normal</td></tr><tr><td>90°C > T_{CASE} ≥ 80°C</td><td>0111b</td><td>Normal</td></tr><tr><td>80°C > T_{CASE} ≥ 10°C</td><td>0110b</td><td>Normal</td></tr><tr><td>10°C > T_{CASE} ≥ 0°C</td><td>0101b</td><td>Normal</td></tr><tr><td>0°C > T_{CASE} ≥ -10°C</td><td>0100b</td><td>Normal</td></tr><tr><td>-10°C > T_{CASE} ≥ -20°C</td><td>0011b</td><td>Normal</td></tr><tr><td>-20°C > T_{CASE} ≥ -30°C</td><td>0010b</td><td>Low-warning</td></tr><tr><td>-30°C > T_{CASE} ≥ -40°C</td><td>0001b</td><td>Low-alarm</td></tr><tr><td>-40°C > T_{CASE}</td><td>0000b</td><td>Low-alarm</td></tr></table>	Case Temperature	temp	Condition	To ≥ 130°C	1100b	High-alarm	130°C > T _{CASE} ≥ 120°C	1011b	High-alarm	120°C > T _{CASE} ≥ 110°C	1010b	High-warning	110°C > T _{CASE} ≥ 100°C	1001b	Normal	100°C > T _{CASE} ≥ 90°C	1000b	Normal	90°C > T _{CASE} ≥ 80°C	0111b	Normal	80°C > T _{CASE} ≥ 10°C	0110b	Normal	10°C > T _{CASE} ≥ 0°C	0101b	Normal	0°C > T _{CASE} ≥ -10°C	0100b	Normal	-10°C > T _{CASE} ≥ -20°C	0011b	Normal	-20°C > T _{CASE} ≥ -30°C	0010b	Low-warning	-30°C > T _{CASE} ≥ -40°C	0001b	Low-alarm	-40°C > T _{CASE}	0000b	Low-alarm
Case Temperature	temp	Condition																																												
To ≥ 130°C	1100b	High-alarm																																												
130°C > T _{CASE} ≥ 120°C	1011b	High-alarm																																												
120°C > T _{CASE} ≥ 110°C	1010b	High-warning																																												
110°C > T _{CASE} ≥ 100°C	1001b	Normal																																												
100°C > T _{CASE} ≥ 90°C	1000b	Normal																																												
90°C > T _{CASE} ≥ 80°C	0111b	Normal																																												
80°C > T _{CASE} ≥ 10°C	0110b	Normal																																												
10°C > T _{CASE} ≥ 0°C	0101b	Normal																																												
0°C > T _{CASE} ≥ -10°C	0100b	Normal																																												
-10°C > T _{CASE} ≥ -20°C	0011b	Normal																																												
-20°C > T _{CASE} ≥ -30°C	0010b	Low-warning																																												
-30°C > T _{CASE} ≥ -40°C	0001b	Low-alarm																																												
-40°C > T _{CASE}	0000b	Low-alarm																																												

2.1.22 CDR/RCLK Loss of Lock Register Alarm Status

Table 2-23. CDR/RCLK Loss of Lock Register Alarm Status (Alarm_LOL: Address 30h)

Bits	Type	Default	Label	Description
7:4	N/A	0000b	MSPD internal	N/A
3:0	R	N/A	LOL	Latched loss of lock alarm status 1b = loss of CDR/RCLK lock 0b = normal operation [3]: CDR/RCLK 3 [2]: CDR/RCLK 2 [1]: CDR/RCLK 1 [0]: CDR/RCLK 0 Note: After a clear (<i>Globctrl</i> [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.

2.1.23 CDR/RCLK Loss of Activity Register Alarm Status

Table 2-24. CDR/RCLK Loss of Activity Register Alarm Status (Alarm_LOA: Address 31h)

Bits	Type	Default	Label	Description
7:4	N/A	0000b	MSPD internal	N/A
3:0	R	N/A	LOA	Latched loss of activity alarm status 1b = Alarm asserted 0b = Alarm de-asserted [3]: CDR/RCLK 3 [2]: CDR/RCLK 2 [1]: CDR/RCLK 1 [0]: CDR/RCLK 0 Note: After a clear (<i>Globctrl</i>[0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.

2.1.24 32h:VCO Trim Alarm Window

Table 2-25. VCO Trim Alarm Window Trim (Alarm_trim: Address 32h)

Bits	Type	Default	Label	Description
7:0	R	0000b	MSPD internal	Indicates that CDR N is unavailable due to VCO coarse trimming (Read only) 1b= Trim, 0b = Normal Operation [3]: CDR #3 (Mapped to Output 3) [2]: CDR #2 (Mapped to Output 2) [1]: CDR #1 (Mapped to Output 1) [0]: CDR #0 (Mapped to Output 0) Note: After a clear (<i>Globctrl</i>[0]=1), the register is cleared and 1) will latch any new alarms that makes a L to H transition and 2) set any pre-existing alarm conditions to H.

2.2 Individual Channel/CDR/RCLK Control

Multiple Instance Nomenclature

1. N = 0 for channel/CDR/RCLK 0, N = 1 for channel/CDR/RCLK 1, ..., N = 3 for channel/CDR/RCLK 3.
2. M = 4 for channel/CDR/RCLK 0, M = 5 for channel/CDR/RCLK 1, ..., M = 7 for channel/CDR/RCLK 3. For example channel/CDR/RCLK 0 starts at address 40h, channel/CDR/RCLK 1 at 50h, channel/CDR/RCLK 2 at 60h, channel/CDR/RCLK 3 at 70h.

2.2.1 M0h:CDR N Control Register A

Table 2-26. CDR N Control Register A (RCLK_ctrlA_N: Address M0h)

Bits	Type	Default	Label	Description
7	R/W	0b	Softreset	Resets an individual CDR#N (Setup registers remain unchanged, need to softreset after rate change) 0b: Normal Operation [Default] 1b: Reset Single CDR only
6	R/W	0b	force_filter_reset	Shorts the charge pump output terminals for free running VCO in the CDR (test mode) 0b: Open Circuit for Normal Operation [Default] 1b: Short Circuit for test
5	R/W	0b	inh_force	Manual Control of the Output Inhibit if Cdr_ctrlA_N[3]=0 0b: Normal operation [Default] 1b: Forced inhibit
4	R/W	0b	lol_force	Manual force LOL and Freq. Acq. only if Cdr_ctrlA_N[2]=0 0b: Force LOL=L and freq. acquisition circuit is disabled for phase lock (Default) 1b: Force LOL=H and both the phase and freq. acquisition circuit is on
3	R/W	1b	autoinh_en	Auto inhibit of the output N to logic L (output P=Low, output N=High) if CDR N has a LOL or LOS condition (or Trim Alarm) 0b: Auto Inhibit disabled, Cdr_ctrlA_N[5] determines inhibit force state 1b: Auto Inhibit enabled [Default]
2	R/W	1b	freqwin_en	Disables use of Frequency Detector for freq. acquisition 0b: Freq. Acquisition is disabled and controlled with Cdr_ctrlA_N[4] (test mode) 1b: Freq. acquisition is enabled for normal operation [Default]
1	R/W	0b	los_en	Enables the transition density based Loss of Signal Detector for Output N 0b: Disable and power down LOS circuit 1b: Enable LOS circuit [default] Note: Signal Detector is not mapped to input channel but the output channel [Delete mapping line for CDR products]
0	R/W	1b	trim_en	Enables Auto trimming of the VCO center frequency 1b: Auto Trim Enabled for Normal Operation [Default] 0b: Force Time with trim_force_N registers

Notes:

- 1: N can denote input channel #, output channel#, or CDR # depending on the context.
- 2: M is the address MSB and its N+4h.
- 3: Example: N=0h & M=4h for CDR0, N=1h & M=5h for CDR1. This implies CDR0 at Address 40h, CDR 1 at 50h, CDR 2 at 60h, ..., CDR 7 at B0h.

2.2.2 M1h:CDR/RCLK N Control Register B

Table 2-27. CDR N Control Register B (RCLK_ctrlB_N: Address M1h)

Bits	Type	Default	Label	Description
7:6	R/W	00b	CDR mode	Determines State of the PLL 00b: CDR Powered Up and Active [Default] 01b: CDR Powered Up and Bypassed 10b: CDR Powered Down (No signal through) 11b: CDR Powered Down and Bypassed
5	R/W	0b		Enables CDR to operate correctly with a 1010 pattern (100% transition density) 1b: enabled 0b: normal mode, 50% transition density expected (Default)
4	R/W	0b	Reserved	Reserved (0=Default)
3:0	R/W	0000b	data_rate	Data rate divider (DRD): This divides down the VCO frequency to the desired data rate to match input data rate. 0000b=VCO/1 [Default] 0001b=VCO/2 0010b=VCO/4 0011b=VCO/8 0100b=VCO/12 0101b=VCO/16 0110b=VCO/24 0111b=VCO/32 1000b=VCO/48 Consult VCO Fvco, max and Fvco, min to determine frequency range of each DRD ratio.

Notes:

1: N can denote input channel #, output channel#, or CDR # depending on the context.

2: M is the address MSB and its N+4h.

3: Example: N=0h & M=4h for CDR0, N=1h & M=5h for CDR1. This implies CDR0 at Address 40h, CDR 1 at 50h, CDR 2 at 60h, ..., CDR 7 at B0h.

2.2.3 CDR/RCLK N Control Register C

Table 2-28. CDR/RCLK N Control Register C (RCLK_ctrlC_N: Address M2h)

Bits	Type	Default	Label	Description
7:0	R/W	10000000b	VCO_divr	VCO comparison divider (VCD): Binary value reflects the divider ratio 1h: Minimum value (VCO /1) . . . FFh: Maximum value (VCO / 255) Note: Refer to Table 3-13 for recommended values of VCD for video data rates.

2.2.4 Output Buffer Control for CDR/RCLK N

Table 2-29. Output Buffer Control for CDR/RCLK N (*Out_ctrl_N*: Address M3h)

Bits	Type	Default	Label	Description
7:6	R/W	10b	outlvl	Determines the output swing of a data buffer for CDR/RCLK N In PCML mode: 00b: Power down 01b: 550 mV 10b: 900 mV (default) 11b: 1200 mV For LVDS, the output swing is reduced to: 00b: Power down 01b: RRL 450 mV 10b: GPL 650 mV (default) 11b: 1000 mV For PCML+, the output swing is increased to: 00b: Power down 01b: 900 mV 10b: 1200 mV (default) 11b: 1600 mV
5:4	R/W	00b	Reserved	N/A
3	R/W	0b	data_pol_flip	Flips the polarity of the output data 0b: Normal (default) 1b: Polarity flip
2	R/W	1b	dataout_en	Enables the data output driver N 1b: Data output enabled to level specified in <i>Out_ctrl_N</i> [7:6] (default) 0b: Data output disabled and powered down
1:0	R/W	00b	MSPD internal	N/A

2.2.5 Output Buffer Pre-Emphasis Control for Output N

Table 2-30. Output Buffer Pre-Emphasis Control for Output N (Preemp_ctrl_N: Address M4h)

Bits	Type	Default	Label	Description
7	R/W	0b	Reserved	Default = 0b
6:3	R/W	1000b	MSPD Internal	N/A
2:0	R/W	000b	preemph	Selects the digital pre-emphasis level 111b: 200% 110b: 150% 101b: 100% 100b: 75% 011b: 50% 010b: 37.5% 001b: 25% 000b: Pre-emphasis off (default)

2.2.6 Input Equalization Control for Output N

Table 2-31. Input Equalization Control for Output N (Ineq_ctrl_N: Address M5h)

Bits	Type	Default	Label	Description
7	R/W	0b	Reserved	N/A
6:5	R/W	00b	MSPD internal	N/A
4	R/W	0b	en_DCservo	Enables DC servo in the input channel to remove offset based deterministic jitter 0b: DC servo t_{DJ} attenuator off (default) 1b: DC servo t_{DJ} attenuator on
3	R/W	0b	MSPD internal	N/A
2:0	R/W	100b	in_eq	Selects the input equalization level 111b: Maximum input equalization level . . . 100b: Nominal input equalization level (default) . . . 001b: Minimum input equalization level 000b: Input equalization disabled Note: The 100b setting is optimized for PCB trace lengths between 10 - 46 inches, although other settings may be optimal for some applications.

2.2.7 CDR/RCLK N Loop Bandwidth and Data Sampling Point Adjust

Table 2-32. CDR/RCLK N Loop Bandwidth and Data Sampling Point Adjust (Phadj_ctrl_N: Address M6h)

Bits	Type	Default	Label	Description
7:6	R/W	10b	i_trim	Adjusts the charge-pump current; the loop bandwidth (F_{LBW}) scales proportionately 00b: 0.65x 01b: 0.8x 10b: Nominal (default) 11b: 1.15x
5:4	R/W	01b	r_sel	Adjusts the resistor of the RCLK loop filter; the loop bandwidth (F_{LBW}) scales proportionately 00b: 80% of the nominal value 01b: Nominal (default) 10b: 4x nominal value 11b: 6x nominal value
3:0	R/W	0000b	phase_adj	Adjusts the static phase offset (sampling point) of the data 1111b: -122.5 mUI 1110b: -105 mUI 1101b: 87.5 mUI 1100b: -70 mUI 1011b: -52.5 mUI 1010b: -35.0 mUI 1001b: -17.5 mUI 1000b: 0 mUI 0000b: 0 mUI (default) 0001b: 17.5 mUI 0010b: 35.0 mUI 0011b: 52.5 mUI 0100b: 70.0 mUI 0101b: 87.5 mUI 0110b: 105 mUI 0111b: 122.5 mUI

2.2.8 CDR#N LOA Window Control (trim)

Table 2-33. CDR#N LOA Window Control (trim) (LOA_ctrl_N: Address M8h)

Bits	Type	Default	Label	Description																																		
7:5	R/W	000b	tacq_LOA	Sets the value for the LOA reference window. <table><thead><tr><th>Code</th><th>Value</th></tr></thead><tbody><tr><td>000b</td><td>128 (default)</td></tr><tr><td>001b</td><td>256</td></tr><tr><td>010b</td><td>512</td></tr><tr><td>011b</td><td>1024</td></tr><tr><td>100b</td><td>2048</td></tr><tr><td>101b</td><td>4096</td></tr><tr><td>110b</td><td>8192</td></tr><tr><td>111b</td><td>16384</td></tr></tbody></table>	Code	Value	000b	128 (default)	001b	256	010b	512	011b	1024	100b	2048	101b	4096	110b	8192	111b	16384																
Code	Value																																					
000b	128 (default)																																					
001b	256																																					
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011b	1024																																					
100b	2048																																					
101b	4096																																					
110b	8192																																					
111b	16384																																					
4:1	R/W	0111b	narwin_LOA	Sets the narrow LOA window for the LOA=H to LOA=L transition (transition to valid signal). <table><thead><tr><th>Code</th><th>Value</th></tr></thead><tbody><tr><td>0000b</td><td>2</td></tr><tr><td>0001b</td><td>3</td></tr><tr><td>0010b</td><td>4</td></tr><tr><td>0011b</td><td>6</td></tr><tr><td>0100b</td><td>8</td></tr><tr><td>0101b</td><td>12</td></tr><tr><td>0110b</td><td>16</td></tr><tr><td>0111b</td><td>24 (default)</td></tr><tr><td>1000b</td><td>9</td></tr><tr><td>1001b</td><td>10</td></tr><tr><td>1010b</td><td>11</td></tr><tr><td>1011b</td><td>12</td></tr><tr><td>1100b</td><td>13</td></tr><tr><td>1101b</td><td>14</td></tr><tr><td>1110b</td><td>15</td></tr><tr><td>1111b</td><td>32</td></tr></tbody></table>	Code	Value	0000b	2	0001b	3	0010b	4	0011b	6	0100b	8	0101b	12	0110b	16	0111b	24 (default)	1000b	9	1001b	10	1010b	11	1011b	12	1100b	13	1101b	14	1110b	15	1111b	32
Code	Value																																					
0000b	2																																					
0001b	3																																					
0010b	4																																					
0011b	6																																					
0100b	8																																					
0101b	12																																					
0110b	16																																					
0111b	24 (default)																																					
1000b	9																																					
1001b	10																																					
1010b	11																																					
1011b	12																																					
1100b	13																																					
1101b	14																																					
1110b	15																																					
1111b	32																																					

Table 2-33. CDR#N LOA Window Control (trim) (LOA_ctrl_N: Address M8h)

Bits	Type	Default	Label	Description																																																			
0	R/W	0b	widwin_LOA	Sets the wide LOA window for the LOA L=H to LOL=S transition (transition to loss of activity). <table><thead><tr><th>Narrow Code</th><th>Wide Code 0b (default)</th><th>Wide Code 1b</th></tr></thead><tbody><tr><td>0000b</td><td>3</td><td>8</td></tr><tr><td>0001b</td><td>4</td><td>12</td></tr><tr><td>0010b</td><td>6</td><td>16</td></tr><tr><td>0011b</td><td>8</td><td>24</td></tr><tr><td>0100b</td><td>12</td><td>32</td></tr><tr><td>0101b</td><td>16</td><td>32</td></tr><tr><td>0110b</td><td>24</td><td>32</td></tr><tr><td>0111b</td><td>32</td><td>32</td></tr><tr><td>1000b</td><td>12</td><td>32</td></tr><tr><td>1001b</td><td>12</td><td>32</td></tr><tr><td>1010b</td><td>12</td><td>32</td></tr><tr><td>1011b</td><td>16</td><td>32</td></tr><tr><td>1100b</td><td>16</td><td>32</td></tr><tr><td>1101b</td><td>16</td><td>32</td></tr><tr><td>1110b</td><td>16</td><td>32</td></tr><tr><td>1111b</td><td>32</td><td>32</td></tr></tbody></table>	Narrow Code	Wide Code 0b (default)	Wide Code 1b	0000b	3	8	0001b	4	12	0010b	6	16	0011b	8	24	0100b	12	32	0101b	16	32	0110b	24	32	0111b	32	32	1000b	12	32	1001b	12	32	1010b	12	32	1011b	16	32	1100b	16	32	1101b	16	32	1110b	16	32	1111b	32	32
Narrow Code	Wide Code 0b (default)	Wide Code 1b																																																					
0000b	3	8																																																					
0001b	4	12																																																					
0010b	6	16																																																					
0011b	8	24																																																					
0100b	12	32																																																					
0101b	16	32																																																					
0110b	24	32																																																					
0111b	32	32																																																					
1000b	12	32																																																					
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1010b	12	32																																																					
1011b	16	32																																																					
1100b	16	32																																																					
1101b	16	32																																																					
1110b	16	32																																																					
1111b	32	32																																																					

2.2.9 CDR/RCLK N LOL Window Control

Table 2-34. CDR/RCLK N LOL Window Control (LOL_ctrl_N: Address M9h)

Bits	Type	Default	Label	Description
7:5	R/W	101b	tacq_LOL	Sets the value for the LOL reference window
				Code Value
				000b128
				001b256
				010b512
				011b1024
				100b2048
				101b4096 (default)
				110b8192
				111b16384

Table 2-34. CDR/RCLK N LOL Window Control (LOL_ctrl_N: Address M9h)

Bits	Type	Default	Label	Description		
4:1	R/W	0100b	narwin_LOL	Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold)		
				Code	Value	
				0000b	2	
				0001b	3	
				0010b	4	
				0011b	6	
				0100b	8 (default)	
				0101b	12	
				0110b	16	
				0111b	24	
				1000b	9	
				1001b	10	
				1010b	11	
				1011b	12	
				1100b	13	
				1101b	14	
				1110b	15	
1111b	32					
0	R/W	0b	widwin_LOL	Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold)		
				Narrow	Wide	Wide
				Code	Code 0b (default)	Code 1b
				0000b	3	8
				0001b	4	12
				0010b	6	16
				0011b	8	24
				0100b	12	32
				0101b	16	32
				0110b	24	32
				0111b	32	32
				1000b	12	32
				1001b	12	32
				1010b	12	32
				1011b	16	32
				1100b	16	32
				1101b	16	32
1110b	16	32				
1111b	32	32				

2.2.10 MAh: Jitter Reduction Control

Table 2-35. Jitter Reduction Control (Jitter_reduc_N: Address MAh)

Bits	Type	Default	Label	Description
7:6	R/W	01b	MSPD internal	N/A
5	R/W	0b	lowjitter	When data-rate is in the range (2.45 Gbps - 2.55 Gbps)/DRD, setting this bit to 1b will reduce output jitter (DRD is data-rate divider). 1b: When data rate is in the range (2.45 Gbps - 2.55 Gbps)/DRD 0b: When data rate is not in the range (2.45 Gbps - 2.55 Gbps)/DRD Note: This bit should be set to 1b for SONET STS-N, and Gigabit Ethernet applications.
4:0	R/W		MSPD internal	Any value may be written to this register with no effect on performance.



3.0 Functional Description

3.1 Applications

Figure 3-1. M21260 Application - Small Routing Switcher

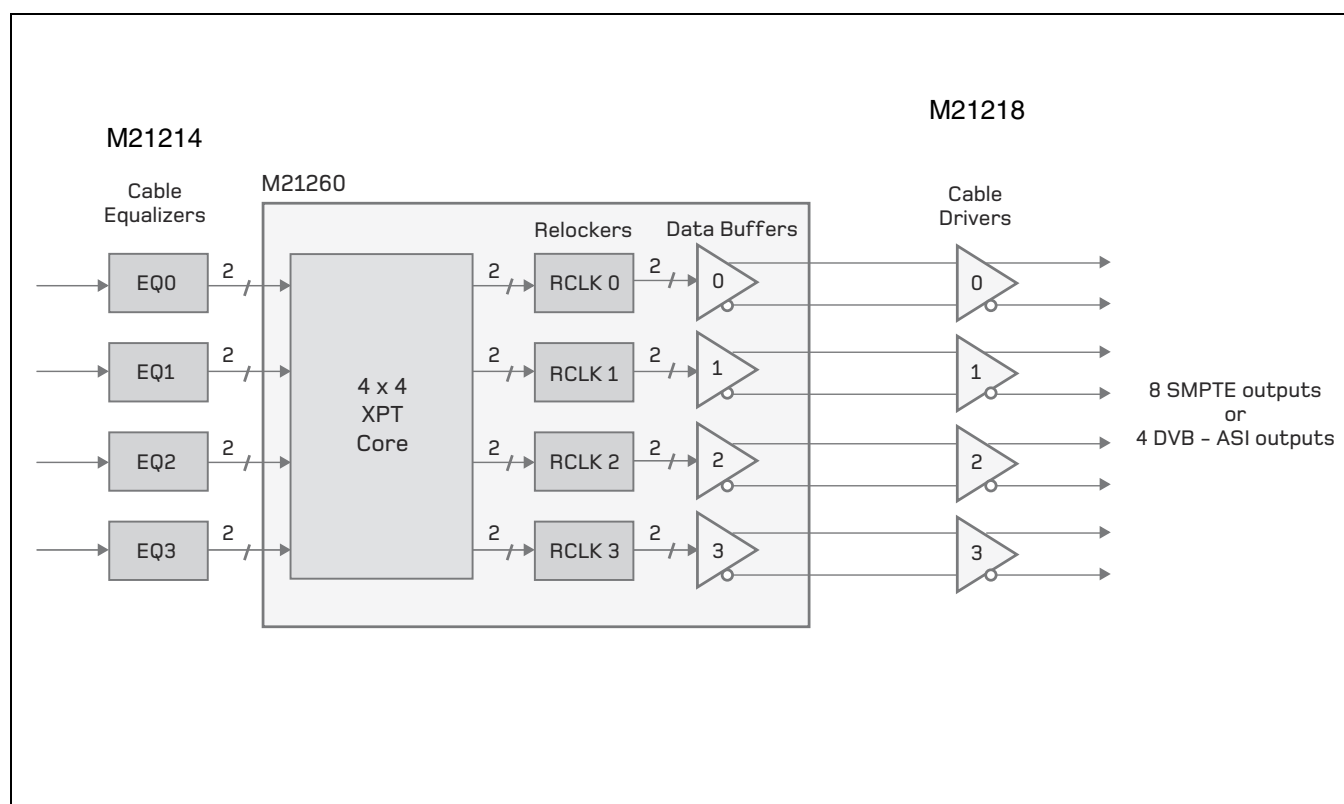


Figure 3-2. Module Application

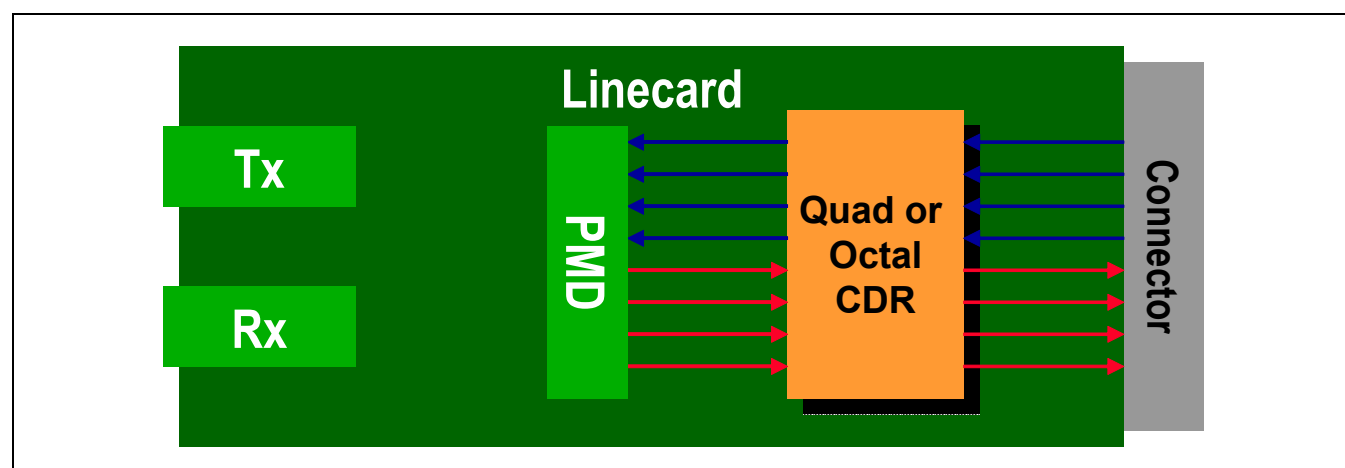


Figure 3-3. Backplane Application

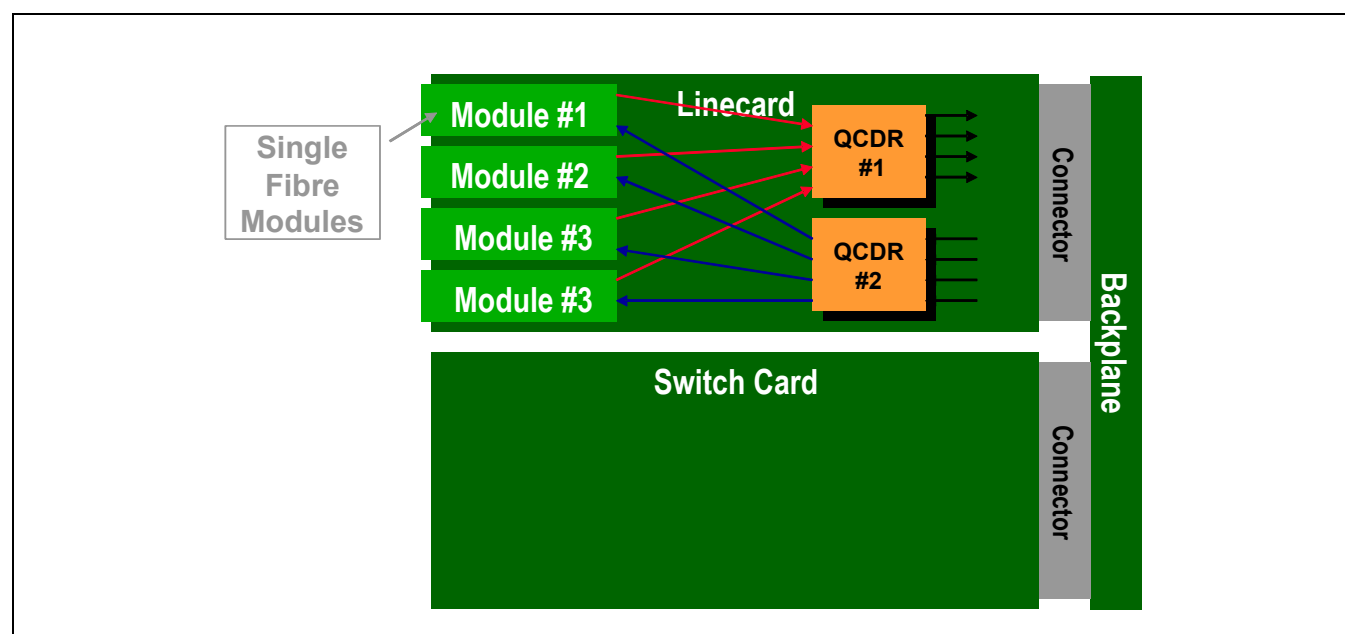
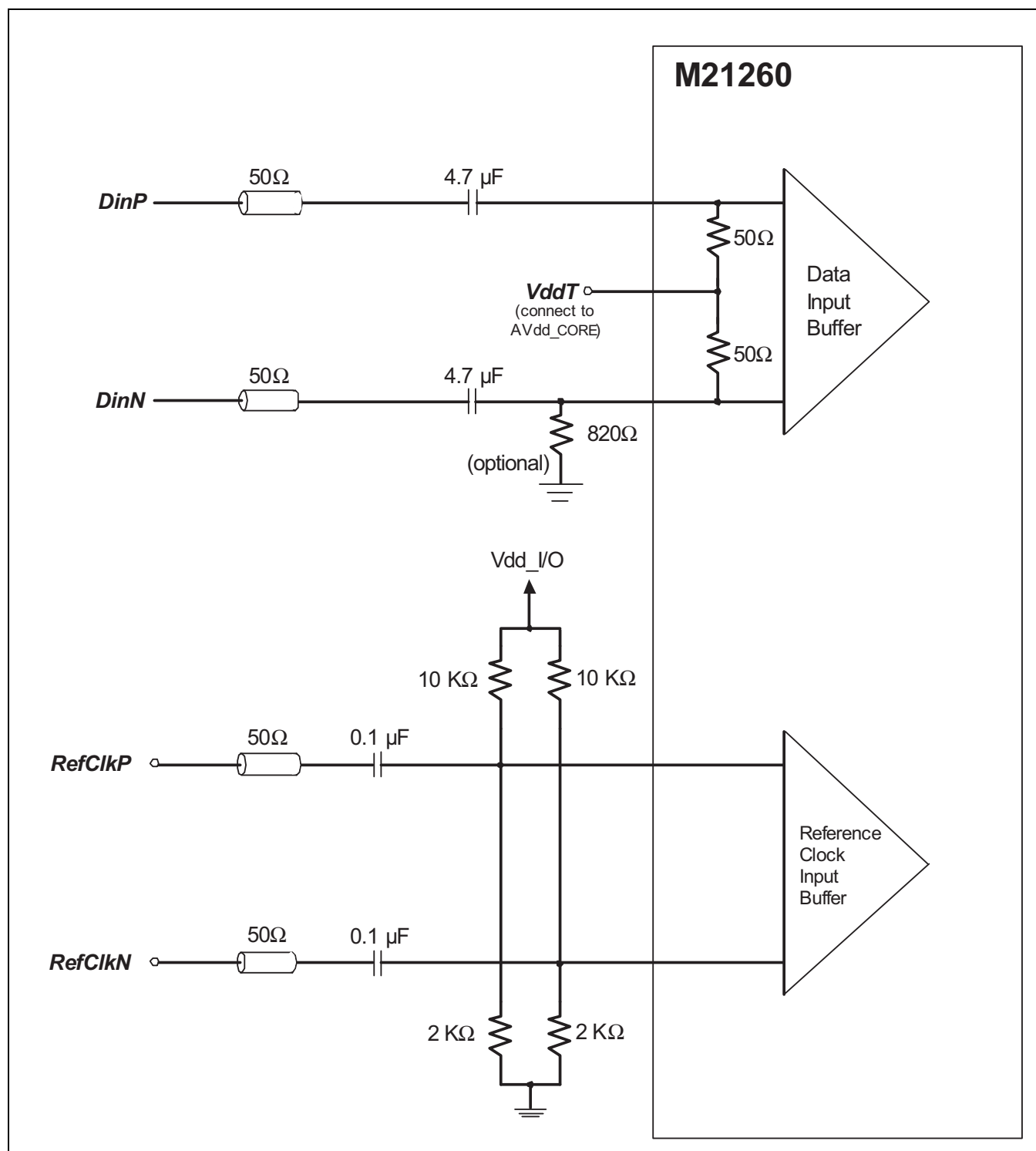


Figure 3-4. Recommended Data and Reference Clock Input Coupling Circuitry



3.2 Detailed Feature Descriptions

3.2.1 Conventions

Throughout this data sheet, physical pins will be denoted in ***bold italic*** print. An array of pins can be called by each individual pin name (e.g. ***MF0***, ***MF1***, ***MF2***, ***MF3***, and ***MF6***) or as an array (e.g. ***MF*** [6,3:0]). The M21260 control is accessed through registers that employ an 8-bit address and an 8-bit data scheme. Registers are denoted in italic print, (e.g. *TestRegister*) and individual bits within the register will be called out as *TestRegister* [4:3] to denote the 4th and 3rd bit where bit 0 is the LSB and bit 7 is the MSB. Many features of the device are bit mapped within a register; if the status of the other bits are uncertain, it is recommended that the user reads the value from the register before writing, to assure only the desired bits change. Writing in the same value to the bits within a register does not cause glitches to the unchanged features. The addresses for the registers as well as their functions can be found in detail in [Chapter 2](#). The purpose of the text description is to highlight the features of the registers. For redundant items, such as the channel number, the registers will have a nomenclature of *TestReg_0* for channel 0, *TestReg_1* for channel 1, *TestReg_2* for channel 2, *TestReg_3* for channel 3. For general reference, the text will denote such registers as *TestReg_N* where N can vary from 0 to 3. Individual RCLK circuits are mapped to output channels.

3.2.2 Reset

Upon application of power, the M21260 automatically generates a master reset. At any time, forcing ***xRST*** = L causes the M21260 to enter the master reset state. A master reset can also be initiated through the registers in the serial interface control mode by writing AAh to *Mastreset*. Once a master reset is initiated, all registers are returned to the default values, the internal state machines cleared, and all RCLK/BIST reset to the out-of-lock condition. After a reset, the register *Mastreset* will automatically return to the default value of 00h.

Each individual RCLK can be soft reset by setting *RCLK_ctrlA_N* [7] = 1 where N = 0 for RCLK 0, N = 1 for RCLK 1 and so on. The bit should be returned to 0b for normal operation. After a soft reset, the registers that determine the RCLK operation options such as data-rate, window sizes, etc., remain unchanged and only the RCLK state-machine is reset, resulting in an out-of lock condition.

3.2.3 Internal Voltage Regulator

The digital and analog core are designed to run at 1.2V, however, for operation from 1.8V to 3.3V, an internal linear regulator is provided. ***xRegu_En*** = L enables the voltage regulator which uses ***AVDDIO*** and ***DVDDIO*** to generate the required 1.2V for ***AVDDCORE*** and ***DVDDCORE***. In this mode, the ***AVDDCORE*** and ***DVDDCORE*** pins should be connected to a floating DC low inductance PCB plane and AC bypassed to ***VSS*** using standard decoupling techniques. If desired, ***AVDDCORE*** and ***DVDDCORE*** can be separated into individual planes. If 1.2V is available, it can be connected directly to ***AVDDCORE*** and ***DVDDCORE***, to save power, by bypassing the internal linear regulator with ***xRegu_En*** = H. In this case, it is recommended that the ***AVDDCORE*** and ***DVDDCORE*** pins be tied together to a common PCB plane, and bypassed to ***VSS*** with standard decoupling techniques.

3.2.4 High-Speed Input/Output Pins

The high-speed input data interface is a differential input buffer, similar to a PCML design that is referenced to ***AVDDCORE*** (1.2V). The high-speed serial differential data (42 Mbps to 1600 Mbps) enters the device via ***Din*** [3:0,P/N]. Inputs 0 and 1 are internally terminated with 50Ω to ***VddT0/1*** and inputs 2 and 3 are terminated with 50Ω to ***VddT2/3***. The ***VddT*** pins should be connected to ***AVDDCORE*** for a proper termination of the inputs. Inputs can be AC-coupled to LVPECL, LVDS, and PCML devices.

The M21260 supports multiple high-speed output modes. The output modes are selectable with hardwired pins only. The I/O interface is set with ***Out_Mode*** [1:0] and the output level with ***MF*** [9:8] as shown in [Table 3-1](#). In the

serial interface mode, the *Out_ctrl_N* [7:6] register is used to set the data level, and **Out_Mode** [1:0] is used to set the interface type. In the serial interface mode, the data output can be enabled with *Out_ctrl_N* [2] = 1b (default) and the output data polarity can be flipped by setting *Out_ctrl_N* [3] = 1b (default: no inversion). Output data polarity flip is an internal function that would have the same effect as switching the P and N terminals. The recommended AV_{DDIO} for the different output interfaces is shown in Table 3-2.

Table 3-1. Output Interface and Level Mapping (For both hardwired and software modes)

Multifunction Pins & Register MF [9:8] <i>Out_ctrl_N</i> [7:6]	PCML Mode <i>Out_Mode</i> [1:0] = 00b	LVDS Mode <i>Out_Mode</i> [1:0] = 01b	PCML+ Mode <i>Out_Mode</i> [1:0] = 11b
00b	Off	Off	Off
01b	550 mV	RRL at 450 mV	900 mV
10b	900 mV	GPL at 650 mV	1200 mV
11b	1200 mV	1000 mV	1500 mV

Table 3-2. Output Interface and Recommended AV_{DDIO} Range

Output Logic	AV_{DDIO} Range (V)
Off	1.8 - 3.3
PCML at 550 mV	1.8 - 3.3
PCML at 900 mV	1.8 - 3.3
PCML at 1200 mV	1.8 - 3.3
PCML+ at 1500 mV	1.8 - 3.3
LVDS GPL	1.8 - 3.3
LVDS RRL	1.8 - 3.3

3.2.5 Switch-State Settings

The M21260 contains a 4x4 non-blocking crosspoint switch with multicast and broadcast capabilities. The switch-state can be set in one of two modes: through the register *XPoint_ctrl* or through the hardwired pins **XPoint_Mode** [3:0].

Table 3-3 details the crosspoint configuration for each setting for the hardwired pins **XPoint_Mode** [3:0].

Table 3-3. Crosspoint Switch-State in Hardwired Mode

XPoint_Mode [3:0]	out0	out1	out2	out3
0000	in0	in1	in2	in3
0001	in1	in2	in3	in0
0010	in2	in3	in0	in1
0011	in3	in0	in1	in2
0100	in0	in0	in0	in0
0101	in1	in1	in1	in1
0110	in2	in2	in2	in2
0111	in3	in3	in3	in3
1000	in0	in0	in2	in2
1001	in2	in2	in0	in0
1010	in1	in0	in3	in2
1011	in1	in1	in3	in3
1100	in3	in3	in1	in1
1101	in3	in2	in1	in0
1110	in1	in0	in2	in3
1111	in0	in1	in3	in2

3.2.6 CDR/Reclocker Reference Frequency

An external 12 MHz reference clock is applied to **RefClk**[P/N] to enable frequency acquisition in the CDR/RCLK. PCML, LVTTTL, CMOS are examples of the wide variety of interfaces supported for the reference clock. The inputs contain a DC-coupled 100Ω differential termination between **RefClkP** and **RefClkN** along with a 100 kΩ pull-down on each terminal to **V_{SS}**. After this termination/pull-down block, the inputs are AC coupled internally. The common-mode and allowable voltage swings are specified in [Table 1-10](#). The **RefClk** common-mode must be above 250 mV, which may require external pull-ups in the case of external AC coupling.

3.2.7 Multifunction Pins Overview

The M21260 is designed to be an extremely versatile device, with many user selectable options in the CDR/RCLK and I/O to optimize performance. All of these options can be accessed and controlled through the serial interface. The serial interface I/O pins and address pins are mapped to the multifunction pins **MF** [11:0]. A subset of the key features for most applications, such as standard data-rates, I/O levels, etc., can be selected through **MF** [11:0] in the hardwired mode. The hardwired mode does not require the use of the serial interface. In this mode, upon power up (auto reset on power up), the M21260 function is determined by the status of the hardwired pins. During operation, the hardwired pins can change states, which would cause the crosspoint switch to follow with the appropriate action. Another feature of the multifunction pins is to support JTAG testing of this device during PCB manufacturing.

The various control and test modes of this device are selected with three pins: **CTRL_Mode** [1:0], and **xJTAG_En**. **xJTAG_En** = L overrides **CTRL_Mode** [1:0], and puts the device in JTAG test mode, while **xJTAG_En** = H allows **CTRL_Mode** [1:0] to determine the M21260 control mode, as summarized in [Table 3-4](#).

Table 3-4. Mode Select Pins

Pin	JTAG Test Mode	Hardwired Mode	MSPD 4-Wire Serial	I ² C-Compatible 2-Wire Serial
<i>xJTAG_En</i>	L	H	H	H
<i>CTRL_Mode</i> [1:0]	no impact	11b	00b	01b

3.2.8 Multifunction Pins Defined for Hardwired Mode

In the hardwired mode, a subset of options in the M21260 can be accessed with hardwired physical pins, as defined in Table 3-5. The hardwired bit rates along with the default reference clock frequency are shown in Table 3-5.

Table 3-5. Multifunction Pins for Hardwired Mode

Pin	Name	Function	Description
MF0	Rate_Sel_0	Data-rate selection	CDR/reclocker data-rate select ⁽¹⁾
MF1	Rate_Sel_1	Data-rate selection	CDR/reclocker data-rate select ⁽¹⁾
MF2	Rate_Sel_2	Data-rate selection	CDR/reclocker data-rate select ⁽¹⁾
MF3	Rate_Sel_3	Data-rate selection	CDR/reclocker data-rate select ⁽¹⁾
MF4	xPre_Emp_En	Pre-emphasis control	L = Pre-emphasis enable H = Pre-emphasis disable (floating default)
MF5	MSPD_Int_0	Mindspeed internal	Internal use only
MF6	MSPD_Int_1	Mindspeed internal	Internal use only
MF7	xPol_Flip_En	Data polarity flip	L = Data polarity flip H = Standard data polarity (floating default)
MF8	Out_Level_[1:0]	Output level selection	00b: All outputs disabled 01b: 550 mV CML
MF9		Output level selection	10b: 900 mV CML 11b: 1200 mV CML (floating default) See Table 3-1 for the other output interface modes.
MF10	xEQ_En	Equalization control	L = Input equalization enabled H = Input equalization disabled (floating default)
MF11	xRCLK_BYP_En	CDR/RCLK bypass control	L = All CDR/reclocker bypassed and powered down H = All CDR/reclocker enabled (floating default)
NOTE:			
1. Video rates are not supported in hardware mode.			

Table 3-6. Hardwired Data-Rates and Associated Reference Clock Frequencies

Pins <i>MF</i> [3:0]	Application	Signal Data-Rate (Mbps)	Reference Frequency (MHz)
0000	10x Fibre Channel	3187.5	159.375
0001	10 Gigabit Ethernet	3125	156.25
0010	STS-48 + FEC	2666	19.44
0011	STS-48	2488.32	19.44
0101	2x Fibre Channel	2125	106.25
0110	Gigabit Ethernet	1250	125
0111	1x Fibre Channel	1062.5	106.25
1000	STS-12	622.08	19.44
1001	STS-3	155.52	19.44
1010	STS-1	51.84	19.44
1011	ESCON	200	10
1100	FDDI	125	12.5
1101	STS-48	2488.32	155.52

Please note that it is possible to configure the device for video rates using the hardware interface, but the video patterns require additional configurations that are not available via hardware interface.

3.2.9 Multi-function Pins: Four-Wire Serial Interface

The second serial interface mode is a four-wire programming interface that has been traditionally used on MSPD earlier generation crosspoints and CDRs and is capable of higher speed operation than the two-wire interface. The interface consists of a uni-directional clock and a data input and data output line. For use with multiple ICs, a serial interface chip select pin is provided. Table 3-7 illustrates how the four-wire serial interface maps into the multi-function pins. This serial interface can operate with a maximum clock rate of 20 MHz.

Table 3-7. Multi-function Pins for Four-Wire Interface

Pin	Function	Description
<i>MF4</i>	SDI	Serial Data In
<i>MF5</i>	xCS	Chip Select, active low
<i>MF10</i>	SCLK	Clock
<i>MF11</i>	SDO	Serial Data Out

The serial I/O shifts data in from the external controller on the rising edge of **SCLK**. The serial I/O operation is gated by **xCS**. Data is shifted in on **SDI** on the falling edge of **SCLK**, and shifted out on **SDO** on the rising edge of **SCLK**. To address a register, a 10-bit input consists of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 1 for read, = 0 for write), followed by the 8-bit ADDR (MSB first) as shown in fig. 4

Figure 3-5. Serial Word Format

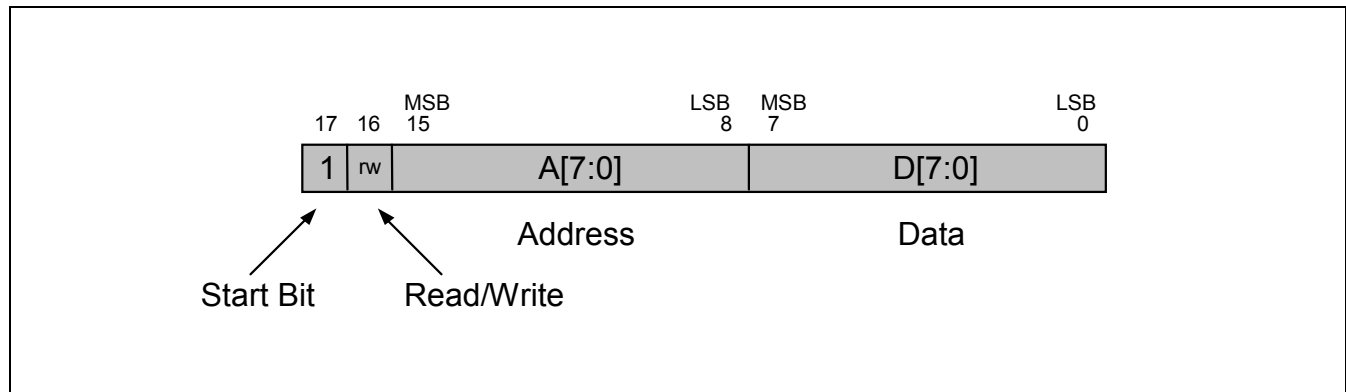


Figure 3-6 illustrates the Serial Write Mode. To initiate a Write sequence, **xCS** goes low before the falling edge of **SCLK**. On each falling edge of the clock, the 18-bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register. The rising edge of **xCS** must occur before the falling edge of **SCLK** for the last bit. Upon receipt of the last bit, one additional cycle of **SCLK** is necessary before DATA transfers from the input shift register to the addressed register. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 3-6. Serial WRITE Mode

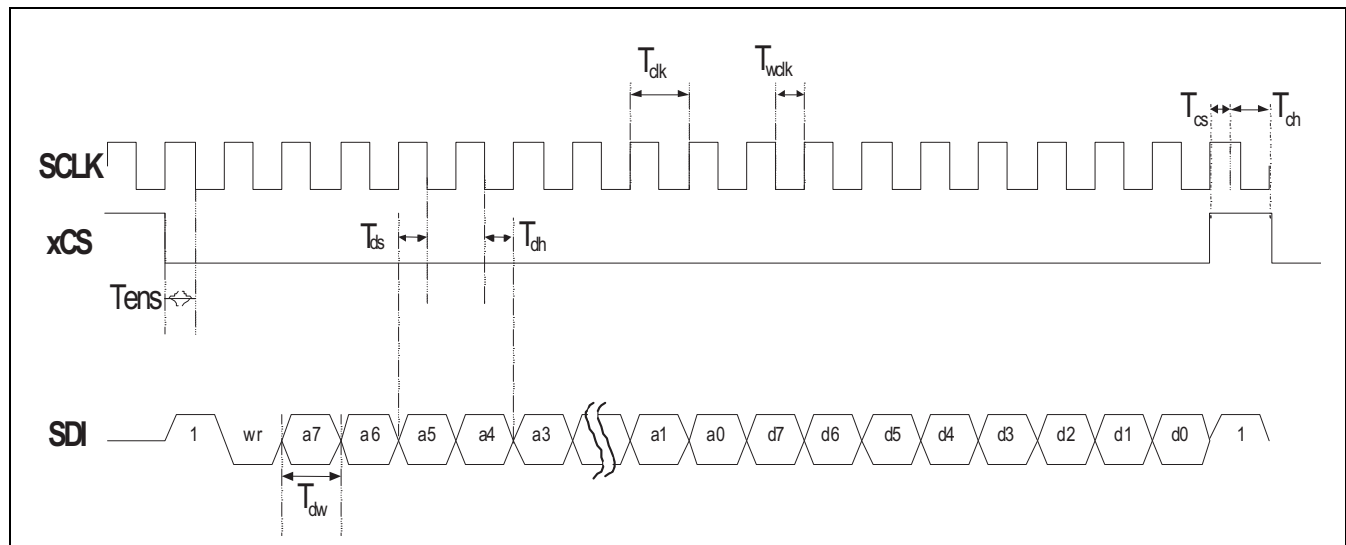
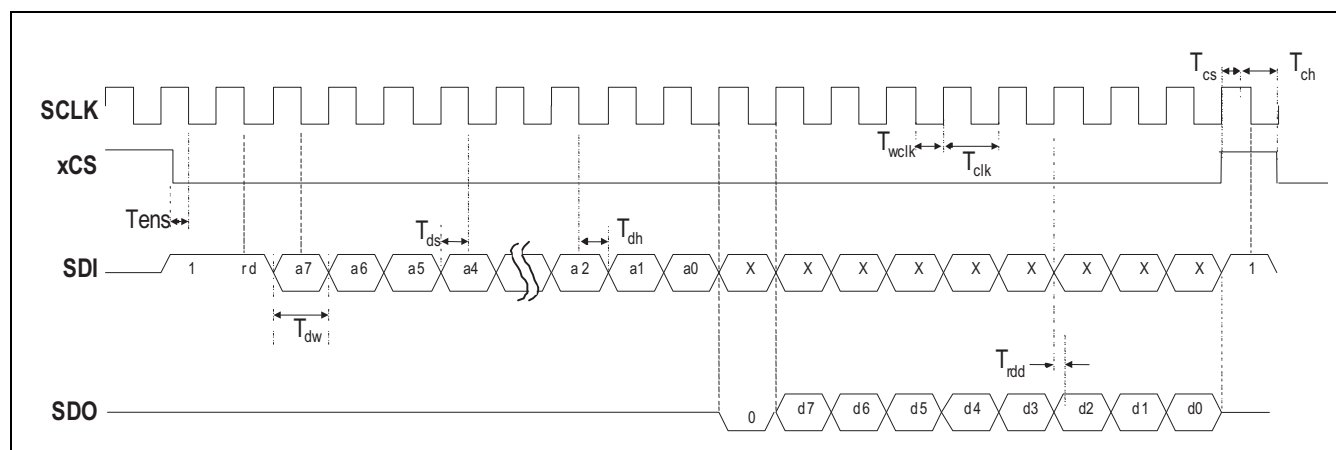


Figure 3-7 illustrates the Serial Read mode in where **xCS** goes low before the falling edge of **SCLK**. On each falling edge of **SCLK**, the 10-bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. On the next rising edge after the address LSB, the SB and 8-bits of the DATA are shifted out. The SB for a Read is always 0.

Figure 3-7. Serial READ Mode


On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 16-bits following SB and OP are used. On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of **xCS** always resets the serial operation for a new Read or Write cycle.

The timing diagrams for the serial write and read operations are shown in [Figure 3-6](#) and [Figure 3-7](#), respectively. [Figure 3-8](#) contains the specifications for the various timing parameters for the serial programming interface.

Table 3-8. Serial Interface Timing – Specified at Recommended Operating Conditions

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
t_{dw}	Data width	—	14	—	—	ns
t_{dh}	Data hold time	—	5	—	—	ns
t_{ds}	Data setup time	—	5	—	—	ns
t_{ens}	Enable setup time	—	5	—	—	ns
t_{cs}	Chip select setup time	—	2	—	$T_{clk} - 2$	ns
t_{ch}	Chip select hold time	—	2	—	—	ns
t_{rdd}	Read data output delay	—	1	—	—	ns
t_{rds}	Read data valid	—	9	—	—	ns
T_{clk}	SCLK period width	—	14	—	—	ns
t_{wclk}	SCLK minimum low duration	—	5	—	$T_{clk} - 5$	ns
t_R	Output rise time	1	1	—	4	ns
t_F	Output fall time	1	1	—	4	ns

NOTES:

- Edge rate in the high edge-rate mode.
- Designed for max serial speed of 20 MHz read/write.

3.2.10 Two-Wire Serial Interface

The two-wire serial interface is compatible with the I²C standard. The M21260 supports the read/write slave-only mode, 7-bit device address field width, and supports the standard rate of 100 Kbps, fast mode of 400 Kbps, and high-speed mode of 3.4 Mbps. The 7-bit address for the device is determined with **MF** [6:0], which allows for a maximum of 124 unique addresses for this device. The four addresses 00001xx (4, 5, 6, 7) are reserved and should not be used. SDA (**MF11**) and SCL (**MF10**) can drive a maximum of 500 pF each at the maximum rate. During the write mode from the master to the M21260, data is latched into the internal M21260 registers on the rising edge of SCL, during the acknowledge phase (ACK) of communication. [Table 3-9](#) summarizes the multifunction pins for the two-wire serial interface mode. For further information on timing, please see the I²C bus specification standard.

Table 3-9. Multifunction Pins for Two-Wire Interface

Pin	Function	Description
MF0	Address bit 0	7-bit device address; address bit 0 is LSB, address bit 6 is MSB
MF1	Address bit 1	
MF2	Address bit 2	
MF3	Address bit 3	
MF4	Address bit 4	
MF5	Address bit 5	
MF6	Address bit 6	
MF10	SCL	Clock input
MF11	SDA	Data input/output

3.2.11 JTAG

The M21260 supports JTAG external boundary scan, which includes all of the high-speed I/O, as well as the traditional digital I/O. [Table 3-10](#) shows the multifunction pins signal mapping for JTAG testing.

Table 3-10. Multifunction Pins for JTAG

Pin	Function	Description
MF8	TMS	Test select
MF9	TDI	Test data input
MF10	TCK	Test clock
MF11	TDO	Test data output

3.2.12 Input Deterministic Jitter Attenuators

Each of the four input channels contains an independent input equalizer (IE). For the IE, the address N is mapped to the input channel. In the hardwired mode, there is the option to set input equalization on or off. In the two-wire serial interface control mode, the default state allows for configurable input equalization settings using *Ineq_ctrl_N* [2:0], for which the setting of 100b is optimized for trace lengths between 10 - 46 inches.

The input equalization settings have been optimized for a variety of backplane and connectivity applications, such as board traces and cables. For board traces on FR4, such as the Tyco Electronics Hm-Zd legacy backplane, the input equalizer can drive trace-lengths of up to 60" at 3.1875 Gbps, and up to 72" at 2.125 Gbps. The equalizer has

similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The input equalizer was designed to compensate for the deterministic jitter accumulation effects of typical backplane interconnects, which have bandwidths of hundreds of MHz to a few GHz. The equalizers are not expected to make a significant difference in performance with signal data-rates less than 1 Gbps.

Another component of input deterministic jitter is inter-symbol interference (ISI) due to DC offsets. By default, a DC servo-like circuit is enabled to correct for this type of deterministic jitter, and can be disabled by setting *Ineq_ctrl_N* [4] = 0b. The DC servo can also be used to track changes in the common mode, for single-ended operation.

Figure 3-8. STS-48 waveform after transmission through 76" of PCB traces (input to M21260)

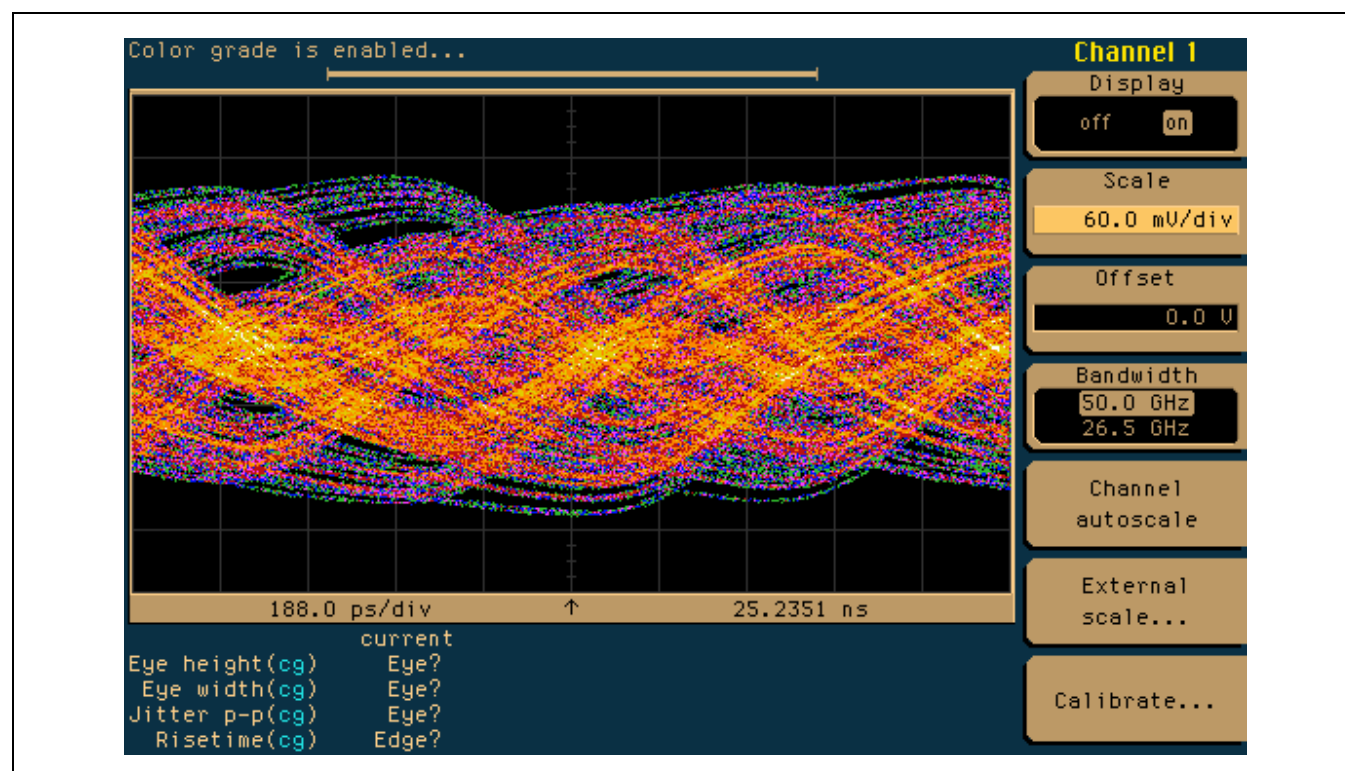
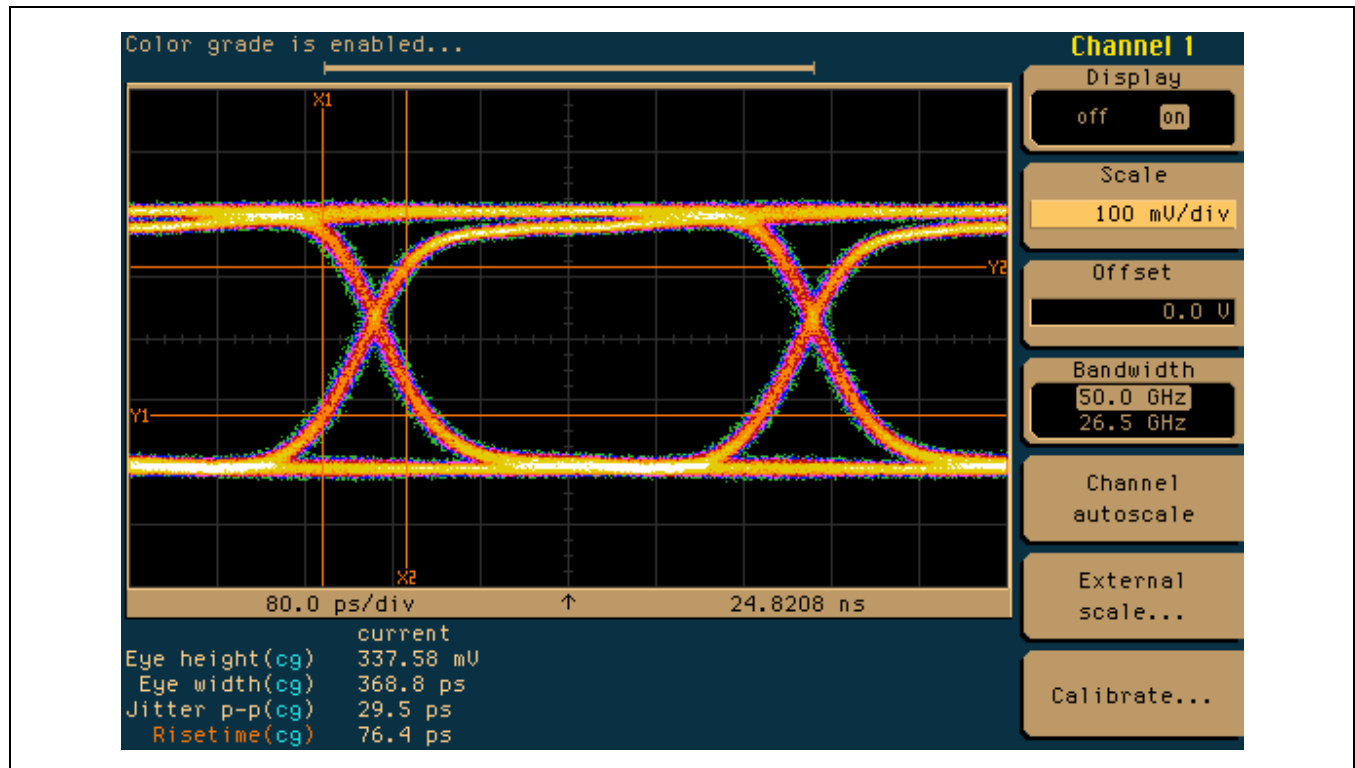


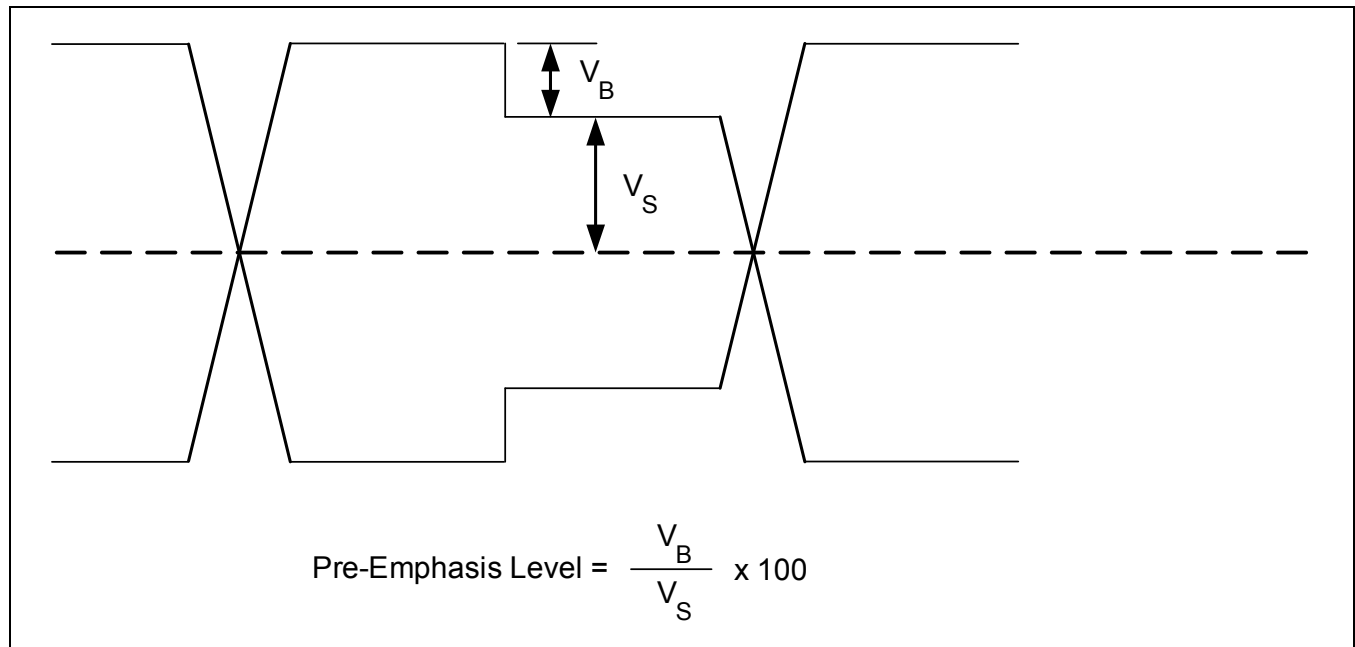
Figure 3-9. STS-48 waveform at M21260 output with input shown in Figure 3-7



3.2.13 Output Pre-Emphasis

Each of the four output channels contains an independent output pre-emphasis circuit that can be used to select the optimal pre-emphasis level. The pre-emphasis settings have been optimized for a variety of backplane PCB applications. For board traces on FR4, the pre-emphasis circuit can drive trace-lengths up to 60" at 1.6 Gbps. Like the input equalizer settings, the output pre-emphasis circuit has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The digital pre-emphasis level is selected, for each output channel, with *Preemp_ctrl_N* [2:0], and the default value of 000b corresponds to pre-emphasis disabled. The pre-emphasis circuit tracks the signal data-rate throughout the multi-rate range, however, like the input equalizer, it is designed to compensate for the bandwidth limitations of the interconnect, and may not have the desired effects at the low end of the multi-rate range. When the RCLKs have been disabled or bypassed, analog pre-emphasis must be used in place of digital pre-emphasis. Writing the data value 1b to the register *Preemp_ctrl_N* [3] enables analog pre-emphasis, whereas writing the data value 0b to the register *Preemp_ctrl_N* [3] enables digital pre-emphasis. Once analog pre-emphasis has been enabled, the boost level may be chosen with *Preemp_ctrl_N* [5:4], and the bandwidth may be chosen with *Preemp_ctrl_N* [6]. The output pre-emphasis function is available for all data interfaces and levels.

Figure 3-10. Definition of Pre-Emphasis Levels



3.2.14 CDR/RCLK Overview

The M21260 contains 4 multi-rate CDR/RCLKs, that can each operate at independent bit rates. When the CDR/RCLK achieves phase lock onto the incoming data stream, it removes the incoming random jitter above its loop bandwidth. The M21260 output data has extremely low jitter, due to retiming with a very low jitter generation CDR/RCLK. Clock outputs are also provided, but are disabled by default.

Each CDR/RCLK is capable of multi-rate operation which is achieved by a combination of built in VCO frequency dividers (VCD), Data Rate Dividers (DRD), and a wide VCO tuning range ($F_{\min}=2.0$ GHz, $F_{\max} = 3.2$ GHz). As a result, the allowed input data range is $F_{\min} / \text{DRD}_{\max}$ to $F_{\max} / \text{DRD}_{\min}$. Although the ranges are not continuous, the ranges are deliberately chosen to cover all typical applications.

By default, the loop-bandwidth is set to pass 3G-SDI Video and SONET STS-48 specifications, with less than 0.1 dB of bandwidth peaking. Within a given VCO frequency range, the bandwidth will scale proportionately. For example, if the loop bandwidth (LBW) is 1.19 MHz at 1.485 GHz, then at 2.97 GHz the LBW will be 2.38 MHz, and peaking will be less than 0.1 dB. When DRD is not equal to 1, the bandwidth at $\text{DRD}=1$ scales by the DRD divide ratio. For example, if the LBW is 2.38 MHz at 3G-SDI with $\text{DRD}=1$, then if $\text{DRD}= 2$ for HD operation, the LBW will be 1.19 MHz. In general, the default bandwidth will meet SMPTE specifications for all bit rates down to 143 MHz. Internal filter components assure that the peaking will not exceed 0.1 dB for all DRDs up to 16. In the hardwired mode, the LBW will be properly set for the hardwired bit rates. In the serial register mode, the default bandwidth scales automatically with the input bit rate, and the bandwidth can be tuned through registers.

The CDR/RCLK requires an external reference clock to be connected to the **RefClkP/N** pins. The CDR/RCLK contains an internal frequency pre-scaler that allows a single reference to be used for multiple bit rates and thereby ease the burden of having to route and switch multiple frequency references.

Frequency acquisition is accomplished with two key sections. The first section is a secondary phase/frequency lock loop (P/FLL) that drives the VCO towards the desired frequency. The second section is the loss-of-lock circuitry (LOLCir), that turns on or off the secondary P/FLL. In general LOL has register bits (*Alarm_LOL*) which are active high, and pins (**xLOL**[3:0]) which are active low, for wired OR use to be wired OR externally. In the general context, they will be referred to as LOL which is active H. With both methods, frequency acquisition takes place when the

LOLCir determines an out of lock condition (LOL=H) for each CDR/RCLK, when the VCO frequency exceeds a given range (window). LOLCir enables the secondary P/FLL to drive the VCO close to the desired frequency (the input data bit rate). When the VCO falls within a given frequency range where the CDR/RCLK loop can acquire phase lock, LOLCir turns off the secondary P/FLL and sets LOL=L, allowing the CDR/RCLK to achieve phase lock. During this time, LOLCir continues to monitor the frequency difference and will signal a LOL=H to start the acquisition routine again; if the frequency falls out of range. The LOLCir range is fixed in hardwired mode, and programmable in 2-wire or 4-wire serial interface mode. In general, the frequency threshold (window) for LOL=H-to-L and LOL=L-to-H are different to prevent LOL from toggling when the frequency is near one of the windows. These registers also control the frequency acquisition time. Suggested values are given in this document for general robust operation, and are used as register defaults, however, the programmability of the registers allow for optimization based on a given application (e.g. faster lock times).

3.2.15 General CDR/RCLK Features

All of the CDR/RCLKs are reset upon **xRST=L**, **Mastreset=AAh**, or upon power up. A soft reset through **RCLK_ctrlA_N[3]=1b** resets the individual CDR/RCLK state machine, and presets the CDR/RCLK to an out-of-lock condition, however, the register contents that are related to CDR/RCLK setup are unchanged. It is required to force a soft-reset if the bit rate is dynamically changed. The soft reset register bit needs to be cleared for proper operation. In general, a reset during operation will cause bit errors, until the CDR/RCLK achieves phase lock.

By default, all of the CDR/RCLKs are active and powered up for normal operation. By setting **RCLK_ctrlB_N[7:6]=11b**, a CDR/RCLK can be bypassed and powered down, to allow for non-standard bit rates, or to save power when the CDR/RCLK is not required at lower bit rates. When **RCLK_ctrlB_N[7:6]=01b**, the CDR/RCLK is bypassed so the output data is not retimed but active (VCO locked to the input data). In the last mode with **RCLK_ctrlB_N[7:6]=10b**, the CDR/RCLK is powered down, and all signals along the input and output paths are also powered down, to save power. In this case, the input data does not reach the output.

To prevent the propagation of noise in the case where there is a LOL condition, the CDR/RCLK contains an auto-inhibit feature, which is enabled by default. When LOL is active, the output of the CDR/RCLK is fixed at a logic high state (**DoutP=H**, **DoutN=L**). This feature can be disabled by setting **RCLK_ctrlA_N[3]=0b**, which allows **RCLK_ctrlA_N[5]** to either force an inhibit (1b) or to never inhibit (0b).

In some applications, the optimal data sampling point is not in the middle of the data eye. By default, the RCLK achieves phase lock very near the center of the eye. For optimal performance (jitter tolerance), the actual sampling point can be adjusted with **Phadj_ctrl_N[3:0]**. The adjustment range is from -122.5 mUI to +122.5 mUI with 17.5 mUI steps.

3.2.16 Multi-Rate CDR Data-Rate Selection

For multi-rate operation, the first step is to determine the desired data-rate range. The input data range must be bracketed by $DF_{min} = F_{vco,min}/DRD_{max}$ to $DF_{max} = F_{vco,max}/DRD_{min}$. $DF_{max/min}$ are the maximum/minimum input data-rate frequencies, $DRD_{max/min}$ are the maximum/minimum data-rate divider settings using **CDR_ctrlB_N [3:0]**, and $F_{vco,min}/F_{vco,max}$ are the minimum/maximum VCO frequencies, which are 2.0 GHz and 3.2 GHz respectively. The valid data-rates are shown in [Table 3-11](#).

Table 3-11. Valid Input Data Ranges

Parameter	DF _{min}	DF _{max}	Units
Data-rate divider (DRD = 1): <i>CDR_ctrlB_N</i> [3:0] = 0000b	2.0	3.2	GHz
Data-rate divider (DRD = 2): <i>CDR_ctrlB_N</i> [3:0] = 0001b	1.0	1.6	GHz
Data-rate divider (DRD = 4): <i>CDR_ctrlB_N</i> [3:0] = 0010b	500	800	MHz
Data-rate divider (DRD = 8): <i>CDR_ctrlB_N</i> [3:0] = 0011b	250	400	MHz
Data-rate divider (DRD = 12): <i>CDR_ctrlB_N</i> [3:0] = 0100b	166.7	266.66	MHz
Data-rate divider (DRD = 16): <i>CDR_ctrlB_N</i> [3:0] = 0101b	125	200	MHz
Data-rate divider (DRD = 24): <i>CDR_ctrlB_N</i> [3:0] = 0110b	83.33	133.33	MHz
Data-rate divider (DRD = 32): <i>CDR_ctrlB_N</i> [3:0] = 0111b	62.5	100	MHz
Data-rate divider (DRD = 48): <i>CDR_ctrlB_N</i> [3:0] = 1000b	42	66.66	MHz

It is important to note the difference between the VCO frequency (F_{VCO}), and the data-rate frequency (DF). F_{VCO} is always between 2 GHz to 3.2 GHz, while DF is the divided down F_{VCO} that matches the input data-rate.

3.2.17 Frequency Acquisition

Frequency acquisition is enabled by the LOLCir when LOL = H (*Alarm_LOL* = H or *xLOL* = L). A secondary FLL attempts to lock the VCO to a frequency derived from the external reference. When the frequency is close to the desired frequency, LOLCir sets LOL = L and disables the secondary FLL, thus, the main CDR/RCLK PLL is free to phase lock to the incoming data. Although the main CDR/RCLK PLL can achieve frequency lock, the VCO frequency tuning range typically exceeds the CDR/RCLK PLL inherent acquisition range. This implies that the FLL needs to get the VCO within the CDR/RCLK PLL range. The loss of lock circuitry (LOLCir) is used to determine when the secondary FLL is active. The LOLCir consists of window detectors that constantly compare a scaled VCO frequency, to a frequency related to the external reference. When LOL = H the loop is out of lock, the FLL is activated until the frequency difference is within the narrow reference window (N_{NARROW}). When LOL = L, the FLL is not engaged until the frequency exceeds the wide reference window (N_{WIDE}). If a signal is not present, the FLL circuit will drive the VCO frequency to the N_{NARROW} and turn off. Without data present, the VCO would then drift until the frequency difference exceeds the N_{WIDE} , and repeat this cycle. To prevent this, by default, the FLL is activated with LOL = H and de-activated with LOL = L.

The diagram illustrates the PLL architecture with the following components and connections:

- VCO (Voltage-Controlled Oscillator):** Receives $F_{vco,max}$ and $F_{vco,min}$ as inputs. Its output F_{vco} is split to feed the DRD, VCD, and LOLCir blocks.
- DRD (Digital Reference Divider):** Receives F_{vco} and outputs F_{CLK} to the CDR block. It is controlled by $CDR_ctrlB [3:0]$.
- VCD (Voltage-Controlled Divider):** Receives F_{vco} and outputs iFV to the FLL block. It is controlled by $CDR_ctrlC [7:0]$.
- RFD (Reference Frequency Divider):** Receives $RefClk$ and outputs iFR to the FLL block. It is controlled by $Refclk_ctrl [3:1]$.
- LOLCir (Loop Filter):** Receives F_{vco} and iFR as inputs. Its output is fed back to the VCO and also branches to feed the CDR and FLL blocks.
- CDR (Charge Pump and Divider):** Receives D_{in} and F_{CLK} as inputs. It outputs D_{out} , C_{out} , and an Error signal.
- FLL (Frequency-Locked Loop):** Receives iFV and iFR as inputs. It outputs an Error signal.
- Feedback and Control:** The Error signals from both the CDR and FLL are combined and fed back to the VCO. The LOLCir block also receives a LOA (Loop Offset Adjustment) input.

Table 3-12. Reference Clock Frequency Ranges

RFD Value	Minimum F _{REF} (MHz)	Maximum F _{REF} (MHz)
RFD (<i>Refclk_ctrl</i> [3:1] = 000b): divide by 1	10	25
RFD (<i>Refclk_ctrl</i> [3:1] = 001b): divide by 2	20	50
RFD (<i>Refclk_ctrl</i> [3:1] = 010b): divide by 4	40	100
RFD (<i>Refclk_ctrl</i> [3:1] = 011b): divide by 8	80	200
RFD (<i>Refclk_ctrl</i> [3:1] = 100b): divide by 12	120	300
RFD (<i>Refclk_ctrl</i> [3:1] = 101b): divide by 16	160	400
RFD (<i>Refclk_ctrl</i> [3:1] = 110b): divide by 32	320	800

For applications that only deal with SDI data rates, a 12 MHz reference clock frequency is recommended.

Table 3-13. DRD/RFD/VCD Settings for Different Data-Rates and Reference Frequencies (1 of 2)

Application	DR (Mbps)	F _{REF} (MHz)	DRD	RFD	VCD	Notes
SD-143	143	12	5	—	191	
SD-177	177	12	4	—	177	
SD-270	270	12	3	—	180	
SD-360	360	12	3	—	240	
SD	540	12	2	—	180	
HD	1483.5/1485	12	1	—	247	
3G	2967/2970	12	0	—	247	
10GE - XAUI	3125	156.25	1	8	160	
10GE-XAUI	3125	25	1	2	250	
10GFC - XAUI	3187.5	159.375	1	8	160	
10GFC-XAUI	3187.5	25	1	2	255	1
STS-48+FEC	2666.06	19.44	1	1	137	1
STS-48 + FEC	2666.06	25	1	2	213	1
STS-48	2488.32	155.52	1	8	128	
STS-48	2488.32	19.44	1	1	128	
STS-48	2488.32	25	1	2	199	1
2GFC	2125	106.25	1	8	160	
2GFC	2125	25	1	2	170	
GE	1250	125	2	8	160	
GE	1250	25	2	2	200	
FC	1062.5	106.25	2	8	160	
FC	1062.5	25	2	2	170	1
STS-12	622.08	19.44	4	1	128	
STS-12	622.08	25	4	2	199	1
FC	531	25	4	2	170	1
FC	266	25	12	2	255	1
ESCON	200	10	12	1	240	
ESCON	200	25	12	2	192	
STS-3	155.52	19.44	16	1	128	
STS-3	155.52	25	16	2	199	1
FC	133	25	24	2	255	1
FE	125	12.5	16	1	160	
FE	125	25	24	2	240	
STS-1	51.84	25	48	2	199	1

Table 3-13. DRD/RFD/VCD Settings for Different Data-Rates and Reference Frequencies (2 of 2)

Application	DR (Mbps)	F _{REF} (MHz)	DRD	RFD	VCD	Notes
STS-1	51.84	19.44	48	1	128	1
DS3	44.736	25	48	2	172	1
NOTES: 1. Set <i>LOL_ctrl_N</i> [0] = 1b, all other bits at default values.						

The FLL drives the iFV to iFR, and it is the primary function of the LOLCir to determine when to turn off the FLL, so the CDR/RCLK can achieve phase lock. The LOLCir uses the frequency difference between iFV and iFR to switch LOL, which turns on and off the secondary FLL. The thresholds where LOL makes a transition are defined as windows. These windows are fixed in the hardwired mode, and programmable in the two-wire interface mode. To prevent LOL from toggling at the thresholds, two windows are used for hysteresis. When LOL = L and the frequency difference exceeds the larger window (N_{WIDE}), LOL L-to-H occurs to signal an out of lock case. When LOL = H (and LOA = L), the frequency difference is brought within the narrow reference window (N_{NARROW}), after which LOL makes a H-to-L transition signaling in-lock. If LOA = H when LOL = L, the FLL remains on to keep the VCO locked to the reference, until a signal is present. N_{ACQ} is defined with *LOL_ctrl_N* [7:5], N_{NARROW} is defined with *LOL_ctrl_N* [4:1], and N_{WIDE} is defined with *LOL_ctrl_N* [0]. The LOLCir averages a large number of transitions before making an LOL decision. This averaging time is referred to as the LOL decision time or DT_{LOL}.

Table 3-14 shows various window sizes for different applications, including the default value in both the hardwired and two-wire serial interface modes.

Table 3-14. LOL Window Size and Decision Time Examples

Condition	N _{ACQ}	N _{NARROW}	N _{WIDE}	Narrow Window (ppm)	Wide Window (ppm)	Decision Time (μs)
Hardwired mode default	101b	0100b	0b	±1955	±2930	420
Two-wire serial interface mode default	101b	0100b	0b	±1955	±2930	420
iFV = iFR	111b	0010b	1b	±245	±975	1685
Fast lock	010b	0001b	0b	±5860	±7800	56
NOTES: 1. Decision time is calculated with iFR = 19.44 MHz; will scale proportionally with iFR range from 10 to 25 MHz. 2. Above are examples showing ability to tailor windows for data-rates, reference frequencies, and acquisition times.						

3.2.18 CDR/Reclocker Data Rate Programming (3G/HD/SD-SDI data rates only)

If the automatic rate detection (ARD) algorithm developed by Mindspeed is used, it is not necessary for the user to manually program the registers of the reclockers to configure the reclockers for operation at a specific data rate. In applications where the ARD is not implemented and the device is used with software control, there are a few parameters that must be configured for the reclocker to correctly lock to the input data. The parameters that need to be programmed are the data rate divider (DRD) and the VCO frequency divider (VCD). The DRD is programmed using bits [3:0] of register addresses 41h, 51h, 61h, and 71h. The VCD is programmed using bits [7:0] of register addresses 42h, 52h, 62h, and 72h. Table 3-13 shows the recommended values of DRD and VCD for standard video data rates.

3.2.19 Ambient Temperature Range Limitations

Table 3-15 summarizes the supported ambient temperature range as a function of data-rate, and indicates when it is required to center the VCO.

Table 3-15. Supported Ambient Temperature Range by Data-Rate

F _{VCO} (GHz)	DR (Gbps)	T _a (°C)	VCO Centering Requirement
2.0 - 2.666	2.0/DRD - 2.666/DRD	-40 - 85	N
2.7 - 2.97	2.7/DRD - 2.97/DRD	0 - 70	N
2.7 - 2.97	2.7/DRD - 2.97/DRD	-40 - 85	Y
3.0 - 3.2	3.0/DRD - 3.2/DRD	0 - 70	Y

F_{VCO} is the VCO frequency, which always lies in the range 2.0 - 3.2 GHz. DR is the data-rate of the input signal, and DRD is the data-rate divider (1, 2, 4, 8, 12, 16, 24, 32, 48) set with *rclk_ctrlB_N*[3:0]. T_a is the ambient temperature supported, which decreases for F_{VCO} > 2.666 GHz. As an example, if the data-rate is 800 Mbps DRD should be set to 4; to lock to this signal the VCO needs to operate at 3.2 GHz. Under these conditions the ambient temperature range supported is 0°C - 70°C, and it is necessary to center the VCO in each of the four lanes.

The VCO tuning range is roughly the same bandwidth as the variation in VCO center frequency between the extremes of the operating temperature range. This issue can be resolved by centering the VCO frequency during the in-circuit testing (ICT) phase prior to shipment of the customer systems.

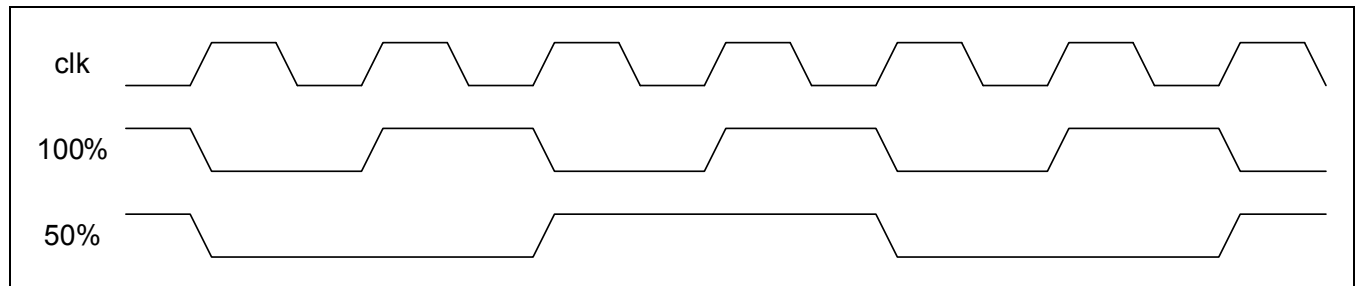
NOTE: The CDR/RCLK must be powered up and configured at 25°C - 40°C ambient temperature during ICT.

1. Power up the device and configure the registers via the serial interface with the appropriate settings for the application of interest.
2. Read and store the VCO trim code from register MBh[4:0].
3. Every time the device is powered up, this trim code must be forced by setting M0h[0] = 0b then writing the code to MAh[4:0]. This can be done during the same write cycle as when the other registers are configured.

It should be noted that it is not possible to center the VCO in the hardwired mode, it is necessary to program the CDR/RCLK using the serial interface.

3.2.20 Loss of Activity

By default, the LOA detector is disabled and can be enabled by setting *CDR_ctrlA_N*[1] = 1b, where N is the channel number. Loss of activity measures the transition density of data to determine if the data is valid. With PRBS data, the transition density is typically 50%+1-12%, averaged over long periods. During small time intervals, data transition density variations are due to data content, packet headers, stress patterns, etc. In some applications, when data is not present, noise produces rail-to-rail transitions that cause problems with level based detectors. These applications include cascaded reclockers, high-gain crosspoints, and other devices. The data transition density based LOA detector can separate data from random noise, determine false lock at the wrong integer and non-integer data-rate, signal stuck high/low conditions, and determine false lock to re-timed noise. Unlike level based detectors, it cannot determine false lock with low amplitude data. Data patterns that have periods of high or low transitions density will cause the LOA alarm to trigger. In these cases, additional filtering of the LOA is needed to ensure correct reading of the LOA.

Figure 3-12.

Common protocols that require additional filtering:

- Video SDI
- 8b/10b

3.2.21 Built-In Self Test (BIST) Overview

The M21260 contains a BIST test pattern generator as well as a test pattern receiver. Both the BIST transmitter (BIST Tx), and BIST receiver (BIST Rx) are designed to operate with fixed patterns. For PRBS evaluation, the PRBS 2^7-1 , $2^{15}-1$, $2^{23}-1$, and $2^{31}-1$ test patterns are provided. For 8b/10b testing, the fibre channel CRPAT and CJTPAT standard patterns are supported. In addition, an 8b/10b countdown pattern is also provided; this is the 8b/10b representation of a binary count from 255 to 0, while maintaining 8b/10b running disparity requirements. User programmable 16 bit (PRBS) and 20 bit (8b/10b) patterns are also provided; they are typically used to generate short patterns for debug, such as 1100b, as well as 8b/10b idle or control characters. The BIST is designed to reduce system development time, as well as product test costs, and can be used by both the equipment provider as well as the equipment end user.

When enabled, the BIST Rx allows one input from the crosspoint switch to enter the BIST receiver. The desired channel to monitor is selected through a control register. The BIST Rx uses the recovered clock and data from the selected RCLK to drive the pattern checker. Every time a bit error is received, the error register is incremented. The maximum number of errors is FFh, and all subsequent errors will not be counted. At any time, the error register can be cleared. By keeping track of the time between a clear and a read, a rough BER number can be obtained.

When enabled, the BIST Tx can broadcast the output test pattern to output channels 0 and 1 (the BIST Tx and Rx can be used at the same time). The BIST Tx contains an internal clock multiplier (PLL), that can take its input from either the external reference frequency, or from the same RCLK that is driving the BIST Rx (only in full-rate mode, DRD = 1).

3.2.22 BIST Test Patterns

The test pattern is selected with *BISTtx_ctrl* [5:2] for the transmitter, and *BISTrx_ctrl* [5:2] for the receiver.

The PRBS patterns generated by the unit are ITU-T 0.151 compliant, and summarized in the table below.

Table 3-16. BIST PRBS Patterns

<i>BISTtx_ctrl</i> [5:2] / <i>BISTrx_ctrl</i> [5:2]	Pattern	Polynomial
0000b	PRBS 2^7-1	2^7+2^6+1
0001b	PRBS $2^{15}-1$	$2^{15}+2^{14}+1$
0010b	PRBS $2^{23}-1$	$2^{23}+2^{18}+1$
0011b	PRBS $2^{31}-1$	$2^{31}+2^{28}+1$

For 8b/10b data, three patterns are available. The CJTPAT and CRPAT comply with the Fibre Channel T11.2/Project 1230/Rev10 specifications.

Table 3-17. BIST 8b/10b Patterns

<i>BISTtx_ctrl</i> [5:2] / <i>BISTrx_ctrl</i> [5:2]	Pattern
0100b	CJTPAT
0101b	CRPAT
0110b	Countdown

Two user programmable patterns that are 16 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 0111b) and 20 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 1000b) are determined with *BIST_pattern0*, *BIST_pattern1*, *BIST_pattern2*. Note that the contents of these registers is used by both the BIST Tx and the BIST Rx, if they are setup in this mode.

3.2.23 BIST Receiver (BIST Rx) Operation

The BIST Rx is enabled and powered up by setting *BISTrx_ctrl* [1] = 1b (off by default), resetting the BIST Rx block with *BISTrx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTrx_ctrl* [5:2]. The signal to the BIST Rx is routed from the input of the device, and the BIST Rx can only check one channel at a time. The desired channel to monitor is selected with *BISTrx_chsel* [2:0]. The BIST Rx uses the recovered clock from the RCLK to drive the BIST state-machine, thus the RCLK must be enabled and locked to data for proper operation. When the data is valid, *BISTrx_ctrl* [6] = 1b is used to clear the error register, and all subsequent errors can be read back through *BISTrx_error*. The BIST Rx automatically synchronizes the input data with the pattern.

3.2.24 BIST Transmitter (BIST Tx) Operation

The BIST Tx is enabled and powered up by setting *BISTtx_ctrl* [1] = 1b (off by default), resetting the BIST Tx block with *BISTtx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTtx_ctrl* [5:2]. The BIST Tx can multicast the test pattern to any channels selected with *BISTtx_chsel* [3:0]. The high-speed clock of the BIST Tx is generated from its own frequency multiplier PLL, that uses a selectable frequency reference determined by *BISTtx_ctrl* [6]. With *BISTtx_ctrl* [6] = 0b (default), the external reference clock is used and typically gives the lowest jitter output. With *BISTtx_ctrl* [6] = 1b the reference clock is derived from the same RCLK used to drive the BIST Rx (this feature only works with DRD = 1 for that RCLK). In this mode, the BIST Tx output is synchronous with the RCLK used in the BIST Rx, however, it contains the low-frequency jitter from the input data. In either case, the BIST Tx PLL needs to be configured for the proper data-rate. When the PLL is properly configured and locked to the reference, the LOL flag should be low (*BISTtx_alarm* [7]). A bit error can be intentionally inserted into the BIST Tx output, by providing a 0b, 1b, 0b sequence to *BISTtx_ctrl* [7].

The BIST Tx PLL setup is similar to the reclocker, thus, the description of similar registers for the RCLK also applies and will not be repeated here. The desired output data-rate is set with the DRD register (*BISTtx_PLL_ctrlB*

[3:0]) and with the VCD register (*BISTtx_PLL_ctrlC* [7:0]). The input reference frequency is the same as for the main RCLKs. Like the RCLKs, if the output data-rate of the BIST Tx needs to be changed, the BIST Tx requires a softreset.

3.2.25 Junction Temperature Monitor

An internal junction temperature monitor with a range of -40°C to 130°C is integrated into the M21260. On the low end, the temperature monitor (*Tmon*) is set to measure -40°C to 10°C in six 10°C steps, and on the high end, 80°C to 130°C in six 10°C steps. The typical temperature resolution is 3°C . The temperature monitor is enabled with *Temp_mon* [1] = 1b. When enabled, the temperature measurement cycle is achieved by providing a rising edge for *Temp_mon* [0]. Afterwards, the correct temperature can be read from *Temp_value* [3:0]. Table 3-18 shows the mapping of the temperature to *Temp_value* [3:0]. Enabling and strobing the temperature in the same write cycle will not yield reliable results.

Table 3-18. Junction Temperature Monitor

Junction Temperature	<i>Temp_value</i> [3:0]	Condition
$T_{\text{CASE}} \geq 130^{\circ}\text{C}$	1100b	High-alarm
$130^{\circ}\text{C} > T_{\text{CASE}} \geq 120^{\circ}\text{C}$	1011b	High-alarm
$120^{\circ}\text{C} > T_{\text{CASE}} \geq 110^{\circ}\text{C}$	1010b	High-warning
$110^{\circ}\text{C} > T_{\text{CASE}} \geq 100^{\circ}\text{C}$	1001b	Normal
$100^{\circ}\text{C} > T_{\text{CASE}} \geq 90^{\circ}\text{C}$	1000b	Normal
$90^{\circ}\text{C} > T_{\text{CASE}} \geq 80^{\circ}\text{C}$	0111b	Normal
$80^{\circ}\text{C} > T_{\text{CASE}} \geq 10^{\circ}\text{C}$	0110b	Normal
$10^{\circ}\text{C} > T_{\text{CASE}} \geq 0^{\circ}\text{C}$	0101b	Normal
$0^{\circ}\text{C} > T_{\text{CASE}} \geq -10^{\circ}\text{C}$	0100b	Normal
$-10^{\circ}\text{C} > T_{\text{CASE}} \geq -20^{\circ}\text{C}$	0011b	Normal
$-20^{\circ}\text{C} > T_{\text{CASE}} \geq -30^{\circ}\text{C}$	0010b	Warning
$-30^{\circ}\text{C} > T_{\text{CASE}} \geq -40^{\circ}\text{C}$	0001b	Low-alarm
$-40^{\circ}\text{C} > T_{\text{CASE}}$	0000b	Low-alarm

3.2.26 IC Identification / Revision Code

The IC identification can be read back from *Chipcode*, and the revision of the device can be read back from *Revcode*. The assigned IC identification for the M21260-12/M21260G-12 is 26h and the revision code is 23h.

3.3 Pin Definitions

Table 3-19. Power Pins

Pin Number	Pin Name	Function	Type
Exposed pad	V_{SS}	IC ground	Power
1,31,54,63,64	AV_{DDIO}	Analog I/O positive supply	Power
21,27,28,34,57,60,67,70	AV_{DDCORE}	Analog core positive supply	Power
10	DV_{DDIO}	Digital I/O positive supply	Power
11,22,33	DV_{DDCORE}	Digital core positive supply	Power

NOTES:

1. If internal regulator is enabled, connect all of the AV_{DDCORE} and/or DV_{DDCORE} pins together to a common floating plane and bypass to V_{SS} .
2. If internal regulator is NOT enabled, it is recommended that all AV_{DDCORE} pins be tied to a plane at 1.2V, that is bypassed to ground. DV_{DDCORE} can be tied to this plane or separately decoupled.
3. IC ground (V_{SS}) is established by contact with exposed pad on underside of package; there are no V_{SS} pins.

Table 3-20. High-Speed Signal Pins

Pin Number	Pin Name	Function	Termination	Type
19	$Din0P$	Serial positive data input for channel 0	50Ω pull up to $V_{ddT0/1}$	PCML referenced to AV_{DDCORE}
20	$Din0N$	Serial negative data input for channel 0	50Ω pull up to $V_{ddT0/1}$	PCML referenced to AV_{DDCORE}
25	$Din1P$	Serial positive data input for channel 1	50Ω pull up to $V_{ddT0/1}$	PCML referenced to AV_{DDCORE}
26	$Din1N$	Serial negative data input for channel 1	50Ω pull up to $V_{ddT0/1}$	PCML referenced to AV_{DDCORE}
29	$Din2P$	Serial positive data input for channel 2	50Ω pull up to $V_{ddT2/3}$	PCML referenced to AV_{DDCORE}
30	$Din2N$	Serial negative data input for channel 2	50Ω pull up to $V_{ddT2/3}$	PCML referenced to AV_{DDCORE}
35	$Din3P$	Serial positive data input for channel 3	50Ω pull up to $V_{ddT2/3}$	PCML referenced to AV_{DDCORE}
36	$Din3N$	Serial negative data input for channel 3	50Ω pull up to $V_{ddT2/3}$	PCML referenced to AV_{DDCORE}
23	$V_{ddT0/1}$	Termination pin for Din [1:0]	Terminate to AV_{DDCORE}	Termination
32	$V_{ddT2/3}$	Termination pin for Din [3:2]	Terminate to AV_{DDCORE}	Termination
72	$Dout0P$	Serial positive data output for channel 0	50Ω pull up to AV_{DDIO}	O - CML/LVDS
71	$Dout0N$	Serial negative data output for channel 0	50Ω pull up to AV_{DDIO}	O - CML/LVDS
66	$Dout1P$	Serial positive data output for channel 1	50Ω pull up to AV_{DDIO}	O - CML/LVDS
65	$Dout1N$	Serial negative data output for channel 1	50Ω pull up to AV_{DDIO}	O - CML/LVDS
62	$Dout2P$	Serial positive data output for channel 2	50Ω pull up to AV_{DDIO}	O - CML/LVDS
61	$Dout2N$	Serial negative data output for channel 2	50Ω pull up to AV_{DDIO}	O - CML/LVDS
56	$Dout3P$	Serial positive data output for channel 3	50Ω pull up to AV_{DDIO}	O - CML/LVDS
55	$Dout3N$	Serial negative data output for channel 3	50Ω pull up to AV_{DDIO}	O - CML/LVDS

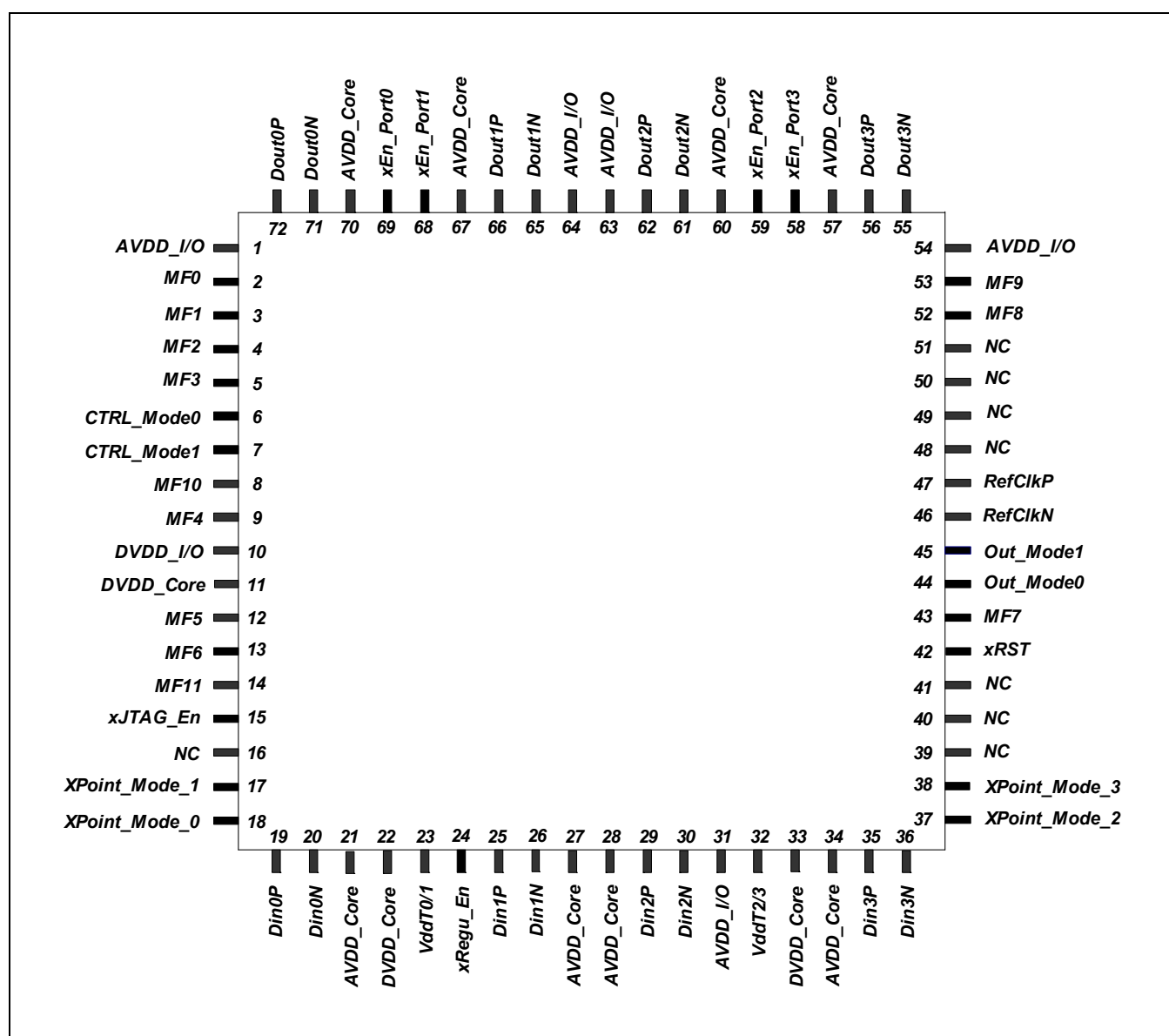
Table 3-21. Control, Interface, and Alarm Pins (1 of 2)

Pin Number	Pin Name	Function	Default	Type
2	MF0	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
3	MF1	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
4	MF2	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
5	MF3	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
9	MF4	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
12	MF5	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
13	MF6	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
43	MF7	Multifunction pin for hardwired mode	Internal pull up	I - CMOS
52	MF8	Multifunction pin for hardwired mode, and JTAG	Internal pull up	I - CMOS
53	MF9	Multifunction pin for hardwired mode, and JTAG	Internal pull up	I - CMOS
8	MF10	Multifunction pin for hardwired mode, serial interface, and JTAG	Internal pull up	I - CMOS
14	MF11	Multifunction pin for hardwired mode, serial interface, and JTAG	Internal pull up	I - CMOS
6	CTRL_Mode0	Hardwired or serial interface mode control pin	Internal pull up	I - CMOS
7	CTRL_Mode1	Hardwired or serial interface mode control pin	Internal pull up	I - CMOS
44	Out_Mode0	Output data interface control pin	Internal pull down	I - CMOS
45	Out_Mode1	Output data interface control pin	Internal pull down	I - CMOS
42	xRST	Reset pin (L = reset)	Internal pull up	I - CMOS
15	xJTAG_En	JTAG testing control pin (L = enable)	Internal pull up	I - CMOS
24	xRegu_En	Internal voltage regulator control pin (L = enable)	Internal pull up	I - CMOS
47	RefClkP	Reference clock positive input	Internal pull down	I - AC coupled
46	RefClkN	Reference clock negative input	Internal pull down	I - AC coupled
18	XPoint_Mode_0	Crosspoint switch-state setting pin	Internal pull down	I - CMOS
17	XPoint_Mode_1	Crosspoint switch-state setting pin	Internal pull down	I - CMOS
37	XPoint_Mode_2	Crosspoint switch-state setting pin	Internal pull down	I - CMOS
38	XPoint_Mode_3	Crosspoint switch-state setting pin	Internal pull down	I - CMOS
69	xEn_Port0	Control pin to enable/disable output for channel 0 (L = enable)	Internal pull up	I - CMOS
68	xEn_Port1	Control pin to enable/disable output for channel 1 (L = enable)	Internal pull up	I - CMOS
59	xEn_Port2	Control pin to enable/disable output for channel 2 (L = enable)	Internal pull up	I - CMOS
58	xEn_Port3	Control pin to enable/disable output for channel 3 (L = enable)	Internal pull up	I - CMOS
16	xLOL0	CDR/RCLK loss of lock alarm for channel 0	No internal pull up or pull down	O-open drain
39	xLOL1	CDR/RCLK loss of lock alarm for channel 1	No internal pull up or pull down	O-open drain
40	xLOL2	CDR/RCLK loss of lock alarm for channel 2	No internal pull up or pull down	O-open drain

Table 3-21. Control, Interface, and Alarm Pins (2 of 2)

Pin Number	Pin Name	Function	Default	Type
41	xL0L3	CDR/RCLK loss of lock alarm for channel 3	No internal pull up or pull down	O-open drain
48	xLOA0	CDR/RCLK loss of activity alarm for channel 0	No internal pull up or pull down	O-open drain
49	xLOA1	CDR/RCLK loss of activity alarm for channel 1	No internal pull up or pull down	O-open drain
50	xLOA2	CDR/RCLK loss of activity alarm for channel 2	No internal pull up or pull down	O-open drain
51	xLOA3	CDR/RCLK loss of activity alarm for channel 3	No internal pull up or pull down	O-open drain

Figure 3-13. M21260 Pinout Diagram (Top View)





Appendix

A.1 Glossary of Terms/Acronyms

Table A-1 contains a list of acronyms used in this data sheet.

Table A-1. Acronyms

AIE	Adaptive Input Equalizer
BER	Bit-Error Rate
BIST	Built-In Self Test
RCLK	Reclocker
DRD	Data-Rate Divider
EVM	Evaluation Module
FLL	Frequency Lock Loop
FRA	Frequency Reference Acquisition
ISI	Inter-Symbol Interference
LOA	Loss of Activity
LOL	Loss of Lock
LOLCir	Loss of Lock Circuitry
N_{NARROW}	Narrow Reference Window
PCB	Printed Circuit Board
PLL	Phase Lock Loop
RFD	Reference Frequency Divider
SONET	Synchronous Optical Network
VCD	VCO Comparison Divider
N_{WIDE}	Wide Reference Window
XPTS	Crosspoint Switch

A.2 Reference Documents

A.2.1 External

The following external documents were referenced in this data sheet.

- Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria GR-253-CORE

- The I²C Bus Specification version 2.1
- Serial ATA: High Speed Serialized AT Attachment revision 1.0a
- Fibre Channel - Methodologies for Jitter and Signal Quality Specification - MJSQ
- Application Notes for Surface Mount Assembly of QFN Packages
- Amkor Technology Thermal Test Report TT-00-06
- SMPTE 292M, SMPTE 259M, SMPTE 344M
- DVB-ASI
- Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria (GR 253-Core)
- Fibre Channel - Methodologies for jitter and signal quality specification - MJSQ and FC-PI-2

A.2.2 Mindspeed

The following Mindspeed documents were referenced in this data sheet.

- Application Note: Equipment Protection Switching Using Low-Cost Crosspoint Elements
- M2125x and M2126x ARD Software Description (212xx-SWG-001)
- Jitter tolerance and generation of Mindspeed crosspoint switches and CDR arrays (2110x-APP-003)

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