SP720

The SP720 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures per input. A total of 14 available inputs can be used to protect up to 14 external signal or bus lines. Over-voltage protection is from the IN (pins 1-7 and 9-15) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 16) or a $-V_{BE}$ diode threshold below V- (Pin 8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

HBM STANDARD	MODE	R	C	ESD (V)
IEC 61000-4-2	Air	330Ω	150pF	>15kV
	Direct	330Ω	150pF	>4kV
	Direct, Dual Pins	330Ω	150pF	>8kV
MIL-STD-3015.7	Direct, In-circuit	1.5kΩ	100pF	>15kV

Refer to Figure 1 and Table 1 for further detail. Refer to Application Note AN9304 and AN9612 for additional information.

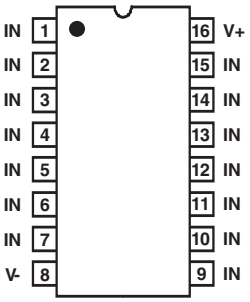
Ordering Information

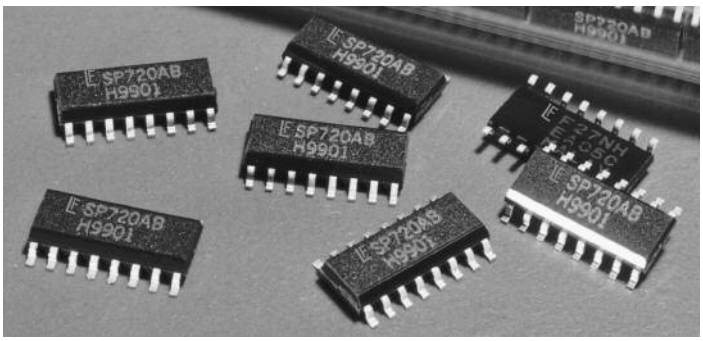
PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. NO.	Min. Order
SP720AP	-40 to 105	16 Ld PDIP	E16.3	1500
SP720AB	-40 to 105	16 Ld SOIC	M16.15	1970
SP720ABT	-40 to 105	16 Ld SOIC Tape and Reel	M16.15	2500

Pinout

SP720 (PDIP, SOIC)

TOP VIEW





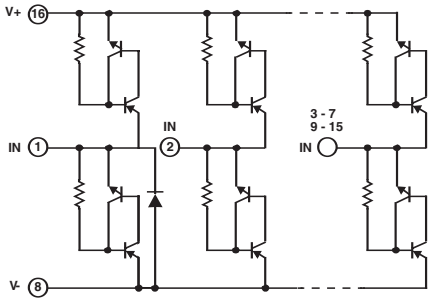
Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 . . . . . 15kV
  - IEC 61000-4-2, Direct Discharge,
    Single Input . . . . . 4kV (Level 2)
    Two Inputs in Parallel . . . . . 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge . . . . . 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs) . . . . . ±3A
  - Single Pulse, 100µs Pulse Width . . . . . ±2A
  - Single Pulse, 4µs Pulse Width . . . . . ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to . . . . . +30V
  - Differential Voltage Range to . . . . . ±15V
- Fast Switching . . . . . 2ns Risetime
- Low Input Leakages . . . . . 1nA at 25°C (Typ)
- Low Input Capacitance . . . . . 3pF (Typ)
- An Array of 14 SCR/Diode Pairs
- Operating Temperature Range . . . . . -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Functional Block Diagram



SP720

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-). . . . . +35V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND
(Refer to Figure 6) . . . . .±2A, 100µs
ESD Ratings and Capability (Figure 1, Table 1)
Load Dump and Reverse Battery (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 1). . . . . θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 130
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = -40°C to 105°C; V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		-	2 to 30	-	V
Forward Voltage Drop: IN to V- IN to V+	 V_{FWDL} V_{FWDH}	I_{IN} = 1A (Peak Pulse)	 - -	 2 2	 - -	 V V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

NOTES:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger from the V+ and V- pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance." These characteristics are given here for thumb-rule information to determine peak current and dissipation under EOS conditions.

ESD Capability

ESD capability is dependent on the application and defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified" MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP720 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ. By strict definition of MIL-STD-3015.7 using "pin-to-pin" device testing, the ESD voltage capability is greater than 6kV. The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2). Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP720 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

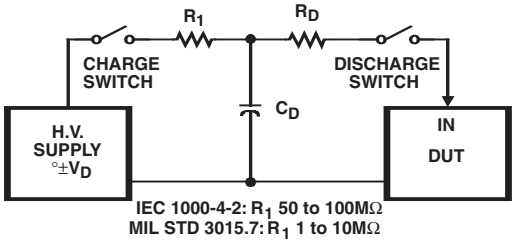


FIGURE 1. ELECTROSTATIC DISCHARGE TEST

SP720

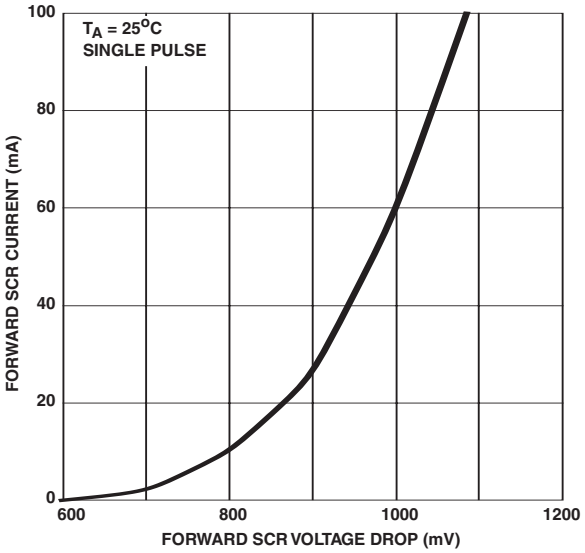


FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

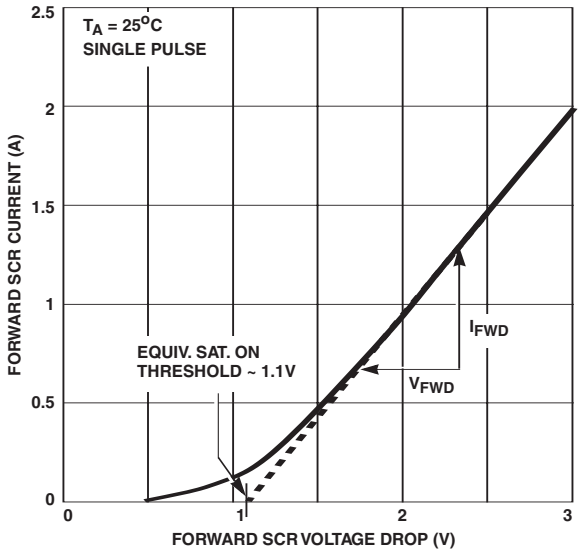


FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

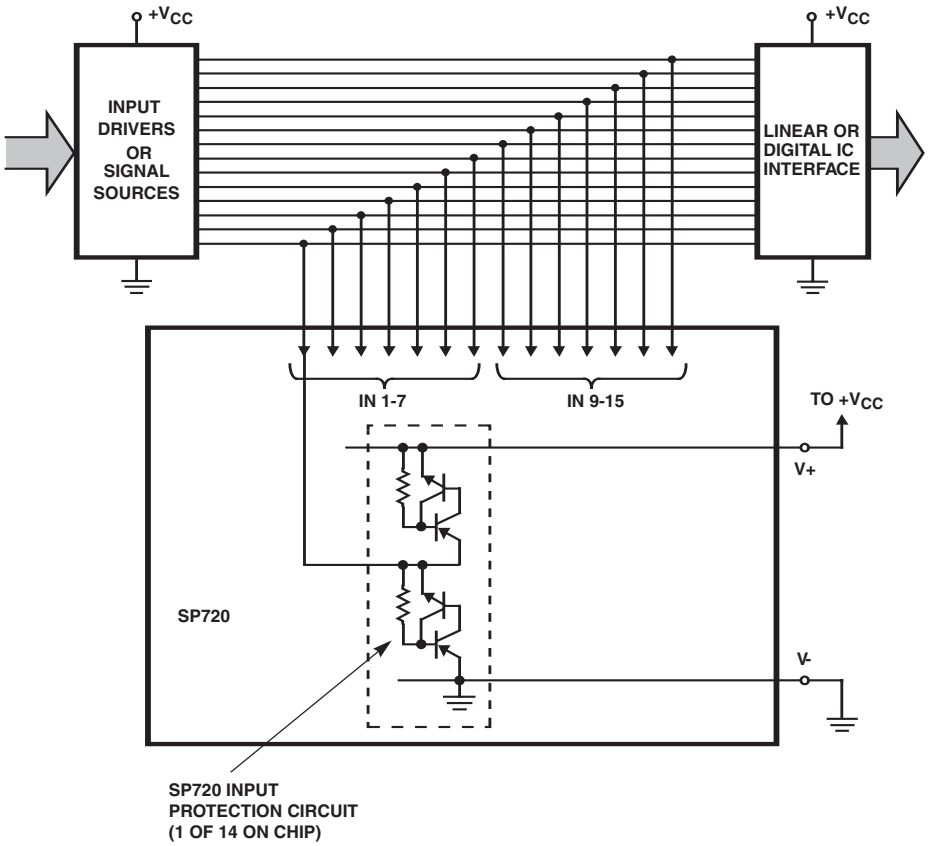


FIGURE 4. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN $1V_{BE}$ ABOVE V+ OR LESS THAN $-1V_{BE}$ BELOW V-

SP720

Peak Transient Current Capability of the SP720

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP720's ability to withstand a wide range of transient current pulses. The circuit used to generate current pulses is shown in Figure 5.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP720 'IN' input pin and the (+) current pulse input goes to the SP720 V- pin. The V+ to V- supply of the SP720 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the V+ to V- voltage supply level, improving as the supply voltage is reduced. Values of 0, 5, 15 and 30 voltages are shown. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in Figure 6.

When adjacent input pins are paralleled, the sustained peak current capability is increased to nearly twice that of a single pin. For comparison, tests were run using dual pin combinations 1+2, 3+4, 5+6, 7+9, 10+11, 12+13 and 14+15.

The overstress curve is shown in Figure 6 for a 15V supply condition. The dual pins are capable of 10A peak current for a 10µs pulse and 4A peak current for a 1ms pulse. The complete for single pulse peak current vs. pulse width time ranging up to 1 second are shown in Figure 6.

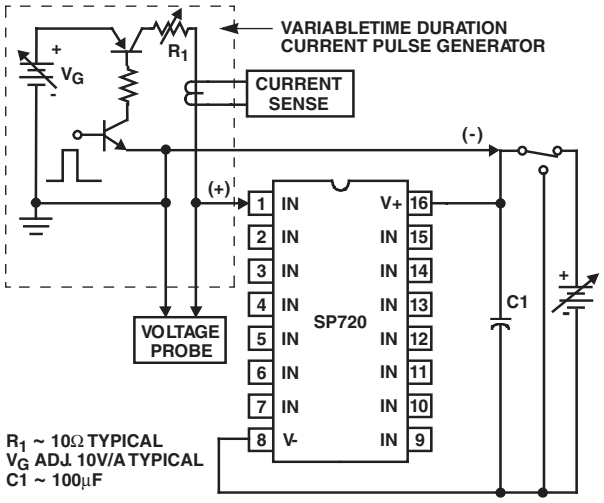


FIGURE 5. TYPICAL SP720 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

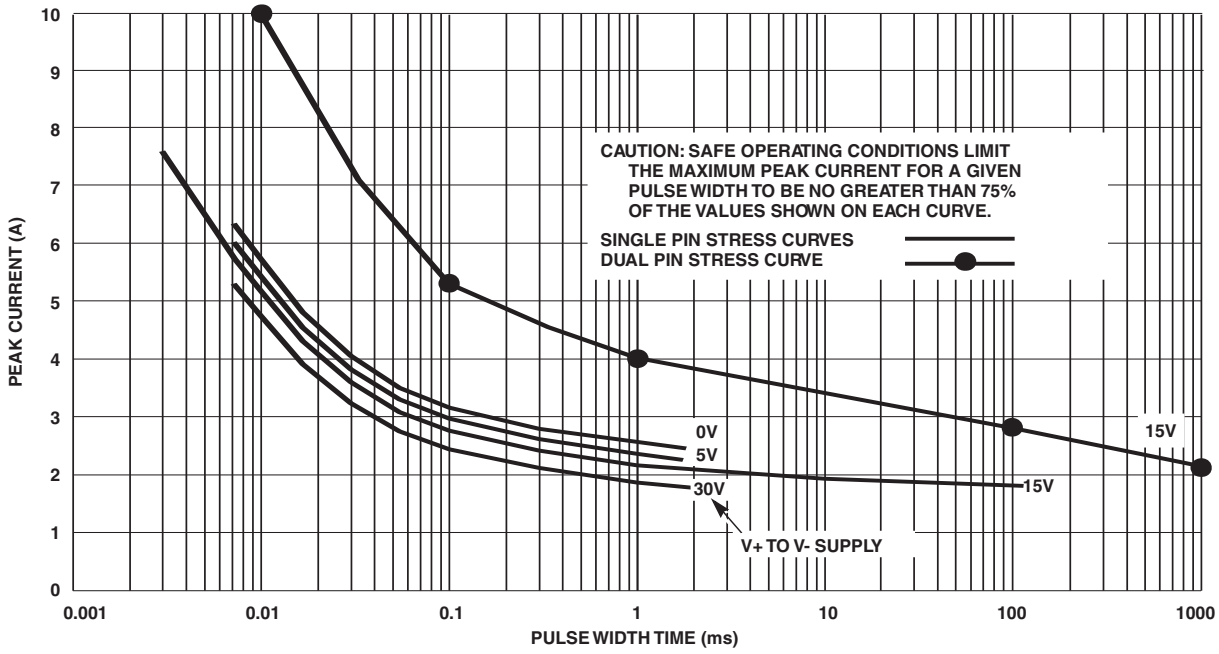
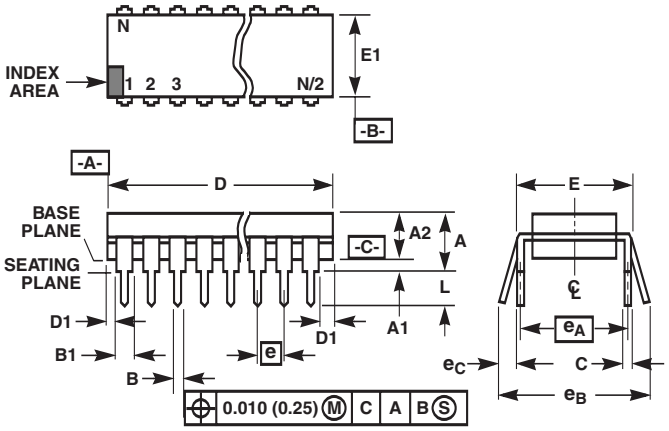


FIGURE 6. SP720 TYPICAL SINGLE PULSE PEAK CURRENT CURVES SHOWING THE MEASURED POINT OF OVER-STRESS IN AMPERES vs PULSE TIME IN MILLISECONDS (T_A = 25°C)

SP720

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

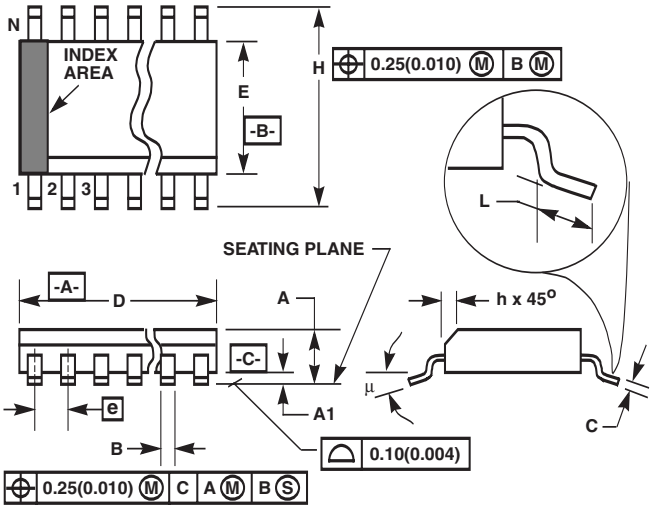
E16.3 (JEDEC MS-001 BB ISSUE D)

16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

SP720

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)

16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
	0^o	8^o	0^o	8^o	-