

IrDA[®] Data 1.2 Low Power Compliant 115.2 kb/s Infrared Transceiver

Technical Data

HSDL-3201 (Front and Top Options)

Features

- Ultra Small Surface Mount Package
- Minimal Height: 2.5 mm
- V_{cc} from 2.7 to 3.6 Volts
- Withstands > 250 mV_{p-p} Power Supply Ripple
- LED Supply Voltage can Range from 2.7 to 6.0 Volts
- Low Shutdown Current - 20 nA Typical

- Complete Shutdown - TxD, RxD, PIN Diode
- One Optional External Component
- Temperature Range: -25°C to 85°C
- 32 mA LED Drive Current
- Integrated EMI Shield
- IEC825-1 Class 1 Eye Safe
- Edge Detection Input

 Prevents the LED from Long Turn on Time





Applications

- Mobile Telecom
 - Cellular Phones
 - Pagers
 - Smart Phones
- Data Communication
 - PDAs
 - Portable Printers
- Digital Imaging
 - Digital Cameras
 - Photo-Imaging Printers

Description

The HSDL-3201 is one of a new generation of low-cost Infrared (IR) transceiver modules from Agilent Technologies. It features the smallest footprint in the industry at 2.5 H x 8.0 W x 3.0 D mm. Although the supply voltage can range from 2.7 V to 3.6 V, the LED drive current is internally compensated to a constant 32 mA to assure that link distances meet the IrDA Data 1.2 (low power) physical layer specifications.

The HSDL-3201 meets the 20 cm link distance to other IrDA 1.2 low power devices, and a 30 cm link distance to IrDA 1.2 standard devices.

HSDL-3201#021/001/011 Pinout, Rear View



HSDL-3201#008/018 Pinout, Rear View



Application Circuit



I/O Pins Configuration Table

Pin	Symbol	Description	Notes
1	GND	Ground	Connect to system ground.
2	NC	No Connection	This pin must be left unconnected.
3	V _{CC}	Supply Voltage	Regulated: 2.7 to 3.6 Volts
4	AGND	Analog Ground	Connect to a "quiet" ground.
5	SD	Shut Down Active High	This pin must be driven either high or low. Do NOT float the pin.
6	RXD	Receiver Data Output. Active Low.	Output is a low pulse for 2.4 µs when a light pulse is seen.
7	TXD	Transmitter Data Input. Active High.	Logic high turns the LED on. If held high longer than $\sim 20 \ \mu$ s, the LED is turned off. TXD must be driven high or low. Do NOT float the pin.
8	VLED	LED Voltage	May be unregulated: 2.7 to 6.0 volts.
-	SHIELD	EMI Shield	Connect to system ground via a low inductance trace. For best performance, do not directly connect to GND or AGND at the part.

Recommended Application	Circuit	Components
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Component	Recommended Value	Note
C1	1.0 µF	1

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is $\leq~50^{\circ}\text{C/W}.$

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T _S	-40	100	°C
Operating Temperature	T _A	-25	85	°C
LED Supply Voltage	V _{VLED}	-0.5	7	V
Supply Voltage	V _{CC}	-0.5	7	V
Input Voltage: TXD, SD	VI	0	$V_{\rm CC} + 0.5$	V
Output Voltage: RXD	Vo	-0.5	$V_{CC} + 0.5$	V
Solder Reflow Temperature Profile	See	Reflow P	rofile, page	19

Transceiver I/O Truth Table

The LED and RXD outputs are controlled by the combination of the TXD and SD pins and light falling on the receiver. As shown in the table below, the transmitter is non-inverting; the LED is on when the TXD pin is high and off when TXD is low. The receiver is inverting; the RXD pin is low during IrDA signal pulses and high when the receiver does not see any light. When shutdown (SD pin high), the LED is off (the state of the TXD pin does not matter), and the RXD pin is pulled high with a weak internal pullup.

SD	TXD	LED	Receiver	RXD	Notes
	High	On	Don't care	Not Valid	2, 3
Low	Low	Off	IrDA Signal	Low	4, 5
	LOW		No Signal	High	
High	Don't care	Off	Don't care	High	6

s Shutdown Mode Notes

When the HSDL-3201 is in Shutdown Mode (SD pin high), the part presents different impedances to the rest of the circuit than when it is in normal mode.

RXD Pin: This pin is NOT Tristate. During shutdown the equivalent circuit is a weak pullup (\sim 300 k Ω) to V_{cc}. The ESD protection diodes to V_{cc} and Ground are also present.

TXD Pin: Input protection diodes are present.

VLED Pin: Possible leakage current of 1.5 nA.

SD Pin: Will draw approximately 16 nA when driven high.

Marking Information

The unit is marked with the letters "A" and the datecode "YWW" on the shield for front options. For top options, the part is marked as "YWW" where Y is the last digit of the year, and WW is the workweek.

Ordering Information

Specify the part number followed by an option number.

HSDL-3201#XXX

There are five options available:

	Front Options
#011	Taped in a short strip
	(no reel), 10 per strip
#001	Taped and 7" Reel
	Packaging, 500 per reel
#021	Taped and 13" Reel
	Packaging, 2500 per reel
	Top Options
#018	Taped in a short strip
	(no reel), 10 per strip
#008	Taped and 13" Reel
	Packaging, 2500 per reel

Caution: The BiCMOS inherent to this design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Param	Symbol	Min.	Max.	Units	Conditions	Notes	
Operating Temperature		TA	-25	85	°C		
Supply Voltage		V _{CC}	2.7	3.6	V		
LED Supply Voltage		V _{LED}	2.7	6.0	V		
TXD, SD Input	Logic High	V _{IH}	2/3 V _{CC}	V _{CC}	V		
Voltage	Logic Low	V _{IL}	0	$1/3 V_{CC}$	V		
Receiver Input	Logic High	EI _H	0.0081	500	mW/cm ²	For in-band signals.	7
Irradiance	Logic Low	EI_{L}		0.3	µW/cm ²	For in-band signals.	7
Receiver Data R	ate		2.4	115.2	kb/s		

Recommended Operating Conditions

RXD Output Waveform



LED Optical Waveform



TXD "Stuck ON" Protection



Receiver Wakeup Time Definition



Transmitter Wakeup Time Definition



Electrical & Optical Specifications

Specifications hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values are at 25° C and 3.0 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Note
Receiver								
Viewing Angl	e	$2\phi_{1/2}$	30			0		
Peak Sensitiv Wavelength	ity	λp		880		nm		
RXD Output	Logic High	V _{OH}	V _{CC} -0.2		V _{CC}	V	I_{OH} =-200 µA, EI ≤ 0.3 µW/cm ²	
Voltage	Logic Low	VOL	0		0.4	V	I _{OL} =200 μA	8
RXD Pulse W	idth	t_{PW}	2.0	2.45	3.0	μs		8
RXD Rise Tin	ne	t _R		11	20	ns	t_{PW} (EI)=1.6 µs, C_L =10 pF	
RXD Fall Tim	e	$t_{\rm F}$		16	25	ns	t_{PW} (EI)=1.6 µs, C_L =10 pF	
Receiver Late	ency Time	tL		25	50	μs		9
Receiver Wal	e Up Time	t _{RW}		28	40	μs		10
Transmitter								
Radiant Inten	sity	EIH	4	9	28.8	mW/Sr	$T_A=25^{\circ}C, \theta_{1/2} \le 15^{\circ}, TXD \ge 2/3 V_{CC}$	
Viewing Angl	e	$2\theta_{1/2}$	30		60	0		
Peak Waveler	ngth	λ_{p}		875		nm		
Spectral Line	Half Width	$\Delta\lambda_{1/2}$		35		nm		
Optical Pulse	Optical Pulse Width		2.0	2.24	2.6	μs	t _{PW} (TXD)=1.6 μs	
Max. Optical	Pulse Width	topwm		20	30	μs	TXD pin stuck high	
Optical Rise Time		tor		180	600	ns	t _{PW} (TXD)=1.6 μs	
Optical Fall 7	ìime	t _{OF}		180	600	ns	t _{PW} (TXD)=1.6 μs	
TXD Logic	High	V _{IH}	2/3 V _{CC}		V _{CC}	V		
Levels	Low	V _{IL}	0		1/3 V _{CC}	V		
TXD Input	High	I _H		25		nA	$V_{\rm I} \ge 2/3 V_{\rm CC}$	
Current	Low	IL		-15		nA	$0 \leq V_{I} \leq 1/3 V_{CC}$	
	On	I _{VLED}		32		mA	$V_{VLED} = V_{CC} = 3.6 \text{ V}, V_{I}(TXD) \ge 2/3 \text{ V}_{CC}$	
LED	Off	I _{VLED}		1.5		nA	$V_{VLED} = V_{CC} = 3.6 \text{ V}, V_{I}(TXD) \le 1/3 \text{ V}_{CC}$	
Current	Shutdown	I _{VLED}		1.5		nA	$V_{I}(SD) \ge 2/3 V_{CC}$	
Transmitter V	Vake Up Time	$t_{\rm TW}$		12	20	μs		11
Transceiver								
SD Logic	High	$V_{\rm IH}$	2/3 V _{CC}		V _{CC}	V		
Levels	Low	V _{IL}	0		1/3 V _{CC}	V		
SD Input	High	I _H		16		nA	$V_{I} \ge 2/3 V_{CC}$	
Current	Low	IL		-150		nA	$0 \leq V_I \leq 1/3 V_{CC}$	
DC Supply	Shutdown	I _{CC1}		20	200	nA	V_{CC} =3.6 V, V_{SD} ≥ V_{CC} - 0.5, T_A =25°C	
Current	Idle	I _{CC2}		100		μΑ	V_{CC} =3.6 V, V_{I} (TXD) $\leq 1/3 V_{CC}$, EI =0	
AC Supply	Active, receive	I _{CC3}		0.8	3.0	mA	V_{CC} =3.6 V, $V_{I}(TXD) \le 1/3 V_{CC}$	12,13
Current	Active, transmit	I _{CC4}		9.0		mA	V_{CC} =3.6 V, $V_{I}(TXD) \ge 2/3 V_{CC}$	14

Notes at top of next page.

6

Notes:

- 1. C1, which is optional, must be placed within 0.7 cm of the HSDL-3201 to obtain optimum noise immunity.
- 2. If TXD is stuck in the high state, the LED will turn off after about 20 $\mu s.$
- 3. RXD will echo the TXD signal while TXD is transmitting data.
- 4. In-Band IrDA signals and data rates ≤ 115.2 Kb/s.
- 5. RXD Logic Low is a pulsed response. The pulse width is $2.4\,\mu\text{s},$ independent of data rate.
- 6. RXD Logic High during shutdown is a weak pullup resistor (300 k Ω).
- 7. An in-band optical signal is a pulse/sequence where the peak wavelength, λp , is defined as 850 nm $\leq \lambda p \leq 900$ nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
- 8. For in band signals ≤ 115.2 Kb/s where 8.1 μ W/cm² $\leq EI \leq 500$ mW/cm².
- 9. Latency is defined as the time from the last TXD light output pulse until the receiver has recovered full sensitivity.
- 10. Receiver wake up time is measured from the SD pin high to low transition or V_{cc} power on, to a valid RXD output.
- 11. Transmitter wake up time is measured from the SD pin high to low transition or V_{cc} power on, to a valid light output in response to a TXD pulse.
- 12. Typical values are at EI = 10 mW/cm^2
- 13. Maximum value is at EI = 500 mW/cm^2 .
- 14. Current is due to internal stages of the LED current mirror. This current is in addition to the ILED current.

Notes on Supply Current

The supply current for the HSDL-3201 has two different components, DC and AC.

The DC component is measured in two states, normal (idle mode) and shutdown. This current is present whenever power is applied to the part.

The AC component is either the extra current drawn from the V_{cc} pin by the photodiode when it sees light, or the current needed by the LED current circuit. The values in the table are peak values. Since IrDA data is transmitted with a 3/16 duty cycle, the average value is 3/16 of the peak. The AC current is not drawn when no light is present.

Distances between Units to See a 10 mW/cm² Light Level

Type of Transceiver	Distance (cm)
Typical HSDL-3201	1.0
Max. Brightness HSDL-3201	1.7
Typical SIR	2.0
Typical FIR	3.2

The 500 mW/cm² light level is for the maximum brightness IrDA unit at 1 cm.



Figure 2. LED Current vs. VLED.







Figure 3. Power Supply Ripple Rejection. (No C1).



HSDL-3201#011/001/021 Package Dimensions



HSDL-3201#011/001/021 Tape and Reel Dimensions



HSDL-3201#008/018 Package Dimensions



UNIT: mm TOLERANCE: ± 0.2 mm COPLANARITY = 0.1 mm MAX.

Pin	Symbol	Description	
1	GND	Ground	
2	NC	No Connection	
3	V _{CC}	Supply Voltage	
4	AGND	Analog Ground	
5	SD	Shutdown (Active High)	
6	RxD	Receive Data	
7	TxD	Transmit Data	
8	VLED	LED Voltage	
9	EMI Shield	EMI Shield	



HSDL-3201#008/018 Tape and Reel Dimensions



UNIT: mm

SYMBOL	Ao	Во	Ko	Po	P1	P2	т
SPEC	3.65 ± 0.10	7.90 ± 0.10	2.75 ^{+0.05} - 0.10	4.00 ± 0.10	8.00 ± 0.10	2.00 ± 0.10	0.40 ± 0.10
SYMBOL	E	F	Do	D1	w	10Po	
SPEC	1.75 ± 0.10	7.50 ± 0.10	1.55 ± 0.05	1.50 (MIN.)	16.00 ± 0.30	40.00 ± 0.20	

NOTES:

1. 10 SPROKET HOLE PITCH CUMULATIVE TOLERANCE IS ± 0.2 mm.

2. CARRIER CAMBER SHALL NOT BE MORE THAN 1 mm PER 100 mm THROUGH A LENGTH OF 250 mm.

3. Ao AND Bo MEASURED ON A PLACE 0.3 mm ABOVE THE BOTTOM OF THE PACKET.

4. Ko MEASURED FROM A PLACE ON THE INSIDE BOTTOM OF THE POCKET TO TOP SURFACE OF CARRIER.

5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.

Moisture Proof Packaging

The HDSL-3201 is shipped in moisture proof packaging. Once opened, moisture absorption begins.

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within two days if stored at the recommended storage conditions. If times longer than two days are needed, the parts must be stored in a dry box.

Baking

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temp.	Time	
In reels	60°C	\geq 48 hours	
In bulk	100℃	\geq 4 hours	
	125℃	≥ 2 hours	
	150℃	\geq 1 hour	

Baking should only be done once.

Recommended Land Pattern for HSDL-3201#011/001/ 021 (Front Options)



Recommended Land Pattern for HSDL-3201#008/018 (Top Options)



Appendix A: HSDL-3201#011/001/021 SMT Assembly Application Note

Solder Pad, Mask, and Metal Stencil



Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inches) or a 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.



Stencil Thickness t (mm)	Aperture Size(mm)		
Steller Intexness, t (http://	length, l	width, w	
0.152 mm	$2.60~\pm~0.05$	0.55 ± 0.05	
0.127 mm	3.00 ± 0.05	0.55 ± 0.05	

Adjacent Land Keep-out and Solder Mask Areas

Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

The minimum solder resist strip width required to avoid solder bridging adjacent pads is **0.2 mm.**

It is recommended that two fiducial crosses be place at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.



PCB Layout Suggestion

Component Side

The following PCB layout shows a recommended layout that should result in good electrical and EMI performance. Things to note:

- 1. The ground plane should be continuous under the part, but should not extend under the shield trace.
- 2. The shield trace is a wide, low inductance trace back to the system ground.
- 3. The AGND pin is connected to the ground plane and not to the shield tab.
- 4. C1 is an optional V_{cc} filter capacitor; it may be left out if the V_{cc} is clean.
- 5. VLED can be connected to either unfiltered or unregulated power. If C1 is used, and if VLED is connected to V_{cc} , the connection should be before the C1 cap.



Circuit Side



Recommended Solder Paste/Cream Volume for Castellation Joints

Based on calculation and experiment, the printed solder paste volume required per castellation pad is **0.22 cubic mm** (based on either no-clean or aqueous solder cream types with typically 60% to 65% solid content by volume). Using the recommended stencil results in this volume of solder paste.

Pick and Place Misalignment Tolerance and Self-Alignment after Solder Reflow

If the printed solder paste volume is adequate, the HSDL-3201 will self align after solder reflow. Units should be properly reflowed in IR/Hot Air convection oven using the recommended reflow profile. The direction of board travel does not matter.

Direction Definition



Allowable Misalignment

Direction	Tolerance
X	$\leq 0.2 \text{ mm}$
Y	See text
θ	$\leq \pm 3$ degrees

Tolerance for X- axis Alignment of Castellation

Misalignment of castellation to the land pad should not exceed 0.2 mm or about one half the width of the castellation during placement of the unit. The castellations will self-align to the pads during solder reflow.

Tolerance for Rotational (θ) Misalignment

Mounted units should not be rotated more than ± 3 degrees with reference to center X-Y as shown in the direction definition. Units that are rotated more than ± 3 degrees will not self align after solder reflow. Units with less than a ± 3 degree misalignment will self-align after solder reflow.

Y- axis Misalignment of Castellation

In the Y direction, the HSDL-3201 does not self align after solder reflow. Agilent recommends that the part be placed in line with the fiducial mark (mid-length of land pad.) This will enable sufficient land length (minimum of one half of the land pad) to form a good joint. See the drawing below.



Solder Paste DryP2, R2125°C to 170Solder ReflowP3, R3170°C to 230P3, R4230°C to 170Cool DownP4, R5170°C to 25°The reflow profile is a straightProcess zone P2line representation of a nominalsufficient time dutemperature profile for asolder paste. TheThe temperature profile is dividedraised to a level julino four process zones, eachliquidus point of t

convective reflow solder process. The temperature profile is divided into four process zones, each with different $\Delta T/\Delta time$ temperature change rates. The $\Delta T/\Delta time$ rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-3201 castellation pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3201 castellations. **Process zone P2** should be of sufficient time duration (greater than 60 seconds), to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170° C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive,

resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3201 castellations to change dimensions evenly, putting minimal stresses on the HSDL-3201 transceiver.

Process Zone	Symbol	ΔΤ	Maximum \Delta T/\Delta time
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3 P3, R4	170°C to 230°C (245°C max.) 230°C to 170°C	4°C/s -4°C/s
Cool Down	P4, R5	170°C to 25°C	-3°C/s

Reflow Profile MAX 245°C 230 200 - - TEMPERATURE - (°C) 183 170 R2 90 sec MAX. 150 125 ABOVE 183°C R1 R5 100 50 25 0 50 100 150 200 250 300 t-TIME (SECONDS) P1 HEAT UP P2 SOLDER PASTE DRY P3 SOLDER COOL

Window Design

To insure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30 degrees, the maximum, to a cone angle of 60 degrees.



X is the width of the window, Y is the height of the window, and Z is the distance from the HSDL-3201 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens is 5.1 mm. The equations for the size of the window are as follows:

 $X = 5.1 + 2(Z + D) \tan \theta$ $Y = 2(Z + D) \tan \theta$

Where θ is the required half angle for viewing. For the IrDA minimum, it is 15 degrees, for the IrDA maximum it is 30 degrees. (D is the depth of the LED image inside the part, 3.17 mm). These equations result in the following tables and graphs:

Minimum and Maximum Window Sizes

Dimensions are in mm.

Depth (Z)	Y min.	X min.	Y max.	X max.
0	1.70	6.80	3.66	8.76
1	2.23	7.33	4.82	9.92
2	2.77	7.87	5.97	11.07
3	3.31	8.41	7.12	12.22
4	3.84	8.94	8.28	13.38
5	4.38	9.48	9.43	14.53
6	4.91	10.01	10.59	15.69
7	5.45	10.55	11.74	16.84
8	5.99	11.09	12.90	18.00
9	6.52	11.62	14.05	19.15
10	7.06	12.16	15.21	20.31

Window Height Y vs. Module Depth Z







Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical design reasons, place a curve on the back side of the window that has the same radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.





Curved Front and Back (Second choice)



Curved Front, Flat Back (Do not use)



Test Methods

Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

- 1. Electromagnetic field: 3 V/m maximum (please refer to IEC 801-3, severity level 3 for details).
- 2. Sunlight:

10 kilolux maximum at the optical port. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased to provide $490 \ \mu\text{W/cm}^2$ (with no modulation) at the optical port. The light source faces the optical port.

This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.

3. Incandescent Lighting: 1000 lux maximum. This is produced with general service, tungsten-filament, gas-filled, inside frosted lamps in the 60 Watt to 100 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 Kelvin range and a spectral peak in the 850 to 1050 nm range.

4. Fluorescent Lighting: 1000 lux maximum. This is simulated with an IR source having a peak wavelength within the range of 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal $(0 \mu W/cm^2 minimum and$ $0.3 \mu W/cm^2$ peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.



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For product information and a complete list of distributors, please go to our web site.

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