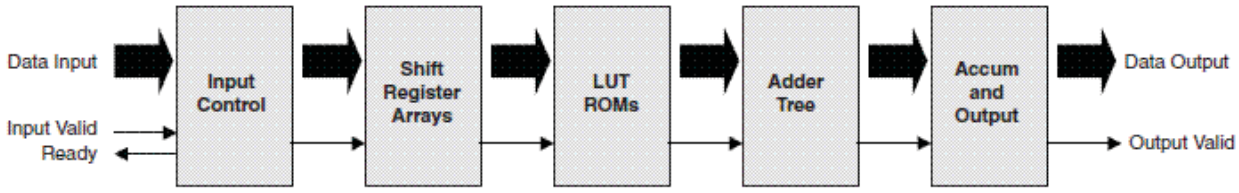
Distributed Arithmetic FIR (DA-FIR) Filter Generator

Overview

The Lattice Distributed Arithmetic Finite Impulse Response (DA-FIR) Filter Generator IP implements a highly configurable, multi-channel DA-FIR filter, using distributed arithmetic algorithms implemented in FPGA Look Up Table (LUT) or Embedded Block Memory (EBR) to efficiently support the sum-of-product calculations required to perform the filter function. These techniques generate very area-efficient utilization of the FPGA LUTs while enabling savings of multiply-accumulate blocks (sysDSP) for other design logic. As a result, the DA-FIR Filter Generator IP core is extremely useful for implementing custom DSP blocks in Lattice FPGAs. Please refer to the user's guide to determine which cores are available for each device family.



Features

- Variable number of taps up to 1024
- Multi-channel support (up to 32 channels)
- Polyphase interpolation/decimation filters
- Halfband filters
- Interpolation and Decimation ratios from 2 to 32
- Input data widths from 4 to 32 bits
- Coefficient widths from 4 to 32 bits
- Signed or unsigned data and coefficients
- Selectable rounding: truncation, rounding away from zero, convergent rounding
- Optional saturation logic for overflow handling
- Full precision arithmetic
- Specification of fractional inputs and outputs
- Support for both serial and parallel filters, with user specified degree of parallelism.
- Configurable pipelining to increase performance
- Optimizations based on filter characteristics (symmetry and halfband).
- Handshake signals to facilitate smooth interfacing

Performance and Resource Utilization

LatticeECP3[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	290	348	-	476	318
1	9	Disable	8	TRUN	512	611	-	877	279
1	36	Enable	12	TRUN	600	709	-	883	308

1. Performance and utilization data are generated targeting a LFE3-70E-7FN484CES device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M/S[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	317	378	-	481	343
1	9	Disable	8	TRUN	550	655	-	887	310

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	36	Enable	12	TRUN	625	743	-	899	291

1. Performance and utilization data are generated targeting a LFE2M20E-6F256C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2/S[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	317	378	-	481	341
1	9	Disable	8	TRUN	550	655	-	887	321
1	36	Enable	12	TRUN	625	743	-	899	320

1. Performance and utilization data are generated targeting a LFE2-20E-6F256C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

LatticeECP/EC[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	296	340	-	481	192
1	9	Disable	8	TRUN	521	594	-	887	180
1	36	Enable	12	TRUN	590	689	-	899	174

1. Performance and utilization data are generated targeting a LFECP15E-4F256C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP family.

LatticeSC/M[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	278	343	-	481	372
1	9	Disable	8	TRUN	564	759	-	895	338
1	36	Enable	12	TRUN	568	668	-	934	390

1. Performance and utilization data are generated targeting a LFSC3GA15E-6F256C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC/M family.

LatticeXP2[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	317	378	-	481	274
1	9	Disable	8	TRUN	550	655	-	887	251
1	36	Enable	12	TRUN	625	743	-	899	270

2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

LatticeXP[1]

Channels	Taps	Interpolation	DWidth	Round	SLICEs	LUTs	EBRs	Registers	Fmax
1	16	Disable	16	TRUN	296	340	-	481	186
1	9	Disable	8	TRUN	521	594	-	887	178
1	36	Enable	12	TRUN	590	689	-	899	168

1. Performance and utilization data are generated targeting a LFXP10E-4F256C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP family.

Ordering Information

Family	Part Number
LatticeECP3	DAFIR-GEN-E3-U2
LatticeECP2M	DAFIR-GEN-PM-U2
LatticeECP2	DAFIR-GEN-P2-U2
LatticeECP/EC	DAFIR-GEN-E2-U2
LatticeSC	DAFIR-GEN-SC-U2
LatticeXP2	DAFIR-GEN-X2-U2
LatticeXP	DAFIR-GEN-XM-U2

IP Version: 2.2
Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the **IP Express Quick Start Guide**.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.