# CPC9909EB
## Hi-Brightness, Off-Line LED Driver Evaluation Board User's Guide

## Specifications

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input Voltage | | | | |
| AC | - | - | 265 | $V_{rms}$ |
| DC | 15 | - | 375 | $V_{DC}$ |
| Load Current | - | - | 350 | mA |
| Efficiency | - | 90 | - | % |

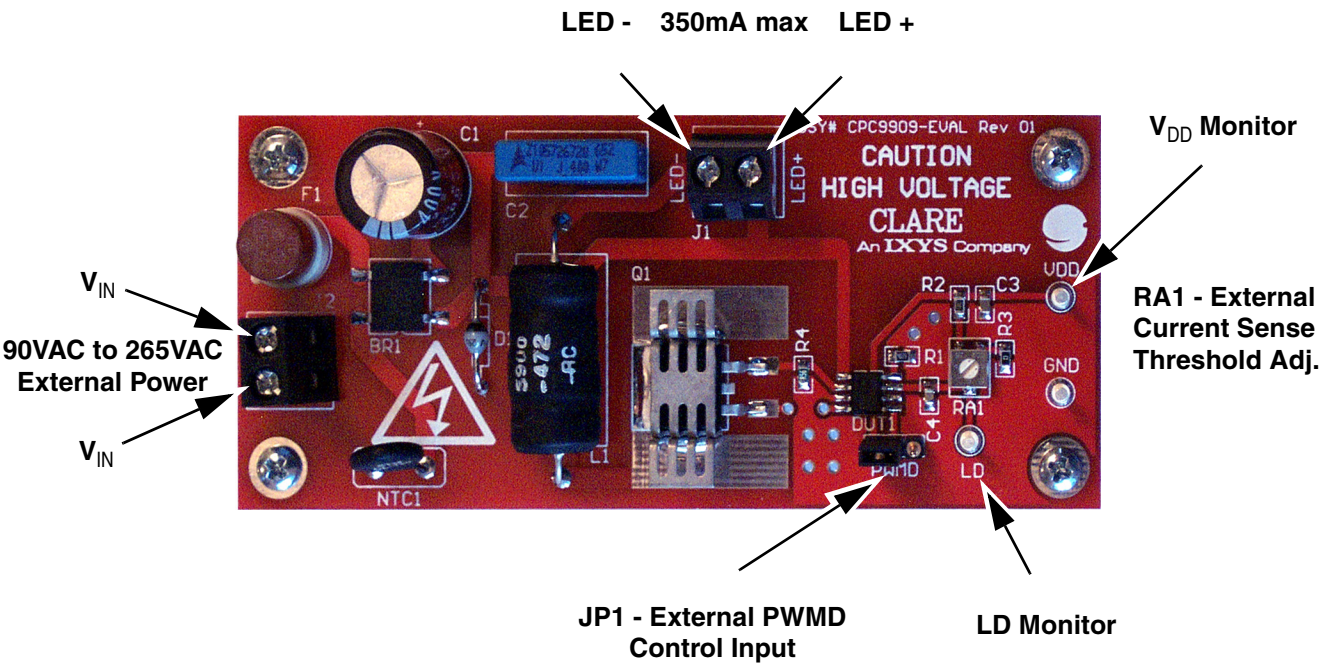
**WARNING!**
This demonstration board must be powered through an isolation transformer before connecting any external AC instrumentation

## Introduction

Clare's CPC9909 Evaluation Board contains all the necessary circuitry to demonstrate all the features of CPC9909 High Brightness (HB), Off-Line LED driver. The CPC9909 IC architecture includes pulse frequency modulation (PFM) with a constant peak-current control scheme. This regulation scheme is inherently stable, allowing the driver to operate above 50% duty cycle without open-loop instability or sub-harmonic oscillations. This greatly increases the number of LEDs in series that can be driven by the CPC9909 and by this Evaluation Board.

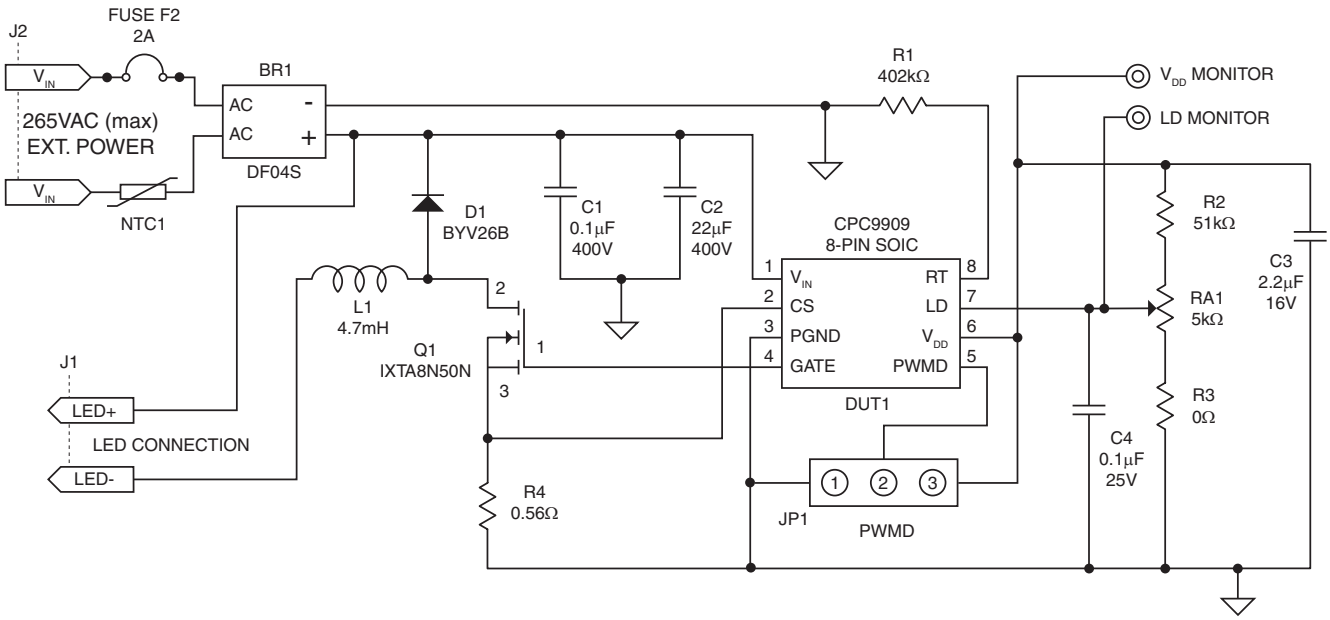
Linear LED dimming can be achieved either by adjusting the on-board potentiometer, RA1, or by adjusting the voltage at the LD pin. In addition, PWM dimming can be achieved with a user-applied TTL-level, low frequency, pulse-width-modulated square wave signal between JP1-1 (GND) and JP1-2 (connected to the PWMD pin of the CPC9909).

**Figure 1. CPC9909 Evaluation Board, Top View**



# 1. Setup

## 1.1 CPC9909 Evaluation Board Schematic




## 1.2 Demo Board Connection Descriptions

| Name | Description |
|---|---|
| J1 | |
| LED+ | LED+ is connected to the anode end of the LED string |
| LED- | LED- is connected to the cathode end of the LED string |
| J2 * | |
| $V_{IN}$ | AC input: $265V_{rms}$ (max) **- or -** DC input: $15V_{DC}$ to $375V_{DC}$ (not DC polarity sensitive) |
| $V_{IN}$ | AC input: $265V_{rms}$ (max) **- or -** DC input: $15V_{DC}$ to $375V_{DC}$ (not DC polarity sensitive) |
| $V_{DD}$ Monitor | This pin is connected to the $V_{DD}$ pin of the CPC9909. The typical voltage regulator output is set at 7.8V, and can be used to provide bias voltage to external circuits. |
| LD Monitor | The LD monitor pin is connected to the wiper of the potentiometer, RA1. The CPC9909 has a preset voltage level $V_{CS(high)}$ which is typically set at 250mV. The LED drive current can be reduced in a linear fashion by adjusting RA1, thus pulling the LD pin down to below 250mV. |
| JP1 | External PWMD Control Input:<br>• Jumper pins 1&2 to disable the CPC9909 and place it into a low-current, standby state.<br>• Jumper pins 2&3 to enable the CPC9909; dimming is accomplished with the potentiometer, RA1.<br>• No Jumper. Apply a TTL-level PWM signal in the 500Hz range to pin 2 to enable dimming under PWM control. The PWM signal's duty cycle determines LED brightness. |
| GND | This pin is connected to the ground of buck LED driver. |

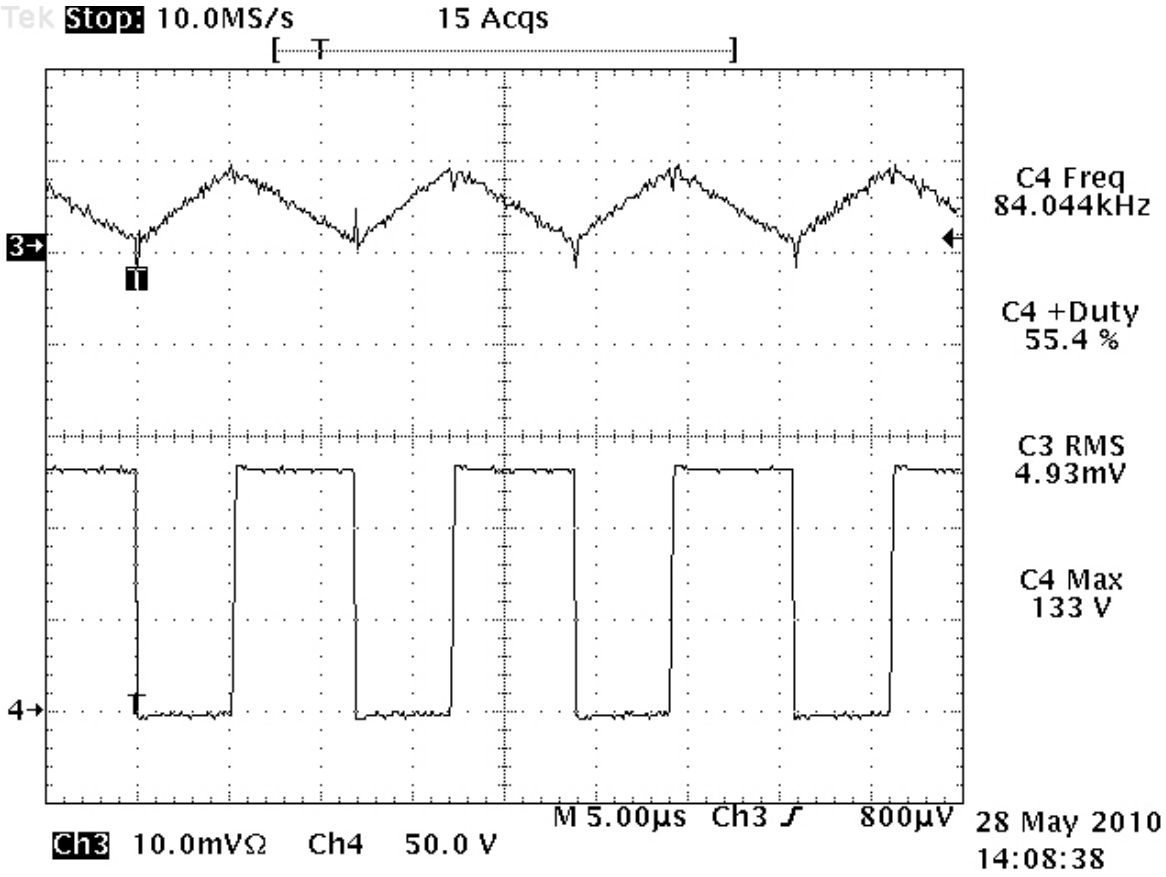
***** Note that the demo board and the connected LED's are not isolated from line voltage, therefore an isolation transformer should be used to protect the user and all measuring instruments such as oscilloscope and multi-meters.

### 1.3 CPC9909 Evaluation Board Bill of Materials

| Designator | Qty. | Description | Part Number |
|---|---|---|---|
| BR1 | 1 | IC, Rectifier Bridge, 400V, 1.5A | DF04S |
| C1 | 1 | Capacitor, Polarized, 0.5 WD, 22µF, 400V | EXXG401ELL22CMK20S |
| C2 | 1 | Capacitor, Axial, 0.6 x 0.35, 0.1µF, 400V | B32652A4104J |
| C3 | 1 | Capacitor, 2.2µF, 16V | GRM21BR61C225KA88L |
| C4 | 1 | Capacitor, 0.1µF, 25V | GRM216F51E104ZA01D |
| D1 | 1 | BYV26B, 1A, 400V | BYV26B-TR |
| DUT1 | 1 | Clare CPC9909 | CPC9909 |
| F1 | 1 | Fuse Holder, Thru-Hole, PC Mount | 5600000100 |
| F2 | 1 | Fuse, 2A, 250V | 37312000410 |
| J1 | 1 | 2-Position Terminal Block | 39544-3002 |
| J2 | 1 | 2-Position Terminal Block | 39544-3002 |
| JP1 | 1 | 3-Position Jumper | 800-10-064-10-001000 w/shunt 929950-00 |
| JP2 | 1 | Wire Jumper, 0.3 | (Included) |
| L1 | 1 | Inductor, Axial, 4.7mH, 0.4A | 5900-472-RC |
| NTC1 | 1 | Thermistor, Inrush Current Limiter | CL-130 |
| Q1 | 1 | IXYS FET, With Aavid Thermalloy Heat Sink | IXTA8N50P w/heatsink 573100D00000 |
| R1 | 1 | Resistor, Surface Mount, 402k | RC0805FR-07402KL |
| R2 | 1 | Resistor, Surface Mount, 51k | RC0805FR-0751K1L |
| R3 | 1 | Resistor, Surface Mount, 0 Ohms | RC0805JR-070RL |
| R4 | 1 | Resistor, Surface Mount, 0.56 | RL1220S-R56-F |
| RA1 | 1 | Variable Resistor, 5k | 3314G-1-502E |
| TP2 | 1 | Test Point | 10-138-2-01 |
| TP3 | 1 | Test Point | 10-138-2-01 |
| TP4 | 1 | Test Point | 10-138-2-01 |

## 2. Performance

### 2.1 Typical Output Waveforms




**Input Voltage = 110VAC**
**CH3: LED Current, 10mVΩ = 100mA/div**
**CH4: MOSFET drain voltage, 50V/div**
**Frequency = 84kHz, positive duty cycle = 55.4%**

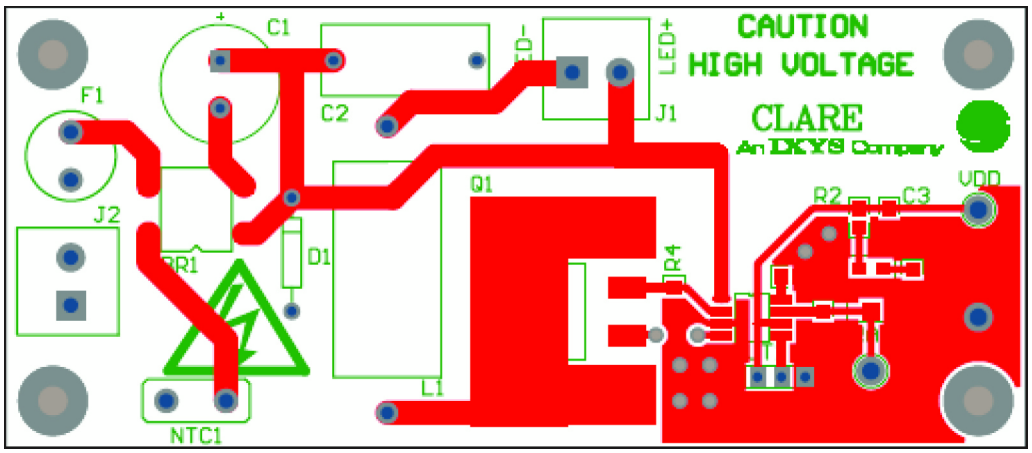
## 3. PC Board Layout Considerations

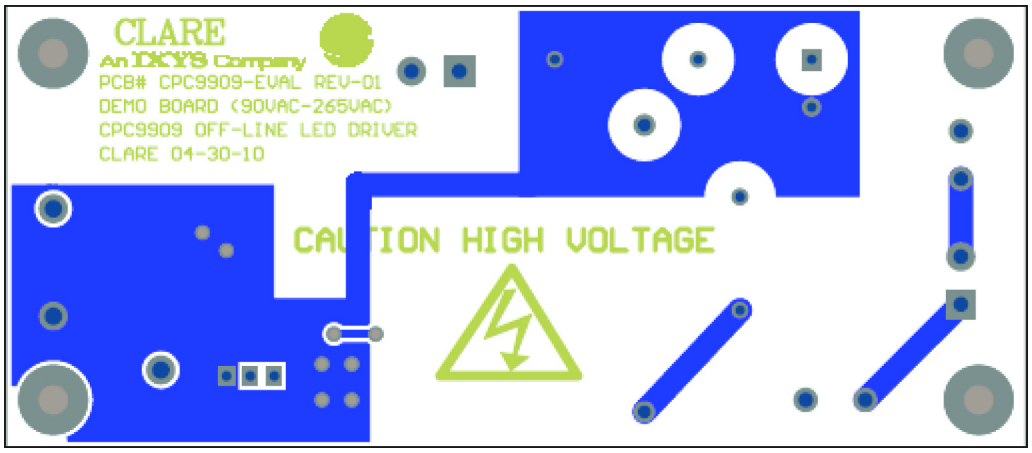
Proper PCB layout should include a short, thick trace from pin 4 of the CPC9909 internal gate driver to the gate of the external power MOSFET.

In addition, the current sense resistor, connected to pin 2, and the one-shot programming resistor, connected to pin 8, should be placed as close as possible to pin 2 and pin 8 respectively to minimize any noise coupling to the CS and RT pins.

Please note that in some cases, during turn-off transitions of the external power MOSFET, high current spikes from the external inductor can develop. In this case, the design may require placing a high voltage capacitor, 100nF or higher, between the LED+ and LED- terminals to filter these current spikes.

## 4. PC Board Layout




**For additional information please visit our website at: www.clare.com**



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