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# Clock Generator for PowerQUICC and PowerPC **Microprocessors and Microcontrollers**

The MPC9817 is a PLL-based clock generator specifically designed for Freescale Semiconductor Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates the microprocessor input clock and other microprocessor system and bus clocks at any one of four output frequencies. These frequencies include the popular 33- and 66-MHz PCI bus frequencies. The device offers five low-skew clock outputs plus three reference outputs. The clock input reference is 25 MHz and may be derived from an external source or by the addition of a 25-MHz crystal to the on-chip crystal oscillator. The extended temperature range of the MPC9817 supports telecommunication and networking requirements.

#### Features

- 5 LVCMOS outputs for processor and other system circuitry •
- 3 Buffered 25-MHz reference clock outputs
- Crystal oscillator or external reference input
- 25-MHz input reference frequency
- Selectable output frequencies include: 25, 33, 50, or 66 MHz •
- Low cycle-to-cycle and period jitter
- Package: 20-lead SSOP
- 3.3-V supply
- Supports computing, networking, and telecommunications applications
- Ambient temperature range: -40°C to +85°C

#### **Functional Description**

The MPC9817 uses a PLL with a 25-MHz input reference frequency to generate a single bank of five configurable LVCMOS output clocks. The output frequency of this bank is configurable to either 25, 33, 50, or 66 MHz by two FSEL pins. The 25-MHz reference may be either an external frequency source or a 25-MHz crystal. The 25-MHz crystal is directly connected to the XTAL IN and XTAL OUT pins with no additional components required. An external reference may be applied to the XTAL IN pin with the XTAL OUT pin left floating. The input reference, whether provided by a crystal or an external input, is also directly buffered to a second bank of three LVCMOS outputs. These outputs may be used as the clock source for processor I/O applications such as an Ethernet PHY. When FSEL0 and FSEL1 are both configured low, the QA outputs are directly fed from the input reference providing a total of eight low-skew 25-MHz outputs. For all other combinations of FSEL0 and FSEL1 the single-ended LVCMOS outputs provide five low-skew outputs for use in driving a microprocessor or microcontroller clock input as well as other system components.

The MPC9817 is packaged in a 20-lead SSOP package.





#### Figure 1. MPC9817 Logic Diagram

#### Table 1. Pin Configurations

Pin	I/O	Туре	Function			
QA0, QA1, QA2, QA3, QA4	Output	LVCMOS	Clock Outputs			
QREF0, QREF1, QREF2	Output	LVCMOS	Reference Output (25 MHz)			
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin			
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin			
FSEL0, FSEL1	Input	LVCMOS	Configures Bank A Clock Output Frequency (pull-up)			
MR/OE	Input	LVCMOS	Enables All Outputs (pull-down)			
V <sub>DD</sub>	_	_	3.3-V Supply			
GND	—	—	Ground			

#### Table 2. Function Table

Control	Default	00	01	10	11
FSEL0,FSEL1	11	25 MHz fed directly from reference input, PLL disabled	33 MHz	50 MHz	66 MHz



Figure 2. MPC9817 20-Lead SSOP Package Pinout (Top View)

#### **MPC9817 OPERATION**

#### **Crystal Oscillator**

The MPC9817 features a fully integrated Pierce oscillator to minimize system implementation costs. Other than the addition of a 25-MHz crystal, no external components are required. The crystal selection should be: 25 MHz, parallel resonant type with a load specification of  $C_L = 10$  pF. Crystals with a load specification of  $C_L = 20$  pF may be used, however,

the reference frequency may be higher than the specified 25 MHz. Externally supplied capacitors on both the XTAL\_IN and XTAL\_OUT pins may be used to trim the frequency as desired.

The crystal should be located as close to the MPC9817 XTAL\_IN and XTAL\_OUT pins as possible to avoid any board level parasitic.

#### **Table 3. Crystal Specifications**

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Shunt Capacitance (CL)	5–7 pF
Load Capacitance (C <sub>O</sub> )	10 pF
Equivalent Series Resistance (ESR)	20–60 Ω

#### **Power Supply Bypassing**

The MPC9817 should have all  $V_{DD}$  pins bypassed with 0.01 capacitors and a minimum of one 1.0 capacitor for the overall package. All capacitors should be located as close to the SSOP pins as possible.

#### **External Clock Source**

An external reference source of 25 MHz may be applied to the XTAL\_IN pin. In this mode of operation, the XTAL\_OUT pin should be left floating.

Symbol	Characteristics	Min	Max	Unit	Condition
V <sub>DD</sub>	Supply Voltage	-0.3	3.8	V	
I <sub>IN</sub>	DC Input Current	_	±20	mA	
I <sub>OUT</sub>	DC Output Current	—	±75	mA	
Τ <sub>S</sub>	Storage Temperature	-65	125	°C	

#### Table 4. Absolute Maximum Ratings<sup>(1)</sup>

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

#### **Table 5. General Specifications**

Symbol	Characteristics	Min	Тур	Max	Unit	Condition
V <sub>TT</sub>	Output Termination Voltage	—	$V_{DD} \div 2$	—	V	
MM	ESD Protection (machine model)	200	_	—	V	
HBM	ESD Protection (human body model)	2000	—	—	V	
LU	Latch-Up Immunity	200	_	—	mA	
C <sub>IN</sub>	Input Capacitance	—	4	—	pF	Inputs
$\theta_{JA}$	Thermal Resistance (junction-to-ambient)	—	80.8	—	°C/W	
т <sub>с</sub>	Ambient Temperature	-40		85	°C	

#### Table 6. DC Characteristics (V<sub>DD</sub> = $3.3 \text{ V} \pm 5\%$ , T<sub>A</sub> = $-40^{\circ}$ to $+85^{\circ}$ C)

Symbol	Characteristics	Min	Тур	Max	Unit	Condition
V <sub>IH</sub>	Input High Voltage (XTAL_IN)	2.4	_	$V_{DD} + 0.3$	V	Input threshold = $V_{DD}/2$
V <sub>IH</sub>	Input High Voltage	2.0	_	$V_{DD}$ + 0.3	V	
V <sub>IL</sub>	Input Low Voltage	—	_	0.8	V	LVCMOS
I <sub>IN</sub>	Input Current <sup>(1)</sup>	_	_	150	μΑ	$V_{IN} = V_{DDL}$ or GND
V <sub>OH</sub>	Output High Voltage	2.4	-	—	V	$I_{OH} = -12 \text{ mA}$
V <sub>OL</sub>	Output Low Voltage	—	_	0.4	V	I <sub>OL</sub> = 12 mA
Z <sub>OUT</sub>	Output Impedance	_	14	—	Ω	
I <sub>DD</sub>	Maximum Quiescent Supply Current	—	8.0	15.0	mA	V <sub>DD</sub> pins

1. Inputs have pull-down resistors affecting the input current.

Symbol	Characteristics	Min	Тур	Max	Unit	Condition
Input and 0	Input and Output Timing Specification					
f <sub>ref</sub>	Input Reference Frequency 25 MHz Input XTAL Input		25 25		MHz MHz	
f <sub>VCO</sub>	VCO Frequency Range	_	400	—	MHz	
f <sub>MCX</sub>	Output Frequency (QAx) FSEL0, FSEL1 = 00 FSEL0, FSEL1 = 01 FSEL0, FSEL1 = 01 FSEL0, FSEL1 = 10 FSEL0, FSEL1 = 11 Output Frequency (QREFx)		25 33 50 66 25		MHz MHz MHz MHz MHz	PLL locked
f <sub>refPW</sub>	Reference Input Pulse Width	10	—	—	ns	@ 25 MHz
DC	Output Duty Cycle	47.5	50	52.5	%	
f <sub>out</sub>	Output Frequency Accuracy Crystal <sup>(3)</sup> External Reference			100 0	ppm ppm	With recommended crystal see Table 3
PLL Specif	fications					
BW	PLL Closed Loop Bandwidth <sup>(4)</sup>		500		kHz	
t <sub>LOCK</sub>	Maximum PLL Lock Time			10	ms	
Skew and	Jitter Specifications					
t <sub>sk(O)</sub>	Output-to-Output Skew (within a bank)			100	ps	
t <sub>sk(O)</sub>	Output-to-Output Skew (between bank A and bank Ref)			200		FSEL0, FSEL1 = 00
t <sub>JIT(CC)</sub>	C) Cycle-to-Cycle Jitter			150	ps	@ 25 MHz Input Reference Q <sub>A</sub> output
t <sub>JIT(PER)</sub>	ER) Period Jitter			100	ps	@ 25 MHz Input Reference Q <sub>A</sub> output
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time			1	ns	20% to 80%

### Table 7. AC Characteristics<sup>(1)</sup> (2) ( $V_{DD} = 3.3 \text{ V} \pm 5\%$ , $T_A = -40^{\circ}$ to +85°C)

1. AC characteristics are design targets and pending characterization.

2. AC characteristics apply for parallel output termination of 50  $\Omega$  to V\_TT.

3. Based upon recommended crystal specifications as outlined in operation section.

4. -3 dB point of PLL transfer characteristics.



Figure 3. MPC9817 AC Test Reference (LVCMOS Outputs)

#### Table 8. MPC9817 Pin List

Pin	Description			
1	XTAL_IN			
2	XTAL_OUT			
3	FSEL0			
4	V <sub>DD</sub>			
5	FSEL1			
6	QREF2			
7	GND			
8	QREF1			
9	QREF0			
10	V <sub>DD</sub>			

Pin	Description
11	GND
12	MR/OE
13	QA0
14	V <sub>DD</sub>
15	QA1
16	QA2
17	GND
18	QA3
19	QA4
20	V <sub>DD</sub>



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