

8-CHANNEL HIGH DEFINITION AUDIO CODEC

STAC9220

DESCRIPTION

The STAC9220 is a high fidelity, 8-channel audio CODEC compatible with Intel's High Definition (HD) Audio Interface. The STAC9220 CODEC provide stereo 24-bit resolution with sample rates up to 192 KHz. SPDIF I/O provides connectivity to consumer electronic equipment. The STAC9220 CODEC incorporate IDT's proprietary $\Sigma\Delta$ technology to achieve an estimated DAC SNR in excess of 95dB. The STAC9220 CODECs provide high quality, HD Audio capability to notebook and media centric desktop PC applications.

FEATURES

- **High performance $\Sigma\Delta$ technology**
 - 95dB DAC SNR
- **Intel HD Audio interface**
- **Eight Channel (4 DAC pairs and 2 stereo ADCs) with 24-bit resolution**
 - Supports 7.1 Audio
 - Supports 5.1 Audio with Auxiliary channel for separate audio stream or Real Time Communication (RTC) channel
- **Sample Rates Up to 192 KHz**
- **Integrated Headphone Amps**
- **Stereo Microphone**
 - Supports Stereo Microphone
 - Microphone Boost 0, 10, 20, 30, 40dB
- **Direct CDROM Recording Mixerless Design**
- **SPDIF In and Out**
- **Two-Pin Volume Up/Down Control**
- **Impedance Sensing**
- **Universal Jacks™ Functionality for Jack Retasking**
 - Headphone, Line Out, Line In & Microphone
 - Pins 35/36
 - Pins 39/41
 - Line Out, Line In and Microphone Support
 - Pins 16/17 (with strong line out)
 - Pins 23/24
 - Pins 21/22
 - Line In/MIC Support
 - Pins 14/15
- **Four Adjustable VREF Out pins for Microphone Bias**
- **Digital PC Beep to all outputs**
- **+3.3 V and +5 V analog power supply options**
- **48-pin LQFP package (7mm x 7mm)**

THIRD PARTY SOFTWARE SUPPORT

- **WOW™ and Tru Surround™ from SRS**
- **Intellisonic Microphone Beam Forming from Knowles™**
- **Maxx BASS™ from Waves**
- **Dolby Technologies**
 - Dolby Headphone™
 - Dolby ProLogic II™
 - Dolby Virtual Speaker™
- **Smart Stream™ from Sonic Focus**

Table of Contents

1. FEATURES	11
1.1. Overview	11
1.2. Features	11
1.3. Third Party Software Support	12
1.4. Description	12
2. CHARACTERISTICS	14
2.1. Electrical Specifications	14
2.1.1. Absolute Maximum Ratings	14
2.1.2. Recommended Operation Conditions	14
2.2. STAC9220 5V Analog Performance Characteristics	15
2.3. STAC9220 4V Analog Performance Characteristics	17
2.4. STAC9220 3.3V Analog Performance Characteristics	19
3. POWER CONSUMPTION	21
3.1. Digital	21
3.2. Analog: AVDD = 5 V	21
3.3. Analog: AVDD = 3.3 V	21
4. DETAILED DESCRIPTION	22
4.1. Audio Jack Presence Detect	22
4.2. SPDIF Output	22
4.3. Universal Jacks™	23
5. FUNCTIONAL BLOCK DIAGRAMS AND CONNECTION DIAGRAMS	24
5.1. STAC9220 Functional Block Diagram	24
5.2. STAC9220 Typical Connection Diagram for 48-pin LQFP	25
5.3. STAC9220 Split Independent Power Supply for 48-pin LQFP	26
6. WIDGET INFORMATION	27
6.1. STAC9220 Widget Diagrams	27
6.2. Widget List STAC9220	28
6.3. Root Node (NID = 0x00)	28
6.3.1. Root ID	29
6.3.2. Root RevID	29
6.3.3. Root NodeInfo	30
6.4. AFG Node (NID = 0x01)	30
6.4.1. AFG Reset	30
6.4.2. AFG NodeInfo	31
6.4.3. AFG Type	31
6.4.4. AFG Cap	32
6.4.5. AFG PCMCap	33
6.4.6. AFG Stream	34
6.4.7. AFG InAmpCap	34
6.4.8. AFG SupPwrState	35
6.4.9. AFG GPIOCnt	35
6.4.10. AFG GPIO Polarity	36
6.4.11. AFG OutAmpCap	38
6.4.12. AFG PwrState	39
6.4.13. AFG UnsolResp	39
6.4.14. AFG GPIO	40
6.4.15. AFG GPIOEn	41
6.4.16. AFG GPIODir	42
6.4.17. AFG GPIOWakeEn	42
6.4.18. AFG GPIOUnsol	43
6.4.19. AFG GPIOSlicky	44
6.4.20. AFG SubID	45
6.5. DAC0 Node (NID = 0x02)	46

6.5.1. DAC0 Cnvtr	46
6.5.2. DAC0 AmpRight	47
6.5.3. DAC0 AmpLeft	48
6.5.4. DAC0 WCap	48
6.5.5. DAC0 PwrState	49
6.5.6. DAC0 CnvtrID	50
6.5.7. DAC0 LR	50
6.6. DAC1 Node (NID = 0x03)	51
6.6.1. DAC1 Cnvtr	51
6.6.2. DAC1 AmpRight	52
6.6.3. DAC1 AmpLeft	53
6.6.4. DAC1 WCap	53
6.6.5. DAC1 PwrState	54
6.6.6. DAC1 CnvtrID	55
6.6.7. DAC1 LR	55
6.7. DAC2 Node (NID = 0x04)	56
6.7.1. DAC2 Cnvtr	56
6.7.2. DAC2 AmpRight	57
6.7.3. DAC2 AmpLeft	58
6.7.4. DAC2 WCap	58
6.7.5. DAC2 PwrState	59
6.7.6. DAC2 CnvtrID	60
6.7.7. DAC2 LR	60
6.8. DAC3 Node (NID = 0x05)	61
6.8.1. DAC3 Cnvtr	61
6.8.2. DAC3 AmpRight	62
6.8.3. DAC3 AmpLeft	63
6.8.4. DAC3 WCap	63
6.8.5. DAC3 PwrState	64
6.8.6. DAC3 CnvtrID	65
6.8.7. DAC3 LR	65
6.9. ADC0 Node (NID = 0x06)	66
6.9.1. ADC0 Cnvtr	66
6.9.2. ADC0 WCap	67
6.9.3. ADC0 ConLst	68
6.9.4. ADC0 ConLstEntry	69
6.9.5. ADC0 ProcState	69
6.9.6. ADC0 PwrState	70
6.9.7. ADC0 CnvtrID	71
6.10. ADC1 Node (NID = 0x07)	71
6.10.1. ADC1 Cnvtr	71
6.10.2. ADC1 WCap	72
6.10.3. ADC1 ConLst	73
6.10.4. ADC1 ConLstEntry	74
6.10.5. ADC1 ProcState	74
6.10.6. ADC1 PwrState	75
6.10.7. ADC1 CnvtrID	76
6.11. SPDIFOut Node (NID = 0x08)	76
6.11.1. SPDIFOut Cnvtr	76
6.11.2. SPDIFOut WCap	77
6.11.3. SPDIFOut PCM	78
6.11.4. SPDIFOut Stream	80
6.11.5. SPDIFOut CnvtrID	80
6.11.6. SPDIFOut DigCnvtr	81
6.12. Reserved Node (NID = 0x09)	81

6.13. PortA Node (NID = 0x0A)	81
6.13.1. PortA WCap	82
6.13.2. PortA PinCap	83
6.13.3. PortA ConLst	83
6.13.4. PortA ConLstEntry	84
6.13.5. PortA PinWCntrl	84
6.13.6. PortA UnsolResp	85
6.13.7. PortA ChSense	86
6.13.8. PortA ConfigDefault	87
6.14. PortB Node (NID = 0x0B)	87
6.14.1. PortB WCap	87
6.14.2. PortB PinCap	88
6.14.3. PortB ConLst	89
6.14.4. PortB ConLstEntry	90
6.14.5. PortB PinWCntrl	90
6.14.6. PortB UnsolResp	91
6.14.7. PortB ChSense	92
6.14.8. PortB ConfigDefault	92
6.15. PortC Node (NID = 0x0C)	93
6.15.1. PortC WCap	93
6.15.2. PortC PinCap	94
6.15.3. PortC ConLst	95
6.15.4. PortC ConLstEntry	95
6.15.5. PortC PinWCntrl	96
6.15.6. PortC UnsolResp	97
6.15.7. PortC ChSense	97
6.15.8. PortC ConfigDefault	98
6.16. PortD Node (NID = 0x0D)	99
6.16.1. PortD WCap	99
6.16.2. PortD PinCap	100
6.16.3. PortD ConLst	101
6.16.4. PortD ConLstEntry	101
6.16.5. PortD PinWCntrl	102
6.16.6. PortD UnsolResp	103
6.16.7. PortD ChSense	103
6.16.8. PortD ConfigDefault	104
6.17. PortE Node (NID = 0x0E)	105
6.17.1. PortE WCap	105
6.17.2. PortE PinCap	106
6.17.3. PortE PinWCntrl	107
6.17.4. PortE UnsolResp	107
6.17.5. PortE ChSense	108
6.17.6. PortE ConfigDefault	108
6.18. PortF Node (NID = 0x0F)	109
6.18.1. PortF WCap	109
6.18.2. PortF PinCap	110
6.18.3. PortF ConLst	111
6.18.4. PortF ConLstEntry	111
6.18.5. PortF PinWCntrl	112
6.18.6. PortF UnsolResp	113
6.18.7. PortF ChSense	113
6.18.8. PortF ConfigDefault	114
6.19. DigOut0 Node (NID = 0x10)	115
6.19.1. DigOut0 WCap	115
6.19.2. DigOut0 PinCap	116

6.19.3. DigOut0 ConLst	117
6.19.4. DigOut0 ConSelectCtrl	117
6.19.5. DigOut0 ConLstEntry	117
6.19.6. DigOut0 PinWCntrl	118
6.19.7. DigOut0 ConfigDefault	118
6.20. DigIn Node (NID = 0x11)	119
6.20.1. DigIn WCap Command	119
6.20.2. DigIn PinCap	120
6.20.3. DigIn PwrState	121
6.20.4. DigIn PinWCntrl	122
6.20.5. DigIn UnsolResp	122
6.20.6. DigIn ChSense	123
6.20.7. DigIn EAPD	123
6.20.8. DigIn ConfigDefault	124
6.21. ADC0Mux Node (NID = 0x12)	125
6.21.1. ADC0Mux WCap	125
6.21.2. ADC0Mux ConLst	126
6.21.3. ADC0Mux AmpCap	126
6.21.4. ADC0Mux AmpRight	127
6.21.5. ADC0Mux AmpLeft	128
6.21.6. ADC0Mux ConSelectCtrl	128
6.21.7. ADC0Mux ConLstEntry0	129
6.21.8. ADC0Mux ConLstEntry4	129
6.22. ADC1Mux Node (NID = 0x13)	129
6.22.1. ADC1Mux WCap	130
6.22.2. ADC1Mux ConLst	131
6.22.3. ADC1Mux AmpCap	131
6.22.4. ADC1Mux AmpRight	132
6.22.5. ADC1Mux AmpLeft	132
6.22.6. ADC1Mux ConSelectCtrl	133
6.22.7. ADC1Mux ConLstEntry0	133
6.22.8. ADC1Mux ConLstEntry4	133
6.23. PCBEEP Node (NID = 0x14)	134
6.23.1. PCBEEP Amp	134
6.23.2. PCBEEP WCap	134
6.23.3. PCBEEP AmpCap	135
6.23.4. PCBEEP Gen	136
6.24. CD Node (NID = 0x15)	136
6.24.1. CD WCap	136
6.24.2. CD PinCap	137
6.24.3. CD PinWCntrl	138
6.24.4. CD ConfigDefault	139
6.25. VolumeKnob Node (NID = 0x16)	139
6.25.1. VolumeKnob WCap	139
6.25.2. VolumeKnob VolKnobCap	140
6.25.3. VolumeKnob ConLst	140
6.25.4. VolumeKnob ConLstEntry	141
6.25.5. VolumeKnob UnsolResp	141
6.25.6. VolumeKnob Cntrl	142
6.26. ADC0Vol Node (NID = 0x17)	143
6.26.1. ADC0Vol WCap	143
6.26.2. ADC0Vol ConLst	144
6.26.3. ADC0Vol AmpRight	144
6.26.4. ADC0Vol AmpLeft	145
6.26.5. ADC0Vol ConLstEntry	145

6.26.6. ADC0Vol LR	146
6.27. ADC1Vol Node (NID = 0x18)	146
6.27.1. ADC1Vol WCap	146
6.27.2. ADC1Vol ConLst	147
6.27.3. ADC1Vol AmpRight	148
6.27.4. ADC1Vol AmpLeft	148
6.27.5. ADC1Vol ConLstEntry	149
6.27.6. ADC1Vol LR	149
7. ORDERING INFORMATION	150
7.1. STAC9220 Part Order Numbers	150
8. PIN INFORMATION	151
8.1. STAC9220 Pin Diagram	151
8.2. Pin Table for STAC9220	151
9. PACKAGE DRAWINGS	154
9.1. 48-Pin LQFP	154
10. SOLDER REFLOW PROFILE	155
10.1. Standard Reflow Profile Data	155
10.2. Pb Free Process - Package Classification Reflow Temperatures	156
11. REVISION HISTORY	157

List of Figures

Figure 1. Functional Block Diagram STAC9220	27
Figure 2. Typical Connection Diagram STAC9220	28
Figure 3. Split Independent Power Supply STAC9220	29
Figure 4. Widget Diagram STAC9220	30
Figure 5. 48-Pin LQFP Package Outline and Package Dimensions	157
Figure 6. Solder Reflow Profile	158

List of Tables

Table 1. Digital Power Consumption	24
Table 2. Analog Power Consumption 5V	24
Table 3. Analog Power Consumption 3.3V	24
Table 4. Audio Jack Presence Detect	25
Table 5. High Definition Audio Widget	31
Table 6. Root ID Command Verb Format	32
Table 7. Root ID Command Response Format	32
Table 8. Root RevID Command Verb Format	32
Table 9. Root RevID Command Response Format	32
Table 10. Root NodeInfo Command Verb Format	33
Table 11. Root NodeInfo Command Response Format	33
Table 12. AFG Reset Command Verb Format	33
Table 13. AFG Reset Command Response Format	34
Table 14. AFG NodeInfo Command Verb Format	34
Table 15. AFG NodeInfo Command Response Format	34

Table 16. AFG Type Command Verb Format	34
Table 17. AFG Type Command Response Format	35
Table 18. AFG Cap Command Verb Format	35
Table 19. AFG Cap Command Response Format	35
Table 20. AFG PCMCap Command Verb Format	36
Table 21. AFG PCMCap Command Response Format	36
Table 22. AFG Stream Command Verb Format	37
Table 23. AFG Stream Command Response Format	37
Table 24. AFG InAmpCap Command Verb Format	37
Table 25. AFG InAmpCap Command Response Format	37
Table 26. AFG SupPwrState Command Verb Format	38
Table 27. AFG SupPwrState Command Response Format	38
Table 28. AFG GPIOCnt Command Verb Format	38
Table 29. AFG GPIOCnt Command Response Format	39
Table 30. AFG GPIO Polarity Command Verb Format	39
Table 31. AFG GPIO Polarity Command Response Format	40
Table 32. AFG OutAmpCap Command Verb Format	41
Table 33. AFG OutAmpCap Command Response Format	41
Table 34. AFG PwrState Command Verb Format	42
Table 35. AFG PwrState Command Response Format	42
Table 36. AFG UnsolResp Command Verb Format	42
Table 37. AFG UnsolResp Command Response Format	43
Table 38. AFG GPIO Command Verb Format	43
Table 39. AFG GPIO Command Response Format	43
Table 40. AFG GPIOEn Command Verb Format	44
Table 41. AFG GPIOEn Command Response Format	44
Table 42. AFG GPIODir Command Verb Format	45
Table 43. AFG GPIODir Command Response Format	45
Table 44. AFG GPIOWakeEn Command Verb Format	45
Table 45. AFG GPIOWakeEn Command Response Format	46
Table 46. AFG GPIOUnsol AFG GPIOUnsol Command Verb Format	46
Table 47. AFG GPIOUnsol Command Response Format	47
Table 48. AFG GPIOSticky Command Verb Format	47
Table 49. AFG GPIOSticky Command Response Format	48
Table 50. AFG SubID Command Verb Format	48
Table 51. AFG SubID Command Response Format	49
Table 52. DAC0 Cnvtr Command Verb Format	49
Table 53. DAC0 Cnvtr Command Response Format	49
Table 54. DAC0 AmpRight Command Verb Format	50
Table 55. DAC0 AmpRight Command Response Format	50
Table 56. DAC0 AmpLeft Command Verb Format	51
Table 57. DAC0 AmpLeft Command Response Format	51
Table 58. DAC0 WCap Command Verb Format	51
Table 59. DAC0 WCap Command Response Format	51
Table 60. DAC0 PwrState Command Verb Format	52
Table 61. DAC0 PwrState Command Response Format	52
Table 62. DAC0 CnvtrID Command Verb Format	53
Table 63. DAC0 CnvtrID Command Response Format	53
Table 64. DAC0 LR Command Verb Format	53
Table 65. DAC0 LR Command Response Format	54
Table 66. DAC1 Cnvtr Command Verb Format	54
Table 67. DAC1 Cnvtr Command Response Format	54
Table 68. DAC1 AmpRight Command Verb Format	55
Table 69. DAC1 AmpRight Command Response Format	55
Table 70. DAC1 AmpLeft Command Verb Format	56

Table 71. DAC1 AmpLeft Command Response Format	56
Table 72. DAC1 WCap Command Verb Format	56
Table 73. DAC1 WCap Command Response Format	56
Table 74. DAC1 PwrState Command Verb Format	57
Table 75. DAC1 PwrState Command Response Format	57
Table 76. DAC1 CnvtrID Command Verb Format	58
Table 77. DAC1 CnvtrID Command Response Format	58
Table 78. DAC1 LR Command Verb Format	58
Table 79. DAC1 LR Command Response Format	59
Table 80. DAC2 Cnvtr Command Verb Format	59
Table 81. DAC2 Cnvtr Command Response Format	59
Table 82. DAC2 AmpRight Command Verb Format	60
Table 83. DAC2 AmpRight Command Response Format	60
Table 84. DAC2 AmpLeft Command Verb Format	61
Table 85. DAC2 AmpLeft Command Response Format	61
Table 86. DAC2 WCap Command Verb Format	61
Table 87. DAC2 WCap Command Response Format	61
Table 88. DAC2 PwrState Command Verb Format	62
Table 89. DAC2 PwrState Command Response Format	62
Table 90. DAC2 CnvtrID Command Verb Format	63
Table 91. DAC2 CnvtrID Command Response Format	63
Table 92. DAC2 LR Command Verb Format	63
Table 93. DAC2 LR Command Response Format	64
Table 94. DAC3 Cnvtr Command Verb Format	64
Table 95. DAC3 Cnvtr Command Response Format	64
Table 96. DAC3 AmpRight Command Verb Format	65
Table 97. DAC3 AmpRight Command Response Format	65
Table 98. DAC3 AmpLeft Command Verb Format	66
Table 99. DAC3 AmpLeft Command Response Format	66
Table 100. DAC3 WCap Command Verb Format	66
Table 101. DAC3 WCap Command Response Format	66
Table 102. DAC3 PwrState Command Verb Format	67
Table 103. DAC3 PwrState Command Response Format	67
Table 104. DAC3 CnvtrID Command Verb Format	68
Table 105. DAC3 CnvtrID Command Response Format	68
Table 106. DAC3 LR Command Verb Format	68
Table 107. DAC3 LR Command Response Format	69
Table 108. ADC0 Cnvtr Command Verb Format	69
Table 109. ADC0 Cnvtr Command Response Format	69
Table 110. ADC0 WCap Command Verb Format	70
Table 111. ADC0 WCap Command Response Format	70
Table 112. ADC0 ConLst Command Verb Format	71
Table 113. ADC0 ConLst Command Response Format	71
Table 114. ADC0 ConLstEntry Command Verb Format	72
Table 115. ADC0 ConLstEntry Command Response Format	72
Table 116. ADC0 ProcState Command Verb Format	72
Table 117. ADC0 ProcState Command Response Format	73
Table 118. ADC0 PwrState Command Verb Format	73
Table 119. ADC0 PwrState Command Response Format	73
Table 120. ADC0 CnvtrID Command Verb Format	74
Table 121. ADC0 CnvtrID Command Response Format	74
Table 122. ADC1 Cnvtr Command Verb Format	74
Table 123. ADC1 Cnvtr Command Response Format	74
Table 124. ADC1 WCap Command Verb Format	75
Table 125. ADC1 WCap Command Response Format	76
Table 126. ADC1 ConLst Command Verb Format	76
Table 127. ADC1 ConLst Command Response Format	77

Table 128. ADC1 ConLstEntry Command Verb Format	77
Table 129. ADC1 ConLstEntry Command Response Format	77
Table 130. ADC1 ProcState Command Verb Format	77
Table 131. ADC1 ProcState Command Response Format	78
Table 132. ADC1 PwrState Command Verb Format	78
Table 133. ADC1 PwrState Command Response Format	78
Table 134. ADC1 CnvtrID Command Verb Format	79
Table 135. ADC1 CnvtrID Command Response Format	79
Table 136. SPDIFOut Cnvtr Command Verb Format	79
Table 137. SPDIFOut Cnvtr Command Response Format	79
Table 138. SPDIFOut WCap Command Verb Format	80
Table 139. SPDIFOut WCap Command Response Format	81
Table 140. SPDIFOut PCM Command Verb Format	81
Table 141. SPDIFOut PCM Command Response Format	82
Table 142. SPDIFOut Stream Command Verb Format	83
Table 143. SPDIFOut Stream Command Response Format	83
Table 144. SPDIFOut CnvtrID Command Verb Format	83
Table 145. SPDIFOut CnvtrID Command Response Format	83
Table 146. SPDIFOut DigCnvtr Command Verb Format	84
Table 147. SPDIFOut DigCnvtr Command Response Format	84
Table 148. PortA WCap Command Verb Format	85
Table 149. PortA WCap Command Response Format	85
Table 150. PortA PinCap Command Verb Format	86
Table 151. PortA PinCap Command Response Format	86
Table 152. PortA ConLst Command Verb Format	86
Table 153. PortA ConLst Command Response Format	87
Table 154. PortA ConLstEntry Command Verb Format	87
Table 155. PortA ConLstEntry Command Response Format	87
Table 156. PortA PinWCntrl Command Verb Format	87
Table 157. PortA PinWCntrl Command Response Format	88
Table 158. PortA UnsolResp Command Verb Format	88
Table 159. PortA UnsolResp Command Response Format	88
Table 160. PortA ChSense Command Verb Format	89
Table 161. PortA ChSense Command Response Format	89
Table 162. PortA ConfigDefault Command Verb Format	90
Table 163. PortA ConfigDefault Command Response Format	90
Table 164. PortB WCap Command Verb Format	90
Table 165. PortB WCap Command Response Format	91
Table 166. PortB PinCap Command Verb Format	91
Table 167. PortB PinCap Command Response Format	92
Table 168. PortB ConLst Command Verb Format	92
Table 169. PortB ConLst Command Response Format	92
Table 170. PortB ConLstEntry Command Verb Format	93
Table 171. PortB ConLstEntry Command Response Format	93
Table 172. PortB PinWCntrl Command Verb Format	93
Table 173. PortB PinWCntrl Command Response Format	94
Table 174. PortB UnsolResp Command Verb Format	94
Table 175. PortB UnsolResp Command Response Format	94
Table 176. PortB ChSense Command Verb Format	95
Table 177. PortB ChSense Command Response Format	95
Table 178. PortB ConfigDefault Command Verb Format	95
Table 179. PortB ConfigDefault Command Response Format	96
Table 180. PortC WCap Command Verb Format	96
Table 181. PortC WCap Command Response Format	96
Table 182. PortC PinCap Command Verb Format	97

Table 183. PortC PinCap Command Response Format	97
Table 184. PortC ConLst Command Verb Format	98
Table 185. PortC ConLst Command Response Format	98
Table 186. PortC ConLstEntry Command Verb Format	98
Table 187. PortC ConLstEntry Command Response Format	99
Table 188. PortC PinWCntrl Command Verb Format	99
Table 189. PortC PinWCntrl Command Response Format	99
Table 190. PortC UnsolResp Command Verb Format	100
Table 191. PortC UnsolResp Command Response Format	100
Table 192. PortC ChSense Command Verb Format	100
Table 193. PortC ChSense Command Response Format	101
Table 194. PortC ConfigDefault Command Verb Format	101
Table 195. PortC ConfigDefault Command Response Format	101
Table 196. PortD WCap Command Verb Format	102
Table 197. PortD WCap Command Response Format	102
Table 198. PortD PinCap Command Verb Format	103
Table 199. PortD PinCap Command Response Format	103
Table 200. PortD ConLst Command Verb Format	104
Table 201. PortD ConLst Command Response Format	104
Table 202. PortD ConLstEntry Command Verb Format	104
Table 203. PortD ConLstEntry Command Response Format	104
Table 204. PortD PinWCntrl Command Verb Format	105
Table 205. PortD PinWCntrl Command Response Format	105
Table 206. PortD UnsolResp Command Verb Format	106
Table 207. PortD UnsolResp Command Response Format	106
Table 208. PortD ChSense Command Verb Format	106
Table 209. PortD ChSense Command Response Format	107
Table 210. PortD ConfigDefault Command Verb Format	107
Table 211. PortD ConfigDefault Command Response Format	107
Table 212. PortE WCap Command Verb Format	108
Table 213. PortE WCap Command Response Format	108
Table 214. PortE PinCap Command Verb Format	109
Table 215. PortE PinCap Command Response Format	109
Table 216. PortE PinWCntrl Command Verb Format	110
Table 217. PortE PinWCntrl Command Response Format	110
Table 218. PortE UnsolResp Command Verb Format	110
Table 219. PortE UnsolResp Command Response Format	110
Table 220. PortE ChSense Command Verb Format	111
Table 221. PortE ChSense Command Response Format	111
Table 222. PortE ConfigDefault Command Verb Format	111
Table 223. PortE ConfigDefault Command Response Format	112
Table 224. PortF WCap Command Verb Format	112
Table 225. PortF WCap Command Response Format	112
Table 226. PortF PinCap Command Verb Format	113
Table 227. PortF PinCap Command Response Format	113
Table 228. PortF ConLst Command Verb Format	114
Table 229. PortF ConLst Command Response Format	114
Table 230. PortF ConLstEntry Command Verb Format	114
Table 231. PortF ConLstEntry Command Response Format	115
Table 232. PortF PinWCntrl Command Verb Format	115
Table 233. PortF PinWCntrl Command Response Format	115
Table 234. PortF UnsolResp Command Verb Format	116
Table 235. PortF UnsolResp Command Response Format	116
Table 236. PortF ChSense Command Verb Format	116
Table 237. PortF ChSense Command Response Format	117

Table 238. PortF ConfigDefault Command Verb Format	117
Table 239. PortF ConfigDefault Command Response Format	117
Table 240. DigOut0 WCap Command Verb Format	118
Table 241. DigOut0 WCap Command Response Format	118
Table 242. DigOut0 PinCap Command Verb Format	119
Table 243. DigOut0 PinCap Command Response Format	119
Table 244. DigOut0 ConLst Command Verb Format	120
Table 245. DigOut0 ConLst Command Response Format	120
Table 246. DigOut0 ConSelectCtrl Command Verb Format	120
Table 247. DigOut0 ConSelectCtrl Command Response Format	120
Table 248. DigOut0 ConLstEntry Command Verb Format	120
Table 249. DigOut0 ConLstEntry Command Response Format	121
Table 250. DigOut0 PinWCntrl Command Verb Format	121
Table 251. DigOut0 PinWCntrl Command Response Format	121
Table 252. DigOut0 ConfigDefault Command Verb Format	121
Table 253. DigOut0 ConfigDefault Command Response Format	122
Table 254. DigIn WCap Command Verb Format	122
Table 255. DigIn WCap Command Response Format	122
Table 256. DigIn PinCap Command Verb Format	123
Table 257. DigIn PinCap Command Response Format	123
Table 258. DigIn PwrState Command Verb Format	124
Table 259. DigIn PwrState Command Response Format	124
Table 260. DigIn PinWCntrl Command Verb Format	125
Table 261. DigIn PinWCntrl Command Response Format	125
Table 262. DigIn UnsolResp Command Verb Format	125
Table 263. DigIn UnsolResp Command Response Format	125
Table 264. DigIn ChSense Command Verb Format	126
Table 265. DigIn ChSense Command Response Format	126
Table 266. DigIn EAPD Command Verb Format	126
Table 267. DigIn EAPD Command Response Format	126
Table 268. DigIn ConfigDefault Command Verb Format	127
Table 269. DigIn ConfigDefault Command Response Format	127
Table 270. ADC0Mux WCap Command Verb Format	128
Table 271. ADC0Mux WCap Command Response Format	128
Table 272. ADC0Mux ConLst Command Verb Format	129
Table 273. ADC0Mux ConLst Command Response Format	129
Table 274. ADC0Mux AmpCap Command Verb Format	129
Table 275. ADC0Mux AmpCap Command Response Format	130
Table 276. ADC0Mux AmpRight Command Verb Format	130
Table 277. ADC0Mux AmpRight Command Response Format	130
Table 278. ADC0Mux AmpLeft Command Verb Format	131
Table 279. ADC0Mux AmpLeft Command Response Format	131
Table 280. ADC0Mux ConSelectCtrl Command Verb Format	131
Table 281. ADC0Mux ConSelectCtrl Command Response Format	131
Table 282. ADC0Mux ConLstEntry0 Command Verb Format	132
Table 283. ADC0Mux ConLstEntry0 Command Response Format	132
Table 284. ADC0Mux ConLstEntry4 Command Verb Format	132
Table 285. ADC0Mux ConLstEntry4 Command Response Format	132
Table 286. ADC1Mux WCap Command Verb Format	133
Table 287. ADC1Mux WCap Command Response Format	133
Table 288. ADC1Mux ConLst Command Verb Format	134
Table 289. ADC1Mux ConLst Command Response Format	134
Table 290. ADC1Mux AmpCap Command Verb Format	134
Table 291. ADC1Mux AmpCap Command Response Format	134
Table 292. ADC1Mux AmpRight Command Verb Format	135

Table 293. ADC1Mux AmpRight Command Response Format	135
Table 294. ADC1Mux AmpLeft Command Verb Format	135
Table 295. ADC1Mux AmpLeft Command Response Format	135
Table 296. ADC1Mux ConSelectCtrl Command Verb Format	136
Table 297. ADC1Mux ConSelectCtrl Command Response Format	136
Table 298. ADC1Mux ConLstEntry0 Command Verb Format	136
Table 299. ADC1Mux ConLstEntry0 Command Response Format	136
Table 300. ADC1Mux ConLstEntry4 Command Verb Format	136
Table 301. ADC1Mux ConLstEntry4 Command Response Format	137
Table 302. PCBEEP Amp Command Verb Format	137
Table 303. PCBEEP Amp Command Response Format	137
Table 304. PCBEEP WCap Command Verb Format	137
Table 305. PCBEEP WCap Command Response Format	138
Table 306. PCBEEP AmpCap Command Verb Format	138
Table 307. PCBEEP AmpCap Command Response Format	138
Table 308. PCBEEP Gen Command Verb Format	139
Table 309. PCBEEP Gen Command Response Format	139
Table 310. CD WCap Command Verb Format	139
Table 311. CD WCap Command Response Format	140
Table 312. CD PinCap Command Verb Format	140
Table 313. CD PinCap Command Response Format	141
Table 314. CD PinWCntrl Command Verb Format	141
Table 315. CD PinWCntrl Command Response Format	141
Table 316. CD ConfigDefault Command Verb Format	142
Table 317. CD ConfigDefault Command Response Format	142
Table 318. VolumeKnob WCap Command Verb Format	142
Table 319. VolumeKnob WCap Command Response Format	143
Table 320. VolumeKnob VolKnobCap Command Verb Format	143
Table 321. VolumeKnob VolKnobCap Command Response Format	143
Table 322. VolumeKnob ConLst Command Verb Format	143
Table 323. VolumeKnob ConLst Command Response Format	144
Table 324. VolumeKnob ConLstEntry Command Verb Format	144
Table 325. VolumeKnob ConLstEntry Command Response Format	144
Table 326. VolumeKnob UnsolResp Command Verb Format	144
Table 327. VolumeKnob UnsolResp Command Response Format	145
Table 328. VolumeKnob Cntrl Command Verb Format	145
Table 329. VolumeKnob Cntrl Command Response Format	145
Table 330. ADC0Vol WCap Command Verb Format	146
Table 331. ADC0Vol WCap Command Response Format	146
Table 332. ADC0Vol ConLst Command Verb Format	147
Table 333. ADC0Vol ConLst Command Response Format	147
Table 334. ADC0Vol AmpRight Command Verb Format	147
Table 335. ADC0Vol AmpRight Command Response Format	147
Table 336. ADC0Vol AmpLeft Command Verb Format	148
Table 337. ADC0Vol AmpLeft Command Response Format	148
Table 338. ADC0Vol ConLstEntry Command Verb Format	148
Table 339. ADC0Vol ConLstEntry Command Response Format	148
Table 340. ADC0Vol LR Command Verb Format	149
Table 341. ADC0Vol LR Command Response Format	149
Table 342. ADC1Vol WCap Command Verb Format	149
Table 343. ADC1Vol WCap Command Response Format	149
Table 344. ADC1Vol ConLst Command Verb Format	150
Table 345. ADC1Vol ConLst Command Response Format	150
Table 346. ADC1Vol AmpRight Command Verb Format	151
Table 347. ADC1Vol AmpRight Command Response Format	151

Table 348. ADC1Vol AmpLeft Command Verb Format	151
Table 349. ADC1Vol AmpLeft Command Response Format	151
Table 350. ADC1Vol ConLstEntry Command Verb Format	152
Table 351. ADC1Vol ConLstEntry Command Response Format	152
Table 352. ADC1Vol LR Command Verb Format	152
Table 353. ADC1Vol LR Command Response Format	152
Table 354. STAC9220 Ordering Information	153

1. FEATURES

1.1. Overview

The STAC9220 is a high fidelity, 8-channel audio CODEC compatible with Intel's High Definition (HD) Audio Interface. The STAC9220 CODEC provide stereo 24-bit resolution with sample rates up to 192 KHz. SPDIF I/O provides connectivity to consumer electronic equipment. The STAC9220 CODEC incorporate IDT's proprietary $\Sigma\Delta$ technology to achieve an estimated DAC SNR in excess of 95dB. The STAC9220 CODECs provide high quality, HD Audio capability to notebook and media centric desktop PC applications.

1.2. Features

- High performance $\Sigma\Delta$ technology
 - 95dB DAC SNR
- Intel HD Audio interface
- Eight Channel (4 DAC pairs and 2 stereo ADCs) with 24-bit resolution
 - Supports 7.1 Audio
 - Supports 5.1 Audio with Auxiliary channel for separate audio stream or Real Time Communication (RTC) channel
- Sample Rates Up to 192 KHz
- Integrated Headphone Amps
- Stereo Microphone
 - Supports Stereo Microphone
 - Microphone Boost 0, 10, 20, 30, 40dB
- Direct CDROM Recording Mixerless Design
- SPDIF In and Out
- Two-Pin Volume Up/Down Control
- Impedance Sensing
- Universal Jacks™ Functionality for jack retasking
 - Headphone, Line Out, Line In & Microphone
 - Pins 35/36
 - Pins 39/41
 - Line Out, Line In and Microphone Support
 - Pins 16/17 (with strong line out)
 - Pins 23/24
 - Pins 21/22
 - Line In/MIC Support
 - Pins 14/15
- Four Adjustable VREF Out pins for Microphone Bias
- Digital PC Beep to all outputs
- +3.3V and +5V/4V¹ analog power supply options
- 48-pin LQFP package option (7mm x 7mm)

Note: 1. The +4V Analog voltage is supported by the +5V version of the STAC9220. Request the +4V configuration of the driver.

1.3. Third Party Software Support

- WOW™ and Tru Surround™ from SRS
- Intellisonic Microphone Beam Forming from Knowles™
- Maxx BASS™ from Waves
- Dolby Technologies
 - Dolby Headphone™
 - Dolby ProLogic II™
 - Dolby Virtual Speaker™
- Smart Stream™ from Sonic Focus

1.4. Description

The STAC9220 is a high fidelity, 8-channel audio CODEC compatible with the Intel High Definition (HD) Audio Interface. The STAC9220 provides high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9220 provides stereo 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9220 DAC, ADC and SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz. Additional sample rates are supported by the driver software.

The STAC9220 support all desired eight channel configurations, including switchable Headphone Out, and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini-disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9220 has three General Purpose I/O (GPIO) pins. The STAC920 also provides a single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9220 integrates a headphone amplifier which is available on Ports A and D. The headphone amplifier is switchable between these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs. An additional headphone is supported on Port F.

The Universal Jack capabilities allow the CODEC to detect when audio devices are connected to the CODEC, and to allow the CODEC to be reconfigured to support these devices regardless of which port they are plugged into the system. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

Note: The Jack Detect circuit and component selection are critical for accurate detection of audio jacks on individual ports. Please see the IDT STAC922x reference design for circuit implementation details.

The STAC9220 operates with a 3.3 V digital supply and is available in either 5 V analog supply or 3.3 V analog supply options.

The STAC9220 is available in a 48-pin LQFP package. The 48-pin LQFP is only available in the Environmental package (Pb-free).

The STAC9220 is supported with IDT's high quality software solutions which include drivers for all major Windows operating systems from Microsoft, parametric SoftEQ, and Digital Rights Management. Third party plug-in capability is easily achieved with the IDT Kernel Processing Interface, to support high-valued, third party technologies like SRS WOW[®], Knowles[®] Microphone Beam Forming, Waves MaxxBASS[®], Dolby Headphone[®], Dolby ProLogic II[®] and Dolby Virtual Speaker[®] and more.

Non-IDT companies mentioned are registered trademarks of their respective companies.

2. CHARACTERISTICS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9220. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0°C to +70°C
Storage temperature		-55 °C to +125 °C
Soldering temperature		260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 158.

2.1.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: The +4 V Analog voltage is supported by the +5 V version of the STAC922x or STAC922xD.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T _{case} (48-LQFP)			+90	°C

ESD: The STAC9220 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9220 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.2. STAC9220 5V Analog Performance Characteristics

($T_{\text{ambient}} = 25^{\circ}\text{C}$, $AV_{\text{dd}} = 5.0\text{ V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 K Ω / 50 pF load, Testbench Characterization BW: 20 KHz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	90	-	dB
Analog Frequency Response (Note 3)	10		30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-93	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-88	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 K Ω load)	-	-90	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	93	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to DAC (1 KHz Signal Frequency) Crosstalk		-101		dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-80	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	K Ω
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	-	100	-	ppm/ $^{\circ}$ C
DAC Offset Voltage	-	5	20	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	K Ω
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μ sec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
3. ± 1 dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25 dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.3. STAC9220 4V Analog Performance Characteristics

($T_{\text{ambient}} = 25^{\circ}\text{C}$, $AV_{\text{dd}} = 4.0\text{ V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 K Ω / 50 pF load, Testbench Characterization BW: 20 KHz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	85	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-85	-	dB
HEADPHONE_OUT (32 Ω load)	-	-88	-	dB
HEADPHONE_OUT (10 K Ω load)	-	-85	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-80	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	K Ω
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	100		-	ppm/ $^{\circ}$ C
DAC Offset Voltage	-	5	20	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	K Ω
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-100		-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μ sec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	750	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
3. ± 1 dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25 dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.4. STAC9220 3.3V Analog Performance Characteristics

($T_{\text{ambient}} = 25^{\circ}\text{C}$, $AV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 VRMS, 10 K Ω / 50 pF load, Testbench Characterization BW: 20 KHz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here, as specific system characteristics, such as layout, routing and external CODEC component selection, influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results. Contact IDT for more information.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	0.7	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	80	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-75	-	dB
HEADPHONE_OUT (32 Ω load)	-	-85	-	dB
HEADPHONE_OUT (10 K Ω load)	-	-88	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	95	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	85	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-85	-	dB

Parameter	Min	Typ	Max	Unit
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-70	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	K Ω
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45 X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	100		-	ppm/ $^{\circ}$ C
DAC Offset Voltage	-	5	20	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	K Ω
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μ sec
PLL (or Azalia Bit CLK) 24.576 MHz clock jitter	-	100	750	psec

1. With +30dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
3. ± 1 dB limits for Line Output & 0dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25 dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

3. POWER CONSUMPTION

3.1. Digital

Power State	Typical*	Max	units
D0	66	75	mA
D1	66	75	mA
D2	18	30	mA
D3	10	20	mA

Table 1. Digital Power Consumption

3.2. Analog: AVDD = 5 V

Power State	Typical*	Max	units
D0	55	65	mA
D1	55	65	mA
D2	25	35	mA
D3	15	20	mA

Table 2. Analog Power Consumption 5V

3.3. Analog: AVDD = 3.3 V

Power State	Typical*	Max	units
D0	45	55	mA
D1	45	55	mA
D2	20	30	mA
D3	13	18	mA

Table 3. Analog Power Consumption 3.3V

*Typical results are with all DACs and all ADCs on, and with audio playing.

4. DETAILED DESCRIPTION

4.1. Audio Jack Presence Detect

SENSE_A pin is used to detect the presence of plugs in ports A, B, C, and D. SENSE_B pin is used to detect the presence of plugs in ports E and F. Refer to the reference design for port detect circuitry. Select the precision of the resistor used as follows.

Table 4. Audio Jack Presence Detect

Nominal Voltage (+/-5%)	Resistor Tolerance Sense A (If port D is used)	Resistor Tolerance Sense A (If port D is not used)	Resistor Tolerance Sense B (For ports E and F)
5V	1%	1%	1%
4.5V	1%	1%	1%
4V	0.50%	1%	1%
3.3V	0.10%	1%	1%

4.2. SPDIF Output

SPDIF Output can operate at 44.1 KHz, 48 KHz and 96 KHz, as defined in the Intel High Definition Audio Specification, with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

4.3. Universal Jacks™

IDT's Universal Jacks™ technology allows for the greatest flexibility in board design and implementation. For the STAC9220 the Universal Jacks™ capabilities are as follows¹:

- Pins 39/41 can be used for²:
 - Headphone Out
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40dB Microphone boost³
- Pins 35/36 can be used for²:
 - Headphone Out
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40dB Microphone boost³
- Pins 23/24 can be used for:
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40dB Microphone boost³
- Pins 21/22 can be used for:
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40dB Microphone boost³
- Pins 16/17 can be used for:
 - Headphone Out
 - Line Out
 - Line In
 - Microphone with 0/10/20/30/40dB Microphone boost³
- Pins 14/15 can be used for:
 - Line In
 - Microphone with 0/10/20/30/40dB Microphone boost³

Note¹: On the STAC9220 only one function can be selected on each pin pair at a time. For example, a pin pair cannot be configured as an input and output at the same time. Configuration can be changed at any time.

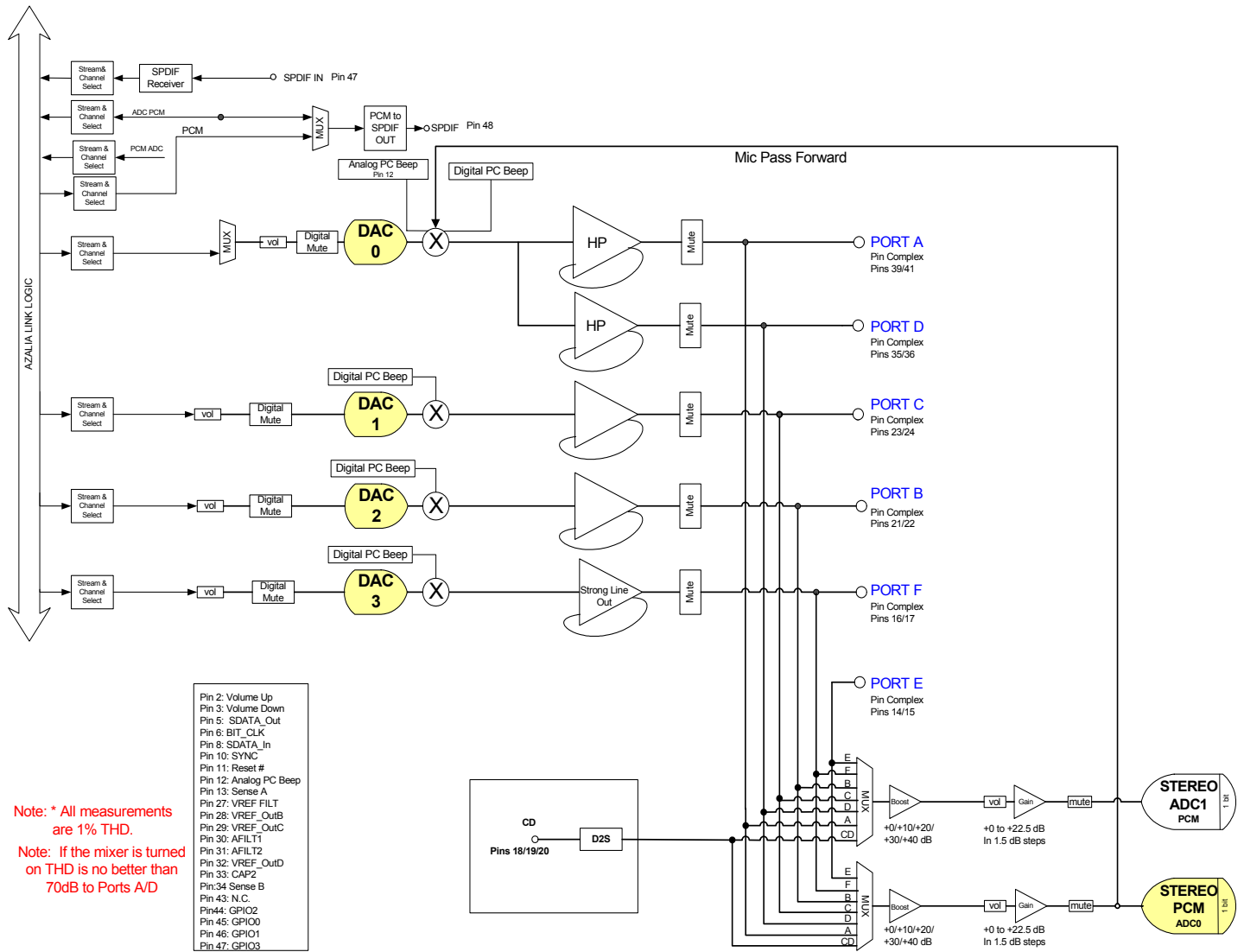
Note²: Headphone capabilities are provided on pins 39/41 and 35/36, but one should not put headphone loads on both sets of pins at the same time.

Note³: 40dB Microphone boost is not recommended.

5. FUNCTIONAL BLOCK DIAGRAMS AND CONNECTION DIAGRAMS

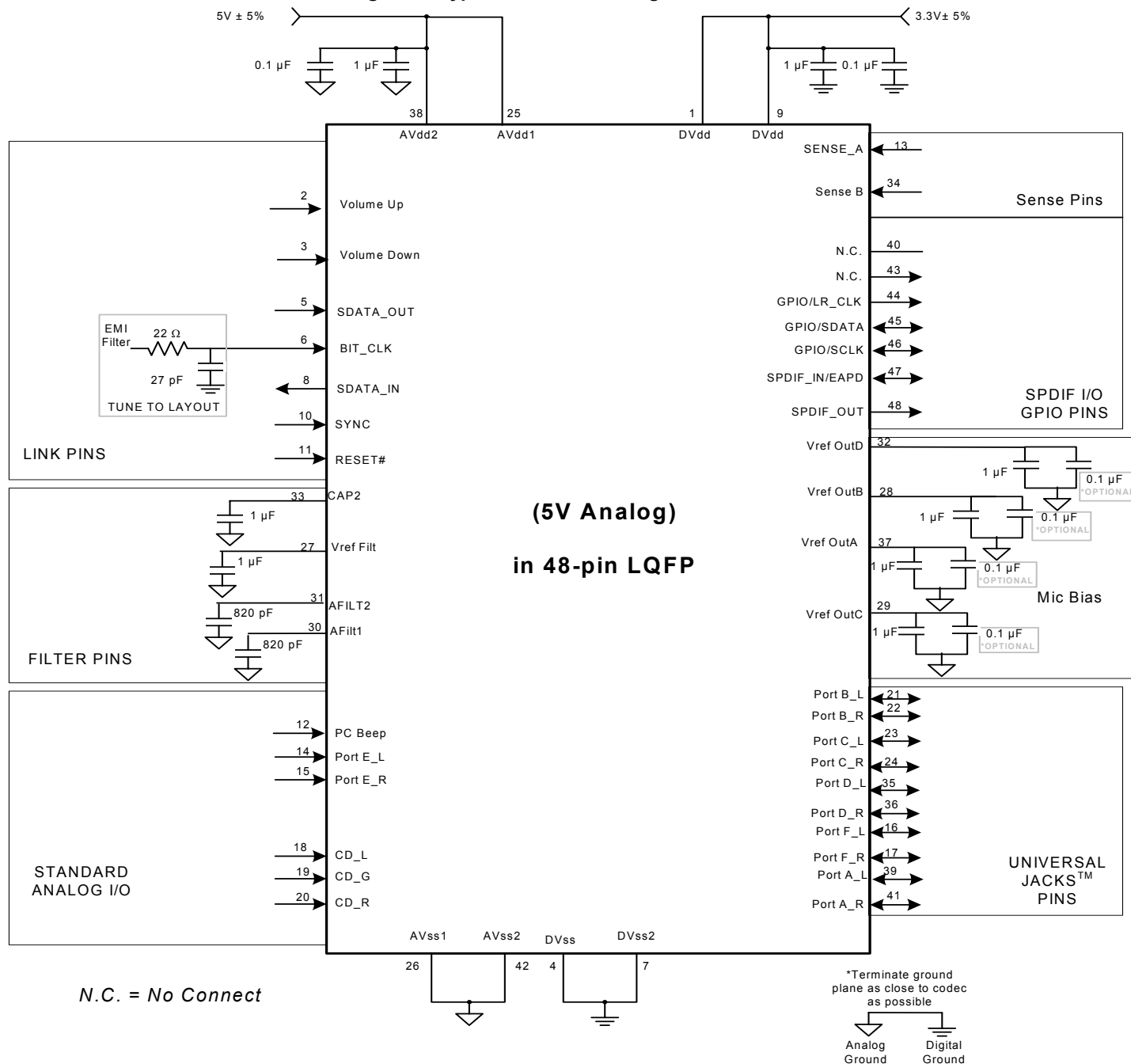
5.1. STAC9220 Functional Block Diagram

Figure 1. Functional Block Diagram STAC9220



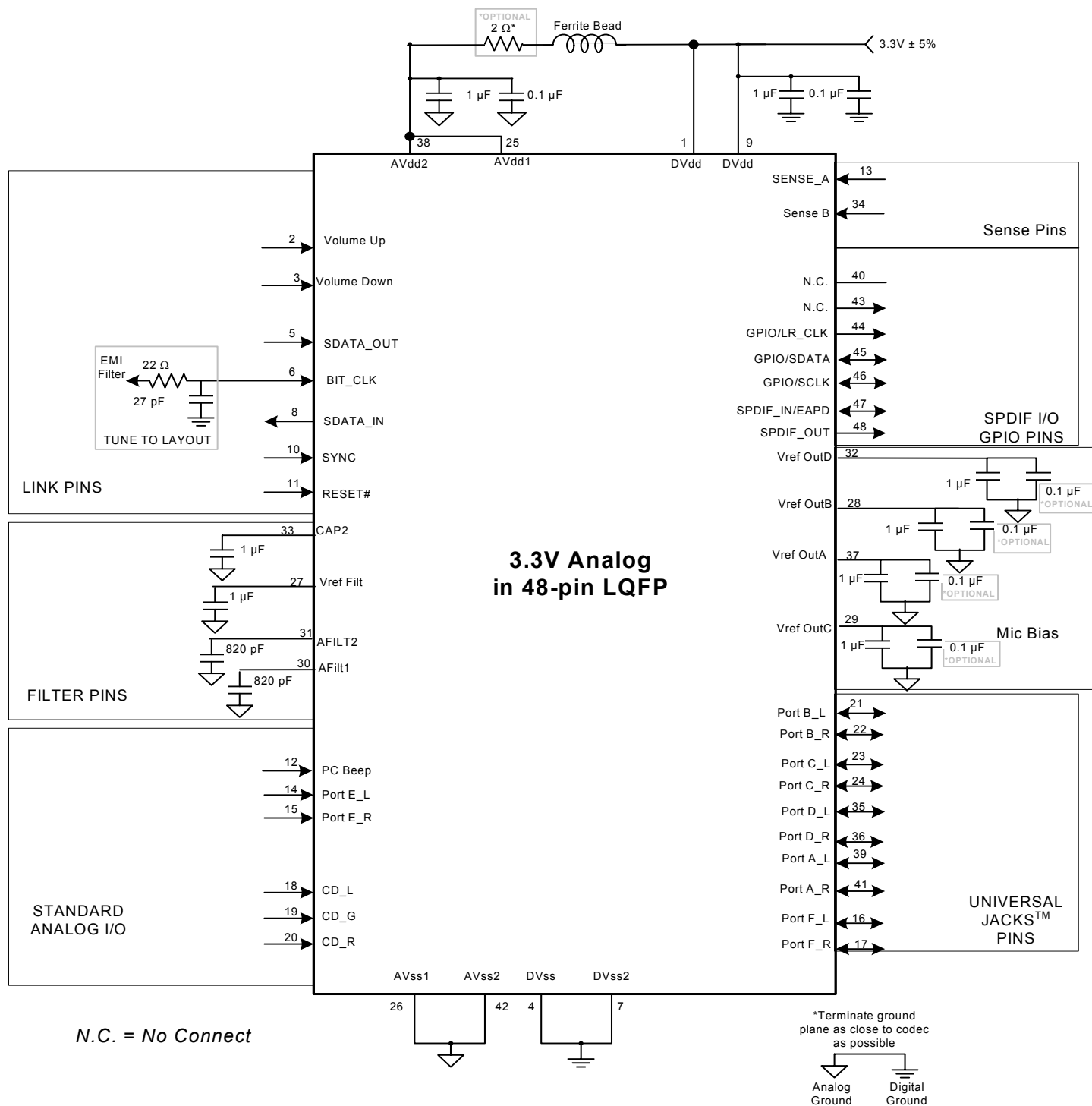
5.2. STAC9220 Typical Connection Diagram for 48-pin LQFP

Figure 2. Typical Connection Diagram STAC9220



5.3. STAC9220 Split Independent Power Supply for 48-pin LQFP

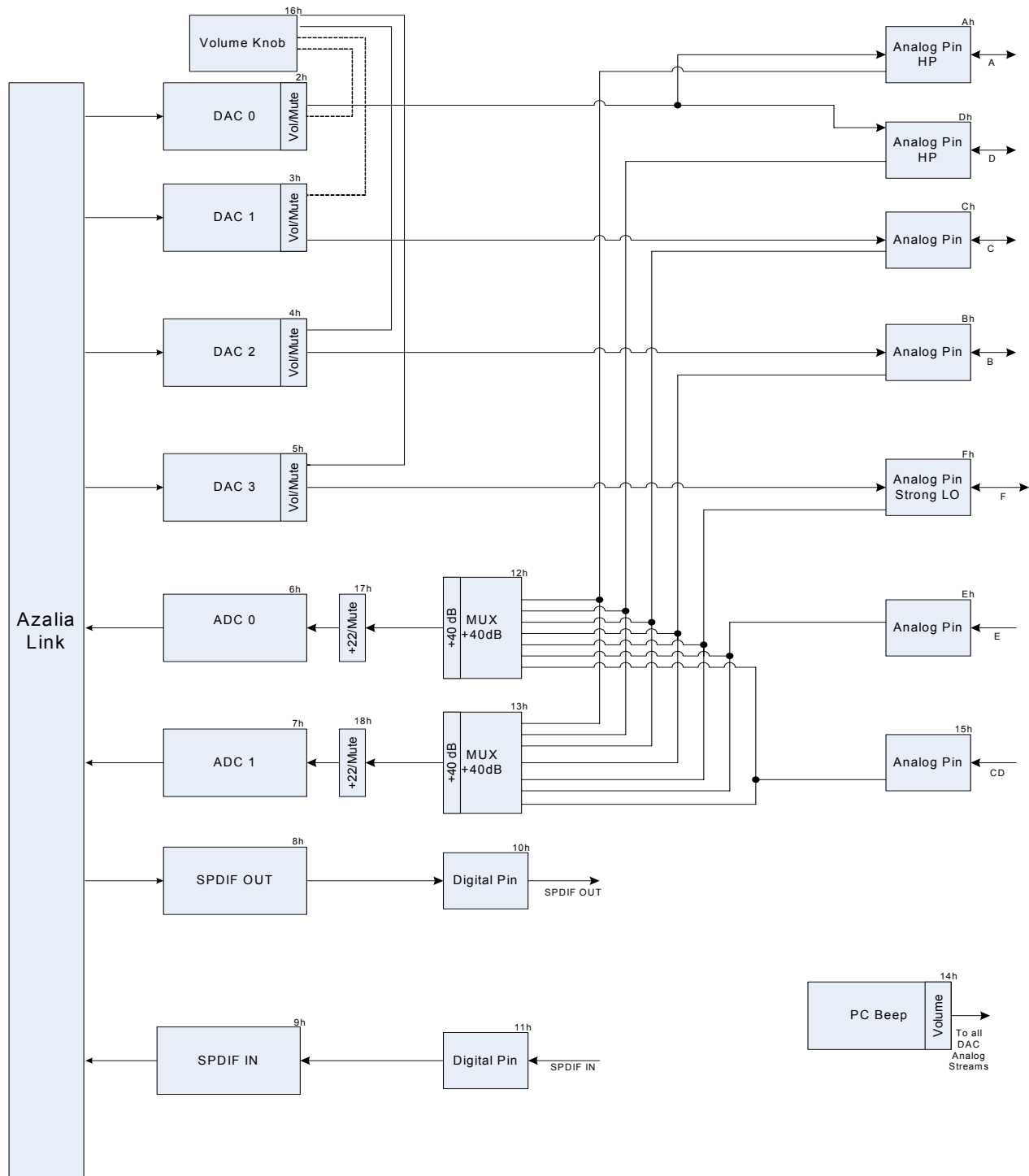
Figure 3. Split Independent Power Supply STAC9220



6. WIDGET INFORMATION

6.1. STAC9220 Widget Diagrams

Figure 4. Widget Diagram STAC9220



6.2. Widget List STAC9220

Table 5. High Definition Audio Widget

ID	Widget Name	Description
1h	Audio Function Group	Audio Function Group
2h	DAC0	Stereo Output to DAC
3h	DAC1	Stereo Output to DAC
4h	DAC2	Stereo Output to DAC
5h	DAC3	Stereo Output to DAC
6h	ADC0	Stereo Input Mux from ADC
7h	ADC1	Stereo Input Mux from ADC
8h	SPDIF_OUT	Stereo Output for SPDIF_Out
9h	SPDIF_IN	Stereo Input for SPDIF_In
10h	SPDIF-Out Pin	Pin Widget for SPDIF_Out pin 48
11h	SPDIF-In Pin	Pin Widget for SPDIF_In pin 47
12h	ADC0Mux	ADC Mux and Boost for inputs to ADC
13h	ADC1Mux	ADC Mux and Boost for inputs to ADC
14h	Digital PC Beep	Digital PC Beep
15h	CD	CD Pin Widget pins 18/19/20
16h	Master Volume	Master Volume Controls
17h	ADC0Vol	ADC Mux and Volume for inputs to ADC
18h	ADC1Vol	ADC Mux and Volume for inputs to ADC
19h	RSVD	Reserved
Ah	Headphone	Headphone Pin Widget pins 39/41 (can also act as Line In, Line Out, or Microphone)
Dh	Headphone	Headphone Pin Widget pins 35/36 (can also act as Line In, Line Out, or Microphone)
Ch	Line In	Line In Pin Widget pins 23/24 (can also act as Microphone or Line Out)
Bh	Microphone	Microphone Pin Widget pins 21/22 (can also act as Line Out and Line In)
Fh	Line Out	Line Out Pin Widget pins 16/17 (can also act as HP, Line In, or Microphone)
Eh	Line In	Line In Pin Widget pins 14/15 (can also act as Microphone)
1ah	RSVD	Reserved*
1bh	RSVD*	Reserved

6.3. Root Node (NID = 0x00)

6.3.1. Root ID

Table 6. Root ID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table

Table 7. Root ID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID: STAC9220/21/23 = 8384h
[15:8]	DeviceFix	R	0x76	Device ID: STAC9220 = 7680h;
[7:0]	DeviceProg	R	0x80	Device ID: STAC9220 = 7680h;

6.3.2. Root RevID

Table 8. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table

Table 9. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant HD Audio specification
[19:16]	Minor	R	0x0	Minor rev number of compliant HD Audio specification
[15:12]	VendorFix	R	0x3	Vendor's rev number for this device: STAC9220 = xxh
[11:8]	VendorProg	R	0x1	Vendor's rev number for this device: STAC9220 = xxh

Table 9. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7:4]	SteppingFix	R	0x0	Vendor stepping number within the Vendor RevID: STAC9220 = xxh
[3:0]	SteppingProg	R	0x1	Vendor stepping number within the Vendor RevID: STAC9220 = xxh

6.3.3. Root NodeInfo

Table 10. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 11. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

6.4. AFG Node (NID = 0x01)

6.4.1. AFG Reset

Table 12. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table
Set1	7FF	See bits [7:0] of bitfield table	0000_0000h

Table 13. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb (7FF) is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

6.4.2. AFG NodeInfo

Table 14. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 15. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x2	Starting node number for function group subordinate nodes.
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x1A	Total number of nodes.

6.4.3. AFG Type

Table 16. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table

Table 17. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:9]	Rsvd	R	0x0	Reserved
[8]	UnSol	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7:0]	NodeType	R	0x01	Node type = Audio Function Group

6.4.4. AFG Cap

Table 18. AFG Cap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table

Table 19. AFG Cap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15:12]	Rsvd2	R	0x0	Reserved
[11:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.
[7:4]	Rsvd1	R	0x0	Reserved
[3:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

6.4.5. AFG PCMCap

Table 20. AFG PCMCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 21. AFG PCMCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) supported

6.4.6. AFG Stream**Table 22. AFG Stream Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 23. AFG Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x0	No support for non-PCM data.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.4.7. AFG InAmpCap**Table 24. AFG InAmpCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table

Table 25. AFG InAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x5	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x0E	Number of steps in the gain range = 15 (0dB to 22.5 dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.4.8. AFG SupPwrState**Table 26. AFG SupPwrState Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table

Table 27. AFG SupPwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	D3Sup	R	0x1	Power State D3 is supported. Allows for lowest possible power consuming state under software control (and still properly respond to a subsequent Power State command).
[2]	D2Sup	R	0x1	Power State D2 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 msec.
[1]	D1Sup	R	0x1	Power State D1 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 msec, excepting analog pass-through circuits which must remain fully on.
[0]	D0Sup	R	0x1	Power State D0 is supported. Node power state is fully on.

6.4.9. AFG GPIOCnt**Table 28. AFG GPIOCnt Command Verb Format**

	Verb ID	Payload	Response
Get	F00	11	See bitfield table

Table 29. AFG GPIOCnt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	GPiWake	R	0x1	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPiUnsol	R	0x1	Unsolicited Response capability. Assuming the Unsolicited Enable Mask controls are enabled, GPIO's configured as inputs can generate an Unsolicited Response on the link when there is a change in level on the pin.
[29:24]	Rsvd	R	0x0	Reserved
[23:16]	NumGPIs	R	0x00	Number of GPI pins supported by function
[15:8]	NumGPOs	R	0x00	Number of GPO pins supported by function
[7:0]	NumGPIOs	R	0x04	Number of GPIO pins supported by function

6.4.10. AFG GPIO Polarity

Table 30. AFG GPIO Polarity Command Verb Format

	Verb ID	Payload	Response
Get	FE7	00	See bitfield table
Set1	70E7	See bits [7:0] of bitfield table	0000_0000h

Table 31. AFG GPIO Polarity Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
3	GP3	RW	0x1	GPIO 3 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)
2	GP2	RW	0x1	GPIO 2 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)

Table 31. AFG GPIO Polarity Command Response Format

Bit	Bitfield Name	RW	Reset	Description
1	GP1	RW	0x1	GPIO 1 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)
0	GP0	RW	0x1	GPIO 0 Input Polarity Control (used in conjunction with GPIOSticky) and Output Type Control. When configured as a level-sensitive input: 0 = inverted 1 = not inverted (default) When configured as an edge-sensitive input: 0 = falling-edge triggered 1 = rising-edge triggered When configured as an output: 0 = push-pull (CMOS) 1 = open drain (default)

6.4.11. AFG OutAmpCap

Table 32. AFG OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 33. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x02	Size of each step in the gain range = 0.75dB
[15]	Rsvd2	R	0x0	Reserved

Table 33. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14:8]	NumSteps	R	0x7F	Number of steps in the gain range = 128 (-96dB to +0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x7F	0dB-step is programmed with this offset

6.4.12. AFG PwrState

Table 34. AFG PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 35. AFG PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x2	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x2	PS-Set: Current power setting of referenced node. 0: All Powered-On 1: D1 = > PR0, PR1 2: D2 = > PR0, PR1, PR2, PR6, EAPD 3: D3 = > PR6, PR5, PR3, PR2, PR1, PR0, EAPD Note: PR4 is not mapped in HD Audio

6.4.13. AFG UnsolResp

Table 36. AFG UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 37. AFG Unsolicited Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x0	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.4.14. AFG GPIO

Table 38. AFG GPIO Command Verb Format

	Verb ID	Payload	Response
Get	F15	00	See bitfield table
Set1	715	See bits [7:0] of bitfield table	0000_0000h

Table 39. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Data3	RW	0x0	Data for GPIO3 (Pin 47). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[2]	Data2	RW	0x0	Data for GPIO2 (Pin 44). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

Table 39. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Data1	RW	0x0	Data for GPIO1 (Pin 46). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[0]	Data0	RW	0x0	Data for GPIO0 (Pin 45). If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

6.4.15. AFG GPIOEn

Table 40. AFG GPIOEn Command Verb Format

	Verb ID	Payload	Response
Get	F16	00	See bitfield table
Set1	716	See bits [7:0] of bitfield table	0000_0000h

Table 41. AFG GPIOEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0x0	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[1]	Mask1	RW	0x0	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0x0	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

6.4.16. AFG GPIODir**Table 42. AFG GPIODir Command Verb Format**

	Verb ID	Payload	Response
Get	F17	00	See bitfield table
Set1	717	See bits [7:0] of bitfield table	0000_0000h

Table 43. AFG GPIODir Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Control3	RW	0x0	Direction control for GPIO3 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[2]	Control2	RW	0x0	Direction control for GPIO2 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[1]	Control1	RW	0x0	Direction control for GPIO1 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[0]	Control0	RW	0x0	Direction control for GPIO0 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output

6.4.17. AFG GPIOWakeEn**Table 44. AFG GPIOWakeEn Command Verb Format**

	Verb ID	Payload	Response
Get	F18	00	See bitfield table
Set1	718	See bits [7:0] of bitfield table	0000_0000h

Table 45. AFG GPIOWakeEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	W3	RW	0x0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[2]	W2	RW	0x0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[1]	W1	RW	0x0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[0]	W0	RW	0x0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.

6.4.18. AFG GPIOUnsol

Table 46. AFG GPIOUnsol AFG GPIOUnsol Command Verb Format

	Verb ID	Payload	Response
Get	F19	00	See bitfield table
Set1	719	See bits [7:0] of bitfield table	0000_0000h

Table 47. AFG GPIOUnsol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	EnMask3	RW	0x0	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO3 is configured as input and changes state.
[2]	EnMask2	RW	0x0	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[1]	EnMask1	RW	0x0	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state.
[0]	EnMask0	RW	0x0	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.

6.4.19. AFG GPIOSticky

Table 48. AFG GPIOSticky Command Verb Format

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table
Set1	71A	See bits [7:0] of bitfield table	0000_0000h

Table 49. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Mask3	RW	0x0	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[2]	Mask2	RW	0x0	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[1]	Mask1	RW	0x0	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[0]	Mask0	RW	0x0	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

6.4.20. AFG SubID

Table 50. AFG SubID Command Verb Format

	Verb ID	Payload	Response
Get	F20	00	See bitfield table
Set1	720	See bits [7:0] of bitfield table	0000_0000h
Set2	721	See bits [15:8] of bitfield table	0000_0000h
Set3	722	See bits [23:16] of bitfield table	0000_0000h
Set4	723	See bits [31:24] of bitfield table	0000_0000h

Table 51. AFG SubID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Subsys3	RW	0x00	Subsystem ID. (Any non-zero value)
[23:16]	Subsys2	RW	0x00	Subsystem ID. (Any non-zero value)
[15:8]	Subsys1	RW	0x01	Subsystem ID. (Any non-zero value)
[7:0]	Assembly	RW	0x00	Assembly ID. (Not applicable to CODEC vendors)

6.5. DAC0 Node (NID = 0x02)

6.5.1. DAC0 Cnvtr

Table 52. DAC0 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 53. DAC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz/44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 53. DAC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.5.2. DAC0 AmpRight

Table 54. DAC0 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 55. DAC0 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.5.3. DAC0 AmpLeft

Table 56. DAC0 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 57. DAC0 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.5.4. DAC0 WCap

Table 58. DAC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 59. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 59. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.5.5. DAC0 PwrState

Table 60. DAC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 61. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 61. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.5.6. DAC0 CnvtrID

Table 62. DAC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 63. DAC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.5.7. DAC0 LR

Table 64. DAC0 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 65. DAC0 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.6. DAC1 Node (NID = 0x03)

6.6.1. DAC1 Cnvtr

Table 66. DAC1 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 67. DAC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 67. DAC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.6.2. DAC1 AmpRight

Table 68. DAC1 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 69. DAC1 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.6.3. DAC1 AmpLeft

Table 70. DAC1 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 71. DAC1 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.6.4. DAC1 WCap

Table 72. DAC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 73. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 73. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.6.5. DAC1 PwrState

Table 74. DAC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 75. DAC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 75. DAC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.6.6. DAC1 CnvtrID

Table 76. DAC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 77. DAC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.6.7. DAC1 LR

Table 78. DAC1 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 79. DAC1 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.7. DAC2 Node (NID = 0x04)

6.7.1. DAC2 Cnvtr

Table 80. DAC2 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 81. DAC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 81. DAC2 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.7.2. DAC2 AmpRight

Table 82. DAC2 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 83. DAC2 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.7.3. DAC2 AmpLeft

Table 84. DAC2 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 85. DAC2 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.7.4. DAC2 WCap

Table 86. DAC2 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 87. DAC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 87. DAC2 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.7.5. DAC2 PwrState

Table 88. DAC2 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 89. DAC2 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 89. DAC2 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.7.6. DAC2 CnvtrID

Table 90. DAC2 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 91. DAC2 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.7.7. DAC2 LR

Table 92. DAC2 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 93. DAC2 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.8. DAC3 Node (NID = 0x05)

6.8.1. DAC3 Cnvtr

Table 94. DAC3 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 95. DAC3 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 95. DAC3 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.8.2. DAC3 AmpRight

Table 96. DAC3 AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 97. DAC3 AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.8.3. DAC3 AmpLeft

Table 98. DAC3 AmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 99. DAC3 AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

6.8.4. DAC3 WCap

Table 100. DAC3 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 101. DAC3 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream

Table 101. DAC3 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.8.5. DAC3 PwrState

Table 102. DAC3 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 103. DAC3 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 103. DAC3 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

6.8.6. DAC3 CnvtrID

Table 104. DAC3 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 105. DAC3 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter.

6.8.7. DAC3 LR

Table 106. DAC3 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 107. DAC3 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.9. ADC0 Node (NID = 0x06)

6.9.1. ADC0 Cnvtr

Table 108. ADC0 Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 109. ADC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 109. ADC0 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.9.2. ADC0 WCap

Table 110. ADC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 111. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved

Table 111. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.9.3. ADC0 ConLst

Table 112. ADC0 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 113. ADC0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.

Table 113. ADC0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	Coal	R	0x01	Number of NID entries in connection list.

6.9.4. ADC0 ConLstEntry

Table 114. ADC0 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 115. ADC0 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x17	ADC0 Vol widget

6.9.5. ADC0 ProcState

Table 116. ADC0 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table
Set1	703	See bits [7:0] of bitfield table	0000_0000h

Table 117. ADC0 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.9.6. ADC0 PwrState

Table 118. ADC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 119. ADC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.9.7. ADC0 CnvtrID**Table 120. ADC0 CnvtrID Command Verb Format**

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 121. ADC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.10. ADC1 Node (NID = 0x07)**6.10.1. ADC1 Cnvtr****Table 122. ADC1 Cnvtr Command Verb Format**

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 123. ADC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.

Table 123. ADC1 Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.10.2. ADC1 WCap

Table 124. ADC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 125. ADC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrCntrl	R	0x1	Power State control is supported
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x1	Software should query the Processing Controls parameter for this widget.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.10.3. ADC1 ConLst

Table 126. ADC1 ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 127. ADC1 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.10.4. ADC1 ConLstEntry

Table 128. ADC1 ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 129. ADC1 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x18	ADC1 Vol widget

6.10.5. ADC1 ProcState

Table 130. ADC1 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table
Set1	703	See bits [7:0] of bitfield table	0000_0000h

Table 131. ADC1 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

6.10.6. ADC1 PwrState

Table 132. ADC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 133. ADC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

6.10.7. ADC1 CnvtrID

Table 134. ADC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 135. ADC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.11. SPDIFOut Node (NID = 0x08)

6.11.1. SPDIFOut Cnvtr

Table 136. SPDIFOut Cnvtr Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table
Set1	2	See bits [15:0] of bitfield table	0000_0000h

Table 137. SPDIFOut Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	FrmtNonPCM	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)

Table 137. SPDIFOut Cnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14]	FrmtSmplRate	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	SmplRateMultp	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	SmplRateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	BitsPerSmpl	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NmbrChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

6.11.2. SPDIFOut WCap

Table 138. SPDIFOut WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 139. SPDIFOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x1	Widget contains format info; software should query
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.11.3. SPDIFOut PCM

Table 140. SPDIFOut PCM Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 141. SPDIFOut PCM Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

6.11.4. SPDIFOut Stream

Table 142. SPDIFOut Stream Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table

Table 143. SPDIFOut Stream Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

6.11.5. SPDIFOut CnvtrID

Table 144. SPDIFOut CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table
Set1	706	See bits [7:0] of bitfield table	0000_0000h

Table 145. SPDIFOut CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Strm	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
[3:0]	Ch	RW	0x0	Integer representing lowest channel used by converter

6.11.6. SPDIFOut DigCnvtr

Table 146. SPDIFOut DigCnvtr Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table
Set1	70D	See bits [7:0] of bitfield table	0000_0000h
Set2	70E	See bits [15:8] of bitfield table	0000_0000h

Table 147. SPDIFOut DigCnvtr Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	Rsvd1	R	0x0	Reserved
[14:8]	CC	RW	0x00	CC[6:0] - Category Code
[7]	L	RW	0x0	L - Generation Level
[6]	PRO	RW	0x0	PRO - Professional
[5]	AUDIO	RW	0x0	/AUDIO - Non-Audio
[4]	COPY	RW	0x0	COPY - Copyright
[3]	PRE	RW	0x0	PRE - Preemphasis
[2]	VCFG	RW	0x0	VCFG - Validity Config
[1]	V	RW	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

6.12. Reserved Node (NID = 0x09)

6.13. PortA Node (NID = 0x0A)

6.13.1. PortA WCap

Table 148. PortA WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 149. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.13.2. PortA PinCap**Table 150. PortA PinCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 151. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement.
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.13.3. PortA ConLst**Table 152. PortA ConLst Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 153. PortA ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.13.4. PortA ConLstEntry

Table 154. PortA ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 155. PortA ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.13.5. PortA PinWCntrl

Table 156. PortA PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 157. PortA PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = Enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.13.6. PortA Unsolicited Response

Table 158. PortA Unsolicited Response Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 159. PortA Unsolicited Response Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.

Table 159. PortA UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.13.7. PortA ChSense

Table 160. PortA ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 161. PortA ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.13.8. PortA ConfigDefault

Table 162. PortA ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 163. PortA ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x02	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x21	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x40	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x20	Configuration bits used by software to determine devices attached to the CODEC.

6.14. PortB Node (NID = 0x0B)

6.14.1. PortB WCap

Table 164. PortB WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 165. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.14.2. PortB PinCap

Table 166. PortB PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 167. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.14.3. PortB ConLst

Table 168. PortB ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 169. PortB ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved

Table 169. PortB ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.14.4. PortB ConLstEntry

Table 170. PortB ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 171. PortB ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x04	DAC2 Converter widget

6.14.5. PortB PinWCntrl

Table 172. PortB PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 173. PortB PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x1	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.14.6. PortB Unsolicited Response

Table 174. PortB Unsolicited Response Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 175. PortB Unsolicited Response Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.14.7. PortB ChSense**Table 176. PortB ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 177. PortB ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.14.8. PortB ConfigDefault**Table 178. PortB ConfigDefault Command Verb Format**

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 179. PortB ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x60	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.

6.15. PortC Node (NID = 0x0C)

6.15.1. PortC WCap

Table 180. PortC WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 181. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present

Table 181. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.15.2. PortC PinCap

Table 182. PortC PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 183. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.

Table 183. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.15.3. PortC ConLst

Table 184. PortC ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 185. PortC ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.15.4. PortC ConLstEntry

Table 186. PortC ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 187. PortC ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x03	DAC1 Converter widget

6.15.5. PortC PinWCntrl

Table 188. PortC PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 189. PortC PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x1	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.15.6. PortC UnsolResp**Table 190. PortC UnsolResp Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 191. PortC UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.15.7. PortC ChSense**Table 192. PortC ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 193. PortC ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.15.8. PortC ConfigDefault

Table 194. PortC ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 195. PortC ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.

Table 195. PortC ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x40	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x10	Configuration bits used by software to determine devices attached to the CODEC.

6.16. PortD Node (NID = 0x0D)

6.16.1. PortD WCap

Table 196. PortD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 197. PortD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 197. PortD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.16.2. PortD PinCap

Table 198. PortD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 199. PortD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% Avdd; 50% Avdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.

Table 199. PortD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.16.3. PortD ConLst

Table 200. PortD ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 201. PortD ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.16.4. PortD ConLstEntry

Table 202. PortD ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 203. PortD ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.

Table 203. PortD ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x02	DAC0 Converter widget

6.16.5. PortD PinWCntrl

Table 204. PortD PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 205. PortD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = Enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z).

6.16.6. PortD UnsolResp**Table 206. PortD UnsolResp Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 207. PortD UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.16.7. PortD ChSense**Table 208. PortD ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 209. PortD ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.16.8. PortD ConfigDefault

Table 210. PortD ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 211. PortD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x02	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0xA1	Configuration bits used by software to determine devices attached to the CODEC.

Table 211. PortD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x90	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x50	Configuration bits used by software to determine devices attached to the CODEC.

6.17. PortE Node (NID = 0x0E)

6.17.1. PortE WCap

Table 212. PortE WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 213. PortE WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	Connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 213. PortE WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.17.2. PortE PinCap

Table 214. PortE PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 215. PortE PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.17.3. PortE PinWCntrl**Table 216. PortE PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 217. PortE PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x1	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	R	0x0	Vref Out not supported on this Port

6.17.4. PortE UnsolicitedResp**Table 218. PortE UnsolicitedResp Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 219. PortE UnsolicitedResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.

Table 219. PortE UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.17.5. PortE ChSense

Table 220. PortE ChSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table

Table 221. PortE ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x0	No impedance sense for Port E.

6.17.6. PortE ConfigDefault

Table 222. PortE ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 223. PortE ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x81	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x30	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x51	Configuration bits used by software to determine devices attached to the CODEC.

6.18. PortF Node (NID = 0x0F)

6.18.1. PortF WCap

Table 224. PortF WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 225. PortF WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present

Table 225. PortF WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.18.2. PortF PinCap

Table 226. PortF PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 227. PortF PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.

Table 227. PortF PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

6.18.3. PortF ConLst

Table 228. PortF ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 229. PortF ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.18.4. PortF ConLstEntry

Table 230. PortF ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 231. PortF ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	Unused list entry.
[23:16]	ConL2	R	0x00	Unused list entry.
[15:8]	ConL1	R	0x00	Unused list entry.
[7:0]	ConL0	R	0x05	DAC3 Converter widget

6.18.5. PortF PinWCntrl

Table 232. PortF PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 233. PortF PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPhnEn	RW	0x0	1 = Enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VRefEn	R	0x0	Vref Out not supported on this Port

6.18.6. PortF UnsolResp**Table 234. PortF UnsolResp Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 235. PortF UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.18.7. PortF ChSense**Table 236. PortF ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h
Set2	709	See bits [15:8] of bitfield table	0000_0000h

Table 237. PortF ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = Perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = Perform impedance sensing on left channel or tip of the connector

6.18.8. PortF ConfigDefault

Table 238. PortF ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 239. PortF ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x11	Configuration bits used by software to determine devices attached to the CODEC.

Table 239. PortF ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x60	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x12	Configuration bits used by software to determine devices attached to the CODEC.

6.19. DigOut0 Node (NID = 0x10)

6.19.1. DigOut0 WCap

Table 240. DigOut0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 241. DigOut0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No support for swapping left and right channels
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex

Table 241. DigOut0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.19.2. DigOut0 PinCap

Table 242. DigOut0 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 243. DigOut0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.19.3. DigOut0 ConLst**Table 244. DigOut0 ConLst Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 245. DigOut0 ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x03	Number of NID entries in connection list.

6.19.4. DigOut0 ConSelectCtrl**Table 246. DigOut0 ConSelectCtrl Command Verb Format**

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 247. DigOut0 ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

6.19.5. DigOut0 ConLstEntry**Table 248. DigOut0 ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 249. DigOut0 ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection
[23:16]	ConL2	R	0x19	Reserved Converter widget
[15:8]	ConL1	R	0x17	ADC0 Vol widget
[7:0]	ConL0	R	0x08	SPDIF Out Converter widget

6.19.6. DigOut0 PinWCntrl

Table 250. DigOut0 PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 251. DigOut0 PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = CODEC output path of Pin Widget is enabled
[5:0]	Rsvd1	R	0x0	Reserved

6.19.7. DigOut0 ConfigDefault

Table 252. DigOut0 ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h

Table 252. DigOut0 ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 253. DigOut0 ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x45	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x10	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x30	Configuration bits used by software to determine devices attached to the CODEC.

6.20. DigIn Node (NID = 0x11)

6.20.1. DigIn WCap Command

Table 254. DigIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 255. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x3	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved

Table 255. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x1	Power State control capability for support of EAPD
[9]	Dig	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x1	Unsolicited Response is supported
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.20.2. DigIn PinCap

Table 256. DigIn PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 257. DigIn PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x1	This widget controls EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on input pins.

Table 257. DigIn PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable. (EAPD is not the output stream)
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.20.3. DigIn PwrState

Table 258. DigIn PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table
Set1	705	See bits [7:0] of bitfield table	0000_0000h

Table 259. DigIn PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - EAPD powered down (Hi-Z). 11 - Powered down (default)

6.20.4. DigIn PinWCntrl**Table 260. DigIn PinWCntrl Command Verb Format**

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 261. DigIn PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.20.5. DigIn UnsolicitedResp**Table 262. DigIn UnsolicitedResp Command Verb Format**

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 263. DigIn UnsolicitedResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon lock or loss-of-lock of SPDIF-in clock recovery circuit.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.20.6. DigIn ChSense**Table 264. DigIn ChSense Command Verb Format**

	Verb ID	Payload	Response
Get	F09	00	See bitfield table
Set1	709	See bits [7:0] of bitfield table	0000_0000h

Table 265. DigIn ChSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = Something is plugged into jack associated with Pin Complex. For this widget, Presence Detect indicates that the SPDIF-in clock recovery circuit has locked onto a valid SPDIF-in sampling frequency. Any change in status will generate an Unsolicited Response, if enabled with verb 708.
[30:0]	Rsvd	R	0x0	Reserved. Impedance sense not supported for this Pin Complex.

6.20.7. DigIn EAPD**Table 266. DigIn EAPD Command Verb Format**

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 267. DigIn EAPD Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd2	R	0x0	Reserved

Table 267. DigIn EAPD Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	Data	RW	0x0	EAPD value reflected on the EAPD pin. 0 = power down external amplifier; 1 = power up external amplifier if PwrState < 0x2. If PwrState > = 0x2, Pin47 is Hi-Z. An external pull-down is required if EAPD must be low when Pin Widget is powered down.
[0]	Rsvd1	R	0x0	Reserved

6.20.8. DigIn ConfigDefault

Table 268. DigIn ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 269. DigIn ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x01	Configuration bits used by software to determine devices attached to the CODEC. Port = no physical connection Location = internal, riser
[23:16]	Config3	RW	0xC5	Configuration bits used by software to determine devices attached to the CODEC. Default Device = SPDIF In Connection = optical

Table 269. DigIn ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Config2	RW	0x10	Configuration bits used by software to determine devices attached to the CODEC. Color = black Misc = Jack detect override -- no external circuitry support for Presence Detect function
[7:0]	Config1	RW	0x60	Configuration bits used by software to determine devices attached to the CODEC.

6.21. ADC0Mux Node (NID = 0x12)

6.21.1. ADC0Mux WCap

Table 270. ADC0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 271. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.

Table 271. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.21.2. ADC0Mux ConLst

Table 272. ADC0Mux ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 273. ADC0Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x07	Number of NID entries in connection list.

6.21.3. ADC0Mux AmpCap

Table 274. ADC0Mux AmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 275. ADC0Mux AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.21.4. ADC0Mux AmpRight

Table 276. ADC0Mux AmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 277. ADC0Mux AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.21.5. ADC0Mux AmpLeft**Table 278. ADC0Mux AmpLeft Command Verb Format**

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 279. ADC0Mux AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.21.6. ADC0Mux ConSelectCtrl**Table 280. ADC0Mux ConSelectCtrl Command Verb Format**

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 281. ADC0Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

6.21.7. ADC0Mux ConLstEntry0**Table 282. ADC0Mux ConLstEntry0 Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 283. ADC0Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x15	CD In
[7:0]	ConL0	R	0x0E	Port E (default)

6.21.8. ADC0Mux ConLstEntry4**Table 284. ADC0Mux ConLstEntry4 Command Verb Format**

	Verb ID	Payload	Response
Get	F02	04	See bitfield table

Table 285. ADC0Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection.
[23:16]	ConL2	R	0x0A	Port A
[15:8]	ConL1	R	0x0D	Port D
[7:0]	ConL0	R	0x0C	Port C

6.22. ADC1Mux Node (NID = 0x13)

6.22.1. ADC1Mux WCap**Table 286. ADC1Mux WCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 287. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.22.2. ADC1Mux ConLst**Table 288. ADC1Mux ConLst Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 289. ADC1Mux ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x07	Number of NID entries in connection list.

6.22.3. ADC1Mux AmpCap**Table 290. ADC1Mux AmpCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 291. ADC1Mux AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

6.22.4. ADC1Mux AmpRight**Table 292. ADC1Mux AmpRight Command Verb Format**

	Verb ID	Payload	Response
Get	B80	00	See bitfield table
Set1	390	See bits [7:0] of bitfield table	0000_0000h

Table 293. ADC1Mux AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.22.5. ADC1Mux AmpLeft**Table 294. ADC1Mux AmpLeft Command Verb Format**

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 295. ADC1Mux AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

6.22.6. ADC1Mux ConSelectCtrl**Table 296. ADC1Mux ConSelectCtrl Command Verb Format**

	Verb ID	Payload	Response
Get	F01	00	See bitfield table
Set1	701	See bits [7:0] of bitfield table	0000_0000h

Table 297. ADC1Mux ConSelectCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x1	Connection select control index. (Default = CD)

6.22.7. ADC1Mux ConLstEntry0**Table 298. ADC1Mux ConLstEntry0 Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 299. ADC1Mux ConLstEntry0 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x0B	Port B
[23:16]	ConL2	R	0x0F	Port F
[15:8]	ConL1	R	0x15	CD In
[7:0]	ConL0	R	0x0E	Port E

6.22.8. ADC1Mux ConLstEntry4**Table 300. ADC1Mux ConLstEntry4 Command Verb Format**

	Verb ID	Payload	Response
Get	F02	04	See bitfield table

Table 301. ADC1Mux ConLstEntry4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No connection.
[23:16]	ConL2	R	0x0A	Port A
[15:8]	ConL1	R	0x0D	Port D
[7:0]	ConL0	R	0x0C	Port C

6.23. PCBEEP Node (NID = 0x14)

6.23.1. PCBEEP Amp

Table 302. PCBEEP Amp Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table
Set1	3A0	See bits [7:0] of bitfield table	0000_0000h

Table 303. PCBEEP Amp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x0	1 = Disable Digital PC Beep
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	Gain	RW	0x0	Mono (left) amplifier gain step number

6.23.2. PCBEEP WCap

Table 304. PCBEEP WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 305. PCBEEP WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x7	Widget type = Beep Generator
[19:4]	Rsvd1	R	0x0	Reserved
[3]	AmpParOvrd	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	N/A
[0]	Stereo	R	0x0	Mono widget

6.23.3. PCBEEP AmpCap

Table 306. PCBEEP AmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table

Table 307. PCBEEP AmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x17	Size of each step in the gain range = 6 dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x03	Number of steps in the gain range = 4 (-18dB to 0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x03	0dB-step is programmed with this offset

6.23.4. PCBEEP Gen

Table 308. PCBEEP Gen Command Verb Format

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table
Set1	70A	See bits [7:0] of bitfield table	0000_0000h

Table 309. PCBEEP Gen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:0]	Divider	RW	0x0	Enable internal PC-Beep generation. Divider = 00h - disables internal PC Beep generation and enables normal operation of the CODEC. When the Divider is not 00h - generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency: $F = (48 \text{ KHz HD Audio SYNC rate}) / (4 * \text{Divider})$ producing tones from 47 Hz to 12 KHz (logarithmic scale). This part generates tones with frequency: $F = 48000 * (257 - \text{Divider}) / 1024$ yielding a linear range from 12 KHz to 93.75 Hz in steps of 46.875 Hz. If JackSenseVSR[Rate2x], then the beep tones generated have frequency: $F = 48000 * (513 - \text{Divider}) / 1024$ yielding a range of 24 KHz to 12093.75 Hz in steps of 46.875 Hz.

6.24. CD Node (NID = 0x15)

6.24.1. CD WCap

Table 310. CD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 311. CD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	N/A for pin complex
[3]	AmpParOvrd	R	0x0	No amplifier
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

6.24.2. CD PinCap

Table 312. CD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table

Table 313. CD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCntrl	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HdphDrvCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

6.24.3. CD PinWCntrl

Table 314. CD PinWCntrl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table
Set1	707	See bits [7:0] of bitfield table	0000_0000h

Table 315. CD PinWCntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = CODEC input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

6.24.4. CD ConfigDefault

Table 316. CD ConfigDefault Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table
Set1	71C	See bits [7:0] of bitfield table	0000_0000h
Set2	71D	See bits [15:8] of bitfield table	0000_0000h
Set3	71E	See bits [23:16] of bitfield table	0000_0000h
Set4	71F	See bits [31:24] of bitfield table	0000_0000h

Table 317. CD ConfigDefault Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Config4	RW	0x90	Configuration bits used by software to determine devices attached to the CODEC.
[23:16]	Config3	RW	0x33	Configuration bits used by software to determine devices attached to the CODEC.
[15:8]	Config2	RW	0x00	Configuration bits used by software to determine devices attached to the CODEC.
[7:0]	Config1	RW	0x52	Configuration bits used by software to determine devices attached to the CODEC.

6.25. VolumeKnob Node (NID = 0x16)

6.25.1. VolumeKnob WCap

Table 318. VolumeKnob WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 319. VolumeKnob WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x6	Widget type = Volume Knob Widget
[19:0]	Rsvd1	R	0x0	Reserved. Software assumes capability of unsolicited responses and a connection list for this widget type.

6.25.2. VolumeKnob VolKnobCap

Table 320. VolumeKnob VolKnobCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	13	See bitfield table

Table 321. VolumeKnob VolKnobCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Delta	R	0x1	Indicates if software can write a base volume to the Volume Control Knob.
[6:0]	NumSteps	R	0x7F	Total number of steps in the range of the volume knob = 128

6.25.3. VolumeKnob ConLst

Table 322. VolumeKnob ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 323. VolumeKnob ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x04	Number of NID entries in connection list.

6.25.4. VolumeKnob ConLstEntry

Table 324. VolumeKnob ConLstEntry Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 325. VolumeKnob ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x05	DAC3
[23:16]	ConL2	R	0x04	DAC2
[15:8]	ConL1	R	0x03	DAC1
[7:0]	ConL0	R	0x02	DAC0

6.25.5. VolumeKnob UnsolResp

Table 326. VolumeKnob UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table
Set1	708	See bits [7:0] of bitfield table	0000_0000h

Table 327. VolumeKnob Unsolicited Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.25.6. VolumeKnob Cntrl

Table 328. VolumeKnob Cntrl Command Verb Format

	Verb ID	Payload	Response
Get	F0F	00	See bitfield table
Set1	70F	See bits [7:0] of bitfield table	0000_0000h

Table 329. VolumeKnob Cntrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Direct	RW	0x0	Direct = 1 causes the volume control to directly control the hardware volume of the slave amps. Direct = 0 causes unsolicited responses to be generated.
[6:0]	Volume	RW	0x7F	Volume, specified in steps of amplifier gain

6.26. ADC0Vol Node (NID = 0x17)

6.26.1. ADC0Vol WCap

Table 330. ADC0Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 331. ADC0Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x1	Input amplifier is present
[0]	Stereo	R	0x1	Stereo widget

6.26.2. ADC0Vol ConLst**Table 332. ADC0Vol ConLst Command Verb Format**

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 333. ADC0Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.26.3. ADC0Vol AmpRight**Table 334. ADC0Vol AmpRight Command Verb Format**

	Verb ID	Payload	Response
Get	B00	00	See bitfield table
Set1	350	See bits [7:0] of bitfield table	0000_0000h

Table 335. ADC0Vol AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.26.4. ADC0Vol AmpLeft**Table 336. ADC0Vol AmpLeft Command Verb Format**

	Verb ID	Payload	Response
Get	B20	00	See bitfield table
Set1	360	See bits [7:0] of bitfield table	0000_0000h

Table 337. ADC0Vol AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.26.5. ADC0Vol ConLstEntry**Table 338. ADC0Vol ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 339. ADC0Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x12	ADC0 Mux widget

6.26.6. ADC0Vol LR**Table 340. ADC0Vol LR Command Verb Format**

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 341. ADC0Vol LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

6.27. ADC1Vol Node (NID = 0x18)**6.27.1. ADC1Vol WCap****Table 342. ADC1Vol WCap Command Verb Format**

	Verb ID	Payload	Response
Get	F00	09	See bitfield table

Table 343. ADC1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrCntrl	R	0x0	No support for Power State control

Table 343. ADC1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[9]	Dig	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnSolCap	R	0x0	No support for Unsolicited Response
[6]	ProcWidget	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FormatOvrd	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpParOvrd	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x1	Input amplifier is present
[0]	Stereo	R	0x1	Stereo widget

6.27.2. ADC1Vol ConLst

Table 344. ADC1Vol ConLst Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table

Table 345. ADC1Vol ConLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	ConL	R	0x01	Number of NID entries in connection list.

6.27.3. ADC1Vol AmpRight**Table 346. ADC1Vol AmpRight Command Verb Format**

	Verb ID	Payload	Response
Get	B00	00	See bitfield table
Set1	350	See bits [7:0] of bitfield table	0000_0000h

Table 347. ADC1Vol AmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.27.4. ADC1Vol AmpLeft**Table 348. ADC1Vol AmpLeft Command Verb Format**

	Verb ID	Payload	Response
Get	B20	00	See bitfield table
Set1	360	See bits [7:0] of bitfield table	0000_0000h

Table 349. ADC1Vol AmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = Mute is active
[6:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

6.27.5. ADC1Vol ConLstEntry**Table 350. ADC1Vol ConLstEntry Command Verb Format**

	Verb ID	Payload	Response
Get	F02	00	See bitfield table

Table 351. ADC1Vol ConLstEntry Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	ConL3	R	0x00	No Connection
[23:16]	ConL2	R	0x00	No Connection
[15:8]	ConL1	R	0x00	No Connection
[7:0]	ConL0	R	0x13	ADC1 Mux widget

6.27.6. ADC1Vol LR**Table 352. ADC1Vol LR Command Verb Format**

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table
Set1	70C	See bits [7:0] of bitfield table	0000_0000h

Table 353. ADC1Vol LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = Enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

7. ORDERING INFORMATION

7.1. STAC9220 Part Order Numbers

The +4 V Analog voltage operation is supported by the +5 V version of the STAC9220.

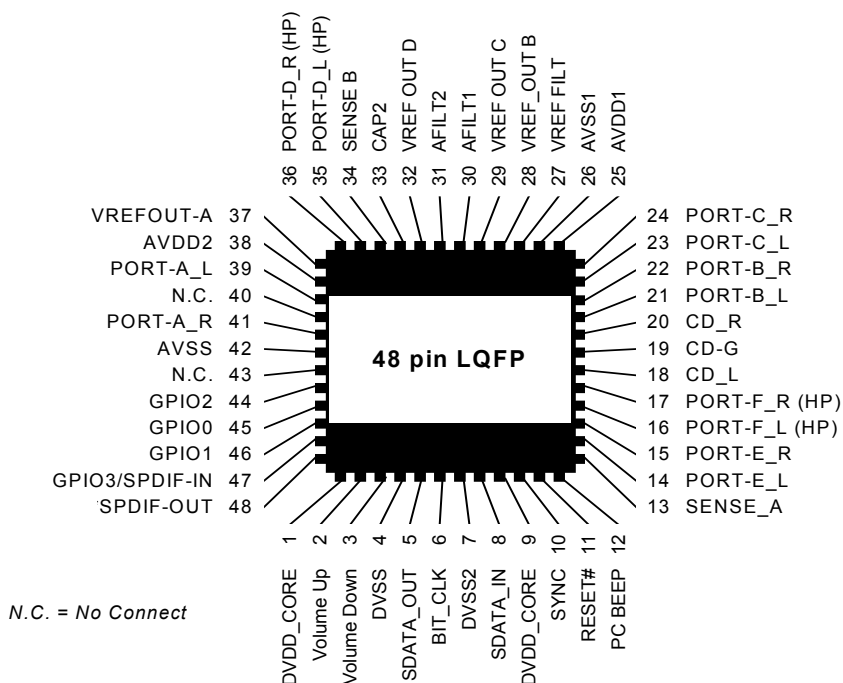
Table 354. STAC9220 Ordering Information

Part Order Number	Voltage	DAC SNR	Pkg Pins
STAC9220X5TAEyyX	5 V / 4 V	95dB	48 LQFP
STAC9220X3TAEyyX	3.3 V	95dB	48 LQFP

NOTE: When ordering these parts the “yy” will be replaced with the CODEC revision. Add an “R” to the end of any of these part numbers for delivery on Tape and Reel. The minimum order quantity for Tape and Reel is 2,000 units for both package options.

8. PIN INFORMATION

8.1. STAC9220 Pin Diagram



8.2. Pin Table for STAC9220

Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
DVDD_CORE1	Digital Vdd = 3.3 V	I(Digital)	None	1
Volume Up	Volume Control	I(Digital)	Pull-Up	2
Volume Down	Volume Control	I(Digital)	Pull-Up	3
DVSS2	Digital Ground	I(Digital)	None	4
SDATA_OUT	HD Audio Serial Data output (inbound stream)	I/O(Digital)	None	5
BIT_CLK	HD Audio Bit Clock	I(Digital)	None	6
DVSS3	Digital Ground	I(Digital)	None	7
SDATA_IN	HD Audio Serial Data input (outbound stream)	O(Digital)	None	8
DVDD_CORE3	Digital Vdd = 3.3 V	I(Digital)	None	9
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
PC BEEP	PC Beep	I(Analog)	None	12

Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
Sense A	Jack insertion detection Ports A, B, C, D	I(Analog)	None	13
PORT-E_L	Input Left Channel Port E	I(Analog)	None	14
PORT-E_R	Input Right Channel Port E	I(Analog)	None	15
PORT-F_L (HP*)	Input/Output of Left DAC3	I/O(Analog)	None	16
PORT-F_R (HP*)	Input/Output of Right DAC3	I/O(Analog)	None	17
CD-L	CD Audio Left Channel	I(Analog)	None	18
CD-G	CD Audio Analog Ground	I(Analog)	None	19
CD-R	CD Audio Right Channel	I(Analog)	None	20
PORT-B_L	Input/Output of Left DAC2	I/O(Analog)	None	21
PORT-B_R	Input/Output of Right DAC2	I/O(Analog)	None	22
PORT-C_L	Input/Output of Left DAC1	I/O(Analog)	None	23
PORT-C_R	Input/Output of Right DAC1	I/O(Analog)	None	24
AVDD1	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	25
AVSS1	Analog Ground	I(Analog)	None	26
VREF FILT	Analog Virtual Ground	O(Analog)	None	27
VREFOUT-B	Reference Voltage out drive (intended for microphone bias) for Port B	O(Analog)	None	28
VREFOUT-C	Reference Voltage out drive (intended for microphone bias) for Port C	O(Analog)	None	29
AFILT1	Anti-Aliasing Filter Cap-ADC left channel	O(Analog)	None	30
AFILT2	Anti-Aliasing Filter Cap-ADC right channel	O(Analog)	None	31
VREFOUT-D	Reference Voltage out drive (intended for microphone bias) for Port D	O(Analog)	None	32
CAP2	ADC reference Cap	O(Analog)	None	33
Sense B	Jack Insertion Detection Port E, F, G, H	I(Analog)	None	34
PORT-D_L(HP)	Input/Output of Left DAC0	I/O(Analog)	None	35
PORT-D_R(HP)	Input/Output of Right DAC0	I/O(Analog)	None	36
VREFOUT-A	Reference Voltage out drive (intended for microphone bias) for Port A	O(Analog)	None	37
AVDD2	Analog Vdd = 5.0 V or 3.3 V	I(Analog)	None	38
PORT-A_L (HP)	Input/Output of Left DAC0	I/O(Analog)	None	39
NC	No Connect	N/C	None	40
PORT-A_R (HP)	Input/Output of Right DAC0	I/O(Analog)	None	41
AVSS3	Analog Ground	I(Analog)	None	42
NC	No Connect	O(Digital)	None	43
GPIO2	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 K Ω or more	44
GPIO0	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 K Ω or more	45

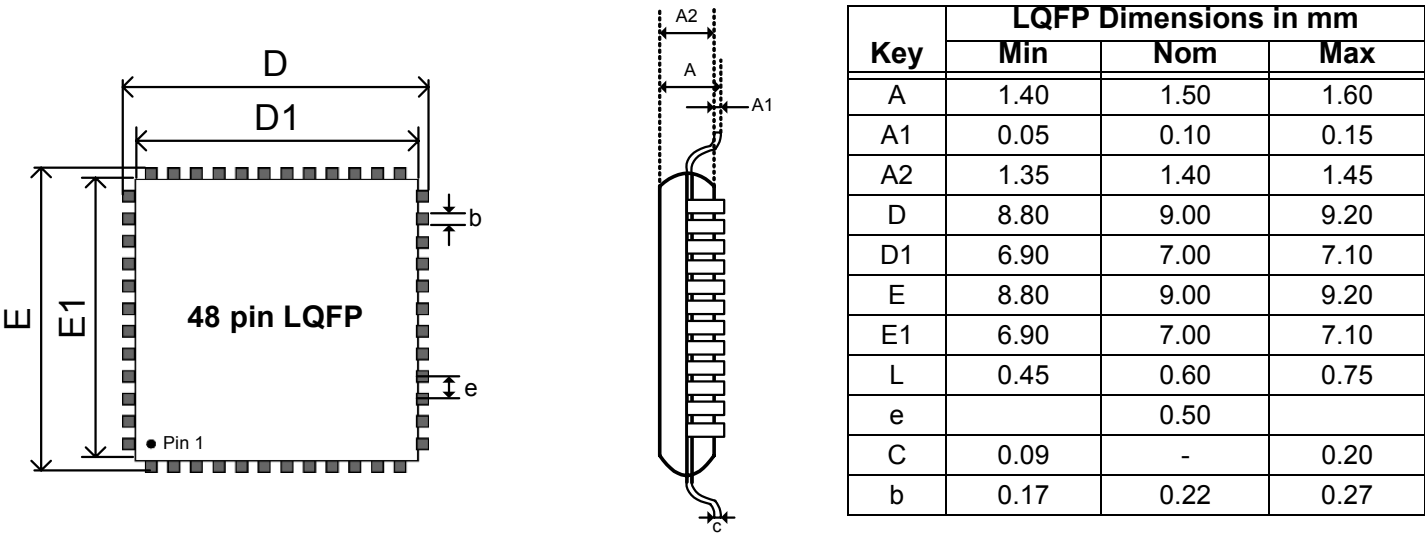
Pin Name	Pin Function	I/O	Internal Pull-up /Pull-down	Pin Location
GPIO1	General Purpose I/O tied to AVDD50K internal pull-up to AVddgnda	I/O(Digital)	Pull-up 50 K Ω or more	46
GPIO3	General Purpose I/O	I/O(Digital)	Pull-up 50 K Ω or more	47
SPDIF-OUT	SPDIF digital output)	O(Digital)	None	48

*Port F can drive 32 ohm headphones but is designed to provide less power than the headphone amplifiers on ports A and D.

9. PACKAGE DRAWINGS

9.1. 48-Pin LQFP

Figure 5. 48-Pin LQFP Package Outline and Package Dimensions



10. SOLDER REFLOW PROFILE

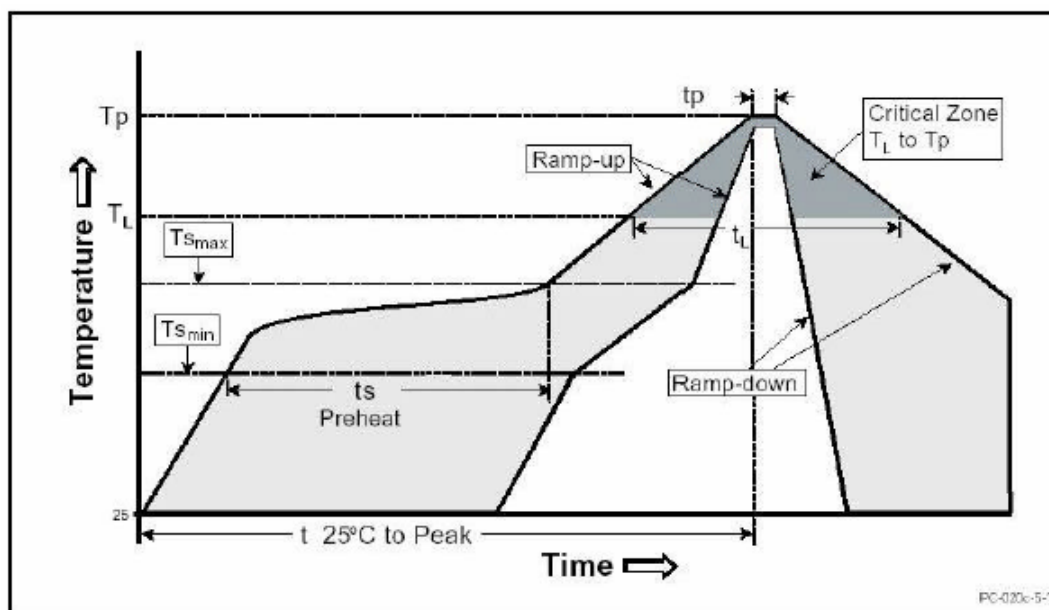
10.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature	Pb Free Assembly
Average Ramp-Up Rate ($T_{s_{max}} - T_p$)	3 °C / second max
Preheat Temperature Min ($T_{s_{min}}$)	150 °C
Preheat Temperature Max ($T_{s_{max}}$)	200 °C
Preheat Time ($t_{s_{min}} - t_{s_{max}}$)	60 - 180 seconds
Time maintained above: Temperature (T_L)	217 °C
Time (t_L)	60 - 150 seconds
Peak / Classification Temperature (T_p)	See "Package Classification Reflow Temperatures" on page 159.
Time within 5 °C of actual Peak Temperature (t_p)	20 - 40 seconds
Ramp-Down rate	6 °C / second max
Time 25 °C to Peak Temperature	8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.	

Figure 6. Solder Reflow Profile



10.2. Pb Free Process - Package Classification Reflow Temperatures

Package Type	MSL	Reflow Temperature
LQFP 48-pin	3	260 + 0 °C*

11. REVISION HISTORY

Revision	Date	Description of Change
		FOR REVISION CA1
0.5	September 2004	Initial Document
0.6	October 2004	Updated 9221 Block and Widget Diagram
0.7	November 2004	Updated Typical Connection Diagram- Fixed the D1 value for the JEDEC 48 pin drawing to say 6.90.
0.8	November 2004	Added Widget Information for CA1. Updated Block Diagrams. fixed Pin out. Updated Connection Diagrams.
0.9	December 2004	Updated 9221 Block Diagram
0.91	January 2005	Updated 48 pin drawing. Updated Reflow Profile information.
		FOR REVISION CA2
0.92	January 2005	Added Widget information for STAC9220/9221 CA2.
0.93	February 2005	Added Ordering Information, Corrected Reflow profile Note, Added 9223 information.
0.94	July 2005	Added Power Consumption Tables. Added Performance Tables for 5V, 4V, and 3.3V Analog. Changed Note 4 on AC tables. Updated ESD statement.
		FOR STAC9220 All Revisions
0.95	January 2006	Updated IDT logo. Added ADAT logo. Added "Audio Jack Presence Detect" section.
0.96	27 October 2006	Released in IDT format.
1.0	January 2008	Removed STAC9220D, STAC9221, STAC9221D, STAC9223, STAC9223D from datasheet as End of Life notices issued. Datasheet is for STAC9220 only. Corrected Device ID.

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