3.3 VOLT M13 MULTIPLEXER
IDT82V8313

Version 3
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2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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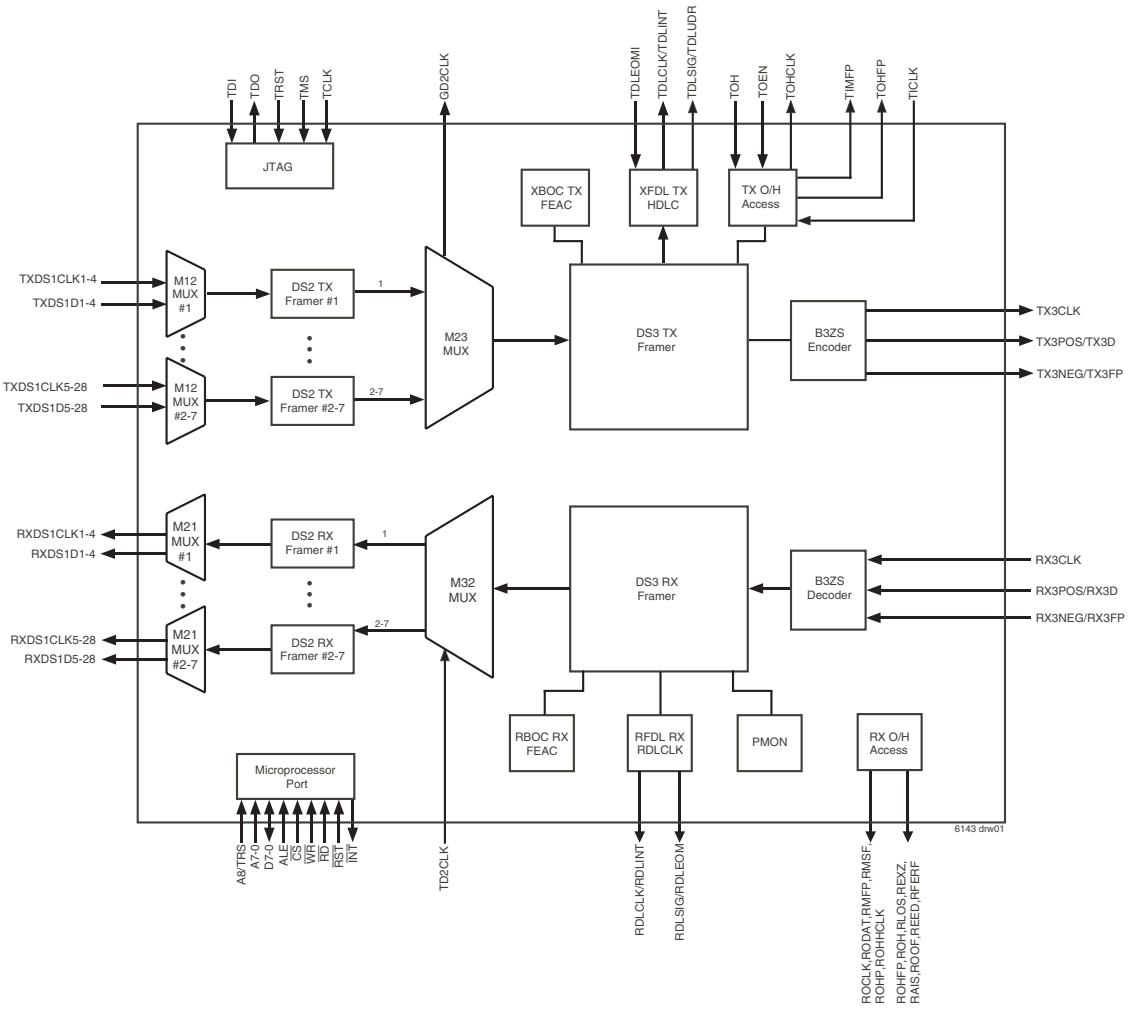
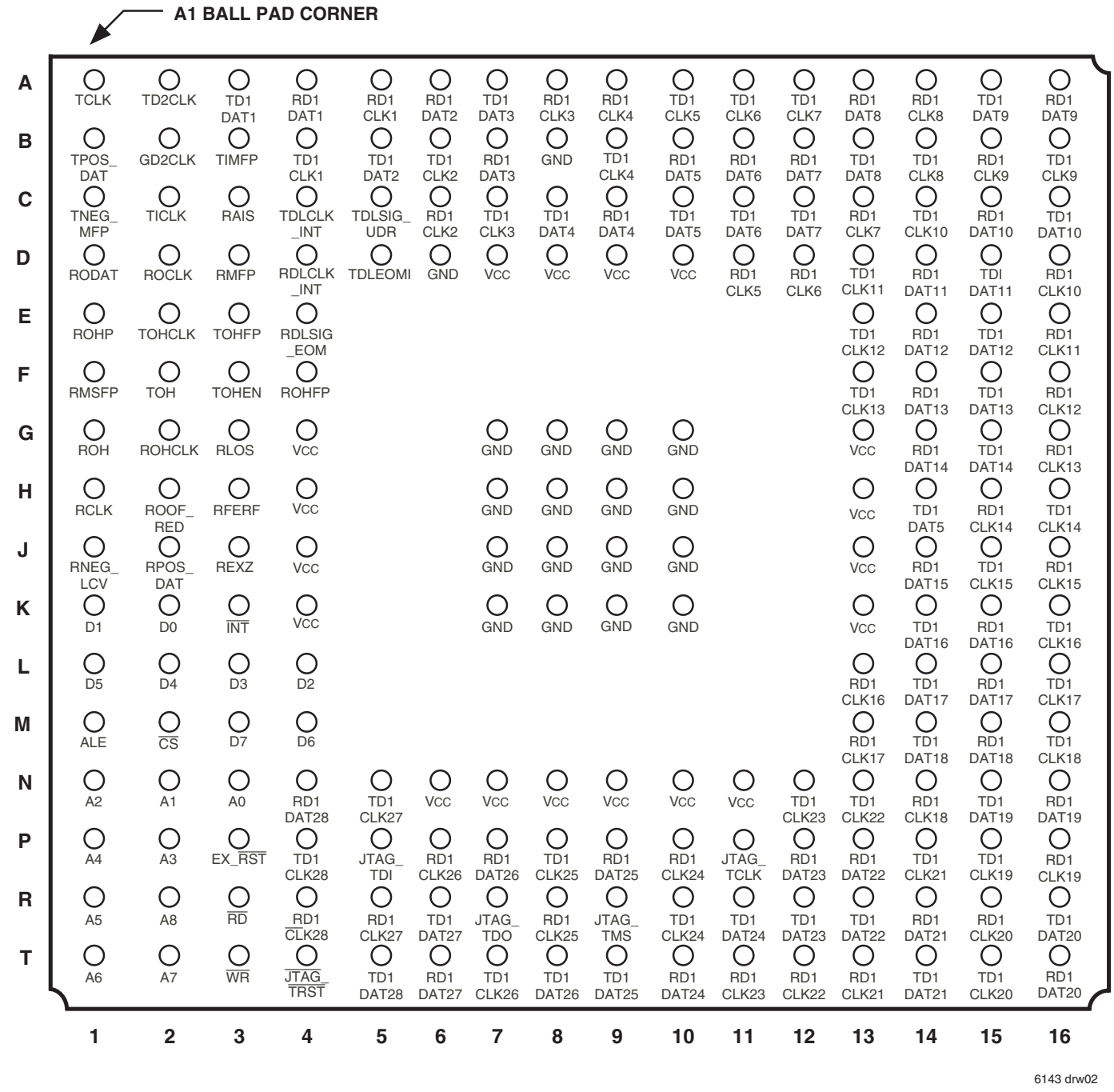
IDT82V8313

FEATURES:

- Full featured single chip M13-ideal for upgrading existing multi-line T1/E1 line cards to single line channelized T3 service
- Small footprint 17mm x 17mm BGA package and 208 pin PQFP packages available
- 3.3V operation with 5V tolerant I/O
- 28 independent DS1 clock inputs each with programmable clock edge adapter
- 28 independent DS1 outputs eatch with programmable clock edge adapter
- M12 bypass for direct input of DS2 in to the M23 multiplexer
- Programmable clock edge
- Supports M23 or C-bit parity format formats
- G.747 formats for E1 to be multiplexed onto a DS3
- DS2 LOF detectors and DS2 AIS DS2 X-bit access
- DS2 transmit/receive X-bit control/status
- DS2 F, M, and X bit insertion
- DS2 FERF and AIS under microprocessor control
- Transmission of RAI and reserved bit under microprocessor control
- Programmable preemptive inversion of C-bits for remote loopback
- DS3 idle signal generators
- DS3 LOS, LOF, P-bit Parity, C-bit Parity, AIS and idle detectors
- DS3 X-bit access
- DS3 transmit and receive AIS generation and detection
- DS3 M-frame and M-subframe boundary indications



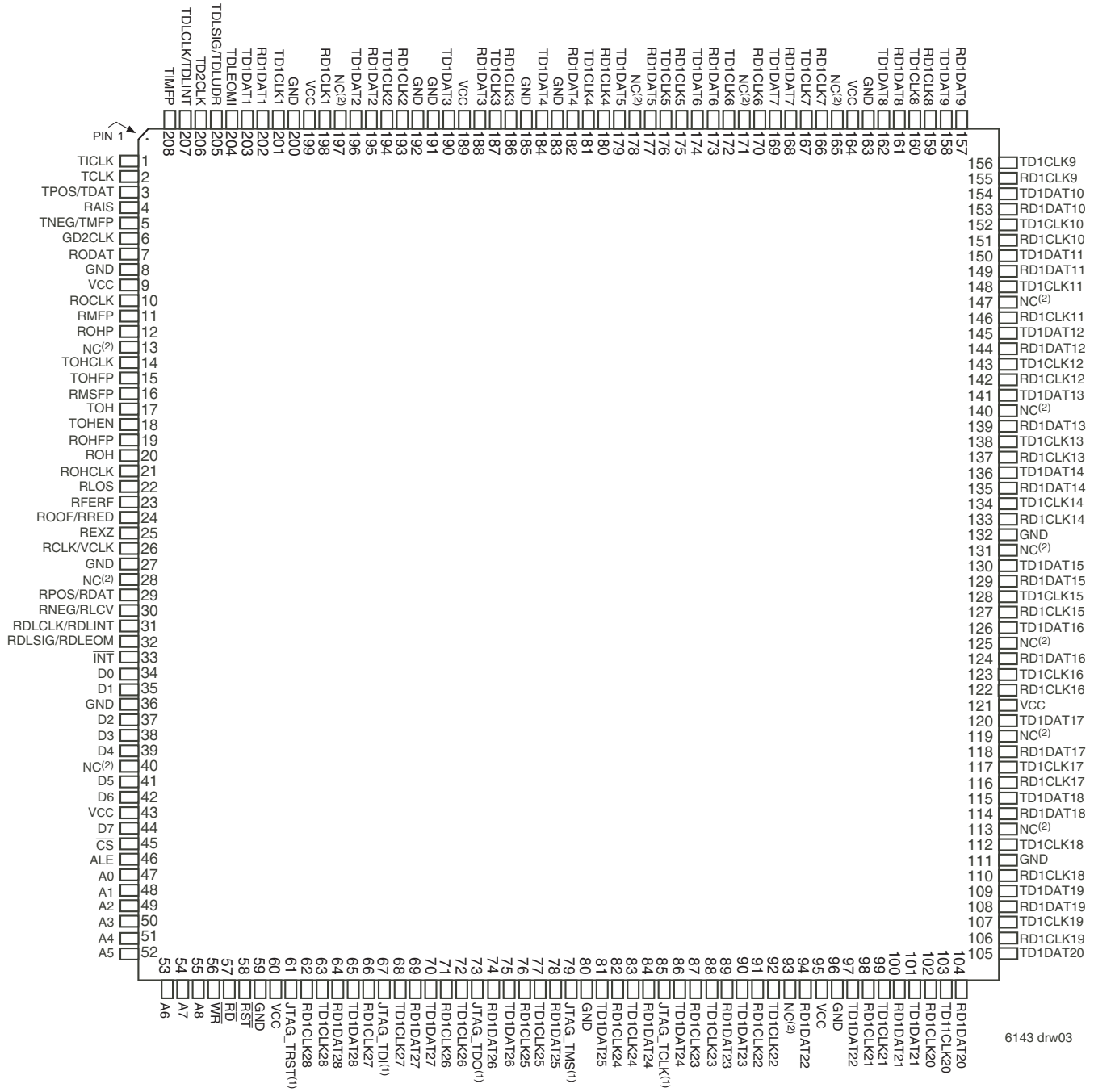
PACKAGE



6143 drw02

PBGA: 1mm pitch, 17mm x 17mm (BB208-1, order code: BB)

TOP VIEW



6143 drw03

NOTE:
1. JTAG
2. NC = No Connect

PQFP: 0.50mm pitch, 28mm x 28mm (DS208-1, order code: DS)

TOP VIEW

PIN DESCRIPTIONS

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
RCLK	Receive Clock	I	26	H1	This is the DS3 receive clock input. RCLK is nominally a 44.736 MHz, 50% duty cycle clock.
RPOS/RDAT	Receive Positive Pulse/Receive Data	I	29	J2	In dual rail mode, this pin is RPOS and represents the positive pulses of a B3ZS-encoded signal. In single rail mode, this pin is RDAT and represents the unipolar DS3 input data. The M13 can be configured to sample data on either the rising or falling edge of RCLK.
RNEG/RLCV	Receive Negative Pulse/ Receive Line Code Violation	I	30	J1	In dual rail mode, this pin is RNEG and represents the negative pulses of a B3ZS-encoded signal. In single rail mode, this pin is RLCV and can be used to insert line code violations on the DS3 input. The M13 can be configured to sample data on either the rising or falling edge of RCLK.
ROCLK	Receive Output Clock	O	10	D2	The DS3 receive output clock is a buffered version of the input RCLK. Like the RCLK, this is nominally a 44.736 MHz, 50% duty cycle clock. REXZ, RLOS, RMFP, RMSFP, and RODAT are updated on the falling edge of ROCLK.
RODAT	Receive Output Data	O	7	D1	This is a 44.736 Mb/s DS3 NRZ receive data stream decoded from the B3ZS line signal. RODAT is aligned to the frame alignment signals RMFP, RMSFP, and ROHP. RODAT is updated in the falling edge of ROCLK.
RMFP	Receive M-Frame Pulse	O	11	D3	The receive M-frame pulse signal and marks the first bit in the M-frame (X1) of the DS3 data on RODAT. In an OOF (Out Of Frame) condition the M13 internal counters will maintain the old M-frame alignment position. When the framer regains frame alignment the RMFP timing will be updated to the new timing. This may result in a change of frame alignment. RMFP is updated on the falling edge of ROCLK.
RMSFP	Receive M-subframe Frame Pulse	O	16	F1	The receive M-subframe pulse signal and marks the first bit of each M-subframe (X, P, and M) in each M-subframe of the DS3 on RODAT. In an OOF (Out Of Frame) condition the M13 internal counters will maintain the old M-frame alignment position. When the framer regains frame alignment the RMSFP timing will be updated to the new timing. This may result in a change of frame alignment. RMSFP is updated on the falling edge of ROCLK.
ROHP	Receive Overhead Pulse	O	12	E1	The receive overhead pulse signal and marks the overhead bit positions (X, P, M, C, and F) in the DS3 data on RODAT. In an OOF (Out Of Frame) condition the M13 internal counters will maintain the old frame alignment position. When the framer regains frame alignment, the ROHP timing will be updated to the new timing. This may result in a change of frame alignment. ROHP is updated in the falling edge of ROCLK.
ROHCLK	Receive Overhead Clock	O	21	G2	The receive overhead clock and transitions on each overhead bit. ROHCLK is nominally a 526 KHz. RAIS, RFERF, RFERR, RIDL, ROH, ROHFP, and ROOF are updated on the falling edge of ROHCLK.
ROH	Receive Overhead Data	O	20	G1	The receive overhead data signal transmits the overhead bits, C, F, M, P, and X bits from the receive DS3 stream. ROH is updated on the falling edge of ROHCLK.
ROHFP	Receive Overhead Frame Pulse	O	19	F4	The receive overhead frame pulse is used to mark the positions of the overhead bits within the overhead stream, ROH. ROHFP will remain high during the X1 overhead bit. ROHFP is updated on the falling edge of ROHCLK.
RLOS	Receive Loss of Signal	O	22	G3	The receive loss of signal will remain high when the dual rail NRZ format stream is selected or when a loss of signal condition is detected (175 successive zeros on RPOS and RNEG). When the one's density is greater than 33% for 175 +/i 1 bit period on the RPOS and RNEG inputs, RLOS will be set low. RLOS is updated on the falling edge of ROCLK.

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
REXZ	Receive Excessive Zeros	O	25	J3	The receive excessive zero indicates the detection of an excessive zero condition. When 3 or more successive zeros are received on the DS3 bipolar stream REXZ pulses high for one ROCLK cycle. In the uni-polar mode, REXZ is low. REXZ is updated on the falling edge of ROCLK.
RAIS	Receive Alarm Indication Signal	O	4	C3	The receive alarm indication signal is used to indicate and AIS (alarm indication) in the received DS3 signal. The RAIS will be set high when the AIS pattern has been detected for 2.23 ms or 13.5 ms as programmed by software. When the AIS pattern is absent in the DS3 signal for 2.23 ms or 13.5 ms the RAIS will be set low. RAIS is updated on the falling edge of ROHCLK.
ROOF/RRED	Receive Out of Frame/Receive Red Alarm	O	24	H2	ROOF/RREF will be ROOF when the REDO bit in the Master Alarm Enable register is 0 and will indicate an receive out-of-frame error. When no out-of-frame errors exist the ROOF will be low. ROOF will be high when there is an out-of-frame condition: 3 out of 16 (default) or 3 out of 8 consecutive F-bit errors are detected, or when more M-bit errors are detected in 3 out of 4 consecutive M-frames. ROOF is updated on the falling edge of ROHCLK. ROOF/RRED will be RRED when the REDO bit the Master Alarm Enable register is 1 and will indicate an out-of-frame condition or a DS3 loss of signal condition. A DS3 out-of-frame condition is considered when there are no transitions for 2.23 ms or 13.5 ms (software programmable) and RRED will be set high. RRED will be reset low when the out-of-frame condition or loss of signal condition are absent for 2.23 or 13.5 ms. RRED is updated on the falling edge of ROHCLK.
RFERF	Receive Far End Receive Failure	O	23	H3	The receive far end receive failure reflects the internal state of the internal FERF but the RFERF state is delayed by two M-frames. FERF is set high when both X1 and X2 are 0 in the M-frame. When X1 and X2 are both high in the M-frame, FERF is set low. Otherwise, FERF remains in its previous state when X1 • X2 in the current frame. The RFERF latency is used to provide better than 99.99% chance of freezing (holding FERF in its previous state) upon a valid state value during an out-of-frame. RFERF is updated every M-frame on the falling edge on ROHCLK.
RDLCLK/ RDLINT	Receive Data Link Clock/ Receive Data Link Interrupt	O	31	D4	RDLCLK/RDLINT will be RDLCLK when the REXHDLC bit in the Master HDLC Configuration Register is set to 1 and is used as the receive data link clock when an external HDLC receiver is selected. The RDLCLK is the clock for the external processing of the data link signal extracted by the DS3 framer. RDLCLK is nominally a 28.2 kHz clock that is low for at least 1.9us per cycle and is updated 3 times per M-frame. RDLCLK is updated on the falling edge of the ROHCLK. RDLCLK/RDLINT will be RDLINT when the REXHDLC bit in the Master HDLC Configuration Register is set to 0 and is used as the data link interrupt when an internal HDLC receiver is selected. When an HDLC receiver event occurs the RDLINT will reflect a change in status. By reading the Interrupt Enable/Status register, the interrupt will be cleared, both the register and the RDLINT pin. RDLINT is updated on the falling edge of ROHCLK. RDLINT is a configurable active low open-drain out or active high open-drain output. In the case where an external DMA device is used, RDLINT would be directly connected, however if the interrupt is being handled by a microprocessor, the RFDL may be wired-ORed with the $\overline{INT}$ output. In this later case, RDLINT should be configured as a active-low open drain output.

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
RDLSIG/ RDLEOM	Receive Data Link Signal/ Receive Data Link End Of Message	O	32	E4	RDLSIG/RDLEOM will be RDLSIG when the REXHDLC bit in the Master HDLC Configuration Register is set to 1 and is used as the receive data link signal when an external HDLC receiver is selected. The RDLSIG is the C-bit message used in C-bit parity mode and transmits the three C-bits from the fifth M-subframe in the DS3 frame. RDLSIG is updated on the falling edge of the RDLCLK. RDLSIG/RDLEOM will be RDLEOM when the REXHDLC bit in the Master HDLC Configuration Register is set to 0 and is used as the receive end of message signal when an internal HDLC receiver is selected. RDLEOM is used to denote the last byte of a sequence that is read from the HDLC receiver or to denote an overflow condition in the receive HDLC buffer. RDLEOM is updated on the falling edge of ROHCLK. In order to clear/deassert the RDLEOM the supervising microprocessor must read the Interrupt Enable/Status Register. In the case where RDLEOM would be connected to a supervising microprocessor, an external DMA is used. The RDLEOM would be programmed to be active-low, open-drain and wired-ORed with the $\overline{INT}$ to signal the microprocessor that the a complete message is ready.
RD1CLK1-28	Receive DS1 Clock	O	*See TQFP table below for details.	*See BGA table below for details,	RD1CLK1-28 are the receive DS1 clocks used in conjunction with the RD1DAT. These clocks are at the T1 nominal rate of 1.544MHz, but will have jitter due to the demultiplexing and destuffing processes. RD1DAT28-1 can be programmed to update on either the rising or falling edge of RD1CLK. For G.747, the internal M12 multiplexers still uses the RD1CLKs to clock RD1DAT out, however every fourth clock, RD1CLK4, 8, 12, 16, 20, 24, and 28 clocks, is unused and in turn output LOW. These clocks run at the nominal rate of 2.048MHz but will have jitter due to the demultiplexing and destuffing processes. If a DS2 is inserted into the M13, thereby bypassing the M12 multiplexer, every fourth clock RD1CLK4, 8, 12, 16, 20, 24, and 28 can be used as a DS2 clock. In this case the unused clocks for that group will output LOW. The DS2 clock has a nominal rate of 6.312MHz.
RD1DAT1-28	Receive DS1 Data	O	*See TQFP table below for details.	*See BGA table below for details	RD1DAT1-28 is the DS1 data demultiplexed from the incoming DS3 stream. RD1DAT1-28 are updated on either the rising or falling edge of the corresponding RD1CLK1-28. In G.747, where the M12 multiplexers mux E1 data, RD1DAT 4, 8, 12, 16, 20, 24, and 28 are held low, while the remaining streams operate at a nominal 2.048MHz data rate. M12 multiplexers are bypassed and DS2 data is output the fourth stream of the group is used to output data. The remaining three streams of the group will be held low.
TD1CLK1-28	Transmit DS1 Clock	I	*See TQFP table below for details.	*See BGA table below for deatils	The transmit DS1 clock, TD1CLK1-28 is used to sample incoming data on TD1DAT1-28 to be multiplexed into a DS3. The M13 expects a nominal 1.544MHz clocks and expects minimal jitter and wander of a standard DS1. TD1DAT1-28 are sampled on either the rising or falling edge of TD1CLK1-28. In G.747 multiplexing not all TD1 inputs are used. In this case, every fourth input (TD1CLK4, 8, 12, 16, 20, 24, and 28) is unused, ignored and must be tied to GND. The remaining clocks should be running at a nominal rate of 2.048MHz and expects minimal jitter and wander of a standard DS1. When the internal M12 multiplexers are bypassed, the M13 device will use every fourth clock (TD1CLK4, 8, 12, 16, 20, 24, and 28) as the DS2 input clock. In this case, the remaining clocks are unused, ignored and the unused inputs must be tied to GND.
TD1DAT1-28	Transmit DS1 Data	I	*See TQFP table below for details.	*See BGA table below fo details	The transmit DS1 data TD1DAT is the input data that is multiplexed in to a DS3. Input data can be programmed to sample on either the rising or falling edges of TD1CLK1-28. In G.747, where the M12 multiplexers mux E1 data, every fourth data stream (TD1DAT4, 8, 12, 16, 20, 24, and 28) is ignored and must be tied to GND. In cases where a DS2 is inserted directly into the M23 stage, every fourth TD1DAT (TD1DAT4, 8, 12, 16, 20, 24, and 28) can be used. In this case the remaining TD1DAT streams of the group are ignored and must be tied to GND.

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
GD2CLK	Generated DS2 Clock	O	6	B2	In M13 and C-bit parity modes, this is the transmit generated DS2 clock. In M13 operation this clock is nominally a 6.311993 MHz clock which translates to a 39.1% stuffing ratio. In C-bit parity mode this clock is nominally a 6.3062723 MHz clock, which translates to a stuffing rate of 100% (used for C-bit parity). The GD2CLK may be tied directly to the TD2CLK clock.
TD2CLK	Transmit DS2 Clock	I	206	A2	The TD2CLK is the transmit DS2 clock and is the clock used in the M12 multiplexer. TD2CLK is nominally a 6.312 MHz, 50% duty cycle clock and can be derived from the GD2CLK.
TDLSIG/ TDLUDR	Transmit Data Link Signal/ Transmit Data Underrun	O	205	C5	The TDLSIG/TDLUDR will be transmit data link, TDLSIG, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 1. When an external HDLC receiver is selected, TDLSIG will carry the the three C-bits in M-subframe #5 in the DS3. When C-bit parity mode is not enabled TDLSIG is ignored. TDLSIG is sampled on the rising edge of TDLCLK.The TDLSIG/TDLUDR will be the transmit data link underrun, TDLUDR, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 0. When an internal HDLC receiver is selected, TDLUDR is asserted when an internal HDLC transmitter underruns. TDLUDR can be cleared (deasserted) by writing to the XFDL Interrupt Status Register. TDLUDR is a programmable polarity, open-drain output. On reset, TDLSIG/TDLUDR is TDLSIG. The TEXHDLC register should be programmed after reset to the appropriate mode. When an external DMA is used, TDLUDR will be configured as an active-low output and wired-ORed with the $\overline{INT}$ output and routed to the supervising microprocessor. In that way, in the case of a transmit buffer underrun the supervising microprocessor will be notified.
TDLCLK/ TDLINT	Transmit Data Link Clock/ Transmit Data Link Interrupt	O	207	C4	The TDLCLK/TDLINT will be transmit data link clock, TDLCLK, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 1. When an external HDLC receiver is selected, TDLCLK will provide the timing for the external maintenance data link inserted by the DS3. TDLCLK is nominally a 28.2 KHz clock which is low for at least 1.9us per cycle. TDLCLK is updated on the falling edge of the TOHCLK and cycles three times per M-frame (one for each C-bit). The TDLCLK/TDLINT will be the transmit data link interrupt, TDLINT, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 0. When an internal HDLC receiver is selected, TDLINT is asserted when the last data byte is written to the internal HDLC transmitter. A write to the XFDL Configuration Register will end the current message transmission while a write to the XFDL Transmit Data Register will provide more data. TDLINT is a programmable polarity, open-drain output. On reset, TDLCLK/TDLINT is TDLINT. The TEXHDLC register should be programmed after reset to the appropriate mode. When an external DMA is used, TDLINT will be configured as an active-low output and wired-ORed with the $\overline{INT}$ output and routed to the supervising microprocessor. In that way, the supervising microprocessor will be notified and can service the XFDL.
TDLEMOI	Transmit Data Link End Of Message Input	I	204	D5	The transmit data link end of message input, TDLEMOI, is an alternate method for an external DMA controller to signal the end of the transmitted message to the HDLC transmitter. As the TDLEMOI is an alternative to writing the XFDL configuration register, appropriately the TDLEMOI will set the EOM bit in the XFD: Configuration register. The TDLEMOI input may be asserted before or after the write of the last byte, but must be asserted before the next byte (within 210 us of the last assertion of TDLINT or the $\overline{INT}$ bit in the XFDL Status Register). If no data transmission is pending, TDLEMOI is ignored.

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
TICLK	Transmit Input Clock	I	1	C2	The transmit input clock, TICLK, provides the timing for the DS3 input. TICLK is nominally a 44.736 MHz, 50% duty cycle clock. TIMFP is sampled on the rising edge of TICLK.
TIMFP	Transmit Input M-frame Frame Pulse	I	208	B3	The transmit M-frame pulse, TIMFP, provides the timing/alignment of the M-frame within the DS3 data, TDAT. The first bit (X1) of the M-frame on TDAT will occur within several TICLK cycle and will be confirmed by the output on TMFP. TIMFP may be pulled low if this kind of feedback is not required. TIMFP is sampled on the rising edge of TICLK.
TOH	Transmit Overhead Data	I	17	F2	The transmit overhead data, TOH, represents the overhead bits (C, F, M, P, and X) that may be inserted into the transmitted DS3. TOH is sampled on the rising edge of TOHCLK.
TOHEN	Transmit Overhead Enable	I	18	F3	The transmit overhead insertion, TOHEN, is the enable signal that is used in conjunction with the TOH, data input. When TOHEN is high the associated data on TOH will be inserted in to the DS3. When the TOHEN is low, the internal DS3 framer generates and inserts the DS3 overhead bits into the output DS3 stream. TOHEN is sampled on the rising edge of TOHCLK.
TOHFP	Transmit Overhead Frame Pulse	O	15	E3	The transmit overhead frame position, TOHFP, marks the beginning of the first M-frame, and aligns the TOH data to the DS3 M-frame. TOHFP will be high during the X1 overhead bit position. TOHFP is updated on the falling edge of TOHCLK.
TOHCLK	Transmit Overhead Clock	O	14	E2	The transmit overhead clock, TOHCLK, provides the timing transmit overhead bits. TOHCLK is nominally a 526 KHz clock. TOHFP is updated on the falling edge of TOHCLK. TOH and TOHEN are sampled on the rising edge of TOHCLK.
JCLK	Transmit DS3 Clock	O	2	A1	The transmit clock, TCLK, provides timing for other circuitry to synchronize with the DS3 transmitter. TCLK is nominally a 44.736 MHz, 50% duty cycle clock.
TPOS/TDAT	Transmit DS3 Positive Pulse/ Transmit DS3 Data	O	3	B1	In dual rail mode, TPOS/TDAT, is TPOS and represents the positive pulses of a B3ZS-encoded line. TPOS is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK. In single rail mode, TPOS/TDAT, is TDAT and represents the unipolar DS3 output data. Like the TPOS, TDAT is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK.
TNEG/TMFP	Transmit DS3 Negative Pulse/ Transmit Multi-frame Pulse	O	5	C1	In dual rail mode, TNEG/TMFP, is TNEG and represents the negative pulses of a B3ZS-encoded line. TNEG is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK. In single rail mode, TNEG/TMFP, is TMFP and represents the transmit multi-frame pulse. TMFP will be high during the first bit of the DS3 multiframe output on TDAT. TMFP is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK.
$\overline{INT}$	Interrupt	O	33	K3	$\overline{INT}$ is the output interrupt pin. When an interrupt occurs in any of the TSBs, DS2 FRMR, DS3 FRMR, MX12, MX23, PMON, or RBOC, $\overline{INT}$ will go low, unless the interrupt is masked. In order to clear $\overline{INT}$, all pending interrupt TSBs must be read and cleared, otherwise $\overline{INT}$ will remain low. $\overline{INT}$ is an open drain output so it can be wired-ORed with other active-low open-drain output pins of the device.
$\overline{CS}$	Chip Select	I	45	M2	This active LOW input is used by a microprocessor to activate the microprocessor port. $\overline{CS}$ must go low for at least once after powerup. If $\overline{CS}$ is not used it must be tied to an inverted version of $\overline{RST}$.
$\overline{RD}$	Microprocessor Read	I	57	R3	This active low input controls the direction of the data bus lines (D0-7) during a microprocessor access. When $\overline{RD}$ is low, D0-7 are output.
$\overline{WR}$	Microprocessor Write	I	56	T3	This active low input controls the direction of the data bus lines (D0-7) during a microprocessor access. When $\overline{WR}$ is low, D0-7 are input.

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
D0-7	Microprocessor Data	I/O	*See TQFP table below for details	*See BGA table below for deatils	These pins are the data bits of the microprocessor port.
A0-8	Microprocessor Address	I	*See TQFP table below for details	*See BGA table below for details	These address lines access all internal memories.
$\overline{RST}$	Reset	I	58	P3	This input puts the IDT82V8313 into a reset state that clears the device internal counters and registers. The RESET pin must be held LOW for a minimum of 100ns to properly reset the device. This pin has a weak internal pull-up resistor.
ALE	Address Latch Enable	I	46	M1	The address latch enable is an active high input that will latch the A0-7 address bus. The ALE is used in a multiplexed address/data microprocessor environment. The ALE has a weak internal pull-up resistor.
VCC	VCC	I	*See TQFP table below for details	*See BGA table below for details	This is the +3.3 Volt power supply for the core of the device.
VCC	VCC	I	*See TQFP table below for details	*See BGA table below for details	This is the +3.3 Volt power supply for the i/o of the device.
GND	Ground	I	*See TQFP table below for details	*See BGA table below for details	Ground Rail.
TDI	JTAG Test Serial Data In	I		P5	JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven.
TDO	JTAG Test Serial Data Out	O		R7	JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled.
TRST	JTAG Test Reset	I		T4	Asynchronously initializes the JTAG Test Access Port controller by putting it in the Test-Logic-Reset state. This pin is pulled HIGH by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V71660 is in the normal functional mode.
TCLK	JTAG Test Clock	I		P11	Provides the clock to the JTAG test logic.
TMS	JTAG Test Mode Select	I		R9	JTAG signal that controls the state transitions of the Test Access Port controller. This pin is pulled HIGH by an internal pull-up when not driven.

TQFP PIN NUMBER TABLE

SYMBOL	NAME	I/O	PIN NUMBER
RD1CLK1-28	Receive DS1 Clock	O	198, 193, 186, 180, 175, 170, 166, 159, 155, 151, 146, 142, 137, 133, 127, 122, 116, 110, 106, 102, 98, 91, 87, 82, 76, 71, 66, 62.
RD1DAT1-28	Receive DS1 Data	O	202, 195, 188, 182, 177, 173, 168, 161, 157, 153, 149, 144, 139, 135, 129, 124, 118, 114, 108, 104, 100, 94, 89, 84, 78, 74, 69, 64.
TD1CLK1-28	Transmit DS1 Clock	I	201, 194, 187, 181, 176, 172, 167, 160, 156, 152, 148, 143, 138, 134, 128, 123, 117, 112, 107, 103, 99, 92, 88, 83, 77, 72, 68, 63.
TD1DAT1-28	Transmit DS1 Data	I	203. 196, 190, 184, 179, 174, 169, 162, 158, 154, 150, 145, 141, 136, 130, 126, 120, 115, 109, 105, 101, 97, 90, 86, 81, 75, 70, 65.
D0-7	Microprocessor Data	I/O	34, 35, 37, 38, 39, 41, 42, 44.
A0-8	Microprocessor Address	I	47, 48, 49, 50, 51, 52, 53, 54, 55.
Vcc	Vcc	I	9, 43, 60, 95, 121, 164, 189, 199.
GND	Ground	I	8, 11, 27, 36, 59, 80, 96, 111, 132, 163, 183, 185, 191, 192, 200.

BGA PIN NUMBER TABLE

SYMBOL	NAME	I/O	PIN DESCRIPTION
RD1CLK1-28	Receive DS1 Clock	O	A 5, C6, A8, A9, D11, D12, C13, A14, B15, D16, E16, F16, G16, H16, J16, L13, M13, N14, R16, R15, T13, T12, T11, P10, R8, P6, R5, R4.
RD1DAT1-28	Receive DS1 Data	O	A4, A6, B7, C9, B10, B11, B12, A13, A16, C15, D14, E14, J14, K15, L15, M15, N16, J15, R14, P13, T10, P9, P7, T6, N4.
TD1CLK1-28	Transmit DS1 Clock	I	B4, B6, C7, B9, A10, A11, A12, B14, B16, C14, D13, E13, F13, H16, J15, K16, L16, M16, P15, T15, P14, N13, N12, R10, P8, T7, N5, P4.
TD1DAT1-28	Transmit DS1 Transmit	I	A3, B5, A7, C8, C10, C11, C12, B13, A15, C16, D15, E15, F15, G15, H14, K14, L14, M14, N15, R16, T14, R13, R12, R11, T9, T8, R6, T5.
D0-7	Microprocessor Data	I/O	K2, K1, L4, L3, L2, L1, M4, M3.
A0-8	Microprocessor Address	I	N3, N2, P2, P1, R1,T1, T2, R2.
Vcc	Vcc	I	G4, H4, J4, K4, N6, N7, N8, N9, N10, N11, K13, J13, K13, G13, D6, D7, D8, D9, D10.
GND	Ground	I	B8, D6, G7-G10, H7-H10, J7-J10, K7-K10.

REGISTER MEMORY MAP

TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
00H	R/W	DS3RCACT	DS3TCACT	DS2TCACT	-	-	-	-	Reset	Master Reset/Clock Status
01H	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Revision/Global PMON Update
02H	R/W	EXD2CLK	BYP7	BYP6	BYP5	BYP4	BYP3	BYP2	BYP1	Master Bypass Configuration
03H	R/W	REXHDLC	TEXHDLC	-	-	REOMPOL	TUDRPOL	RINTPOL	TINTPOL	Master HDLC Configuration
04H	R/W	-		-	-	LINEAIS1	LINEAIS2	LLBE	DLBE	Master Loopback Configuration
05H	R/W	-	-	-	TINV	TFALL	TUNI	RINV	RFALL	Master Interface Configuration
06H	R/W	TNR	RNR	ALTFEBE	REDO	RED2ALME	DS2ALME	RED3ALME	DS3ALME	Master Alarm Enable/Network Requirement Bit
07H	R/W	-	-	-	-	DBCTRL	-	HIZDATA	HIZIO	Master Test
08H	R	REG2	REG3	XFDLINT	MX23	DS3FRMR	RFDLINT	RFDLEOM	RBOC	Master Interrupt Source #1
09H	R	XFDLUDR	DS2FRMR7	DS2FRMR6	DS2FRMR5	DS2FRMR4	DS2FRMR3	DS2FRMR2	DS2FRMR1	Master Interrupt Source #2
0AH	R	DS3PMON	MX12 7	MX12 6	MX12 5	MX12 4	MX12 3	MX12 2	MX12 1	Master Interrupt Source #3
0BH	-	-	-	-	-	-	-	-	-	Reserved
0CH	R/W	CBTRAN	AIS	IDL	FERF	SBOW	-	-	CBIT	DS3 TRAN Configuration
0DH	R/W	DLOS	DLCV	-	DFERR	DMERR	DCPERR	DPERR	DFEBE	DS3 TRAN Diagnostic
0EH - 11H	-	-	-	-	-	-	-	-	-	Reserved
11H	R/W	-	-	-	-	-	INTE	INTR	OVR	DS3 PMON Interrupt Enable/Status
12H - 13H	-	-	-	-	-	-	-	-		Reserved
14H	R	LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	DS3 PMON LCV Count (LSB)
15H	R	LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	DS3 PMON LCV Count (MSB)
16H	R	FERR7	FERR6	FERR5	FERR4	FERR3	FERR2	FERR1	FERR0	DS3 PMON FERR Count (LSB)
17H	R	-	-	-	-	-	-	FERR9	FERR8	DS3 PMON FERR Count (MSB)
18H	R	EXZS7	EXZS6	EXZS5	EXZS4	EXZS3	EXZS2	EXZS1	EXZS0	DS3 PMON EXZS Count (LSB)

TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
19H	R	EXZS15	EXZS14	EXZS13	EXZS12	EXZS11	EXZS10	EXZS9	EXZS8	DS3 PMON EXZS Count (MSB)
1AH	R	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0	DS3 PMON PERR Count (LSB)
1BH	R	-	-	PERR13	PERR12	PERR11	PERR10	PERR9	PERR8	DS3 PMON PERR Count (MSB)
1CH	R	CPERR7	CPERR6	CPERR5	CPERR4	CPERR3	CPERR2	CPERR1	CPERR0	DS3 PMON CPERR Count (LSB)
1DH	R	-	-	CPERR13	CPERR12	CPERR11	CPERR10	CPERR9	CPERR8	DS3 PMON CPERR Count (MSB)
1EH	R	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0	DS3 PMON FEBE Count (LSB)
1FH	R	-	-	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8	DS3 PMON FEBE Count (MSB)
20H	R/W	-	-	-	EOM	INTE	ABT	CRC	EN	XFDL TSB Configuration
21H	R/W	-	-	-	-	-	-	INT	UDR	XFDL TSB Interrupt Status
22H	R/W	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	XFDL TSB Transmit Data
23H	--	-	-	-	-	-	-	-	-	Reserved
24H	R/W	-	-	-	-	-	-	TR	EN	RFDL TSB Configuration
25H	R/W	-	-	-	-	-	INTC1	INTC0	INT	RFDL Interrupt Control/Status
26H	R	FE	OVR	FLG	EOM	CRC	NVB2	NVB1	NVB0	RFDL TSB Status
27H	R	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	RFDL TSB Receive Data
28H	R/W	-	-	-	-	LBCOD1	LBCODE0	CBE	INTE	MX23 Configuration
29H	R/W	-	DAIS7	DAIS6	DAIS5	DAIS4	DAIS3	DAIS2	DAIS1	MX23 Demux AIS Insert
2AH	R/W	-	MAIS7	MAIS6	MAIS5	MAIS4	MAIS3	MAIS2	MAIS1	MX23 Mux AIS Insert
2BH	R/W	-	LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	MX23 Loopback Activate
2CH	R/W	0	ILBE7	ILBE6	ILBE5	ILBE4	ILBE3	ILBE23	ILBE1	MX23 Loopback Request Insert
2DH	R	-	LBRD7	LBRD6	LBRD5	LBRD4	LBRD3	LBRD2	LBRD1	MX23 Loopback Request Detect
2EH	R	-	LBRI7	LBRI6	LBRI5	LBRI4	LBRI3	LBRI2	LBRI1	MX23 Loopback Request Interrupt
2FH - 30H	-	-	-	-	-	-	-	-	-	Reserved
31H	R/W	-	-	BC5	BC4	BC3	BC2	BC1	BC0	FEAC XBOC Code

TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
32H	R/W	-	-	-	-	-	IDLE	AVC	BOCE	FEAC RBOC Configuration/ Interrupt Enable
33H	R	IDLEI	BOCI	BOC5	BOC4	BOC3	BOC2	BOC1	BOC0	FEAC RBOC Interrupt Status
34H	R/W	AISPAT	FDET	MBDIS	M3O8	UNI	REFR	AISC	CBE	DS3 FRMR Configuration
35H ACE=0 ACE=1	R/W	 COFAE -	 REDE -	 CBITE AISONES	 FERFE BPVO	 IDLE EXZSO	 AISE EXTYPE	 OOFE SALGO	 LOSE ALGOTYPE	DS3 FRMR Interrupt Enable/Additional Configuration
36H	R	COFAI	REDI	CBITI	FERFI	IDLI	AISI	OOFI	LOSI	DS3 FRMR Interrupt Status
37H	R/W	ACE	REDV	CBITV	FERFV	IDLV	AISV	OOFV	LOSV	DS3 FRMR Status
38H - 3FH	-	-	-	-	-	-	-	-	-	Reserved
40H	R/W	G747	-	WORD	M2O5	MDBIS	REF	-	-	DS2 #1 FRMR PERR Configuration
41H	R/W	COFAE	-	REDE	FERFE	RESE	AISE	OOFE	-	DS2 #1 FRMR PERR Interrupt Enable
42H	R	COFAI	-	REDI	FERFI	RESI	AISI	OOFI	-	DS2 #1 FRMR PERR Interrupt Status
43H	R	-	-	REDV	FERFV	RESV	AISV	OOFV	-	DS2 #1 FRMR PERR Status
44H	R/W	-	-	-	-	-	INTE	INTR	OVR	DS2 #1 FRMR Monitor Interrupt Enable/Status
45H	R	FERR7	FERR6	FERR5	FERR4	FERR3	FERR2	FERR1	FERR0	DS2 #1 FRMR FERR Count
46H	R	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0	DS2 #1 FRMR PERR Count (LSB)
47H	R	-	-	-	PERR12	PERR11	PERR10	PERR9	PERR8	DS2 #1 FRMR PERR Count (MSB)
48H	R/W	G747	PINV	MINV	FINV	ZAIS	XFERF	XRES	INTE	DS2 #1 MX12 Configuration and Control
49H	R/W	-	-	-	-	-	-	LBCODE1	LBCODE0	DS2 #1 MX12 Loopback Code Select
4AH	R/W	MAIS4	MAIS3	MAIS2	MAIS1	DAIS4	DAIS3	DAIS2	DAIS1	DS2 #1 MX12 AIS Insert
4BH	R/W	ILBR4	ILBR3	ILBR2	ILBR1	LBA4	LBA3	LBA2	LBA1	DS2 #1 MX12 Loopback Active
4CH	R	LBRI4	LBRI3	LBRI2	LBRI1	LBRD4	LBRD3	LBRD2	LBRD1	DS2 #1 MX12 Loopback Interrupt

TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
4DH	R/W	TXESEL4	TXESEL3	TXESEL2	TXESEL1	RXESEL4	RXESEL3	RXELES2	RXESEL2	DS1 #1 Transmit and Receive Edge Select
50H - 57H	R/W									DS2 #4 MX12 Registers
58H - 5DH	R/W									DS2 #2 MX12 Registers
60H - 67H	R/W									DS2 #3 FRMR Registers
68H - 6DH	R/W									DS2 #3 MX12 Registers
70H - 77H	R/W									DS2 #4 FRMR Registers
78H - 7DH	R/W									DS2 #4 MX12 Registers
80H - 87H	R/W									DS2 #5 FRMR Registers
88H - 8DH	R/W									DS2 #5 MX12 Registers
90H - 97H	R/W									DS2 #6 FRMR Registers
98H - 9DH	R/W									DS2 #6 MX12 Registers
A0H A1H A2H A3H A4H A5H A6H A7H	R/W	G747 COFAE COFAI - - FERR7 PERR7 -	- COFAE - - - FERR6 PERR6 -	WORD REDE REDI REDV - FERR5 PERR5 -	M2O5 FERFE FERFI FERFV - FERR4 PERR4 PERR12	MDBIS RESE RESI RESV - FERR3 PERR3 PERR11	REF AISE AISI AISV INTE FERR2 PERR2 PERR10	- OOFE OFFI OOFV INTR FERR1 PERR1 PERR9	- - - - OVR FERR0 PERR0 PERR8	DS2 #7 FRMR Registers
A8H A9H AAH ABH ACH ADH	R/W	G747 - MAIS4 ILBR4 LBR4 TXESEL4	PINV - MAIS3 ILBR3 LBR3 TXESEL3	MINV - MAIS2 ILBR2 LBR2 TXESEL2	FINV - MAIS1 ILBR1 LBR1 TXESEL1	XAIS - DAIS4 LBA4 LBDR4 RXESEL4	XFERF - DAIS3 LBA3 LBDR3 RXESEL3	XREF LBCODE1 DAIS2 LBA2 LBDR2 RXESEL2	INTE LBCODE0 DAIS1 LBA1 LBDR1 RXESEL1	DS2 #7 MX12 Registers
AEH - FFH	-	-	-	-	-	-	-	-	-	Reserved
100H - 1FFH	-	-	-	-	-	-	-	-	-	Reserved

Note:

All Reserved Registers should not be read/written

REGISTER DESCRIPTIONS

MASTER RESET/CLOCK STATUS

Read/Write Addresses: 00H
Reset Value: 00H

7	6	5	4	3	2	1	0
DS3RCACT	DS3TCACT	DS2TCACT	0	0	0	0	RESET

Bit	Name	Description
7	DS3RCACT (DS3 Receive Clock Activity)	The DS3 Receive Clock Activity (DS3RCACT) bit indicates at least one LOW to HIGH transaction has occurred on the RCLK input since the last read of this register. The DS3RCACT bit is set to a logic 1 by a rising edge on the RCLK input and is cleared to a logic 0 by a read of this register.
6	DS3TCACT (DS3 Transmit Clock Activity)	The DS3 Transmit Clock Activity (DS3TCACT) bit indicates at least one LOW to HIGH transaction has occurred on the TD2CLK input since the last read of this register. The DS3TCACT bit is set to a logic 1 by a rising edge on the TICLK input and is cleared to a logic 0 by a read of this register.
5	DS2TCACT (DS2 Transmit Clock Activity)	The DS2 Transmit Clock Activity (DS2TCACT) bit indicates at least one LOW to HIGH transaction has occurred on the TICLK input since the last read of this register. The DS2TCACT bit is set to a logic 1 by a rising edge on the TD2CLK input and is cleared to a logic 0 by a read of this register. Note that if the TD2CLK signal is absent for a period of time (i.e., TD2CLK clock failure), the D3MX must be reset once the TD2CLK signal is restored.
4-1	Unused	Must be zero for normal operation.
0	RESET (Software Reset)	The RESET bit implements a software reset. If the RESET bit is a logic1, the entire D3MX is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the D3MX out of reset. Holding the D3MX in a reset clears the RESET bit, thus deasserting the software reset.

REVISION/GLOBAL PMON UPDATE

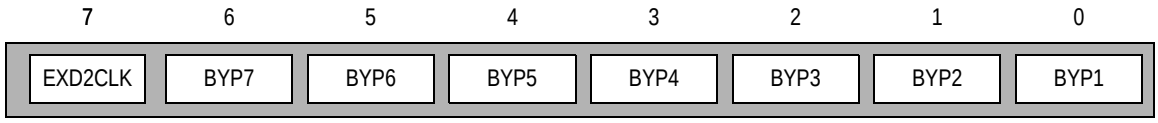
Read/Write Addresses: 01H
Reset Value: 00H

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bit	Name	Description
7-0	ID 7-0 (Identification Bits)	The version identification bits ID 7-0, are set to a fixed value representing the version number of the D3MX. These bits can be read by software to determine the version number. Writing to this register causes all performance monitor counters (DS3 and DS2/G.747) to be updated simultaneously.

MASTER BYPASS CONFIGURATION

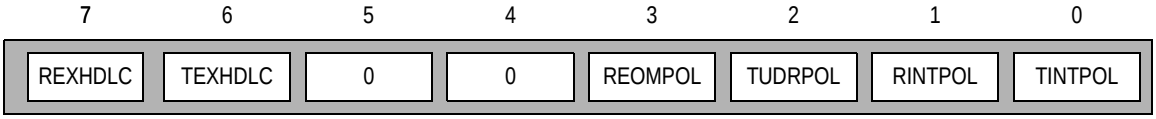
Read/Write Addresses: 02H
Reset Value: 00H



Bit	Name	Description
7	EXD2CLK (External DS2 CLK)	The EXD2CLK bit selects between an internally generated DS2 clock and the clock input on the TD2CLK pin. If EXD2CLK is a logic 0, the DS2 clock for the multiplexing side becomes the generated clock derived from the DS3 transmit TICLK clock. The generated DS2 clock is nominally 6.306272 MHz while in C-bit parity mode and while in M23 mode, it is nominally 6.311993 MHz. If EXD2CLK is a logic 1, the transmit DS2 clock becomes TD2CLK.
6-0	BYP 7-1 (M12 Bypass)	The BYP 7-1bits allow for each of the seven MX12blocks to be individually bypassed so that the external DS2 may be multiplexed and duplexed directly without the intermediate M12 multiplexing. If BYP[n] is a logic 1, the following applies: 1. A nominally 6.312 MHz clock is expected on TD1CLK(4n). 2. A data stream synchronous to TD1CLK(4n) is expected on TD1DAT(4n). 3. The clocks on TD1CLK(4n-1), TD1CLK(4n-2) and TD1CLK(4n-3) have no effect and should be tied to ground. 4. The data streams in TD1DAT(4n-1), TD1CLK(4n-2) and TD1CLK(4n-3) are ignored and should be tied to ground. 5. A nominally 6.312 MHz clock is presented on RD1CLK(4n). 6. A data stream synchronous to RD1CLK(4n) is presented on RD1DAT(4n). 7. The signals on RD1CLK(4n-1), RD1CLK(4n-2),RD1CLK(4n-3), RD1DAT(4n-1), RD1DAT(4n-2) and RD1DAT(4n-3) are always LOW.

MASTER HDLC CONFIGURATION

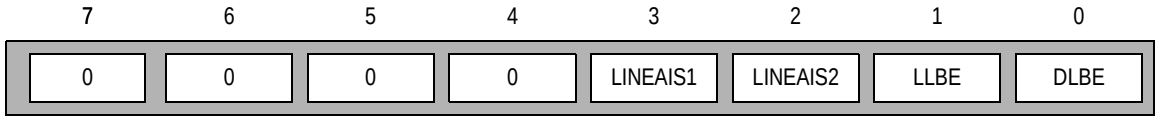
Read/Write Addresses: 03H
Reset Value: 40H



Bit	Name	Description
7	REXHDLC (Receive External HDLC)	The state of the receive external HDLC (REXHDLC) bit determines weather the C-bit parity path maintenance data link is terminated by the internal HDLC receiver or by an external HDLC receiver. When the REXHDLC bit is a logic 0, the internal HDLC receiver is selected; the RDLCLK/RDLINT pin is configured to output the interrupt signal (RDLINT) from the internal HDLC receiver and the RDLSIG/RDLEOM pin is configured to output the end-of-message signal (RDLEOM) from the internal HDLC receiver. When the REXHDLC bit is a logic 1, the use of an external HDLC receiver is selected; the RDLSIG/RDLEOM pin is configured to output the data stream (RDLSIG) and the RDLCLK/RDLINT pin is configured to output the data link clock signal (RDLCLK). The REXHDLC bit is cleared to logic 0 upon reset.
6	TEXHDLC (Transmit External HDLC)	The state of the transmit external HDLC (TEXHDLC) bit determines weather the C-bit parity path maintenance data link is sourced by the internal HDLC transmitter or by an external HDLC transmitter. When the TEXHDLC bit is a logic 0, the internal HDLC transmitter is selected; the TDLCLK/TDLINT pin is configured as an output to present the interrupt signal (TDLINT) from the internal HDLC transmitter and the TDLSIG/TDLUDR pin is configured to output the underrun signal (TDLUDR) from the internal HDLC transmitter. When the TEXHDLC bit is a logic 1, the use of an external HDLC transmitter is selected; the TDLSIG/TDLUDR pin is configured to output the data link data stream (TDLSIG) and the TDLCLK/TDLINT pin is configured to output the data link clock signal (TDLCLK). The TEXHDLC bit is set to logic 1 upon reset.
5-4	Unused	Must be zero for normal operation.
3	REOMPOL (Receive End-of-Message Polarity)	The Receive End-of-Message Polarity (REOMPOL) bit determines the assertion level of the RDLEOM output. If REOMPOL is a logic 0, the RDLEOM output is an active LOW open-drain output. If REOMPOL is a logic 1, the RDLEOM output is asserted HIGH and always has a strong drive. If the REXHDLC bit is a logic 1, this bit has no effect.
2	TUDRPOL (Transmit Underflow Polarity)	The Transmit Underflow Polarity (TUDRPOL) bit determines the assertion level of the TDLUDR output. If TUDRPOL is a logic 0, the TDLUDR output is an active LOW open-drain output. If TUDRPOL is a logic 1, the TDLUDR output is asserted HIGH and always has a strong drive. If the TEXHDLC bit is a logic 1, this bit has no effect.
1	RINTPOL (Receive Interrupt Polarity)	The Receive Interrupt Polarity (RINTPOL) bit determines the assertion level of the RDLINT output. If RINTPOL is a logic 0, the RDLINT output is an active LOW open-drain output. If RINTPOL is a logic 1, the RDLINT output is asserted HIGH and always has a strong drive. If the REXHDLC bit is a logic 1, this bit has no effect.
0	TINTPOL (Transmit Interrupt Polarity)	The Transmit Interrupt Polarity (TINTPOL) bit determines the assertion level of the TDLINT output. If TINTPOL is a logic 0, the TDLINT output is an active LOW open-drain output. If TINTPOL is a logic 1, the TDLINT output is asserted HIGH and always has a strong drive. If the TEXHDLC bit is a logic 1, this bit has no effect.

MASTER LOOPBACK CONFIGURATION

Read/Write Addresses: 04H
Reset Value: 00H



Bit	Name	Description
7-4	Unused	Must be zero for normal operation.
3-2	LINEAIS 1-2 (Line Alarm Indication Signal)	The line AIS (LINEAIS 1-0) bits allow the generation of various AIS patterns on the TDAT output when TUNI is set to logic 1, or on the TPOS and TNEG outputs when TUNI is set to logic0, independent of the data stream being transmitted. The LINEAIS 1-0 option is expected to be used when the diagnostic loopback is invoked, ensuring that only a valid DS3 stream enters the network. The LINEAIS 1-0 bits select one of the following AIS patterns for transmission: **LINEAIS 1-0** / **AIS Transmitted** 00 / none 01 / Framed, repetitive 1010... pattern with C-bits forced to logic 0 10 / Framed, repetitive 1111... pattern with C-bits forced to logic 0 11 / Unframed, all-ones pattern The LINEAIS 1-0=01 option is compatible with TR-TSY000009 Section 3.7 objectives.If the intention is to loopback the AIS, the AIS bit in the DS3 TRAN Configuration Register should be written instead.
1	LLBE (Diagnostic loopback Enable)	The diagnostic loopback enable (LLBE) bit allows the looping back of the received DS3 into the transmitted DS3 path. If the LLBE bit is a logic 1, the RPOS, RNEG, and RCLK signals are connected internally to replace the signals normally output on the TPOS, TNEG, and TCLK pins.
0	DLBE (Diagnostic Loopback Enable)	The diagnostic loopback enable (DLBE) bit allows the looping back of the transmitted DS3 into the receive DS3 path for diagnostic purposes. If the DLBE bit is a logic 1, the TPOS, TNEG, and TCLK signals are connected internally to replace the signals normally input on the RPOS, RNEG, and RCLK pins.

MASTER INTERFACE CONFIGURATION

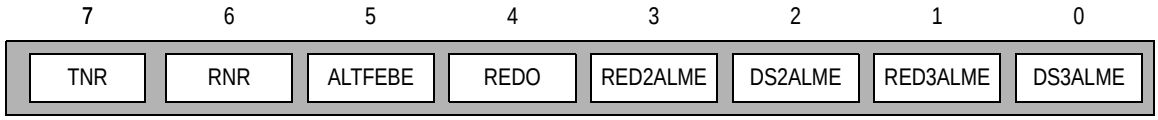
Read/Write Addresses: 05H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	TINV	TRISE	TUNI	RINV	RFALL

Bit	Name	Description
7-5	Unused	Must be zero for normal operation.
4	TINV (DS3 Transmit Edge Invert)	The transmit invert (TINV) bit enables data inversion of the DS3 transmit interface. When TINV is a logic 1, the TPOS and TNEG signals are active LOW. When TINV is a logic 0, the TPOS and TNEG signals are active HIGH. Inversion only takes place when the DS3 transmit interface is configured for dual rail operation.
3	TRISE (DS3 Transmit Edge Falling)	The transmit falling edge select (TRISE) bit configures the updating edge used on the DS3 transmit interface. When TRISE is a logic 1, the DS3 transmit interface is updated on the rising edge of TCLK. When TRISE is a logic 0, the DS3 transmit interface is updated on the falling edge of TCLK.
2	TUNI (DS3Transmit Unipolar)	The transmit unipolar (TUNI) bit configures the DS3 transmit interface for unipolar or dual rail operation. When TUNI is a logic 1, the DS3 transmit interface is configured as TDAT and TMFP. When TUNI is a logic 0, the DS3 transmit interface is configured as TPOS and TNEG.
1	RINV (DS3 Receive Edge Invert)	The receive invert (RINV) bit enables data inversion of the DS3 receive interface. When RINV is a logic 1, the RPOS and RNEG signals are active LOW. When RINV is a logic 0, the RPOS and RNEG signals are active HIGH. Inversion only takes place when the DS3 receive interface is configured for dual rail operation.
0	RFALL (DS3 Receive Edge Falling)	The receive falling edge select (RFALL) bit configures the sampling edge used on the DS3 receive interface. When RFALL is a logic 1, the DS3 receive interface is sampled on the falling edge of RCLK. When RFALL is a logic 0, the DS3 receive interface is sampled on the rising edge of RCLK.

MASTER ALARM ENABLE/NETWORK REQUIREMENT BIT

Read/Write Addresses: 06H
Reset Value: 80H



Bit	Name	Description
7	TNR (Transmit Network Requirement)	The Transmit Network Requirement (TNR) bit determines the value inserted into the Network Requirement (N_r) bit transmitted in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. A logic 1 in the TNR bit causes a one to be transmitted in the N_r overhead bit timeslot. The TNR bit is set to a logic 1 upon either a hardware or software reset. If C-bit parity is not selected, the TNR bit has no effect. Note that the serial control input, TOHEN, takes precedence over the effect of this bit when TOHEN is asserted during the Network Requirement Bit position. While TOHEN is asserted at the second C-bit position of M-subframe 1, the data on the TOH input is transmitted in the N_r, bit.
6	RNR (Receive Network Requirement)	The Receive Network Requirement (RNR) bit reflects the real time value of the Network Requirement (N_r) bit presented in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. The RNR bit is a logic 1 if a logic one occurs in the N_r overhead bit timeslot. If C-bit parity is not selected, the value of RNR is meaningless and random.
5	ALTFEBE (Alternate Far End Block Error)	The Alternate Far End Block Error (ALTFEBE) bit selects the error conditions detected to define a FEBE indication. If ALTFEBE is a logic 1, a FEBE indication is generated in the outgoing C-bit Parity DS3 transmit stream if a C-bit parity error occurred in the last received M-frame. If no C-bit Parity error occurred, no FEBE is generated. If ALTFEBE is a logic 0, a FEBE indication is generated if either one or more framing bit errors or a C-bit parity error has occurred in the last received M-frame. If no framing bit errors nor C-bit parity errors have occurred, then no FEBE is generated.
4	REDO (RED DS2 Alarm Output Enable)	The RED DS2 Alarm Output Enable (REDO) bit selects the type of signal output on the ROOF/RRED pin. If REDO is a logic 1, DS3 RED status signal is available on the ROOF/RRED output pin. If REDO is a logic O, DS3 OOF status signal is available on the ROOF/RRED output pin.
3	RED2ALME (RED DS2 Alarm Enable)	The RED DS2 Alarm Enable (RED2ALME) bit works in conjunction with the DS2ALME and enables detection of DS2 RED condition to be used in place of DS2/G.747 out-of-frame in the above criteria for demultiplexed AIS generation. When DS2ALME is set to logic 1 and RED2ALME is set to logic 1, the occurrence of OOF for 53 consecutive DS2/G.747 “M-frames” causes a DS2 RED alarm condition and generates the DS1 AIS. When DS2ALME is set to logic 1 and RED2ALME is set to 0, any occurrence of OOF generates the DS1 AIS. If DS3ALME is a logic 0, the RED3ALME bit is ignored.
2	DS2ALME (DS2 Alarm Enable)	The DS2 Alarm Enable (DS2ALME) bit allows the automatic generation of AIS in the DS1s demultiplexed from a DS2 or G.747 stream which is in an alarm condition. If DS2ALME is a logic 1, a DS2 or G.747 out-of-frame (OOF) condition (i.e. immediately after 2-of-n F-bit errors where n is 4 or 5, or 3-of-4 M-frames containing M-bit errors for DS2, or immediately after 4 consecutive framing word errors for G.747) or detection of DS2 or G.747 AIS causes each of the associated DS1s to be replaced by an unframed all ones pattern immediately. If DS2ALME is a logic 0, AIS can still be generated in the demultiplexed DS1s under software control by setting the bits in the appropriate MX12 AIS Insert Register. Note that the removal of the auto all-ones insertion is performed upon the first DS2 M-frame or G.747 frame pulse after the DS2 FRMR has found frame alignment.
1	RED3ALME (RED DS3 Alarm Enable)	The RED DS3 Alarm Enable (RED3ALME) bit works in conjunction with the DS3ALME and enables detection of DS3 RED alarm condition to be used in place of DS3 loss if signal and DS3 out-of-frame in the above criteria for demultiplexed AIS generation. When DS3ALME is set to logic 1 and RED3ALME is set to logic 1, the occurrence of LOS or OOF for 127 consecutive M-frames (or 21 consecutive M-frames, if FDET is set to logic 1 in the DS3 FRMR configuration register) causes a DS3 RED alarm condition and generates the DS2 AIS. When DS3ALME is set to logic 1 and RED3ALME is set to 0, any occurrence of LOS or OOF generates the DS2 AIS. If DS3ALME is a logic 0, the RED3ALME bit is ignored.
0	DS3ALME (DS3 Alarm Enable)	The DS3 Alarm Enable (DS3ALME) bit allows the automatic generation of AIS in all of the demultiplexed DS2s upon a DS3 alarm condition. If DS3ALME is a logic 1, a DS3 loss of signal (>175 zeros), a DS3 out-of-frame (OOF) condition (i.e. immediately after 3-of-n F-bit errors where n is 8 or 16, or 3-of-4 M-frames containing M-bit errors). DS3 idle code detection or DS3 AIS detection causes all of the DS2s to be replaced by an unframed all ones pattern immediately. Generation of AIS continues while the detected alarm condition persists. If DS3ALME is a logic 0, AIS can still be generated in the demultiplexed DS2s under software control by setting the bits in the MX23 Demux AIS Insert Register.

MASTER TEST

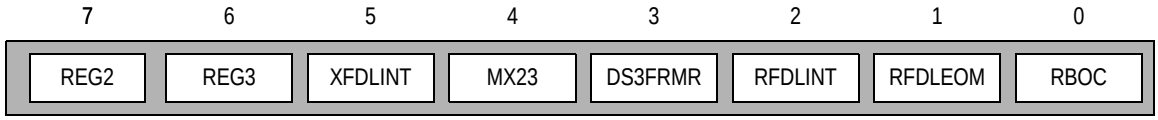
Read/Write Addresses: 07H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	DBCTRL	0	HIZDATA	HIZIO

Bit	Name	Description
7-4	Unused	Must be zero for normal operation.
3	DBCTRL (Data Bus Control)	The DBCTRL bit is used to pass control of the data bus to the $\overline{CS}$ pin. While the DBCTRL is set, holding the $\overline{CS}$ pin HIGH causes the D2MX to drive the data bus and holding the $\overline{CS}$ pin LOW tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.
2	Unused	Must be zero for normal operation.
1- 0	HIZDATA, HIZIO (Hi-Z Data) (Hi-Z I/O)	The HIZDATA and HIZIO bits control the tri-state modes of the D3MX. While the HIZIO bit is a logic 1, all output pins of the D3MX. While the HIZIO bit is a logic 1, all output pins of the D3MX except the data bus are held in a HIGH-impedance state. The microprocessor interface is sill active. While the HIZDATA bit is a logic 1, the data bus is also held in a HIGH-impedance state which inhibits microprocessor read cycles.

MASTER INTERRUPT SOURCE #1

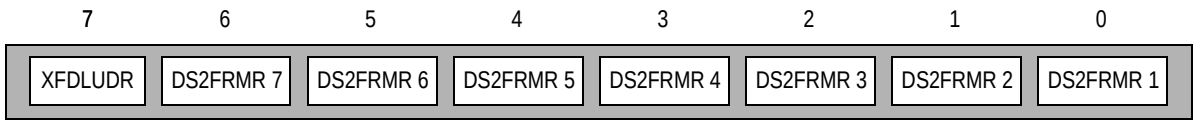
Read/Write Addresses: 08H
Reset Value: 00H



Bit	Name	Description
7	REG2 (Red Alarm 2)	If REG2 bit is a logic 1, at least one bit in the Master Interrupt Source #2 Register is set, that is, at least one DS2 Farmer or the XFDL is generating an interrupt.
6	REG3 (Red Alarm 3)	If REG3 bit is a logic 1, at least one bit in the Master Interrupt Source #3 Register is set, that is, at least one M12 Multiplexer is generating an interrupt.
5	XFDLINT (Transmit Facility Data Link Interrupt)	If XFDLINT bit is a logic 1, the XDFL TSB is generating an interrupt (also visible on the TDLINT output when configured for internal HDLC, i.e. TEXHDLC=0)
4	MX23 (MX23 TX Interrupt)	If MX23 bit is a logic 1, the MX23 FRMR TSB is generating an interrupt due to the detection of a DS2 loopback request.
3	DS3FRMR (D3 Framer Interrupt)	If DS3FRMR bit is a logic 1, the DS3 FRMR TSB is generating an interrupt. Register 36H should be read to determine which event in DS3 FRMR has caused to interrupt.
2	RFDLINT (Receive Facility Data Link Interrupt)	If RFDLINT bit is a logic 1, the RFDL TSB is generating an interrupt (also visible on the RFDLINT output when configured for internal HDLC, i.e. REXHDLC=0).
1	RFDLEOM (Receive Facility Data Link End of Message Interrupt)	If RFDLEOM bit is a logic 1, the RFDL TSB is generating an interrupt due to an end of message occurrence (also visible on the RDLEOM output when configured for internal HDLC, i.e. REXHDLC=0).
0	RBOC (Receive Bit Oriented Code Interrupt)	If RBOC bit is a logic 1, the FEAC RBOC TSB is generating an interrupt. Register 33H should be read to determine which event in RBOC has caused to interrupt.

MASTER INTERRUPT SOURCE #2

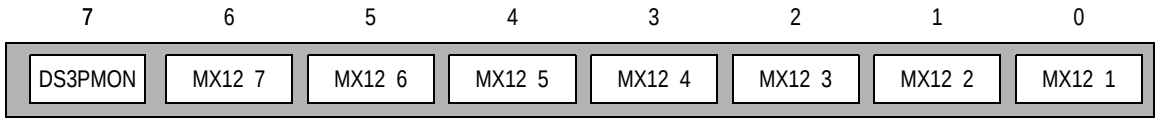
Read/Write Addresses: 09H
Reset Value: 00H



Bit	Name	Description
7	XFDLUDR (Transmit Facility Data Link Underrun Interrupt)	This bit allows software to determine whether the XFDL TSB produced an underrun condition. If the XFDLUDR bit is a logic 1, the XFDL TSB is generating an interrupt due to an underrun of the transmit data buffer (also visible on the TDLUDR output when configured for internal HDC, i.e. TEXHDLC=0). Reading this register does not remove the interrupt indication; the corresponding TSB's interrupt status register must be read to remove the interrupt indication.
6-0	DS2FRMR 7-1 (DS2 Framer Interrupt)	These bits allow software to determine which of the seven DS2 framer TSBs produced the interrupt on the INTB output pin. Reading this register does not remove the interrupt indication; the corresponding TSB's interrupt status register must be read to remove the interrupt indication.

MASTER INTERRUPT SOURCE #3

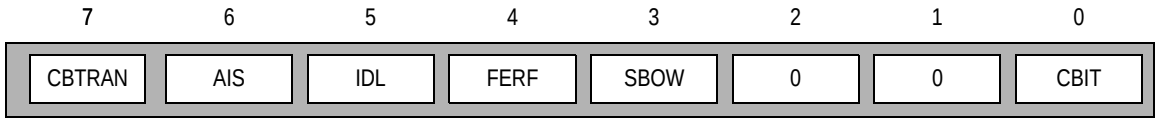
Read/Write Addresses: 0AH
Reset Value: 00H



Bit	Name	Description
7	DS3PMON (DS3 Performance Monitor Interrupt)	DS3 PMON TSB produced the interrupt on the INTB output pin.
6-0	M12 7-1 (M12 Performance Monitor Interrupt)	These bits correspond to which M12 TSB produced an interrupt. Reading this register does not remove the interrupt indication; the corresponding TSB's interrupt status register must be read to remove the interrupt indication.

DS3 TRANSMIT CONFIGURATION

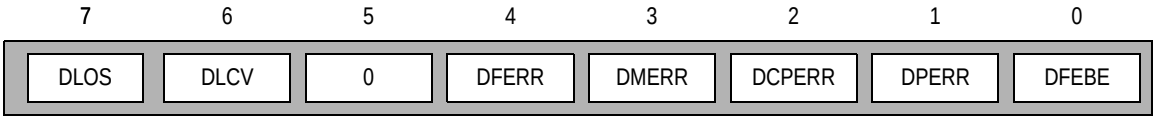
Read/Write Addresses: 0CH
Reset Value: 00H



Bit	Name	Description
7	CBTRAN (DS3 C-Bit Transmit Configuration)	The CBTRAN bit controls the C-bits during AIS transmission. When CBTRAN is a logic 0, the C-bits are overwritten with zeros during AIS transmission (as is currently specified in ANSI T1.107a Section 8.1.3.1). The only exception is the network requirement bit, which is forced to the TNR register value. When CBTRAN is a logic 1 and the M23 application is enabled the C-bits pass through transparently during AIS transmission. When CBTRAN is a logic 1, and the C-bit parity application is enabled, the C-bits are overwritten with the appropriate C-bit parity functions during AIS transmission.
6	AIS (DS3Alarm Indication Signal Configuration)	The AIS bit enables transmission of the alarm indication signal. When AIS is a logic 1, the transmit DS3 payload (on the TDAT/TPOS and TNEG outputs) is overwritten with the pattern 1010...
5	IDL (DS3 Idle Pattern Configuration)	The IDL bit enables transmission of the alarm indication signal and the idle signal. When IDL is a logic 1, the transmit DS3 payload is overwritten with the pattern 1100...
4	FERF (DS3 Far End Receive Failure Configuration)	The FERF bit enables transmission of far end receive failure in the outgoing DS3 stream. When FERF is a logic 1, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 0. When FERF is a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.
3	SBOW (DS3 Stuff Bit Opportunity Window Configuration)	The SBOW bit selects weather to insert the bit from the TOH input into the stuff opportunity bit or into the F4 bit. When SBOW is a logic 1, the bit from the TOH input is inserted into the stuff opportunity bit. When SBOW is a logic 0, the bit from the TOH input is inserted into the F4 bit.
2-1	Unused	Must be zero for normal operation.
0	CBIT (DS3 C-Bit parity Configuration)	The CBIT bit enables the C-bit parity application. When CBIT is a logic 1, C-bit parity is enabled, and the associated functions are inserted in the C-bit positions of the incoming DS3 stream. When CBIT is a logic 0, the M23 application is selected, and the C-bits are passed transparently through the DS3 TRAN.

DS3 TRANSMIT DIAGNOSTIC

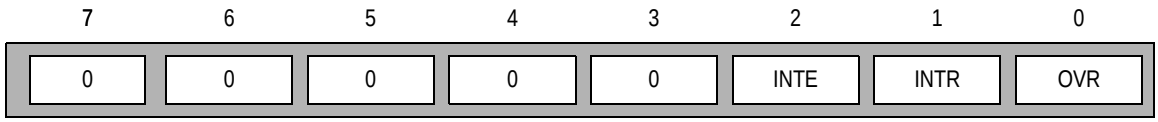
Read/Write Addresses: 0DH
Reset Value: 00H



Bit	Name	Description
7	DLOS (DS3 Loss of Signal)	The DLOS controls the insertion of loss of signal in the outgoing DS3 stream. When DLOS is set to a logic 1, the data on outputs TPOS, TNEG, and TDAT are forced to continuous zeros.
6	DLCV (DS3 Line Code Violation)	The DLCV controls the insertion of a single line code violation in the outgoing DS3 stream. When DLCV is set to a logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example line code violations may not be inserted when transmitting AIS, but will be inserted when transmitting the idle signal. This bit is automatically cleared upon insertion of the line code violation.
5	Unused	Must be zero for normal operation.
4	DFERR (DS3 F-Bit Errors)	The DFERR controls the insertion of framing errors (F-bit errors) in the outgoing DS3 stream. When DFERR is set to a logic 1, and the F-bits are inverted before insertion in the DS3 stream.
3	DMERR (DS3 M-Bit Errors)	The DMERR controls the insertion of framing errors (M-bit errors) in the outgoing DS3 stream. When DMERR is set to a logic 1, and the M-bits are inverted before insertion in the DS3 stream.
2	DCPERR (DS3 C-Bit Parity Errors)	The DCPERR controls the insertion of C-bit parity errors in the outgoing DS3 stream. When DCPERR is set to a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion in the DS3 stream.
1	DPERR (DS3 P-Bit Errors)	The DPERR controls the insertion of parity errors (P-bit errors) in the outgoing DS3 stream. When DPERR is set to a logic 1, and the P-bits are inverted before insertion in the DS3 stream.
0	DFEBE (DS3 Far End Block Errors)	The DFEBE controls the insertion of far end block errors in the outgoing DS3 stream. When DFEBE is set to a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0.

DS3 PMON INTERRUPT ENABLE/STATUS

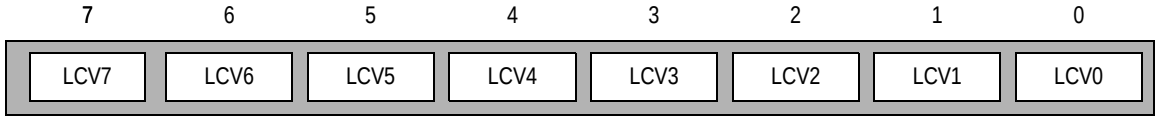
Read/Write Addresses: 11H
Reset Value: 00H



Bit	Name	Description
7-3	Unused	Must be zero for normal operation.
2	INTE (DS3 Performance Monitor Interrupt Enable)	A logic 1 in the INTE bit position enables the DS3 PMON to generate a microprocessor interrupt and assert the INTB output when the counter values are transferred to the holding registers. A logic 0 in the INTE bit position disables the DS3 PMON from generating an interrupt. When the TSB is reset, the INTE bit is set to logic 0, disabling the interrupt. The interrupt is cleared when this register is read.
1	INTR (DS3 Interrupt)	The interrupt (INTR) bit indicates the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit.
0	OVR (DS3 Overrun)	The overrun (OVR) bit indicates the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

DS3 LCV COUNT LSB

Read/Write Addresses: 14H
Reset Value: 00H



Bit	Name	Description
7-0	LCV 7-0 (DS3 Line Code Violation)	These bits indicate the number of DS3 Line Code Violation (LCV) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either LCV Count Register.

DS3 LCV COUNT MSB

Read/Write Addresses: 15H
Reset Value: 00H

7	6	5	4	3	2	1	0
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8

Bit	Name	Description
7-0	LCV 15-8 (DS3 Line Code Violation)	These bits indicate the number of DS3 Line Code Violation (LCV) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either LCV Count Register.

DS3 FERR COUNT LSB

Read/Write Addresses: 16H
Reset Value: 00H

7	6	5	4	3	2	1	0
FERR7	FERR6	FERR5	FERR4	FERR3	FERR2	FERR1	FERR0

Bit	Name	Description
7-0	FERR 7-0 (DS3 Far End Receive Error)	These bits indicate the number of DS3 framing error (FERR) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FERR Count Register.

DS3 FERR COUNT MSB

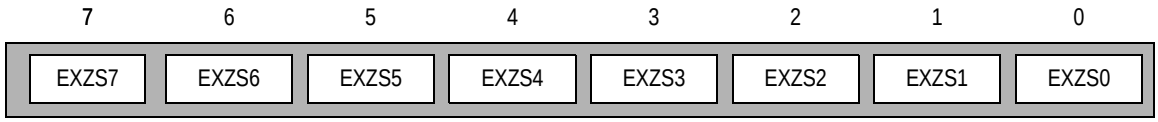
Read/Write Addresses: 17H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FERR9	FERR8

Bit	Name	Description
7-2	Unused	Must be zero for normal operation.
1-0	FERR 9-8 (DS3 Far End Receive Error)	These bits indicate the number of DS3 framing error (FERR) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FERR Count Register.

DS3 EXZS COUNT LSB

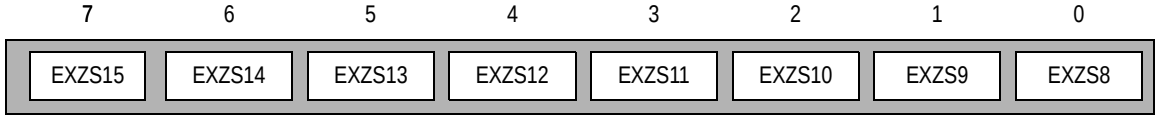
Read/Write Addresses: 18H
Reset Value: 00H



Bit	Name	Description
7-0	EXZS 7-0 (DS3 Excessive Zero Suppression)	These registers indicate the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit block is counted as one summed excessive zero. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FERR Count Register.

DS3 EXZS COUNT MSB

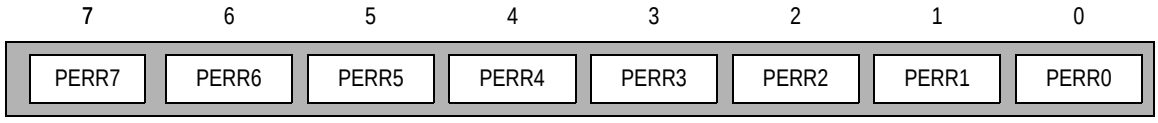
Read/Write Addresses: 19H
Reset Value: 00H



Bit	Name	Description
7-0	EXZS 7-0 (DS3 Excessive Zero Suppression)	These registers indicate the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit block is counted as one summed excessive zero. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FERR Count Register.

DS3 PERR COUNT LSB

Read/Write Addresses: 1AH
Reset Value: 00H



Bit	Name	Description
7-0	PERR 7-0 (DS3 Parity Error)	These bits indicate the number of P-bit parity error (PERR) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either EXZS Count Register or writing to the Global PMON Update Register 0x01.

DS3 PERR COUNT MSB

Read/Write Addresses: 1BH
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	PERR13	PERR12	PERR11	PERR10	PERR9	PERR8

Bit	Name	Description
7-0	PERR 13-8 (DS3 Parity Error)	These bits indicate the number of P-bit parity error (PERR) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either EXZS Count Register.

DS3 CPERR COUNT LSB

Read/Write Addresses: 1CH
Reset Value: 00H

7	6	5	4	3	2	1	0
CPERR7	CPERR6	CPERR5	CPERR4	CPERR3	CPERR2	CPERR1	CPERR0

Bit	Name	Description
7-0	CPERR 7-0 (DS3 C-Bit Parity Error)	These bits indicate the number of C-bit parity error (CPERR) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either CPERR Count Register.

DS3 CPERR COUNT MSB

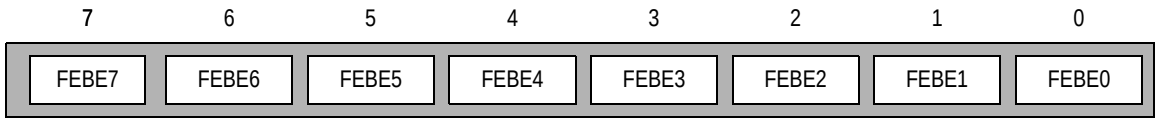
Read/Write Addresses: 1DH
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	CPERR13	CPERR12	CPERR11	CPERR10	CPERR9	CPERR8

Bit	Name	Description
7-6	Unused	Must be zero for normal operation.
5-0	CPERR 13-8 (DS3 C-Bit Parity Error)	These bits indicate the number of C-bit parity error (CPERR) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either CPERR Count Register.

DS3 FEBE COUNT LSB

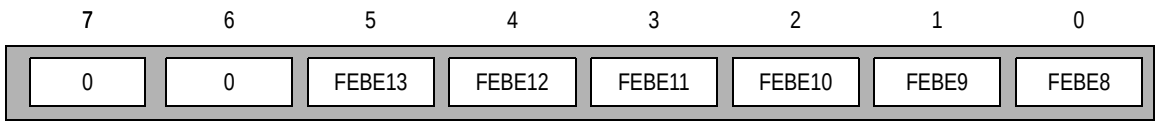
Read/Write Addresses: 1EH
Reset Value: 00H



Bit	Name	Description
7-0	FEBE 7-0 (DS3 Far End Bit Error)	These bits indicate the number of far end block error (FEBE) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FEBE Count Register.

DS3 FEBE COUNT MSB

Read/Write Addresses: 1FH
Reset Value: 00H



Bit	Name	Description
7-0	FEBE 13-8 (DS3 Far End Bit Error)	These bits indicate the number of far end block error (FEBE) events that occurred during the previous accumulation interval. A transfer operation of all counter registers within the selected PMON can be triggered by writing to either FEBE Count Register.

XFDL TSB CONFIGURATION

Read/Write Addresses: 20H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	EOM	INTE	ABT	CRC	EN

Bit	Name	Description
7-5	Unused	Must be zero for normal operation.
4	EOM (XFDL End of Message)	The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins. The EOM register bit value can be set to logic 1 by pulsing the TDLEMOI input pin.
3	INTE (XFDL Interrupt Enable)	The INTE bit enables the generation of an interrupt via the TDLINT output. Setting the INTE bit to logic 1 enables the generation of an interrupt by asserting the TDLINT output; setting INTE to logic 0 disables the generation of an interrupt.
2	ABT (XFDL Abort Code)	The Abort (ABT) controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the Transmit Data Register. Aborts are continuously sent until this bit is reset to logic 0.
1	CRC (XFDL Cyclical Redundancy Check)	The CRC enable bit controls the generation of the CCITT-CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial = $x^{16}+x^{12}+x^5+1$. The HIGH order bit of the FCS word is transmitted first.
0	EN (XFDL Enable)	The enable bit (EN) controls the overall operation of the XFDL TSB. When the EN bit is set to a logic 1, the XDFL TSB is enabled and flag sequences are sent until data is written into the Transmit Data Register. When the EN bit is set to logic 0, the XFDL TBS is disabled.

XFDL TSB INTERRUPT STATUS

Read/Write Addresses: 21H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	INT	UDR

Bit	Name	Description
7-2	Unused	Must be zero for normal operation.
1	INT (XFDL Interrupt)	The INT bit indicates when the XFDL TSB is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register.
0	UDR (XFDL Underrun)	The UDR bit indicates when the XFDL TSB has underrun the data in the Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the Transmit Data register has completed before the new byte was written into the Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in the register.

XFDL TSB TRANSMIT DATA

Read/Write Addresses: 22H
Reset Value: 00H

7	6	5	4	3	2	1	0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Bit	Name	Description
7-0	TD 7-0 (XFDL Transmit Data Byte)	Data written to this register is serialized and transmitted on the path maintenance data lint least significant bit first. The XFDL TSB signals when the next data byte is required by asserting the TDLINT output (if enabled) and by setting the INT bit in the Status register high. When INT and/or TDLINT is set, the Transmit Data register must be written with the next message byte within 4 data bit periods to prevent the occurrence of an underrun. At a nominal 28.2 kbit/sec link data rate the required write interval is 110μsec.

RFDL TSB CONFIGURATION

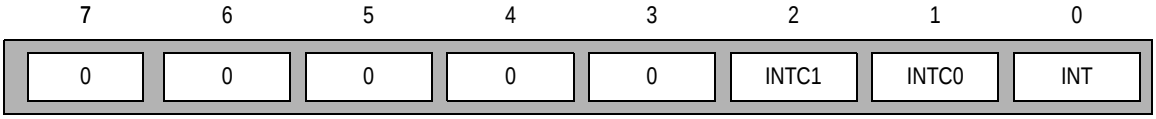
Read/Write Addresses:24H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TR	EN

Bit	Name	Description
7-2	Unused	Must be zero for normal operation.
1	TR (RDFL Terminate Reception)	Setting the terminate reception bit (TR) forces the RFDL TSB to immediately terminate the reception of the current LAPD frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration register will reset itself after a rising and falling edge have occurred on the CLK input to the RFDL TSB once the write to this register has completed and WEB goes inactive. If the Configuration register is read after this time, the TR value returned will be zero. The RFDL TSB handles the TR input in the same manner as clearing and setting the EN bit, therefore, the RFDL state machine will begin searching for flags and an interrupt will be generated when the first flag is detected.
0	EN (RFDL Enable)	The enable bit (EN) controls the overall operation of the RFDL TSB. When set, the RDFL TSB is enabled; When reset, the RDFL TSB is disabled. When the TSB is disabled, the FIFO and interrupts are all cleared, however, the programming of the Interrupt Control/Status Register is not affected. When the TSB is enabled, it will immediately begin looking for flags.

RFDL TSB INTERRUPT CONTROL/STATUS

Read/Write Addresses: 25H
Reset Value: 00H



Bit	Name	Description
7-3	Unused	Must be zero for normal operation.
2, 1	INTC1, INTC0 (RDFL Interrupt Control Bits)	The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:
0	INT (RDFL Interrupt Status)	The INT bit reflects the Status of the external RDLINT interrupt unless the INTC1 and INTC0 bits are set to disable interrupts, In that case, the RDLINT output is forced to 0 and the INT bit of the Interrupt Control/Status register will reflect the state of the internal interrupt latch.

INTC1	INTC0	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

RFDL TSB STATUS

Read/Write Addresses:26H
Reset Value: 00H

7	6	5	4	3	2	1	0
FE	OVR	FLG	EOM	CRC	NVB2	NVB1	NVB0

Bit	Name	Description
7	FE (RDFL FIFO Empty)	The FIFO Empty bit (FE) is HIGH when the last FIFO entry is read and goes LOW when the FIFO is loaded with new data.
6	OVR (RDFL Overrun)	The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status register is read. While OVR is HIGH, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.
5	FLG (RDFL Flag)	The flag bit (FLG) is set if the RFDL TSB has detected the presence of the LAPD flag sequence (01111110) in the data. FLG is reset only when the LAPD abort sequence (01111111) is detected in the data or when the RFDL TSB is disabled. This bit is passed through the FIFO with the Data so that the status will correspond to the Data just read from the FIFO. The reception of bit oriented codes over the data link will also force an abort due to its eight ones pattern.
4	EOM (RFDL End of Message)	The End of Message bit (EOM) follows the RDLEOM output. It is set when: 1. The last byte in the LAPD frame (EOM) is being read from the Receive Data Register. 2. An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO, 3. Immediately on detection of FIFO overrun. The EOM bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO.
3	CRC (RFDL Cyclical Redundancy Check)	The CRC bit is set if a CRC error was detected in the last received LAPD frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.
2-0	NVB 2-0 (RFDL Number of Valid Bits)	The NVB 2-0 bit positions indicate the number of valid bits in the Receive Data Register byte. It is possible that not all of the bits in the Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB 2-0 value of 000 binary indicates that only the MSB in the register is valid. NVB 2-0 is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0.

RFDL TSB RECIVE DATA

Read/Write Addresses: 27H
Reset Value: 00H

7	6	5	4	3	2	1	0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Bit	Name	Description
7-0	RD 7-0 (RFDL Receive Byte)	RD0 corresponds to the first bit of the serial byte received by the RFDL.

MX23 CONFIGURATION

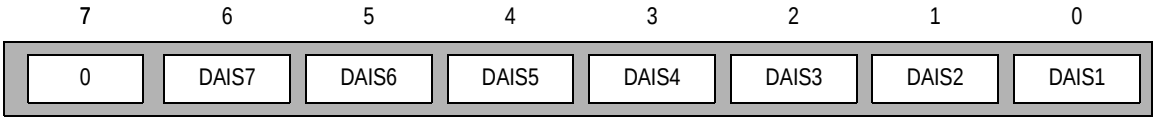
Read/Write Addresses: 28H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	LBCODE1	LBCODE0	CBE	INTE

Bit	Name	Description
7-4	Unused	Must be zero for normal operation.
3-2	LBCODE 1-0 (Loopback Code)	The LBCODE 1-0 bits select the valid state for a loopback request coded in the C-bits of the DS3 signals. Transmit and receive are not independent; the same code is expected in the receive DS3 as is inserted in the transmitted DS3. The following table gives the correspondence between LBCODE 1-0 bits and the valid codes: **LBCODE1:0]** / **Loopback Code** 00 / C1 = C2 and C1 = $\overline{C3}$ 01 / C1 = C3 and C1 = $\overline{C2}$ 10 / C2 = C3 and C1 = $\overline{C2}$ 11 / C1 = C2 and C1 = $\overline{C3}$ If LDCODE 1-0 is 'b00 or 'b11, the loopback code is as per ANSI T1.107a Section 8.2.1 and TR-TDY-000009 Section 3.7. Because TR-TSY 000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported The LBCODE 1-0 bits become logical 0 upon either a hardware or software reset.
1	CBE (C-Bit Parity Enable)	When set HIGH, the CBE bit enables C-bit parity operation. When CBE is LOW, M23 operation is enabled. While in C-bit parity mode, loopback request insertion are disabled. The generated DS2 clock, GD2CLK, is nominally 6.3062723 MHz while in C-bit parity mode, received C bits are ignored, and transmitted C bits are set to 1. While in M23 mode, the generated DS2 clock, GD2CLK, is nominally 6.311993 MHz and C bit decoding and encoding is fully operational.
0	INTE (M23 Interrupt Enable)	When set HIGH, the INTE bit enables the MX23 to activate the interrupt output, INTB, whenever any of the LBRI 7-1 bits are set HIGH in the MX23 Loopback Request Interrupt register. MX23 interrupts are masked when INTE is cleared LOW.

DEMUX AIS INSERT REGISTER

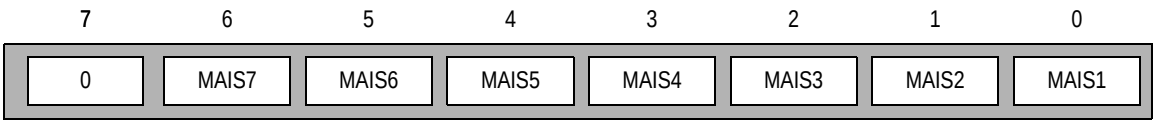
Read/Write Addresses: 2AH
Reset Value: 00H



Bit	Name	Description
7	Unused	Must be zero for normal operation.
6-0	DAIS 7-1 (Demux Alarm Indication Signal)	Setting any of the DAIS7-1 bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream demultiplexed from the DS3 signal input on RDAT. Demux AIS Insertion takes place after the point where per DS2 loopback may be invoked using the Loopback Activate register thus allowing demux AIS to be inserted into the through path while a DS2 loopback is activated, if desired.

MX23 MUX AIS INSERT REGISTER

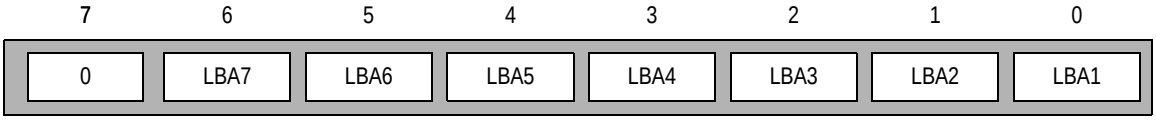
Read/Write Addresses: 2AH
Reset Value: 00H



Bit	Name	Description
7	Unused	Must be zero for normal operation.
6-0	MAIS 7-1 (Multiplexed Alarm Indication Signal)	Setting any of the MAIS 7-1 bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream multiplexed into the DS3 signal output on TDAT. Mux AIS Insertion takes place before the point where per DS2 loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a DS2 loopback is activated.

MX23 LOOPBACK ACTIVATE REGISTER

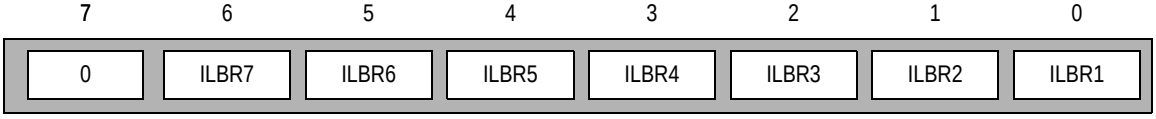
Read/Write Addresses: 2BH
Reset Value: 00H



Bit	Name	Description
7	Unused	Must be zero for normal operation.
6-0	LBA 7-1 (DS2 Loopback)	Setting any of the LBA 7-1 bits activates loopback of the corresponding DS2 stream from the input DS3 signal to the output DS3 signal. The demultiplexed DS2 signals continue to present valid payloads while loopbacks are activated. The MX23 Demux AIS Insert Register allows insertion of DS2 AIS if required.

MX23 LOOPBACK REQUEST INSERT REGISTER

Read/Write Addresses: 2CH
Reset Value: 00H



Bit	Name	Description
7	Unused	Must be zero for normal operation.
6-0	ILBR 7-1 (MX23 Insertion Loopback Request)	Setting any of the ILBR 7-1 bits enables the insertion of a loopback request in corresponding DS2 stream in the output DS3 signal. The format of the loopback request is determined by the LBCODE 1-0 bits in the MX23 Configuration Register.

MX23 LOOPBACK REQUEST DETECT REGISTER

Read/Write Addresses: 2DH
Reset Value: 00H

7	6	5	4	3	2	1	0
0	LBRD7	LBRD6	LBRD5	LBRD4	LBRD3	LBRD2	LBRD1

Bit	Name	Description
7	Unused	Must be zero for normal operation.
6-0	LBRD 7-1 (MX23 Loopback Request Detector)	The LBRD 7-1 bits are set HIGH while a loopback request is detected for the corresponding DS2 stream in the input DS3 signal. The LBRD 7-1 bits are set LOW otherwise. The format of the loopback request expected is determined by the LBCODE 1-0 bits in the MX23 Configuration Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has be absent for five successive M-frames.

MX23 LOOPBACK REQUEST INTERRUPT REGISTER

Read/Write Addresses: 2EH
Reset Value: 00H

7	6	5	4	3	2	1	0
0	LBRI7	LBRI6	LBRI5	LBRI4	LBRI3	LBRI2	LBRI1

Bit	Name	Description
7	Unused	Must be zero for normal operation.
6-0	LBRI 7-1 (MX23 Loopback Request Interrupt)	The LBRI 7-1 bits are set HIGH while a loopback request is asserted or deasserted for the corresponding DS2 stream in the input DS3 signal. The LBRI 7-1 bits are set HIGH whenever the corresponding LBRI 7-1 bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB is activated. The LBRI 7-1 bits are to logic 0 immediately following a read of the register, acknowledging the interrupt and deactivating the INTB output.

FEAC XBOC TSB CODE

Read/Write Addresses: 31H
Reset Value: 3FH

7	6	5	4	3	2	1	0
0	0	BC5	BC4	BC3	BC2	BC1	BC0

Bit	Name	Description
7-6	Unused	Must be zero for normal operation.
5-0	BC 5-0	This register enables the XBOC TSB to generate a bit oriented code and selects the 6-bit code to be transmitted. When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the far-end alarm and control (FEAC) channel with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0. When the register is written with 111111, the XBOC TSB is disabled.

RBOC CONFIGURATION/INTERRUPT ENABLE

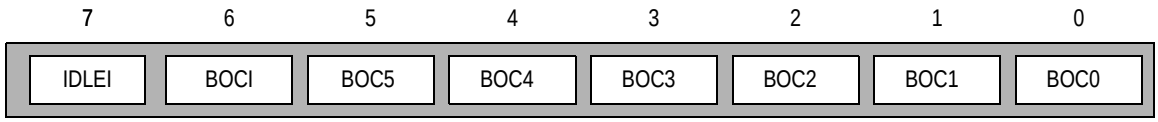
Read/Write Addresses: 32H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	IDLE	AVC	BOCE

Bit	Name	Description
7-3	Unused	Must be zero for normal operation.
2	IDLE (Idle)	The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.
1	AVC (Alternative Validation Criterion)	The AVC bit position selects the validation criterion used in determining a valid BOC. A logic 0 selects the 8 out of 10 matching BOC criterion; a logic 1 in the AVC bit position selects the “alternative” validation criterion of 4 out of 5 matching BOCs.
0	BOCE (Bit Oriented Code Enable)	The BOCE bit position enables or disables the generation of an interrupt when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation. When the D3MX is reset, BOCE is reset to logic 0; therefore, interrupt generation is disabled.

RBOC INTERRUPT STATUS

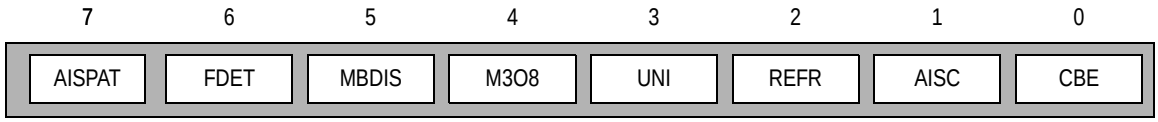
Read/Write Addresses: 33H
Reset Value: 00H



Bit	Name	Description
7	IDLEI (Idle Interrupt)	The IDLEI bit indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.
6	BOCI (Bit Oriented Code Interrupt)	Indicates a logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. Since the bit-oriented code “111111” is not recognized by the RBOC, the BOC 5-0 bits are set to all ones (“111111”) if no valid code has been detected. The BOCI bit position is cleared to logic 0 and the interrupt is deasserted when this register is read.
5-0	BOC 5-0 (Bit Oriented Code)	The bit positions BOC 5-0 contain the received bit-oriented codes. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. Since the bit-oriented code “111111” is not recognized by the RBOC, the BOC 5-0 bits are set to all ones (“111111”) if no valid code has been detected. The BOCI bit position is cleared to logic 0 and the interrupt is deasserted when this register is read.

DS3 FRMR CONFIGURATION

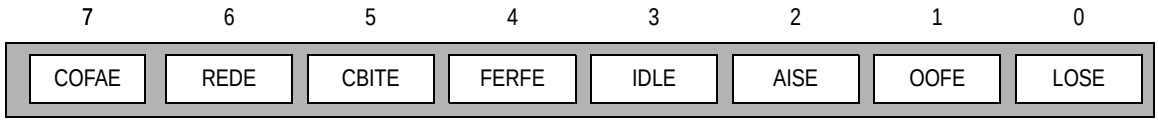
Read/Write Addresses: 34H
Reset Value: 80H



Bit	Name	Description
7	AISPAT (DS3 Alarm Indication Pattern)	The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010...is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).
6	FDET (DS3 Fast Detection)	The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.
5	MBDIS (DS3 M-Bit Error Disable)	The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.
4	M3O8 (DS3 M-Bit 3 out of 8 Framing Error)	The M3O8 bit configures the out of frame decision criteria. If M3O8 is a logic 1, out of frame is declared if at least 3 of 8 framing bits are in error. If M3O8 is a logic 0, the standard 3 of 16 bits in error criteria is used.
3	UNI (DS3 Unipolar Select)	The UNI bit is used to configure the FRMR to accept either unipolar or bipolar data streams. When a logic 1 is written to UNI, the FRMR accepts unipolar data and line code violation indication on its inputs. When a logic 0 is written to UNI, the FRMR accepts bipolar data on its inputs and performs B3ZS decoding and line code violation reporting.
2	REFR (DS3 Re-Framing)	The REFR bit is used to trigger reframing. If a logic 1 is written to REFR when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a LOW to HIGH transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transitions
1	AISC (DS3 Alarm IndicationSignal Configuration)	The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).
0	CBE (DS3 C-Bit Parity Enable)	The CBE bit selects whether the C-bit parity application is enabled. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written, C-bit parity mode is disabled.

DS3 FRMR INTERRUPT ENABLE (ACE=0)

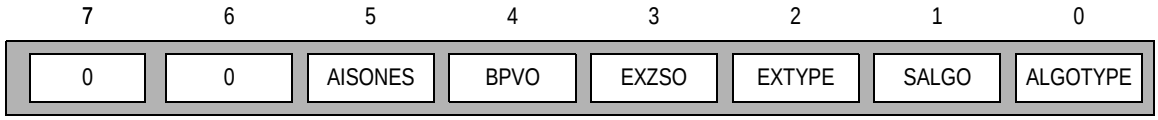
Read/Write Addresses: 35H
Reset Value: 00H



Bit	Name	Description
7	COFAE (DS3 Change of Frame Alignment Enable)	The COFAE bit enables an interrupt to be generated when a change of frame alignment (i.e. a COFA event) occurs. When COFAE is set to logic 1, the interrupt output, INTB, is set LOW when the COFA event occurs.
6	REDE (DS3 RED Alarm Enable)	The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location in the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register (register 06Hex) is set to logic 1. When REDE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the RED indication changes.
5	CBITE (DS3 C-Bit Identification Enable)	The CBITE bit enables an interrupt to be generated when a change of state in the C-bit Identification indication internal to the DS3 FRMR occurs. When CBITE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the C-bit Identification indication changes.
4	FERFE (DS3 Far End Receive Failure Enable)	The FERFE bit enables an interrupt to be generated when a change of state of the FERF indication occurs. The FERF indication is visible in the FERFV bit location in the DS3 FRMR Status register and on the RFERF pin. When FERFE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the FERF output changes.
3	IDLE (DS3 Idle Enable)	The IDLE bit enables an interrupt to be generated when a change of state of the DS3 AIS signal detector occurs. When IDLE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the IDLE detector changes.
2	AISE (DS3 Alarm Indication Signal Enable)	The AISE bit enables an interrupt to be generated when a change of state of the DS3 AIS signal detector occurs. The state of the AIS detector is visible in the AISV bit location in the DS3 FRMR Status register and on the RAIS pin. When AISE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the AIS detector changes.
1	OOFE (DS3 Out of Frame Enable)	The OOFE bit enables an interrupt to be generated when a change of state of the DS3 FRMR frame alignment acquisition circuitry occurs. The state of the frame alignment acquisition circuitry occurs. The state of the frame alignment acquisition circuitry is visible in the OOFV bit location in the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register is logic 0. When the circuitry has lost frame aliment and is searching for the new alignment, and out frame is indicated and the OOFV bit and ROOF pin are set to logic 1. When the circuitry has found frame alignment, the OOFV bit and ROOF pin are set to logic 0. When OOFE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the OOF indication changes.
0	LOSE (DS3 Loss of Signal Enable)	The LOSE bit enables an interrupt to be generated when a change of state of the loss of signal detector occurs. The state of the detector is visible in the LOSV bit position in the DS3 FRMR Status register and on the RLOS pin. When LOSE is set to logic 1, the interrupt output, INTB, is set LOW when the state of the LOS indication changes.

DS3 FRMR ADDITIONAL CONFIGURATION REGISTER (ACE=1)

Read/Write Addresses: 35H
Reset Value: 00H

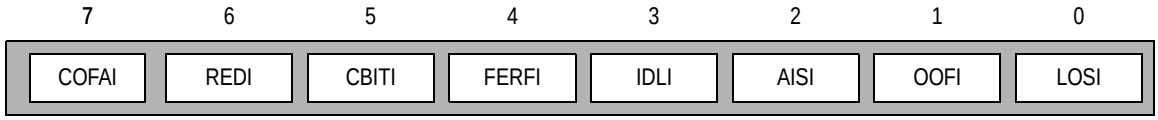


Bit	Name	Description
7-6	Unused	Must be zero for normal operation.
5	AISONES (DS3 Alarm Indication Signal)	The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register (34H) are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:
4	BPVO (DS3 Bipolar Violations)	The BPVO bit enables only bipolar violations to indicate line code violates and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.
3	EXZSO (DS3 Excessive Zero Occurrences)	The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zero occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.
2	EXTYPE (DS3 Excessive Zero Type)	The EXTYPE bit determines the type of zero occurrences to be included in the LCV indication. When EXTYPE is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV.When EXTYPE is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXTYPE=1 only a single LCV would be indicated for this string of excessive zeros; with EXTYPE=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).
1	SALGO (DS3 Signature Algorithm)	The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.
0	ALGOTYPE (DS3 Algorithm Type)	The ALGOTYPE bit determines the criteria used to decode a valid B3ZS signature. When the ALGOTYPE is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the ALGOTYPE bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010... pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010... pattern and C-bits all logic 0.
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

DS3 FRMR INTERRUPT STATUS

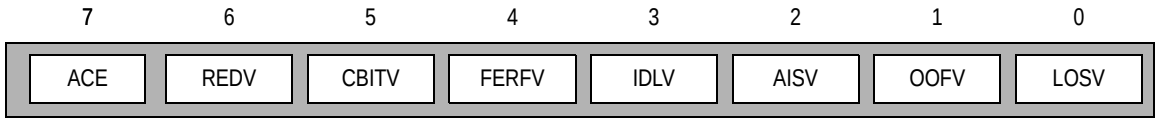
Read/Write Addresses: 36H
Reset Value: 00H



Bit	Name	Description
7	COFAI (DS3 Change of Frame Alignment Indication)	The COFAI bit indicates that a change of frame alignment (i.e. a COFA event) signal detector has occurred. When the COFAI bit is a logic 1, the frame alignment acquisition circuitry has detected that the new alignment differs from the previous frame alignment. When the COFAI bit is logic 0, there was no difference from the current frame alignment and the previous frame alignment.
6	REDI (DS3 RED Indication)	The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register (register 06Hex) is set to logic 1. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.
5	CBITI (DS3 C-Bit Identification)	The CBITI bit indicates that a change of state in the C-bit identification indication internal to the DS3 FRMR has occurred. When the CBITI bit is a logic 1, a change in the internal CBIT state has occurred. When the CBITI bit is logic 0, no change in the CBIT state has occurred.
4	FERFI (DS3 FERF Indication)	The FERFI bit indicates that a change of state of the FERF indication has occurred. The FERF indication is visible in the FERFV bit location of the DS3 FRMR Status register and on the RFERF pin. When the FERFI bit is a logic 1, a change in the FERF state has occurred. When the FERFI bit is logic 0, no change in the FERF state has occurred.
3	IDLI (DS3 IDLE Signal Detector)	The IDLI bit indicates that a change of state of the DS3 IDLE signal detector has occurred. When the IDLI bit is a logic 1, a change in the IDLE detector state has occurred. When the IDLI bit is logic 0, no change in the IDLE signal detector state has occurred.
2	AISI (DS3 AIS Signal Detector)	The AISI bit indicates that a change of state of the DS3 AIS signal detector has occurred. The state of the AIS detector is visible in the AISV bit location in the DS3 FRMR Status register and on the RAIS pin. When the AISI bit is a logic 1, a change in the AIS detector state has occurred. When the AISI bit is logic 0, no change in the AIS detector state has occurred.
1	OOFI (DS3 FRMR Status)	The OOFI bit indicates that a change of state of the DS3 FRMR Status frame alignment acquisition circuitry has occurred. The state of the frame alignment acquisition circuitry is visible in the OOFV bit location in the DS3 FRMR Status register and on the ROOF/RRED pin when the REDO bit in the Master Alarm Enable register is logic 0. When the circuitry has lost frame alignment and is searching for the new alignment, an out frame is indicated and the OOFV bit and ROOF pin are set to logic 1. When the circuitry has found frame alignment, the OOFI bit and ROOF pin are set to logic 0. When the OOFV bit is a logic 1, a change in the OOF state has occurred. When the OOFV bit is logic 0, no change in the OOF state has occurred.
0	LOSI (DS3 Loss of Signal)	The LOSI bit indicates that a change of state of loss of signal detector has occurred. The state of the detector is visible in the LOSV bit position in the DS3 FRMR Status register and on the RLOS pin. When the LOSI bit is a logic 1, a change in the LOS state has occurred. When the LOSI bit is logic 0, no change in the LOS state has occurred.

DS3 FRMR STATUS

Read/Write Addresses: 37H
Reset Value: 00H



Bit	Name	Description
7	ACE (DS3 Additional Configuration Enable)	The ACE bit selects the Additional Configuration Register. This register is located at address 35H, and is only accessible when the ACE bit is to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address 35H.
6	REDV (DS3 Red Alarm Violation)	The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OODFV=0) for 2.23ms (or 13.4ms if FDET=0)
5	CBITV (DS3 C-Bit Violation)	The CBITV bit indicates the current state in the C-bit Identification indication. When the CBITV bit is a logic 1, the first C-bit or M sub-frame 1 has been observed to be logic 1 for 63 consecutive occasions. When the CBITV bit is logic, the first C-bit of sub-frame 1 has either not been logic 1 for 63 consecutive occasions or, if CBITV was previously logic 1, the first C-bit of sub-frame 1 has been observed to be logic 0 for 2 or more times within 15 consecutive occasions.
4	FERFV (DS3 Far End Enable Error Violation)	The FERFV bit indicates the current state of the FERF indication. When the FERFV bit is a logic 1, the FRMR detects that the second to last M-frame's X2=X1=0. When the FERFV bit is logic 0, the second to last M-frame's X2=X1=1.
3	IDLV (DS3 Idle Violation)	The IDLV bit indicates the current state of the DS3 IDLE signal detector. When the IDLV bit is a logic 1, the DS3 IDLE pattern has been received for 2.23ms (or for 13.5ms when FDET is logic 0). When the IDLV bit is logic 0, the DS3 IDLE pattern has not been received for either 2.23ms or 13.5ms.
2	AISV (DS3 Alarm Indication Violation)	The AISV bit indicates the current state of the DS3 AIS signal detector. When the AISV bit is a logic 1, the DS3 AIS pattern has been received for 2.23ms (or for 13.5ms when FDET is logic 0). When the AISV bit is logic 0, the DS3 AIS pattern has not been received for either 2.23ms or 13.5ms.
1	OOFV (DS3 Out of Frame Violation)	The OOFV bit indicates the current state of the DS23 FRMR frame alignment acquisition circuitry. When the circuitry has lost frame alignment and is searching for the new alignment, an out of frame is indicated and the OOFV bit is set to logic 1. When the circuitry has found frame alignment, the OOFV bit is set to logic 0.
0	LOSV (DS3 Los of Signal Violation)	The LOSV bit indicates the current state of the loss of signal detector. When the LOSV bit is a logic 1, a sequence of 175 consecutive zeros was detected on the dual-rail RPOS and RNEG DS3 inputs. When the LOSV bit is logic 0, a valid DS3 signal with a ones' density greater than 33% for 175 ± 1 bit periods was detected on the dual-rail inputs.

DS2 FRMR CONFIGURATION

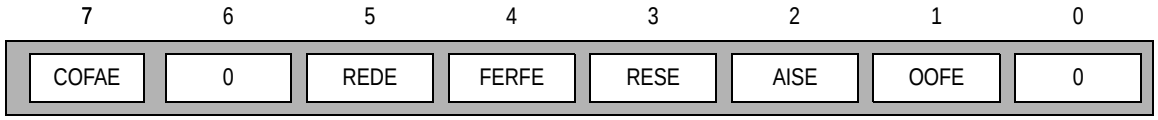
Read/Write Addresses: 40H, 50H, 60H, 70H, 80H, 90H, A0H
Reset Value: 00H

7	6	5	4	3	2	1	0
G747	0	WORD	M2O5	MDBIS	REF	0	0

Bit	Name	Description
7	G747 (DS2 G.747 Enable)	The G747 bit configures the FRMR for G.747 operation. If the G747 bit is a logic 1, the FRMR will process a G.747 signal. If the G747 bit is a logic 0, the FRMR will process a DS2 signal as defined in ANSTI T1.107 Section 7.
6	Unused	Must be zero for normal operation.
5	WORD (DS2 Frame Alignment Signal Errors Method)	The WORD bit determines the method of accumulating G.747 framing errors. If the WORD bit is a logic 0, each frame alignment signal (FAS) bit error results in a single FERR count. If the WORD bit is a logic 1, one or more bit errors in a FAS word result in a single FERR count.
4	M2O5 (DS2 M-bit 2 out of 5)	The M2O5 bit selects the error ratio for declaring out-of-frame (OOF) when in DS2 mode only. When a 1 is written to M2O5, the framer declares OOF when 2 F-bit errors out of 5 consecutive F-bits are observed. When a 0 is written, the framer declares OOF when 2 F-bit errors out of 4 consecutive F-bits are observed. (These two ratios are recommended in T-TSY000009 Section 4.1.2). When the FRMR is configured for G.747 operation (the G747 bit is set to logic 1), the OOF status is declared when 4 consecutive framing word errors occur (as per CCITT Rec. G747 Section 4), regardless of the M2O5 bit setting.
3	MBDIS (DS2 M-bit Error Disable)	The MBDIS bit disables the declaration of out-of-frame upon excessive M-bit errors. If MBDIS is a logic 0, out-of-frame is declared when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. If MBDIS is a logic 1, the state of the M-bits is ignored once in frame. Regardless of the state of the MBDIS bit, the F-bits are always monitored for invalid framing.
2	REF (DS2 Reframing Mode)	The REF bit is used to trigger reframing. If a logic 1 is written to REF when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a LOW-to-HIGH transition of the REF bit triggers reframing; multiple write operations are required to ensure such a transition.
1-0	Unused	Must be zero for normal operation.

DS2 FRMR INTERRUPT ENABLE

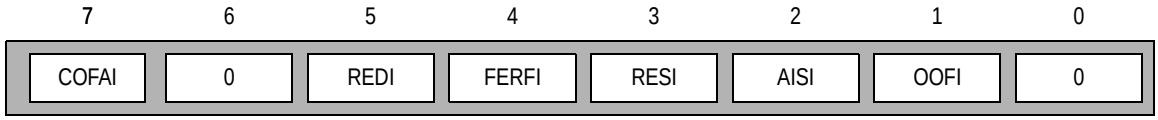
Read/Write Addresses: 41H, 51H, 61H, 71H, 81H, 91H, A1H
Reset Value: 00H



Bit	Name	Description
7	COFAE (DS2 Change of Frame Alignment Enable)	The COFAE bit is an interrupt enable. A change of frame alignment (COFA) event causes the interrupt output to be set HIGH when the COFAE bit is written with a logic 1.
6	Unused	Must be zero for normal operation.
5	REDE (DS2 Red Alarm Enable)	The REDE bit is a interrupt enable. A change of state on a corresponding DS2 FRMR status causes the interrupt output INTB, to be asserted low when the corresponding interrupt enable bit is written with a logic 1.
4	FERFE (DS2 Far End Receive Error Enable)	The FERFE bit is a interrupt enable. A change of state on a corresponding DS2 FRMR status causes the interrupt output INTB, to be asserted low when the corresponding interrupt enable bit is written with a logic 1.
3	RESE (Reserved Bit Enable)	The RESE bit is an interrupt enable. A change in the debounced value of the reserved bit in Set II when in G.747 mode causes the interrupt output to be set HIGH when the RESE bit is written with a logic 1. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. The RESE bit has no effect in DS2 mode The interrupt output, INTBm is deasserted when the Interrupt Status Register is read if its assertion was a result an OOF, AIS, FERF, RED, RES, or COFA event.
2	AISE (DS2 Alarm Indication Signal Interrupt Enable)	The AISE bit is a interrupt enable. A change of state on a corresponding DS2 FRMR status causes the interrupt output INTB, to be asserted low when the corresponding interrupt enable bit is written with a logic 1.
1	OOFE (DS2 Out of Frame Interrupt Enable)	The OOFE bit is a interrupt enable. A change of state on a corresponding DS2 FRMR status causes the interrupt output INTB, to be asserted low when the corresponding interrupt enable bit is written with a logic 1.
0	Unused	Must be zero for normal operation.

DS2 FRAMER INTERRUPT STATUS

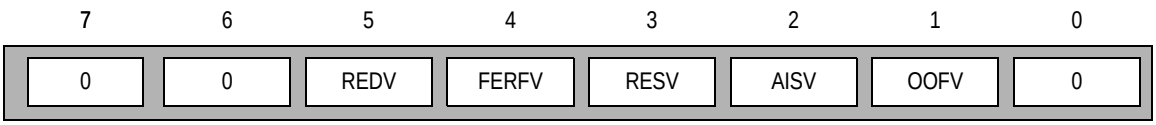
Read/Write Addresses: 42H, 52H, 62H, 72H, 82H, 92H, A2H
Reset Value: 00H



Bit	Name	Description
7	COFAI (DS2 Change of Frame Alignment Indication)	The COFAI bit is an interrupt status indicator. As per TR-TSY-000820, the Change of Frame Alignment (COFA) interrupt is only asserted if a frame search results in a frame alignment which is different from the prior frame alignment.
6	Unused	Must be zero for normal operation.
5	REDI (DS2 Red Alarm Interrupt Indication)	The REDI bit is a interrupt status indicator. A change of state on the corresponding DS2 FRMR status causes the corresponding interrupt status bit to be set to logic 1.
4	FERFI (DS2 Far End Receive Frame Interrupt Indication)	The FERFI bit is a interrupt status indicator. A change of state on the corresponding DS2 FRMR status causes the corresponding interrupt status bit to be set to logic 1.
3	RESI (DS2 Reserved Bit Indication)	The RESI bit is an interrupt status indicator. A change in the debounced value of the reserved bit in Set II when in G.747 mode causes this bit to be set to logic 1. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames, This bit has no effect in DS2 mode.
2	AISI (DS2 Alarm Indication Signal Interrupt Indication)	The AISI bit is a interrupt status indicator. A change of state on the corresponding DS2 FRMR status causes the corresponding interrupt status bit to be set to logic 1.
1	OOFI (DS2 Out of Frame Violation Interrupt Indication.	The OOFI bit is a interrupt status indicator. A change of state on the corresponding DS2 FRMR status causes the corresponding interrupt status bit to be set to logic 1.
0	Unused	Must be zero for normal operation.

DS2 FRAMER STATUS

Read/Write Addresses: 43H, 53H, 63H, 73H, 83H, 93H, A3H
Reset Value: 00H



Bit	Name	Description
7-6	Unused	Must be zero for normal operation.
5	REDV (DS2 Red Alarm Violation)	The REDV bit is a logic 1 if an out-of-frame condition has persisted for 9.9ms (6.9ms in G.747 mode). This is less than 1.5 times the maximum average reframe time allowed. The REDV status will remain asserted for 9.9ms (6.6ms in G.747 mode) after frame alignment has been declare and then become logic 0.
4	FERFV (DS2 Far End Receive Frame Violation)	The FERFV bit in this register reflects the status of the corresponding DS2 FRMR value. In DS2 mode, the FERFV bit reflects the debounced state of the X bit (first bit of the M4-Subframe). If the X-bit has been a ZERO for two consecutive M-frames, the FERFV bit becomes a logic 1. If the X-bit has been a one for two consecutive M-frames, the FERFV bit becomes a logic 0. In G.747 mode, FERFV bit reflects the debounced state of the Remote Alarm Indication (RAI, bit 1 of Set II) bit. If the RAI bit has been a one for two consecutive frames, the FERFV bit becomes logic 1. If the RAI bit has been a zero for two consecutive frames, the FERFV bit becomes a logic 0. A six frame latency of the FERFV status ensures a virtually 100% probability of freezing correctly in DS2 mode upon an out-of-frame condition and a better than 99.9% probability of freezing correctly in G.747 mode.
3	RESV (DS2 Reserved Bit Violation)	The RESV bit reflects the debounced state of the reserved bit in Set II when in G.747 mode. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames.
2	AISV (DS2 Alarm Indication Signal Violation)	The AISV bit in this register reflects the status of the corresponding DS2 FRMR value. The AISV bit is a logic 1 if AIS has been declared.
1	OOFV (DS2 Out of Frame Violation)	The OOFV bit in this register reflects the status of the corresponding DS2 FRMR value. The OOFV bit is a logic 1 if the DS2 framer is presently out-of-frame.
0	Unused	Must be zero for normal operation.

DS2 FRAMER MONITOR INTERRRUP ENABLE/STATUS

Read/Write Addresses: 44H, 54H, 64H, 74H, 84H, 94H, A4H
Reset Value 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	INTE	INTR	OVR

Bit	Name	Description
7-3	Unused	Must be zero for normal operation.
2	INTE (DS2 Interrupt Enable)	The interrupt enable (INTE) bit allows the DS2 FRMR to assert the INTB output upon register transfers. A logic 1 in the INTE bit position enables the DS2 to generate a microprocessor interrupt when the counter values are transferred to a Holding Registers. A logic 0 in the INTE bit position disables the DS2 FRMR from generating an interrupt. When the TSB is reset, the INTE bit is set to logic 0, disabling the interrupt. The interrupt is cleared when this register is read if its assertion was a result a transfer operation.
1	INTR (DS2 Interrupt)	The interrupt (INTR) bit indicated the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the Holding Registers has occurred; a logic 0 indicates that no transfer has occurred. This bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit.
0	OVR (DS2 Overrun)	The overrun (OVR) bit indicates the overrun status of the Holding Registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the Holding Registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read. To generate a transfer of the counters to the holding registers, a microprocessor write to the Global PMON Update Register is required.

DS2 FRMR FERR COUNT

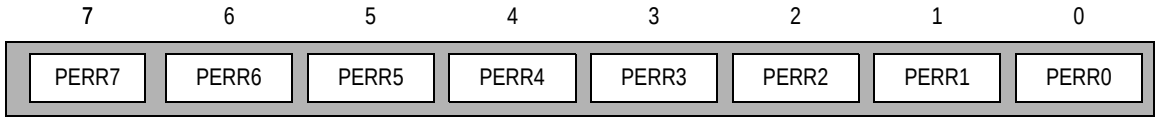
Read/Write Addresses: 45H, 55H, 65H, 75H, 85H, 95H, A5H
Reset Value: 00H

7	6	5	4	3	2	1	0
FERR7	FERR6	FERR5	FERR4	FERR3	FERR2	FERR1	FERR0

Bit	Name	Description
7-0	FERR7-0 (DS2 Framing Bit Error)	This register indicates the number of DS2 framing bit error events or G.747 framing word errors that occurred during the previous accumulation interval. A DS2 framing bit error event is either an M-bit or and F-bit error. One or more bit errors in a G.747 frame alignment signal results in a single framing word error. A transfer operation can be triggered by writing to the Global PMON Update Register.

DS2 FRMR PERR COUNT (LSB)

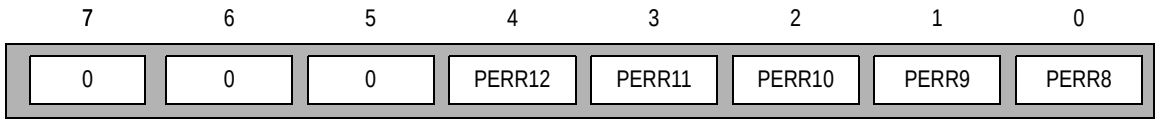
Read/Write Addresses: 46H, 56H, 66H, 76H, 86H, 96H, A6H
Reset Value: 00H



Bit	Name	Description
7-0	PERR 7-0 (DS2 Parity Bit Error)	These registers indicate the number of G.747 parity events that occurred during the pervious accumulation interval. A transfer operation can be triggered by writing to the Global PMON Update Register

DS2 FRMR PERR COUNT (MSB)

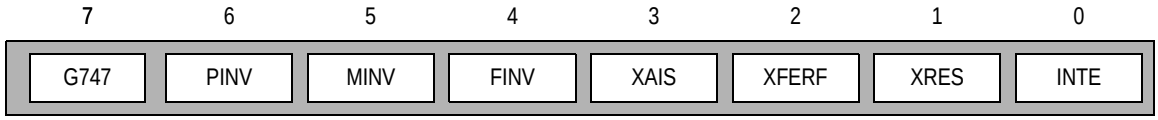
Read/Write Addresses: 47H, 57H, 67H, 77H, 87H, 97H, A7H
Reset Value: 00H



Bit	Name	Description
7-5	Unused	Must be zero for normal operation.
4-0	PERR 12-8 (DS2 Parity Bit Error)	These registers indicate the number of G.747 parity events that occurred during the pervious accumulation interval. A transfer operation can be triggered by writing to the Global PMON Update Register

MX12 CONFIGURATION AND CONTROL

Read/Write Addresses: 48H, 58H, 68H, 78H, 88H, 98H, A8H
Reset Value: 00H



Bit	Name	Description
7	G747 (G747 Configuration)	When G747 is HIGH, the MX12 supports CCITT Recommendation G.747. In this mode, three 2048b/bits tributaries are multiplexed into and demultiplex out of a 840 bit frame. If G747 is LOW, the frame is compatible with DS2 as specified in the ANSI T1.107 Standard.
6	PINV (G747 Parity Inversion)	When PINV is set HIGH, the transmitted parity bit in the G.747 formatted output stream is inverted for diagnostic purposes. This only has effect when the G747 bit is HIGH.
5	MINV (G747 M-Bit Inversion)	When MINV is set HIGH, the transmitted M bits in the DS2 output stream are inverted for diagnostic purposes. This only has effect when the G747 bit is LOW.
4	FINV (G747 F-Bit Inversion)	When FINV is set HIGH and G747 is LOW, all the transmitted F bits in the DS2 output stream are logically inverted for diagnostic purposes. If G.747 is HIGH when FINV is set HIGH, the nine bit frame alignment signal (111010000) is logically inverted (i.e. 000101111).
3	XAIS (Transmit AIS)	When set HIGH, the XAIS bit enables the transmission of the alarm indication signal (AIS) in the 6312kbit/s output stream. When XAIS is set HIGH, the transmitted data is set to all ones; otherwise the transmitted data is not affected.
2	XFERF (Transmit Far End Receive Failure)	When set HIGH, the XFERF bit enables the transmission of the far end receive failure (FERF0 signal in the DS2 output stream when in DS2 mode (i.e.G747 bit LOW). When XFERF is set HIGH, the transmitted X bit is set to 0, provided that AIS is not being transmitted; otherwise the transmitted X bit is set to 1. When in G.747 mode (i.e. G747 bit HIGH), the remote alarm indication (RAI) is set to 1 when XFERF is set HIGH; otherwise, the transmitted RAI bit is set to 0 unless AIS is being transmitted.
1	XRES (Transmit Reserved Bit)	The XRES bit only has effect in G.747 mode. When XRES is set HIGH and AIS is not being transmitted, the reserved bit (Set II, bit 3) is set to 0; otherwise, the transmitted reserved bit is set to 1.
0	INTE (Loopback Requirement Interrupt Enable)	When set HIGH, the INTE bit enables the activation of the interrupt output, INTB, whenever any of the LBRI 4-1 bits are set HIGH in the Loopback Request Interrupt register. Interrupts are masked when INTE is cleared LOW.

MX12 LOOPBACK CODE SELECT REGISTER

Read/Write Addresses: 49H, 59H, 69H, 79H, 89H, 99H, A9H
Reset Value: 00H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LBCODE1	LBCODE0

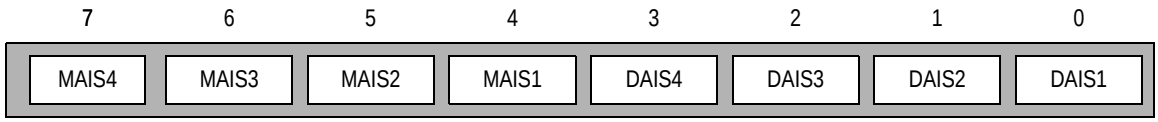
Bit	Name	Description
7-2	Unused	Must be zero for normal operation.
1-0	LBCODE1-0 (Loopback Code)	The LBCODE 1-0 bits select the valid state for a loopback request coded in the C-bits of the DS2 signals. Transmit and receive are not independent; the same code is expected in the demultiplexed DS2 as is inserted in the DS2 to be multiplexed. The following table gives the correspondence between LBCODE 1-0 bits and the valid codes:

LBCODE 1-0	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C1 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE 1-0 is ‘b00 or ‘b11, the loopback code is as per ANSI T1.107 Section 7.2.1.1 and TR-TSY-000009 Section 3.7. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. The LBCODE 1-0 bits will also select the valid state for a loopback request coded in the C-bits of the G.747 formatted signal. Again, the transmit and receive are not independents; the same code is expected in the demultiplexed G.747 stream as is inserted in the G.747 stream to be multiplexed. The valid codes are the same as those for the DS2 formatted stream given in the table above. The LBCODE 1-0 bits become logical 0 upon either a hardware or software reset.

MX12 AIS INSERT REGISTER

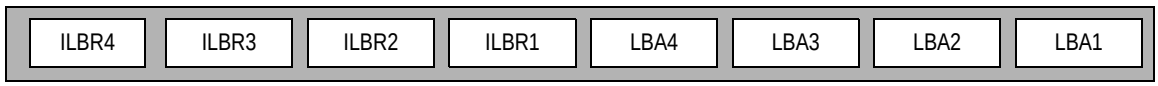
Read/Write Addresses: 4AH, 5AH, 6AH, 7AH, 8AH, 9AH, AAH
Reset Value: 00H



Bit	Name	Description
7-4	MAIS4-1 (M12 MUX Alarm Indication Signal)	Setting any of the MAIS [4:1] bits activate insertion of the alarm indication signal (all ones) into the corresponding LOW speed stream multiplexed into the 6312kbits HIGH speed output signal. Mux AIS insertions takes place before the point where remote loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a loopback is activated.
3-0	DAIS4-1 (M12 DeMux Alarm Indication Signal)	Setting any of the DAIS 4-1 bits activates insertion of the alarm indication signal (all ones) into the corresponding LOW speed stream demultiplexed from the 6312kbits HIGH speed input signal. Demux AIS insertion takes place after the point where remote loopback may be invoked using the Loopback Activate register thus demux AIS to be inserted into the through path while a loopback is activated, if desired.

MX12 LOOPBACK ACTIVATE REGISTER

Read/Write Addresses: 4BH, 5BH, 6BH, 7BH, 8BH, 9BH, ABH
Reset Value: 00H



Bit	Name	Description
7-4	ILBR 4-1 (Insertion Loopback Request)	In DS2 mode, setting any of the ILBR 4-1 bits enable the insertion of a loopback request in the corresponding DS1 stream in the DS2 output signal. The format of the loopback request is determined by the LBCODE 1-0 bits in the Loopback Code Select MX12 Register. In G.747 mode, ILBR[j] inverts bit Cj1, Cj2, or Cj3 in the G.747 frame in an analogous fashion.
3-0	LBA 4-1 (Loopback Activation)	Setting any of the LBA 4-1 bits activates loopback of the corresponding LOW speed stream from the HIGH speed input signal to the HIGH speed output signal. LBA4 has no effect in G.747 mode, but LBA 3-1 activates the loopback of the corresponding 2048kbits signals. The demultiplexed DS1 signals continue to present valid payloads while loopbacks are activated. The MX12 AIS Insert Register allows insertion of DS1 AIS if required.

MX12 LOOPBACK INTERRUPT REGISTER

Read/Write Addresses: 4CH, 5CH, 6CH, 7CH, 8CH, 9CH, ACH
Reset Value: 00H

7	6	5	4	3	2	1	0
LBRI4	LBRI3	LBRI2	LBRI1	LBRD4	LBDR3	LBDR2	LBDR1

Bit	Name	Description
7-4	LBRI4-1 (Loopback Request Interrupt)	The LBR 4-1 bits are set HIGH when a loopback request is asserted or deasserted for the corresponding LOW speed stream in the HIGH speed input signal. The LBR 4-1 bits are set HIGH whenever the corresponding LBRD 4-1 bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB is activated. The LBRI 4-1 bits are cleared LOW immediately following a read of the register, acknowledging the interrupt and deactivating the INTB output.
3-0	LBRD4-1 (Loopback Request Detached)	The LBRD 4-1 bits are set HIGH while a loopback request is detected for the corresponding LOW speed stream in the HIGH speed input signal. The LBRD 4-1 bits are set LOW otherwise. The format of the loopback request expected is determined by the LBCODE 1-0 bits in the MX12 Loopback Code Select Register. As per TR-TSY000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS1 TRANSMIT AND RECEIVE EDGE SELECT

Read/Write Addresses: 4DH, 5DH, 6DH, 7DH, 8DH, 9DH, ADH
Reset Value: 00H

7	6	5	4	3	2	1	0
TXESEL4	TXESEL3	TXESEL2	TXESEL1	RXESEL4	RXESEL3	RXESEL2	RXESEL1

Bit	Name	Description
7-4	TXESEL4-0 (DS1 Transmit Edge Select)	Transmit Edge Select when 0 the DS1 data will be transmitted on the rising edge of TD1CLK. When 1 the DS1 data will be transmitted on the falling edge of TD1CLK.
3-0	RXESEL4-0 (DS1 Receive Edge Select)	Receive Edge Select when 1 the DS1 data will be sampled on the rising edge of RD1CLK. When 0 the DS1 data will be sampled on the falling edge of RD1CLK.

1.1 DS3 Framer

The nominal DS3 interface is 44.736 Mb/s ± 20ppm (± 895 b/s).

A DS3 M-frame (Multiframe) is composed of seven DS3 M-subframes. Each M-subframe contains eight blocks of 84 payload bits (bit-interleaved from the seven DS2 or 28 DS1 streams) plus one overhead bit (the seven subframes do not represent each separate DS2 signals).

The DS3 frame contains a total of 4,760 bits of which there are 4,704 payload bits and 56 overhead bits. The total period of a DS3 frame is 106.4µs (44.736E-6 x 4,760).

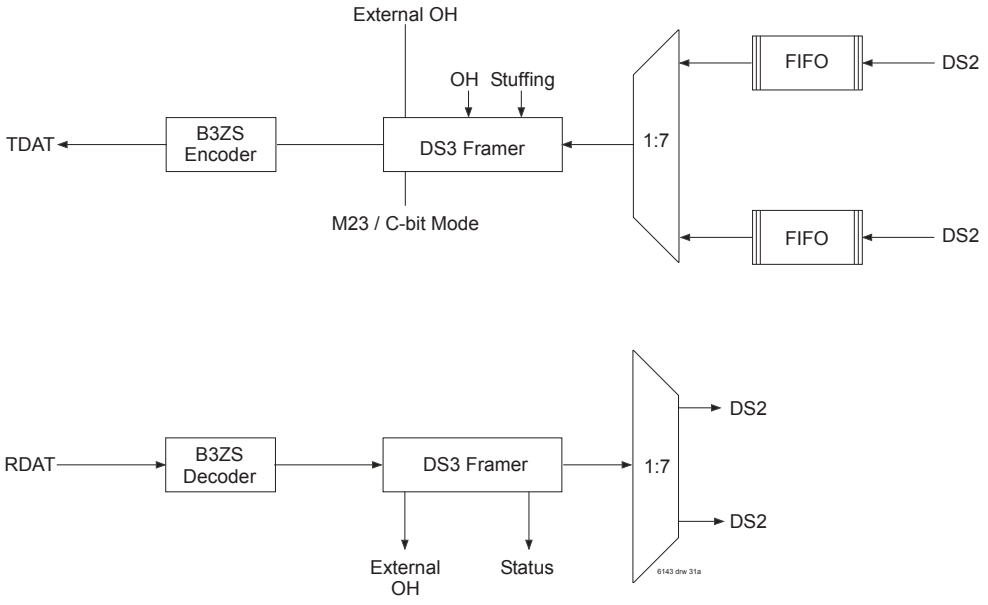


Figure 1 DS3 Framer Block

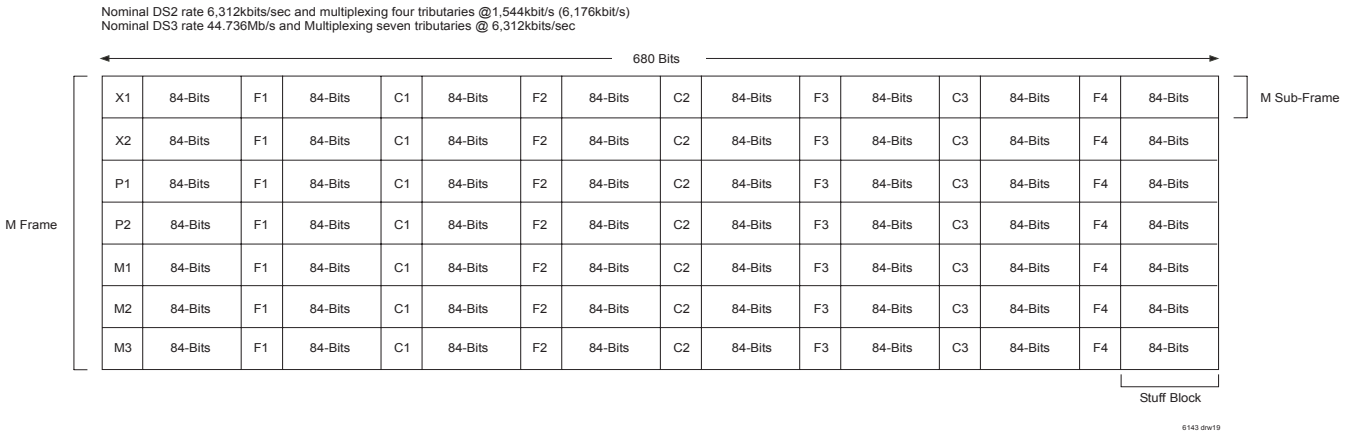


Figure 2 DS3 Frame

1.1.1 Framing modes

1.1.1.1 M23 Mode

In M23 Mode the three C-bits per DS3 M-subframe indicate the nature of stuff opportunity bit in the last block of the M-subframe. Stuffing is further explained in the M23 section.

1.1.1.2 C-bit Parity Mode

In C-bit parity mode the DS2s operate at the nominal DS2 rate and thus no stuffing is required. As such all the stuff opportunity bits contain stuffing (null bit) and the C-bits are used to carry performance monitoring, alarm, control and Data Link channel.

1.1.1.3 Transparent Mode

1.1.2 Reframing

1.1.2.1 Procedure

The search of frame alignment (based on F-bits and M-bits) will happen in two cases:

- After a reset.
- After an internal out of frame (OOF) declaration.
- When the microprocessor forces the reframing process.

The algorithm of reframing is based on the following steps:

- The DS3 framer will search for the F-bits in order to find one potential M-subframe alignment.
- Then the DS3 framer will process the M-bits to detect the M-Frame structure (X-bits and P-bits are ignored during the reframing operation).
- Framing is declared if the M-bits are correct for three consecutive M-frames (and no F-bits error is detected).
- X-bits and P-bits are ignored

1.1.2.2 Max Time

The MART, maximum average reframing time (the average time necessary when processing all the bits in the M-frame), is 1.5ms. Framing goes from DS3 framing to DS2 framing.

1.1.3 Errors and Alarms

1.1.3.1 Line Management

All the alarms and errors associated with line management must be processed if the coding/decoding function is implemented. The 82V8313 will manage the DS3 LIU (counting and reporting errors). But the DS3 LIU has to control the DS3 line (encoding / decoding and errors detection).

1.1.3.1.1 BnZS coding overview

BnZS corresponds to an AMI line code with the substitution of a unique code to replace occurrences of n consecutive zero signal elements. For DS3 lines, a B3ZS code (three-zero substitution) is used. In the B3ZS format, each block of three consecutive zeros is removed and replaced by a B0V or 00V code:

- B represents a pulse conforming to the bipolar rule.
- 0 is a zero (no pulse).
- V represents a pulse violating the bipolar rule.

The choice of B0V or 00V is made so that the number of B pulses between consecutive V pulses is odd. For DS1 lines, a B8ZS code is used (no more than seven consecutive zeros on a DS1 line).

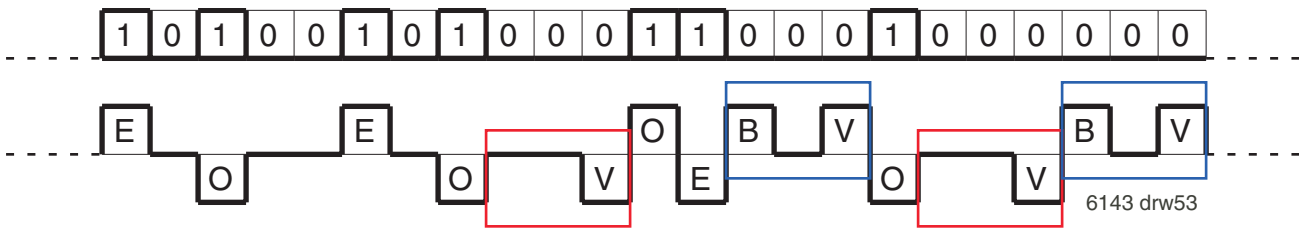


Figure 3 B3ZS Coding

1.1.3.1.2 Bipolar Violation description

Bipolar Violation Error (BPV) is declared when a pulse presents the same polarity as the previous "1" while also not following the B3ZS coding. This is the mechanism used to determine if there is a true line code violation or if there is a substitution. For each DS3 Line Code Violation the 82V8313 will increment the DS3LCV Count Register (0x14 and 0x15).

1.1.3.1.3 Excessive zeros error description

EXZ is declared on occurrence of more than n consecutive zeros for BnZS coded signal. For each EXZ violation the 82V8313 will increment the DS3 EXZS Count Register (0x18 and 0x19).

1.1.3.1.4 LOS description

A LOS defect occurs when there are 175 ± 75 contiguous pulse positions shifted in the device with no pulses of either positive or negative polarity at the line interface. A LOS defect is ended when there is a detection of an average pulse density of at least 33% (for T3 Line) over a same period (12.5% for T1 Line). LOS failure is declared when LOS defect persists for 2.5 ± 0.5s. LOS failure is cleared when LOS defect is absent for 10 ± 0.5 seconds for T3 Line (20 seconds or less for T1 Line). A LOS is indicated in the DS3 Framer Interrupt Status Register (0x36) and the DS3 Framer Status (0x37).

1.1.3.2 OOF (Out of Frame)

OOF shall be declared when there is a significant ratio of frame alignment, F-bit, errors. The typical ratio is three (or more) errors out of 16 (or fewer) consecutive framing F-bits—a sliding window methodology is implemented in the 82V8313. The algorithm used is a logical ORing of 1 (or more) M-bit errors in 2 (or more) out of 4 (or fewer) consecutive M-frames with the F-bit error criteria. The OOF defect is ended when the signal does not contain any more framing bits (F-bits and M-bits) error in several consecutive frames (1 M-frame or more). The defect detection and termination must be done in less than 2.3ms (1.5 times the Maximum Average Reframe Time (MART). The 82V8313 can be configured for either 3 out of 16 consecutive F-bit errors or 3 out of 8 consecutive F-bit errors (DS3 Framer Configuration Register 0x34). OOF violations are monitored in the DS3 Framer Status Register (0x37).

1.1.3.3 RED ALARM

RED defect is defined by the occurrence of OOF or LOS in one M-frame.

1.1.3.4 LOF (Loss of Frame)

Loss of Frame:

- LOF is declared when the OOF persists for 2.5 ± 0.5 s.
- LOF is cleared when the OOF defect is absent for 10.0 ± 0.5 s. FCP (Failure Count Path) is incremented each time LOF failure appears.

1.1.3.5 AIS

AIS signal is transmitted downstream (instead of the normal signal to):

- Maintain transmission continuity
- Indicate to the receiving equipment that there is a transmission interruption located either at the equipment originating the AIS signal or upstream of that equipment (AIS is sent downstream until the incoming signal becomes correct again).

Different events can be declared as AIS:

- Incoming signal with valid framing (M and F-bits), valid parity, all DS3 stuff indicators C-bits set to 0, X-bits set to 1 and repeated information pattern 1010... (A 1 immediately following any of the control bit position) shall be identified as being DS3 AIS.
- Unframed all-ones signal = Blue code.
- Framed DS3 signal with the repeated payload pattern 1010.
- Framed DS3 arbitrary pattern with all DS3 stuff indicators C-bits set to 0.
- Framed DS3 1010 pattern with all DS3 stuff indicators C-bits set to 0.
- Framed all-ones signal (the overhead bits are ignored).

OOF detection implies to insert AIS downstream in 2.25 to 3ms. LOS or incoming AIS implies to send AIS downstream in maximum 0.15ms (0.1 MART). AIS defect occurs upon detection of AIS in contiguous M-frames for a time T, 0.2ms ≤T≤100ms. This defect must be detected and cleared properly in the presence of a random BER 10^{-3}.

In GR-499-CORE, it is specified that AIS defect detection and termination must be done in 2.3ms (1.5 x MART) and maximum removal time is 0.15ms (0.1 x MART).

The 82V8313 has an integration counter which decrements for each invalid M-frame and increments the integration counter. In slow detection mode the count saturates 127 which results in a detection time of 13.5ms. In fast detection mode the saturation point is 21 and results in a detection time of 2.23ms.

DS3 AIS failure is declared if an AIS defect persists for 2.5 ± 0.5 s. AIS failure is cleared if AIS defect is absent for 10.0 ± 0.5 s. Typically an Alarm Indication Signal Counter on the system is incremented each time an AIS failure appears. On the downstream data flow, two strategies must be activated during AIS defect:

- Continue data processing with the last correct frame alignment (off-line framer).

  Note: due to the amount of errors (AIS, LOF or LOS failure activated), incoming data can have a M23 and M12 stuffing ratio between 0 and 100%. In the worst case, some applications can have problems due to DS1 clock deviation: DS1 clock can vary between 1.544 MHz ± 1745 ppm and 1.544 MHz – 3218 ppm.

- **Send a full 1's signal to the HDLC controller:**

Send downstream full 1's (stopping DS2 and DS1 framers allowed: in that case, a full 1's signal must be sent downstream the DS1 signals).

1.1.3.6 RAI (Remote Alarm Indication)

1.1.3.6.1 RAI for C-bit Parity Mode

The RAI signal has to be immediately transmitted upon declaring LOS failure, LOF or AIS failure. An RAI failure is declared as soon as any of the four following alarm signals are detected on the far-end alarm channel (FEAC, explained the following section):

- Equipment failure (service affecting)
- LOS failure, LOF or AIS failure.

RAI failure is cleared as soon as the absence of all of the above alarm signals is detected. A system counter must be incremented by one each time the RAI failure begins.

1.1.3.6.2 RAI for M23 Mode

RAI failure is declared when the far-end SEF/AIS defect (if implemented, X-bits) persists for 2.5 ± 0.5s. The RAI failure is cleared when SEF/AIS disappears for 10.0 ± 0.5s. A counter must be incremented by one each time the RAI failure begins.

1.1.3.7 Parity error

The 82V8313 uses even parity, which is defined as: if the digital sum of all information bits (4704 bits in the M-frame) is equal to 1 in the previous M-frame, the two P bits are set to 1 (similar for 0).

Error is indicated if the received P-bits do not match the locally calculated parity, or when the two P-bits do not agree. P-bit errors are counted in the P-bit Error Register (0xA and 0xB).

Parity Error Ratio, PER, is typically defined as the number of Parity errors detected divided by the number of M-frames examined.

1.1.3.8 X-bit: FERF (Far-End SEF/AIS = RDI)

The two X-bits must be equal in an M-frame.

If X1 = X2 = 0, the Far End Receive Failure (FERF) is declared as soon as a valid framing is not identified or AIS is received.

FERF status remains in the previous state in the following cases:

- If X1 ≠ X2
- If OOF is detected: FERF status can be updated only after having completely processed the current incoming M-frame. If the current M-frame is numbered n, the last valid FERF information comes from M-Frame numbered n-2 (error can start in end of M-frame n-1 and can be declared at the beginning of M-Frame n).

The X-bits must not change more than once per second.

TABLE 3 —FERF Status (X1 & X2 State)

X1	X2	FERF Status
0	0	1
0	1	Previous State
1	0	Previous State
1	1	0

1.1.3.9 Idle Signal

If implemented, the idle signal must have correct M-bits, F-bits and P-bits. The 3 C-bits in subframe 3 of the M-frame must be set to 0 and all other C-bits can take any values (and may vary with time). The X-bits shall be set to 1 and the repeated information pattern 1100 must be sent (started with 11 after each M-frame alignment, M-subframe alignment, X-bit, P-bit and C-bit). Such a signal is used before the customer initializes the channel to avoid declaration of alarm. The identification of the idle signal should not exceed 10 seconds in duration.

1.1.3.10 C-bits signification if C-bit parity mode activated

The C-bit parity mode (see M23 chapter) affected C-bits for special purposes (no more stuffing bit indicators):

TABLE 4 —C-BIT PARITY MODE DS3 C-BIT ASSIGNMENTS

M-SUBFRAME NUMBER	C-BIT NUMBER	FUNCTION
1	1 2 3	Application Identifications Reserved for future network use Far-End Alarm and Control (FEAC)
2	1 2 3	Unused Unused Unused
3	1 2 3	CP (Parity) CP (Parity) CP (Parity)
4	1 2 3	Far-End Block Error (FEBE) Far-End Block Error (FEBE) Far-End Block Error (FEBE)
5	1 2 3	Data Link (DL) Data Link (DL) Data Link (DL)
6	1 2 3	Unused Unused Unused
7	1 2 3	Unused Unused Unused

1.1.3.10.1 AIC

The Application Identification Channel is used to identify the specific DS3 M-frame application:

- In M23 mode: AIC shall be random 1s and 0s.
- In C-bit Parity mode: AIC shall be set to 1 (In this mode, AIC is not sufficient for determining identification of C-bit parity application. The process needs the confirmation by secondary methods such as the presence of 0s in the FEBE bit positions)
- Unchannelized applications may have either any AIC value (if developed before ANSI T1.107 — 1995 standards) or all 1s (as C-bit parity mode). The process to identify the DS3 application should typically not exceed 10 seconds in duration.

1.1.3.10.2 FEAC

Far End Alarm and Control signals are encoded into repeating 16-bit 0xxxxxx011111111 codewords (right-most bit transmitted first): the 6–bits x allowed 64 distinct signals; assigned codewords GR-499-Core code words areincluded for reference:

- Listing order is in decreasing priority order. Codewords shall be transmitted continuously for the duration of the condition being reported, or 10 repetiions whichever is longer.
- Control messages are higher in priority then any of the far end alarm signals.

The idle state of the FEAC channel (no codeword is transmitted) is a full ones signal. A code is correct (no error during transmission) after being received 10 times. Some implementations also use algorithms that take care of BER: a valid BOC message is declared if a code is received 4 out of 5 times, or 8 out of 10 times as determined by the AVC bit in the FEAC Configuration Register (0x32).

TABLE 5 —DS3 FEAC LOOPBACK CONTROL MESSAGES

Condition	Codeword
Line Loopback Activate (4)	0 000111 0 11111111
Line Loopback Deactivate (4)	0 011100 0 11111111
DS3 Line	0 011011 0 11111111
DS1 Line Number n	0 1---n--- 0 11111111
(1£ n £ 28) (5)	
DS1 Line - All	0 010011 0 11111111

TABLE 6 —DS3 FEAC ALARM AND STATUS MESSAGES

Function	Codeword
DS3 Equipment Failure (Sa)	0 011001 0 11111111
DS3 LOS (1)	0 001110 0 11111111
DS3 OOF	0 000000 0 11111111
DS3 AIS Received	0 010110 0 11111111
DS3 Idle Signal Received	0 011010 0 11111111
DS3 Equipment Failure (Nsa)	0 001111 0 11111111
Common Equipment Failure (Nsa)	0 011101 0 11111111
Multiple DS1 LOS (2 and 3)	0 010101 0 11111111
DS1 Equipment Failure (Sa) (3)	0 000101 0 11111111

NOTES

Sa: Service affecting.

Nsa: Non-service affecting Single DS1 LOS (2 and 3) 0 011110 0 11111111

1. Applicable to B2ZS-coded signal. DS1 Equipment Failure (Nsa) (3) 0 000011 0 11111111
2. Network equipment must not respond to or generate these codewords.
3. Applicable to all type of loopbacks.
4. Code must be transmitted 10 times, followed immediately by 10 repetitions of the DS3 or DS1 line codeword.
5. For Unchannelized DS3 applications, DS1s are unassigned.

*Listing order is in decreasing priority order. Codewords shall be transmitted continuously for the duration of the condition being reported, or 10 repetitions whichever is longer.

**Control messages are higher in priority than any of the far end alarm signals.

1.1.3.10.3 Bit Oriented Code Detector (BOC)

The Receive Bit Oriented Code Detector (RBOC) is designed to detect the presence of BOCs in the DS3 C-bit parity Far End Alarm and Control (FEAC) channel. The RBOC recognizes 63 of the 64 possible BOCs, and purposefully ignores the “111111” code which is similar to the HDLC flag sequence. BOCs are received in a FEAC channel as 16–bit sequences composed of an 8–ones header, a zero, six BOC bits, and a trailing 0 (“111111110xxxxxx0”). In order to validate a BOC, the same code must be repeated at least ten times with at least 8 of 10 or 4 out 5 times (as specified by the AVC bit) being the same.

The RBOC block will trigger an interrupt, unless masked, to indicate the receipt of a BOC or when the BOC disappears. If the BOC receives an invalid code the BOC bits will be set to “111111” The Transmit Bit Oriented Code (XBOC) is designed to transmit BOCs in the DS3 C-bit parity Far End Alarm and Control (FEAC) channel. The XBOC can transmit 63 of the 64 possible BOCs, and purposefully ignores the “111111” code which is similar to the idle HDLC flag sequence. BOCs are transmitted in a FEAC channel as 16–bit sequences composed of an 8–ones header, a zero six BOC bits, and a trailing 0 (“11111111xxxxxx0”). The 16–sequence is repeated until disabled by forcing the six code bits to “111111” Some of the common BOCs are listed here for reference.

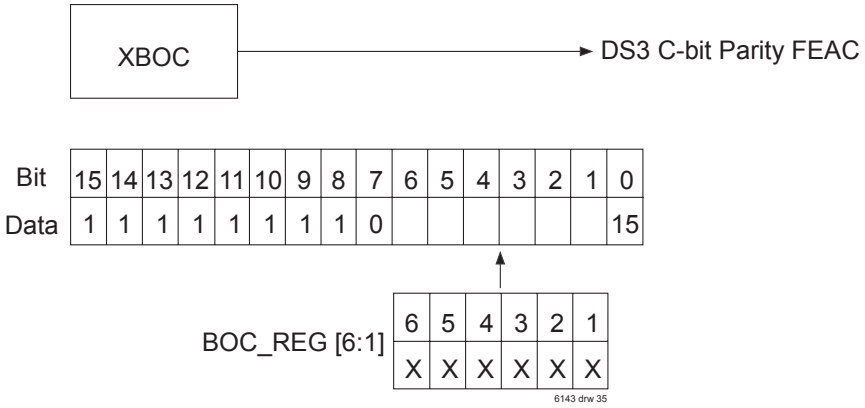


Figure 4 Transmit BOC

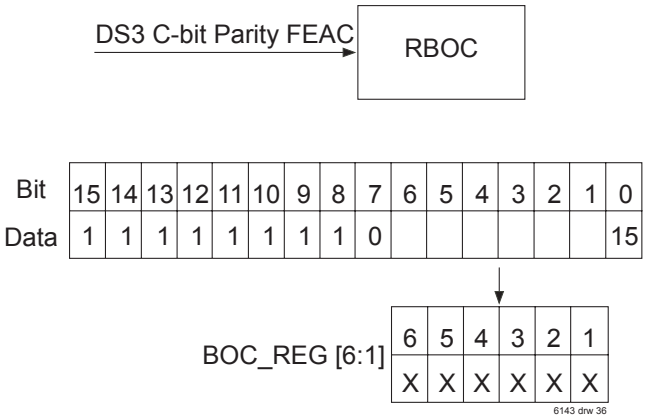


Figure 5 Receive BOC

TABLE 7 —DS1 BIT ORIENTED CODES COMMAND AND RESPONSE MESSAGE

Function	Codeword
Line Loopback Activate	0 000111 0 11111111
Line Loopback Deactivate	0 011100 0 11111111
Payload Loopback Activate	0 001010 0 11111111
Payload Loopback Deactivate	0 011001 0 11111111
For Network Use (Loopback Activate)	0 001001 0 11111111
Universal Loopback Deactivate	0 010010 0 11111111
ISDN Line Loopback (NT2)	0 010111 0 11111111
C1/CSU Line Loopback	0 010000 0 11111111
For Network Use (NT1 Power Off)	0 001110 0 11111111
Protection Switch Line n ($1 \leq n \leq 27$)	0 1---n--- 0 111111111
Protection Switch Acknowledge	0 001100 0 11111111
Protection Switch Release	0 010011 0 11111111
Do not use for synchronization	0 011000 0 11111111
Status 2 Traceable	0 000110 0 11111111
SONET Minimum Clock Traceable	0 010001 0 11111111
Stratum 4 Traceable	0 010100 0 11111111
Stratum 1 Tracable	0 000010 0 11111111
Synchronization Traceability Unknown	0 000100 0 11111111
Stratum 3 Traceable	0 001000 0 11111111
Reserved for NetworkSynchronization	0 1000000 0 11111111
Transmit Node Clock (TNC)	0 111100 0 11111111
Stratum 3E Traceable	0 111110 0 11111111

TABLE 8 —DS1 BIT ORIENTED PRIORITY MESSAGES

RAI/Yellow Alarm	0 000000 0 11111111
Loopback Retention	0 010101 0 11111111
RAI-CI	0 011111 0 11111111

TABLE 9 —DS1 BIT ORIENTED CODES RESERVED MESSAGES

Under Study for Maintenance	0 010110 0 11111111 0 011010 0 11111111
Reserved for Network Use	0 001011 0 11111111 0 001101 0 11111111 0 001111 0 11111111 0 011101 0 11111111
Reserved for Customer	0 000011 0 11111111 0 000101 0 11111111 0 000010 0 11111111 0 011011 0 11111111
RAI-CI	0 011111 0 11111111

NOTES:

1. Sa-Service affecting
2. Nsa-Non Service Affecting
3. Applicable to B3ZS - coded signal
4. Newtork equipment must not respond to or generate these code words.
5. Applicable to all types of loopbacks
6. Code must be transmitted 10 times, followed immediately by 10 repetition of the DS3 or DS1 line code word.
7. For unchannelized DS3 applications, DS1 are unassigned.

1.1.3.10.4 Terminal-to-Terminal application specific data link

The nine C-bits in M-subframes 2, 6 and 7 are reserved for application specific uses in DS3 terminal equipment. If they are not used, they will be set to one.

1.1.3.10.5 DS3 Path Parity Bits

The three CP-bits (Parity bits instead of stuffing indication in C-bit parity mode) must be set to the same value as the two P-bits in the M-frame structure. Some transport equipment in the network may alter P-bits, but any intermediate equipment on the DS3 path typically does not modify CP–bits. Parity error detection (also called Path Error) is done by computing the parity of the information bits in the nth M-frame and is compared to the result with the majority value of the CPbits received in M-frame n + 1.

1.1.3.10.6 FEBE (Far End Block Error)

The three FEBE bits shall be set to any pattern other than 111 to indicate a far-end CP-bits error or framing (M or F-bits) error. The FEBE-bits are equal to 111 if no error is detected.

1.1.3.10.7 DS3PMON counters

The DS3 Performance Monitor is a collection of counter registers for tracking C-bit Parity Errors (CPERR), Excessive Zeros Occurrences (EXZS), Far End Block Errors (FEBE), Framing Bit Error (FERR), Line Code Violations (LCV), and P-bit Parity Errors (PERR). Each counter can be individually cleared and accessed via microprocessor. If the counter is not cleared in an appropriate interval defined by the specific counter register, the counter will stay at the maximum value and not roll over.

During a microprocessor access to a PMON register, an internal clock transfer signal is generated to transfer the internal count value to the holding registers. Once this transfer is made the internal counter is reset until the next interval. In this way, error events occurring during the reset period are not missed. To preempt an overrun condition, whenever a counter-to-holding-register transfer occurs, an interrupt is generated (unless masked). However, if the holding register is not read since the last interrupt, an overrun will occur and the overrun status bit in the corresponding register will be set.

1.1.3.10.8 Terminal-to-Terminal Path Maintenance Data Link

The three C-bits in M-subframe 5 may be used as a 28.2 kbit/s terminal-to-terminal data link for path maintenance data. Data link protocol follows a subset of the LAPD specification (Recommendation Q.921) with three messages defined (others are ignored):

Messages shall be transmitted continuously at a minimum rate of once per second (when no message is transmitted, the data link contains the repeated idle pattern (“01111110”). The transmitting terminal must perform zero stuffing to avoid flag pattern occurrence between opening and closing flags (equipment in receives path must suppress extra 0s). If the full length of an information field is not needed (or if the field is not used), the ASCII null character shall be used to indicate the end of the string. The remaining bit positions of the data field can contain any combination of 1s and 0s. At any time, the abort code can be also sent. A carrier may use this data link for the provisioning or maintenance of the DS3 facility or network. That may cause interruptions, delays or reduction of throughput on the data link. However, that should not affect the timely transmission of the messages. If not used, the three bits shall be set to 1.

TABLE 10 —DATA LINK FORMAT

Bit	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	
Flag	0	1	1	1	1	1	1	0	
SAPI	0	0	1	1	1	1	C/R	0	EA
TEI	0	0	0	0	0	0	0	1	EA
Control	0	0	0	0	0	0	1	1	
	76 or 82 Bytes Information Field Type (1 byte) EIC (10 bytes LIC (11 bytes) FIC (10 bytes) Unit (6 bytes) Final Field (38 bytes)								
FCS-16	2^{-8}							2^{-15}	
	2^{-0}							2^{-7}	

NOTES:

1. C/R = 0 if DTE (from user side)
2. C/R = 1 if Carrier (from network side)
3. FCS: is the Frame Check Sequence CRC16 (can be disabled) Polynomial = $x^{16} + x^{12} + x^5 + 1$
4. Type: identify type of message (1 byte) with the following value
   - For PID message: 00111000 (76 byte info field)
   - For ISID message: 00110100 (76 byte info field)
   - For TSID message: 00110010 (76 byte info field)
   - For ITU-T path ID: 00110010 (82 byte info field)
5. EIC: identify the specific piece of equipment (10 bytes).
6. LIC: identify a particular location (11 bytes).
7. FIC: identify where the equipment is located with in a building (10 bytes).
8. UNIT: identify the equipment location with in a bay (6 bytes).
9. Final field (38 bytes):
   - For PID message: FI to identify a specific DS3 path
   - For ISID message: PORT number to identify the port number of the equipment that initiated the idle signal.
   -For TSID message: GEN nnumber to identify the signal generator that initiated the test signal.

1.1.3.10.7 Data Link Receiver

The RDL block first searches for the flag characters before identifying the first byte of data where the RDL block then removes the stuff bits, calculates the CRC-CCITT frame check sequence (FCS), and then stores the framed data into a 4-level FIFO buffer. The RDL buffer has an associated control buffer, which will indicate data ready, flag detected, end of message (EOM) and overrun (OVR) status to maintain the RDL.

In an EOM condition, the Status Register also indicates the FCS status and the number of valid bits in the last data byte of the message. An interrupt will be generated not only when the FIFO reaches a programmable threshold, but also when an abort sequence, FIFO overrun, or terminating flag sequence are detected.

1.1.3.10.8 Data Link Transmitter

The XDL transmitter is designed to provide a serial path for HDLC data in C-bit parity applications. The XDL transmitter, will automatically perform data serialization, CRC generation, bit-stuffing, flag generation, idle sequence, and abort sequence. The XDL transmitter performs all of the necessary signaling to maintain the channel. An interrupt is provided so that a double buffered transmit data register remains full for the duration of the message. The XDL at the end of the frame will automatically calculate the CRC-CCITT FCS if enabled. Once the frame is complete the XDL will transmit idle codes until the following frame begins. Should an underrun condition occur, the XDL transmitter will automatically transmit an abort sequence and notify the controlling processor via the XDL Status Register UDR status bit. An underrun occurs when, the controller does not write a word to the transmit data register before the previous byte has been transmitted. Also, at any time, an abort sequence can be continuously transmitted by setting the ABT control bit in the XFDL TSB Configuration Register (0x20).

The XDL can also be enabled to continuously transmit a flag character “01111110.” The data flow sequence for the XDL works as such:

1. Step 1 continues until the all bytes for the frame are written.
2. Transmit data bytes are written to the Transmit Data register.
3. The XDL prepares the byte by performing a serial-to-parallel conversion of the byte.
4. An interrupt is generated to signal the controller to write the next byte.
5. After the last byte is written to the transmit data register, the EOM bit in the XDL configuration register should be set or the TDLEOMI pin should be set to indicate the end of message.
6. The XDL sends the last data byte and then the CRC word is sent (if enabled) or a flag (if CRC is not enabled).
7. Once complete, the flag character is sent.

To prevent unintentional transmission of abort or flag characters, if more than five consecutive ones exist in the raw transmit data of in the CRC data, a zero is stuffed into the serial data output.

The Data Link Section provides additional information about the data link function.

1.1.3.11 DS3 Loopback

The DS3 can be looped back on the line level (asked by remote equipment via FEAC message or local host decision). However, no remote DS3 payload loopback is defined. In both these cases, transmit and receive clocks can be of a different frequency (independent clocks). In that case, a slip buffer must be provided in order to manage the discrepancy between the incoming and outgoing data streams. When the slip buffer underrun (transmit clock faster than receive clock) or overflow (transmit clock slower than receive clock) an alarm is generated (these events must also be counted).

For more information on the loopback capability see the Loopback Section.

1.1.3.12 Jitter

Jitter is the short-term variations of digital edges from their ideal positions in time. Short-term variations are phase oscillations of frequency greater than 10Hz (variations at frequency under 10 Hz are defined as wander). Jitter amplitude is measured in unit intervals (UI) where one UI is the phase deviation of one clock period.

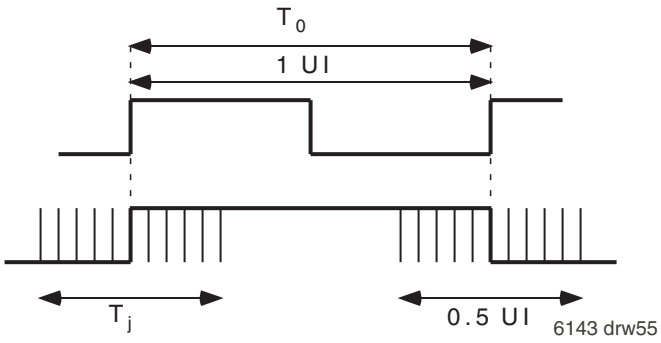


Figure 6 Jitter Definition

There are several kinds of jitter measurement:

- Jitter tolerance (GR-499-CORE 7.3.1): minimum jitter at the input of equipment that results in more than two errored seconds in a 30-second interval.
- Jitter transfer (GR-499-CORE 7.3.2): ratio of (amplitude of equipment output jitter) / (applied input jitter).
- Jitter generation (GR-499-CORE 7.3.3): added jitter by the equipment or chip. There also exists two categories of jitter:
- Category I: when the correspondent line does not physically exists.
- Category II: when the line physically exists.

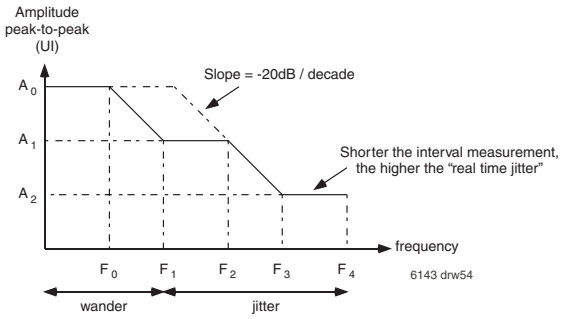


Figure 7 Maximum Jitter Tolerance on DSn Interface Inputs

1.1.4.1.1 Dual Rail Configuration (bipolar mode)

- Rx3CLK (Input): 44.736 MHz clock with duty cycle between 40 and 60 %; clock used to sample (on positive or negative edge: user-selected edge) Rx signals.
- Rx3POS (Input): positive pulse received on the B3ZS-encoded line.
- Rx3NEG (Input): negative pulse received on the B3ZS-encoded line.
- Tx3CLK (Output): 44.736 MHz clock with duty cycle between 40 and 60%. This clock is used to sample (user-selected edge) all the Tx signals.
- Tx3POS (Output): positive pulses that must be sent on B3ZS encoded line.
- Tx3NEG (Output): negative pulses that must be sent on B3ZS encoded line.

1.1.4.1.2 Single Rail Configuration (unipolar mode)

- Rx3CLK (Input): 44.736 MHz clock with duty cycle between 40 and 60%. This clock is used to sample (user-selected edge) all the Rx signals.
- Rx3D (Input): logical incoming data stream received on B3ZS-encoded line.
- RxLCV (Input): Line code violation detected on B3ZS-encoded line.
- Tx3CLK (Output): 44.736MHz clock with duty cycle between 40 and 60%. This clock is used to sample (user-selected edge) all the Tx signals.
- Tx3D (Output): logical data that must be encoded and sent by the DS3 LIU.

TxMFP (Output): M-frame pulse synchronization signal that must be high during one bit time (the first of the M-frame (X1).

TABLE 11 —MAX JITTER TOLERANCE ON DS IF CAT II

Data Rate (Mbit/s	UI (ns)	Jitter Amplitude			Filter Frequencies				
		A0 (ms)*	A1 (UI)	A2 (UI)	f_0 (HZ)	f_1 (HZ)	f_2 (HZ)	f_3 (HZ)	f_5 (HZ)
1.544	648	18	10	0.3	1.2×10^{-5}	10	192.9	6.43	40
							78.9	2.63	20
							669	22.3	300

1.1.4 DS3 Framer ⇔ to LIU interface

1.1.4.1 If DS3 Framer ⇔ DS3 LIU

The interface between a DS3 LIU and a DS3 Framer depends on which device is performing the line coding / decoding function:

- If the line encoder / decoder is in the LIU: signals follow single rail configuration.
- If the line encoder / decoder is in the framer: signals follow dual rail configuration.

1.2 M23 MULTIPLEXER

To multiplex 7 DS2 signals into a formatted DS3 signal (respectively, to terminate a framed DS3 and to generate 7 independent DS2 signals). The M23 function is not activated when the M13 is used in an unchannelized mode. When the M23 function is used, the DS3 formatted data stream (but not framed) is made by taken one bit from each DS2 data streams in a round robin fashion.

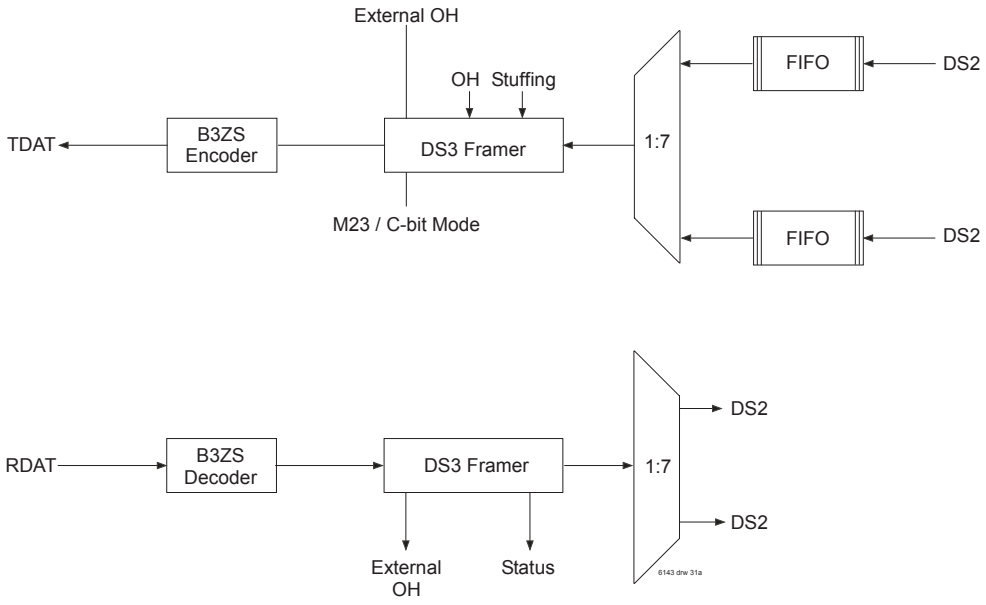


Figure 8 M23 Mulitplexer Block

1.2.1 Stuffing

1.2.1.1 Description

The seven DS2 are asynchronous relative to each other and therefore may be operating at different rate. Bit Stuffing adjusts the different incoming rates. The stuff opportunity bit position exits in the last block of each DS3 M-subframe to adjust the transmission rate of each DS2 stream independently (just one bit stuffing opportunity per DS2 and per DS3 M-subframe). The signal data rate limits are:

- Maximum data rat: 6.3157Mbit/s (more than 6.312 M/bits ± 20 ppm)
- Minimum data rate: 6.3063Mbit/s (less than 6.312 M/bits ± 20 ppm)

Stuffing indication bits are the C overhead bits, 3 C bits for each DS2 (Ci1, Ci2, and Ci3 for DS2-i)

If 2 or 3 C-bits are “1”s, the bit in the correspondent stuffing position is a stuff bit (either 0 or 1): if zero or one C-bit equals, “1”, the bit in the stuffing position is a data.

M1 Sub-Frame	F4	Stuff Bit 3	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	• • •	Info Bit 84
M2 Sub-Frame	F4	Info Bit 1	Stuff Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	• • •	Info Bit 84
M3 Sub-Frame	F4	Info Bit 1	Info Bit 2	Stuff Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	• • •	Info Bit 84
M4 Sub-Frame	F4	Info Bit 1	Info Bit 2	Info Bit 3	Stuff Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	• • •	Info Bit 84
M5 Sub-Frame	F4	Info Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Stuff Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	• • •	Info Bit 84
M6 Sub-Frame	F4	Info Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Stuff Bit 6	Info Bit 7	Info Bit 8	• • •	Info Bit 84
M7 Sub-Frame	F4	Info Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Stuff Bit 7	Info Bit 8	• • •	Info Bit 84

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Figure 9 DS3 Stuff Block

1.2.1.2 Stuffing strategies

1.2.1.2.1 On receive line adaptation

The number of real stuffing bits inserted in transmission is equal to the number of real stuffing observed in reception. It is called loop-timing mode.

1.2.1.2.2 M23 Mechanism

As each DS2 signals can be considered asynchronous, the host must be able to give each DS2s the stuffing speed for transmission. The range of each DS2 data rates is:

- If zero stuff: 6.31567 MHz (6.312 MHz ± 581 ppm).
- If full stuff: 6.306272 MHz (6.312 MHz ± 907 ppm).

A particular case is the nominal stuff (DS2 signal frequency equal to 6.312 Mbit/s). To multiplex such a DS2 in one DS3 signal, the host must program the stuffing speed at a special value that corresponds to a 39.06 % stuffed M-frames (for the particular DS2). As the DS2 level is most often a transition between DS1 and DS3 signals, it is possible to use always the M23 mode with a fixed stuff: zero stuff, full stuff or nominal stuff.

1.2.1.2.3 C-bit parity Mechanism

In this mode, the decision is a full stuff: each stuffing bit opportunity (for all the DS2) in all DS3 M-Frames contains a stuff except when the DS3 signal is unchannelized. In this case, it is possible to have a C-bit parity mode with a null stuff strategy. C-bits are not used for stuffing indication (always full or zero stuff): they can be used for others purposes presented in DS3 framer chapter.

1.3 DS2 FRAMER

The nominal DS2 interface rate is 6.312 Mbit/s ± 33 ppm (± 208 bit/s). Then DS2 framer function is not activated when unchannelized DS3 is initalized. DS2 signal is a combination of four DS1 signals. A DS2 M-frame is composed of four DS2 M-subframes. Moreover, each M-subframe contains six blocks of 48 payload bits (bit-interleaved from the four DS1 streams; made by M12 function) plus 1 overhead bit (the four subframes do not represent each separate DS1 signals). The DS2 frame contains 1176 bits (1152 payload bits ± 24 overhead bits) and the period is 186.31ms.

The DS2 Framer can also be used to frame G.747 bit streams. In this case the nominal DS2 rate is 6.312 Mb/s multiplexed from three tributaries of 2.048 Mbit/s.

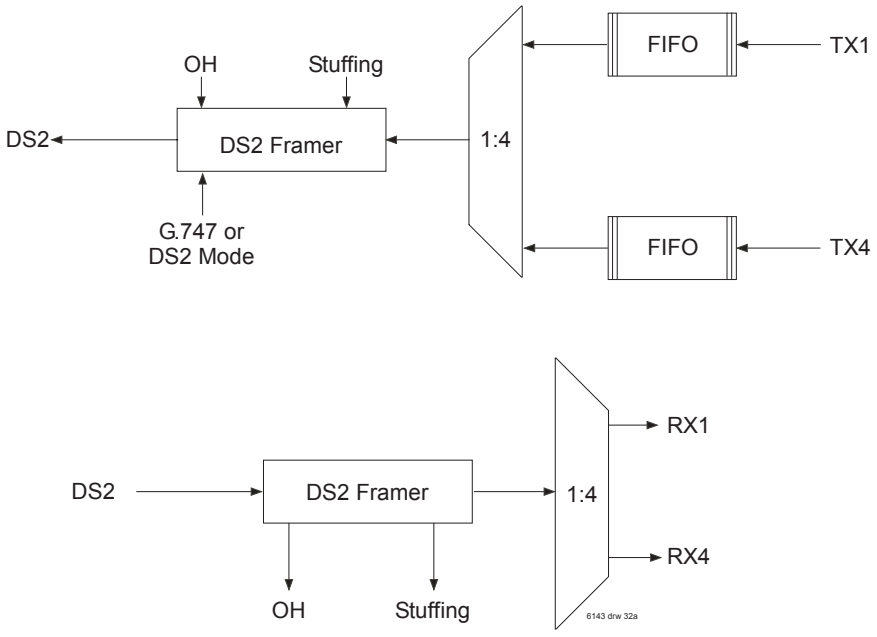

Figure 10 DS2 Framer Block

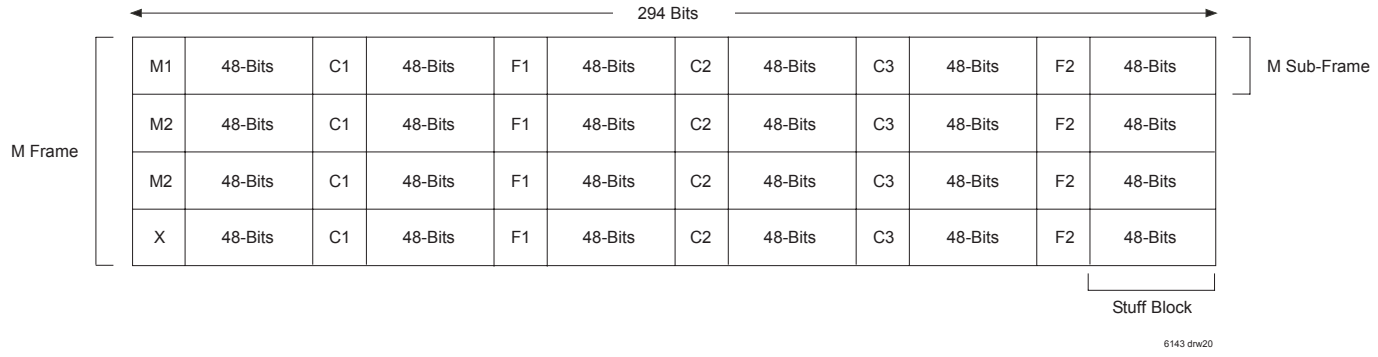

Figure 11 DS2 Frame

1.3.1 Reframing

1.3.1.1 Procedure

The search of frame alignment must be activated in three cases:

- After a reset.
- When the microprocessor forced the reframing process.
- After an internal out of frame (OOF) declaration (but reframing asked by microprocessor). When a DS2 reframing is in process, All-ones AIS signal is sent downstream for the duration of the reframing.

1.3.1.2 Max Time

The standard indicates a maximum average framing time of 7ms to resynchronize the incoming data flow (time necessary to check every bits of a structure before declaring frame synchronization). This time is significant only if neither mimic pattern (data payload that ìsimulateî a frame alignment pattern) nor other trouble (like errors) is present inside the incoming data flow.

1.3.2 Alarms and errors

1.3.2.1 OOF

Out Of Frame is declared when n out of m consecutive framing bits are in error (n = 2 and m = 4 or 5). Optionally, the OOF detection can take into accounts one or more M-bits in error in 3 or 4 consecutive M-frames. If configured, during DS2 OOF, an all-ones AIS signal is sent downstream to all concerned DS1s. Otherwise the payload extracted with the previous frame alignment is transmitted downstream because it is an off-line framer. OOF defect is terminated when the signal does not contain any more framing bits (F-bits and M-bits) error in several consecutive frames (1 M-frame or more). Defect detection / termination must be done in less than 10.5 ms (1.5 x MART).

1.3.2.2 LOF

LOF failure is declared if OOF defect is present for 2.5 ± 0.5 seconds except when a DS2 AIS defect is present or DS2 AIS failure has been declared. LOF is cleared if no error has been detected in 10 ± 0.5 seconds.

G.747
Nominal DS2 rate 6312Kbit/s multiplexing three tributaries of 2048 kbit/s
Nominal DS3 rate 44.736Mb/s multiplexting seven tributaries of 6,312kbits/sec

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9		Bit 167
Set 1	1	1	1	0	1	0	0	0	0	0		
Set 2	AIS	PAR	REV									
Set 3	C11	C21	C31									
Set 4	C12	C22	C32									
Set 5	C13	C23	C33	Stuff 1	Stuff 2	Stuff 3						

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Parity = 1 Odd
Parity = 0 Even
REV Reserved, should be set to 1
Cji (j = 1,2,3 i = 1,2,3) indicates the ith justification control bit of the jth tributary
Stuff (j) : Stuff bit for the jth tributary
Positive Justification = 111 (Majority decision)
No Justification = 000 (Majority decision)

Figure 12 G.747 Frame Format

1.3.2.3 AIS

AIS Defect is declared when at least one of the three following conditions (it should be detected in less than 10.5 ms = 1.5 x MART.) is true:

- Incoming signal with more than 99.9% of ones density (unframed all-ones signal = AIS from upper level).

(Incoming signal with unframed condition (DS2 LOS or OOF).

- Host command.

The insertion of AIS (same for the AIS removal) in the downstream signal has to be made in less than 0.7 ms (0.1 x MART) AIS failure is declared if an AIS defect is present for 2.5 ± 0.5 seconds and is cleared if AIS a defect is absent for 10 ± 0.5 seconds. The activation of an AIS failure must not exceed 0.7 ms and a host can configure one of the two downstream transmission strategies:

- Payload transmission taking with the last correct frame alignment (off-line framer).
- Transmission of AIS (unframed all-ones signal).

1.3.2.4 RAI

The RAI signal (last M-bit Mx) is transmitted upon declaration of LOF or AIS failure for the duration of the failure (downstream failure). RAI is declared when this bit presents for an interval of 0.5 to 1.5 seconds with no more than 10^{-3} “1”s (active state is zero). Similarly, the inactive state of RAI signal must be sampled between 0.5 and 1.5 seconds with no more than 10^{-3} “0”s.

1.4 G.747 Applications

1.4.1 Reframing

1.4.1.1 Procedure

The search of frame alignment must be activated in three cases:

- After a reset.
- When the microprocessor forced the reframing process.
- After an internal out of frame (OOF) declaration (but reframing asked by microprocessor). When a DS2 reframing is in process, All-ones AIS signal is sent downstream for the duration of the reframing.

1.4.1.2 Max Time

For G.747 applications the DS2 framer has a maximum reframe rime of less than 1ms. In order for the framer to declare framing however, the candidate frame alignment signal must be present for 3 consecutive frames in accordance with CCITT Rec. G.747 Section 4. Once in frame the DS2 framer will provide frame boundary indications as well as overhead bit positions.

1.4.2 Alarms and errors

1.4.2.1 OOF

For alarm indications the DS2 framer is designed to indicate OOF conditions when 4 consecutive frame alignment signals are incorrect in accordance with CCITT Rec. G.747 Section 4. Much like the DS3 framer, the DS2 framer is an "off-line" framer and will continue to indicate errors when OOF based on the previous frame alignment.

1.4.2.2 AIS

In G.747 applications the DS2 framer also uses an integration algorithm with a 1:1 slope to detect RED alarm and AIS. Instead of using DS2 frames however the DS2 framer uses G.747 frames with the integrator counter. AIS is defined as the occurrence of less than 9 zeros while the framer is OOF during that G.747-frame. RED alarm is defined as the detection of a RED defect, or OOF in an M-frame. For each interval, a G.747 frame, if the framer detects a Red defect or AIS event, the integrator counter is incremented. Accordingly, if a valid G.747 frame is received then integrator counter is decremented. As a result the DS2 Framer can detect RED alarm and AIS in 6.9ms.

1.4.2.3 RAI

The DS2 framer also extracts the DS2 X-bit and G.747 Remote Alarm Indication bit, RAI, to indicate a Far End Receive Failure, FERF. The DS2 framer uses an internal status FIFO to insure that for an OOF condition, nearly 100% of the time for DS2 applications and 99.9% of the time for G.747 applications, that the DS2 framer will freeze in a valid state. If two successive X-bits or RAI bits are the same, then a FERF status is indicated and entered into the internal status FIFO. Each M-frame or G.747 frame the status FIFO will be updated and shifted. After a total of six M-frames or G.747 frames, the error condition will reach the sixth (last) position of the FIFO. When the error condition reaches the last position in the FIFO, the DS2 Status Register will be updated to indicate to the controller that a FERF has occurred. The error indication/value will be held in that sixth(last) position while the fifth through second positions will freeze the FERF state of the four M-frames following the FERF condition. The first position of the status FIFO will contain the present FERF state and will be continually updated with the present FERF status. Once correct frame alignment has been reestablished and the OOF condition is gone, then the first FIFO status location will have a valid indication. At this point the FIFO will continue to operate normally, by shifting the FERF status through the FIFO.

1.5 M12

To multiplex 4 DS1 signals into a formatted DS2 signal (respectively, to terminate a framed DS2 and to generate 4 independent DS1 signals). The M12 can also multiplex/demultiplex three E1 (2.048 Mbit/s) streams into a G.747 formatted 6.312 Mbit/s serial stream. The M12 function is not activated when unchannelized DS3 initialized.

1.5.1 Actions on the four multiplexed DS1 bit-streams

The DS2 data stream is built by taking one bit from each of the four DS1 data streams in a round robin fashion. However, the second and fourth DS1 signals must have their all bits inverted.

1.5.2 Stuffing

1.5.2.1 Mechanism

The four DS1 are asynchronous relative to each other and may be operating at different rates. Bit Stuffing is used to adjust the different incoming rates. Stuff opportunity bit position exists in the last block of each DS2 M-subframe to adjust the transmission rate of each DS1 streams independently (just one bit stuffing opportunity per DS1 and per DS2 M-subframe). Stuffing indicator bits are the C overhead bits, 3 C–bits for each DS1 (Ci1, Ci2 and Ci3 for DS1-i). If in these three bits there are 2 or 3 “1”s, the bit in the stuffing position is stuff (value not specified: either 0 or 1); if there are 0 or 1 “1”, the bit in the stuffing position is a data.

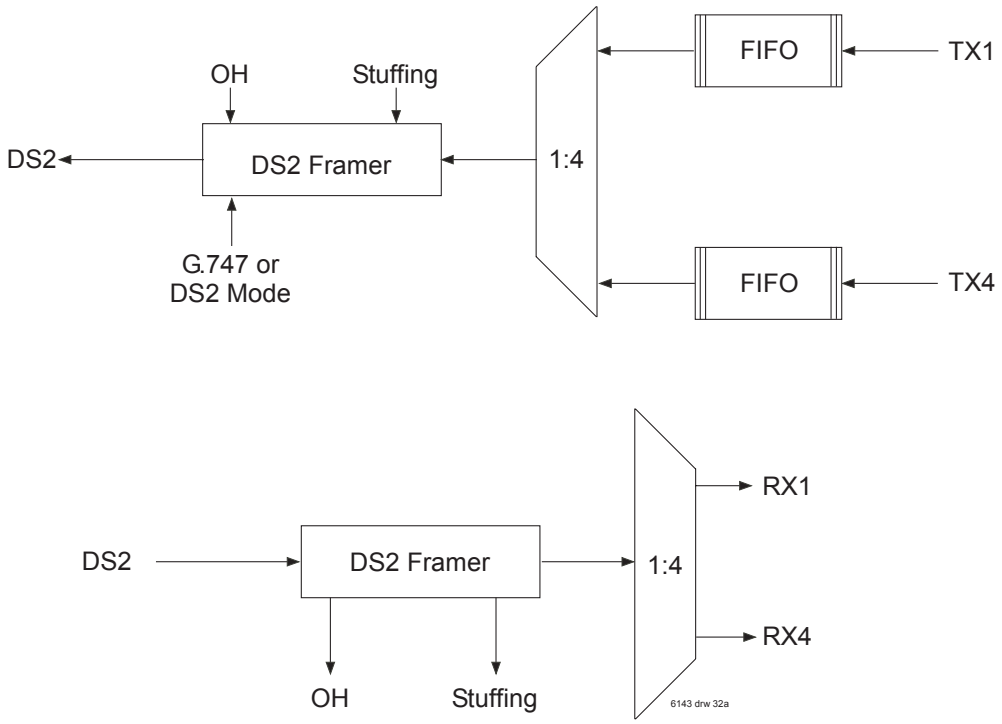


Figure 13 M12 Block

1.5.2.2 Stuffing strategies

1.5.2.2.1 On receive line adaptation

The number of real stuffing bits inserted in transmission is equal to the number of real stuffing observed in reception. This mode is also called per–T1 loop timing. In this mode, the system must free run under trouble condition at 1.544 Mbit/s ± 200 bit/s (1.544 Mbit/s ± 130 ppm). Such a mode seems to be used only if remote loopback (line or payload) is activated.

1.5.2.2.2 Adaptive frequency

As each DS1 signal comes from its own source (asynchronous), the host processor must be able to give for each DS1 the stuffing speed for transmission in order to adapt the DS1 data rates independently. An external reference has to be used to synchronize the DS1 signals (this reference is also called Building Integrated Timing Source, BITS). Such a reference can come from one DS1 received data stream (line-timing mode) or from an external reference such as GPS for example (external reference mode). In reception, each DS1stuffing ratio must be estimated. However, the real time stuffing value depends on the mode used to multiplex DS2s into a DS3 signal:

- If M23 mode, every DS1 signal works at its own speed. (Near the nominal stuffing value if M23 stuffing programmed near the nominal value for example).
- If C-bit parity mode, DS1 stuffing value must be under the nominal value (less stuff) due to the full stuff processing when DS2 signals are multiplexed into the DS3 formatted signal.

1.5.2.2.2.1 DS1 nominal stuffing value if M23 mode used between DS2 and DS3 level

The per-DS1 in a DS2 signal (6.312 Mbit/s) data rate limits are:

- Maximum data rate: 1.5458 Mbit/s (more than 1.544 Mbit/s ± 20 ppm).
- Minimum data rate: 1.5404 Mbit/s (less than 1.544 Mbit/s-20 ppm). The nominal stuffing ratio is 33.46 % of stuffed frames (if DS2 at nominal data rate).

1.5.2.2.2.2 DS1 nominal stuffing value if C-bit parity mode used between DS2 and DS3 level

The per-DS1 in a DS2 signal (6.306 Mbit/s) data rate limits are:

- Maximum data rate: 1.5444 Mbit/s (more than 1.544 Mbit/s ± 20 ppm).
- Minimum data rate: 1.5390Mbit/s(less than 1.544 Mbit/s-20 ppm).

The nominal stuffing ratio is 7.41% of stuffed frames.

1.5.3 OH Insertion

During the muxing process the M12 MUX also inserts X, F, M and C bits.

1.5.4 Per DS1 Payload Loopback

The M12 multiplex should loopback the DS1 signal if it detects that Ci3 bit is the inverse of Ci1 and Ci2 bits (i defines the concerned DS1). It is necessary to repeat this information at least 10 times.

More information on the Loopback modes are provided in the Loopback section of the data sheet.

M1 Sub-Frame	F2	Stuff Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	• • •	Info Bit 48
M2 Sub-Frame	F2	Info Bit 1	Stuff Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	• • •	Info Bit 48
M3 Sub-Frame	F2	Info Bit 1	Info Bit 2	Stuff Bit 3	Info Bit 4	Info Bit 5	• • •	Info Bit 48
M4 Sub-Frame	F2	Info Bit 1	Info Bit 2	Info Bit 3	Stuff Bit 4	Info Bit 5	• • •	Info Bit 48

6143 drw20a

Figure 14 DS2 Stuff Block

Internal Data Link Transmitter:

The Transmitter Data Link Configuration Register and the Transmit Data Link Control Register are the two main registers used for controlling the Transmit Data Link function in the M13. After reser, XFDL is disabled because the EN bit in the TSB Configuration Register will be 0. The INTE bit, also in the XFDL TSB Configuration Register, should be set so that the TDLINT output is masked.

When a frame is ready to be transmitted, the XFDL TSB should be configured accordingly. If the CCITT-CRC frame check sequence is desired this should be enabled. Then the INTE bit should be enabled (if in the interrupt driver mode), and then finally the EN bit is set to 1 enable the overall operation of the XFDL.

The XFDL can be run in three different modes: polled, interrupt driven, and DMA-controlled. In the polled mode, the TDLINT and TDLUDR output of the XFDL are unused and the microprocessor must periodically poll (read) the XFDL Status Register to determine when to write the next byte to the Transmit Data FIFO. In the interrupt driven mode, the microprocessor will use the TDLINT pin as an interrupt pin to determine when the Transmit Data FIFO is ready for the next data byte. In the DMA controlled mode the TDLINT output acts as a DMA request to the DMA controller while DMA end signal feeds the TDLEOMI of the M13. In an under run condition the TDLUDR drives an interrupt on the controlling microprocessor.

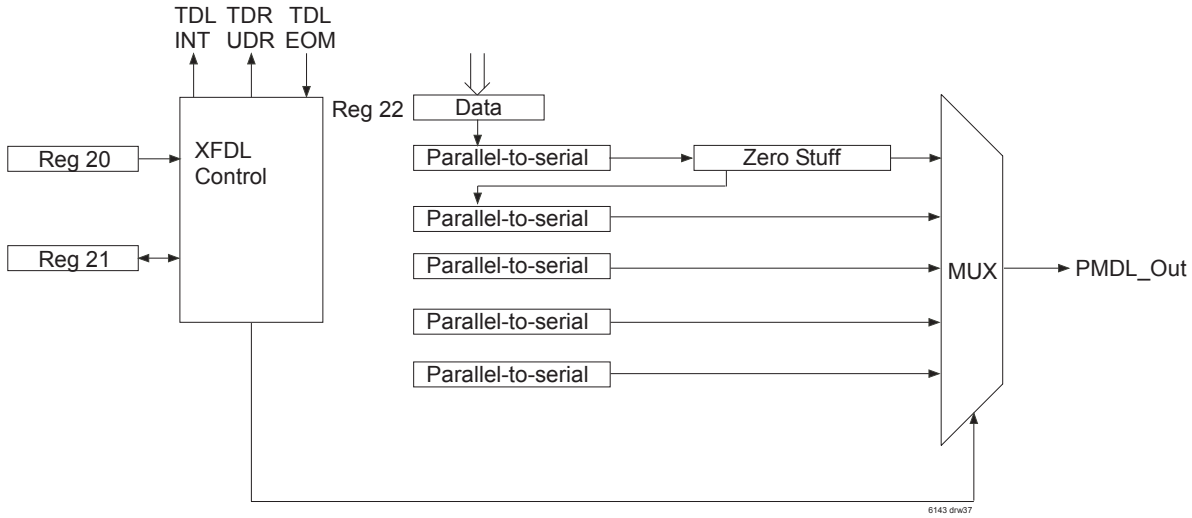


Figure 15. XFDL

Polled Mode:

In the polled mode the controlling microprocessor will periodically initiate a service routine to complete the following.

1) Read the XFDL Status Reg.
2) If UDR = 1 clear the Status register by setting UDR = 0, de-asserting TDLEOMI input pin and clearing EOM. Restart the current frame.
3) If INTR = 1 then
   a) Write next data byte to XFDL TSB Data Reg.
   b) Set EOM = 1 and INTE = 0 or assert TDLEOMI input pin.
4) Repeat steps 1 an 2 to confirm no underrun occurred during step 3.

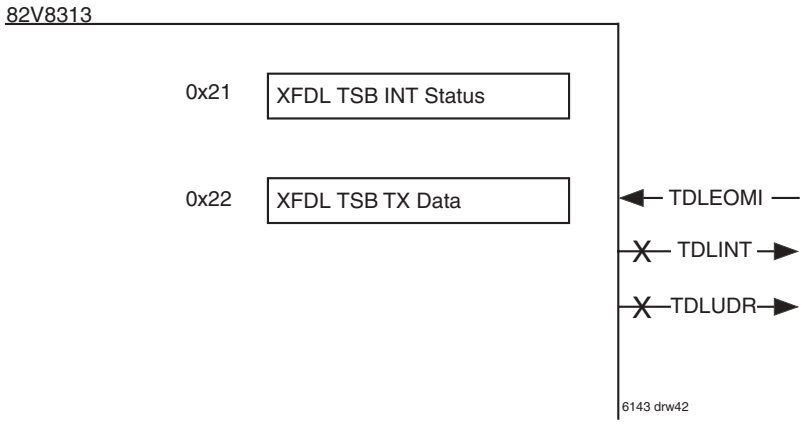


Figure 16. XFDL Polled Mode

Interrupt Driven Mode:

In the interrupt driven mode the microprocessor will service the M13 when the XFDL is ready to accept another byte or when an underrun condition occurs. The ISR will be the same as described above.

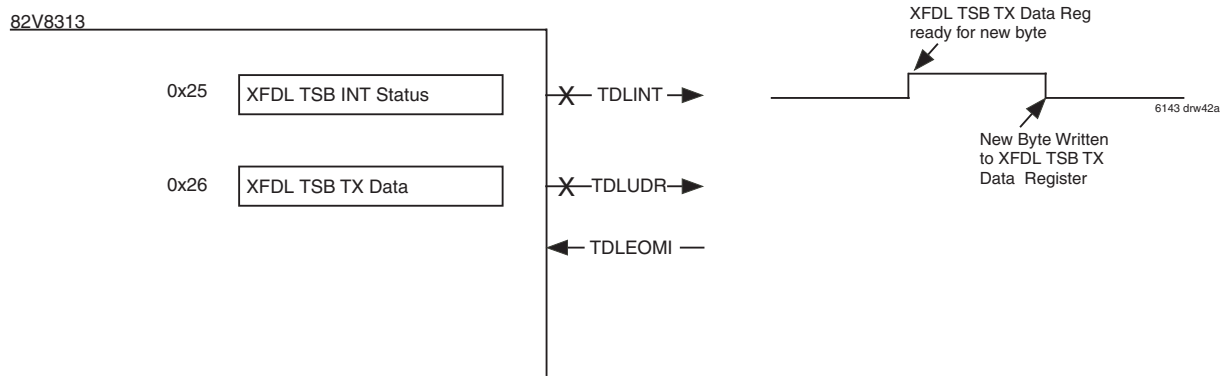


Figure 17. XFDL Interrupt Mode

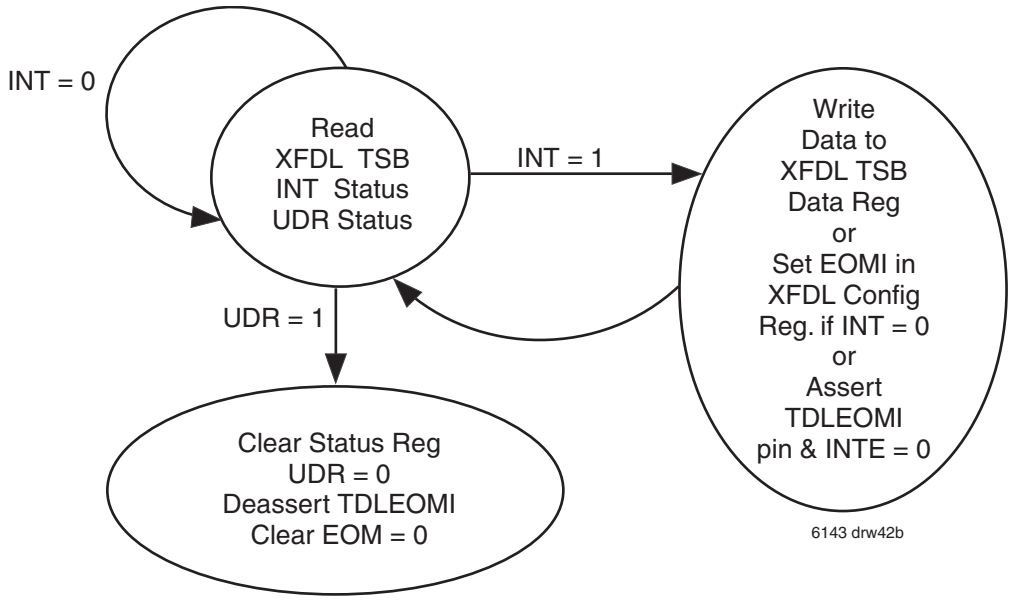


Figure 18. XFDL Interrupt Service Routine

DMA Mode:

When a DMA controller is used with the XFDL, the TDLINT will initiate a DMA request and consequently the DMA controller will send a byte to the M13. For each assertion of the TDLINT the DMA controller should send a byte. Once the last byte is sent from the DMA controller to the M13, to finish the request, the DMA controller should assert the TDLEOMI When the DMA controller sets TDLEOMI high, the EOM bit in the XFDL Configuration register will be set to complete the transaction. If an underrun condition occurs the TDLUDR will interrupt the microprocessor and will stop DMA controller, clear the condition, reset any necessary data pointers, and restart the DMA to resend the data frame.

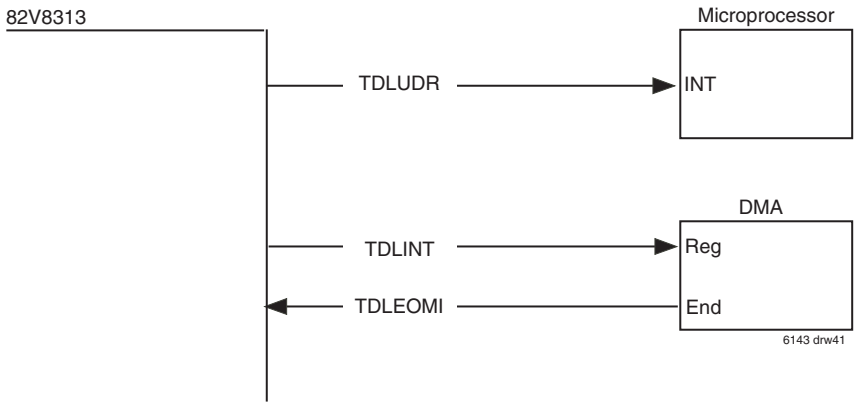


Figure 19. XFDL DMA Mode

XFDL Normal Data Sequence:

This example shows a normal XFDL interrupt driven sequence with the CRC enabled. In order to begin the sequence the microprocessor must first set the INTE bit in the XFDL Configuration/Control Register to enable the TDLINT interrupt. Once the interrupt is enabled the M13 will assert the TDLINT to interrupt the microprocessor. The interrupt routine described above will cause the microprocessor to write the first data byte of the frame to the transmit FIFO. Once the byte is written to the FIFO, the TDLINT will de-assert. When the XFDL begins to transmit the first byte, TDLINT will assert again to signal that it is ready for the next byte in the frame. Again the microprocessor will enter the XFDL ISR and load the data byte in to the FIFO. Again the TDLINT will de-assert when it begins to transmit that data byte. This process continues until the last byte of the frame. Once the last data byte begins to transmit, the TDLINT will be asserted, as normal. Since all of the data has been written to the FIFO the ISR should set the EOM bit (or assert the TDLEMI pin) to end the frame. Also, the INTE bit should be set to 0 so that the TDLINT interrupt is disabled and the CRC bytes and the closing flag are transmitted. When new data for the next frame is ready, the TDLINT can be re-enabled by setting the INTE bit to 1, and thus beginning the sequence over again.

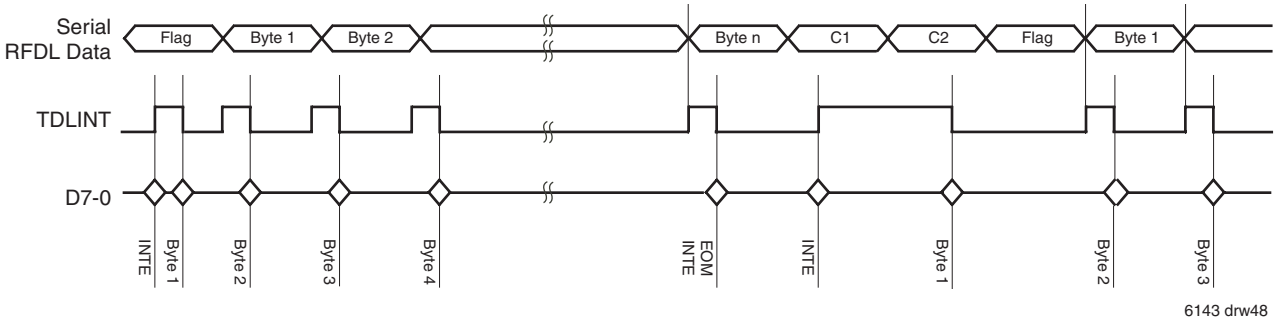


Figure 20. XFDL Normal Data Sequence

XFDL Underrun Sequence:

This example is also an interrupt driven example, but shows the XFDL inputs and outputs during and underrun error. Similar to the last example, the microprocessor begins by setting the INTE bit in the Configuration/Control Register to 1 thus enabling TDLINT interrupts. The TDLINT is asserted and the microprocessor enters the interrupt routine to write the first data byte to the transmit FIFO. Once the byte is written to the FIFO, the TDLINT is de-asserted. As with the previous example, once the XFDL begins to transmit the data, the TDLINT will be asserted to start the next ISR transmit data write sequence. When D3 begins to transmit the TDLINT is asserted and the interrupt routine should be started. For some reason, the routine was not able to write to the transmit FIFO within five rising clock edges, so the Transmit Data Link Underrun pin, TDLUDR, is asserted. Once the TDLUDR is asserted, an abort followed by a flag is automatically sent out on the data link. The XFDL is stopped, the UDR bit is set, and the M13 must be serviced by the microprocessor. The UDR bit should be cleared and the INTE bit should be set to 0. Once this is done, the frame can be restarted again by setting the INTE bit to 1.

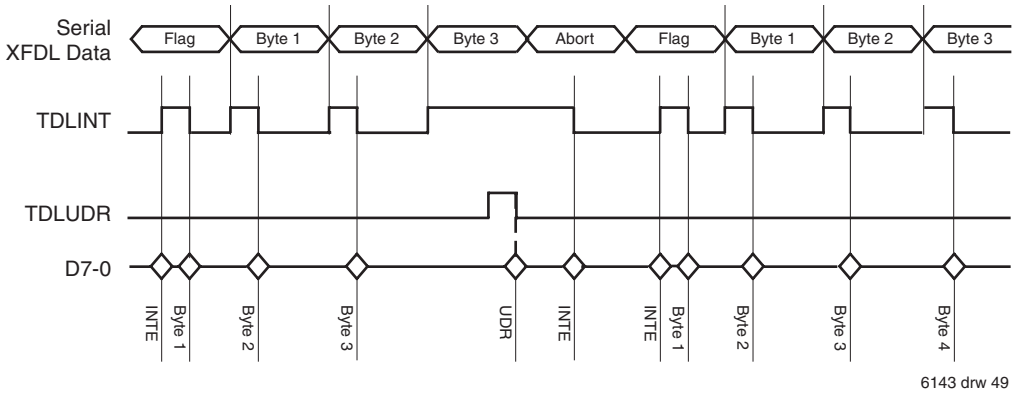


Figure 21. XFDL Underrun Sequence

TDLINT Timing Normal Data Transmission:

This figure shows the timing requirements for the microprocessor to adequately service the transmit data link FIFO. Each byte of the packet must be written within 110µSec of the rising edge of the TDLINT without causing an underrun. The time from rising edge to rising edge of TDLINT is a result of the variation in time to transmit the data link byte over the 3 C-bits of the 5th M-subframe over multiple M-frames, and for the M13 to latch in the next byte. As shown above, the third byte write to the XFDL FIFO is missed and thus the TDLUDR goes high when it was supposed to transmit that third byte.

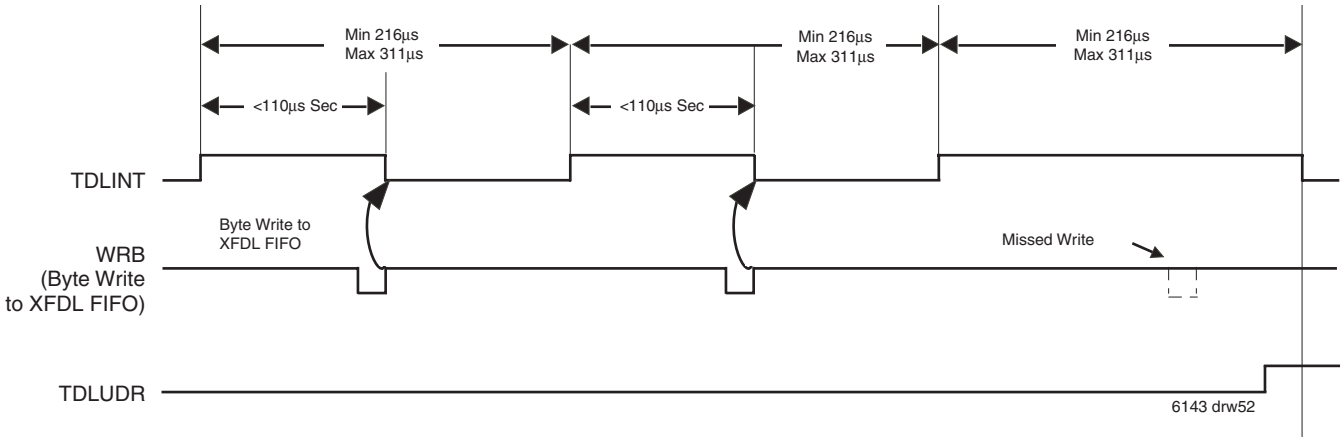


Figure 22. TDLINT Timing Normal Data TX

TDLEOMI Timing:

The Transmit Data Link End Of Message Indicator, TDLEMOI, is used to indicate to the XFDL block that the last byte of the frame has been written to the XFDL Transmit Data Register. When TDLEOMI has been asserted, the XFDL will insert the FCS, if enabled, and flags (“01111110”) after the last byte has been transmitted. To aid designers, the M13 can accept a wide range of timing for the TDLEOMI. The above diagram will help illustrate this broad range. At the earliest, the TDLEOMI can be asserted synchronously with the falling edge of the write strobe that is used to write the last data byte to the XFDL Transmit FIFO. At the latest, TDLEOMI must be asserted before the next rising edge of TDLINT, when the XFDL would expect the next data byte to be written to the XFDL Transmit FIFO (210µSec). For de-assertion a similar logic applies and the earliest TDLEOMI can be de-asserted would be just after the rising edge of the TDLINT that registered the TDLEOMI. At the latest, TDLEOMI must be de-asserted before the write of the first byte of the nest frame. If TDLEOMI is still high when TDLINT goes high, that byte will be considered that last byte and thus the CRC bytes and flag bytes will automatically be transmitted on the data link

In the above diagram, TDLEMOI is shown going high synchronously with the write strobe but can be asserted any time up to 210µSec after the rising edge of TDLINT. TDLEMOI is de-asserted before the end of the second CRC byte (or before the flag transmission). In this example TDLINT is still active and remains high while waiting for the first byte of the next frame to be written to the XFDL Transmit FIFO. In this example, it is important to note that the TDLUDR is not asserted. In this situations, no underrun can occur since it is the first byte of the frame. However, once the first byte is written, the XFDL FIFO must be serviced regularly to prevent an underrun condition. As noted previously, TDLEOMI must be glitch free. If TDLEMOI is not used, it can be tied to ground or held low. In this case, the EOM bit can be used and the same restrictions that apply to the TDLEOMI apply to the EOM bit. It is strongly recommended that the interrupt routine described in this data sheet be used.

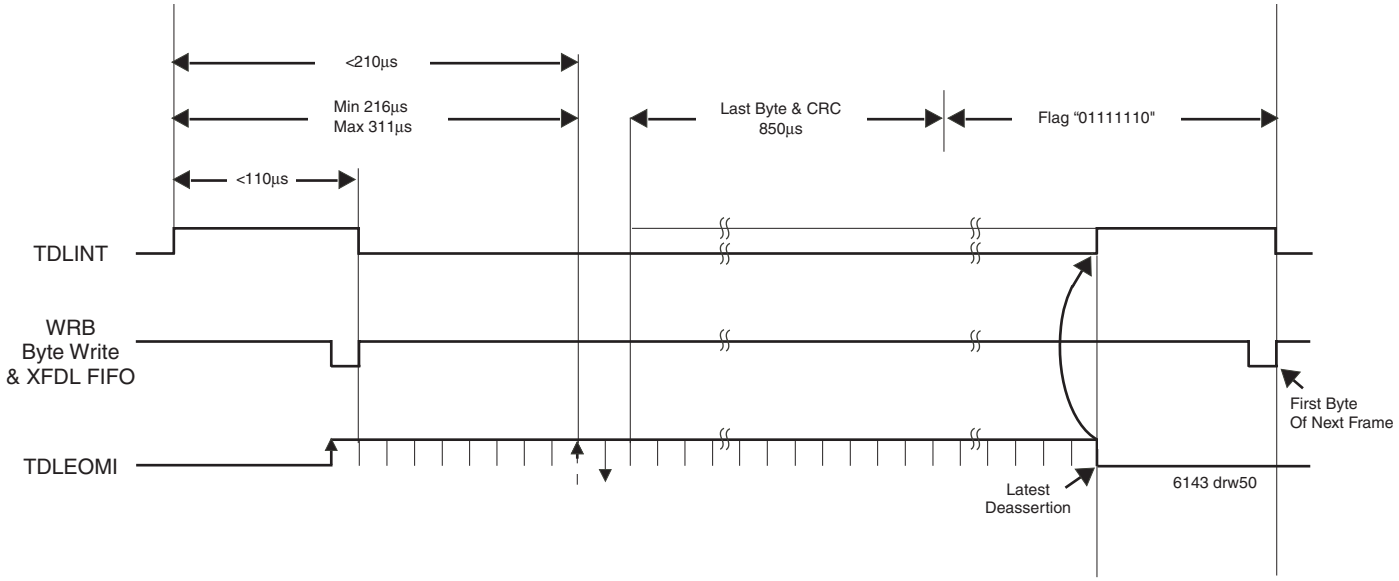


Figure 23. TDLEOMI Timing EOMI After CRC

Internal Data Link Receiver:

Like the data link transmitter, the Data Link Receiver should be disabled at start up by setting the EN bit in the RFDL Configuration Register. Before initiating the RFDL, the FIFO depth for generating an interrupt should be set by writing to the RFDL Interrupt Control/Status register.

By setting the EN bit in the Configuration Register to 1, the RFDL will be enabled and assumes the link will be idle (all ones). Immediately after enabling the RFDL however, the RDFL will begin searching for flags. When the first flag is found, an interrupt will be generated and the data byte found before the flag will be written to the FIFO. When an interrupt is generated the RFDL control block guarantees that the FLG and EOM bits will also be written to the status register reflect the current state. After the interrupt is generated the data should be read out and EOM should be logic 1 and the FLG bit logic 1. It is important to note that after the RFDL is enabled (EN = 1 or TR = 1) the RFDL will generate an interrupt to indicate the status of the link. As a result, the first data byte read should be discarded. The M13 is designed as a passive RFDL, any link state in the form of BOC, IDL, active flags, or other indications should be handled by the controlling microprocessor.

Much like the XFDL, the RFDL can be run in a polled, interrupt driven, or DMA controlled mode. In the polled mode the RDLINT and RDLEOM outputs are not used and the microprocessor must periodically read (poll) the Status register to determine when to read the data. In the Interrupt driven mode the M13 will generate an interrupt via RDLINT pin to indicate to the microprocessor that data is ready to be read. In the DMA controlled mode the RDLINT and RDLEOM are used as a hardware handshake to initiate, indicate and terminate the DMA.

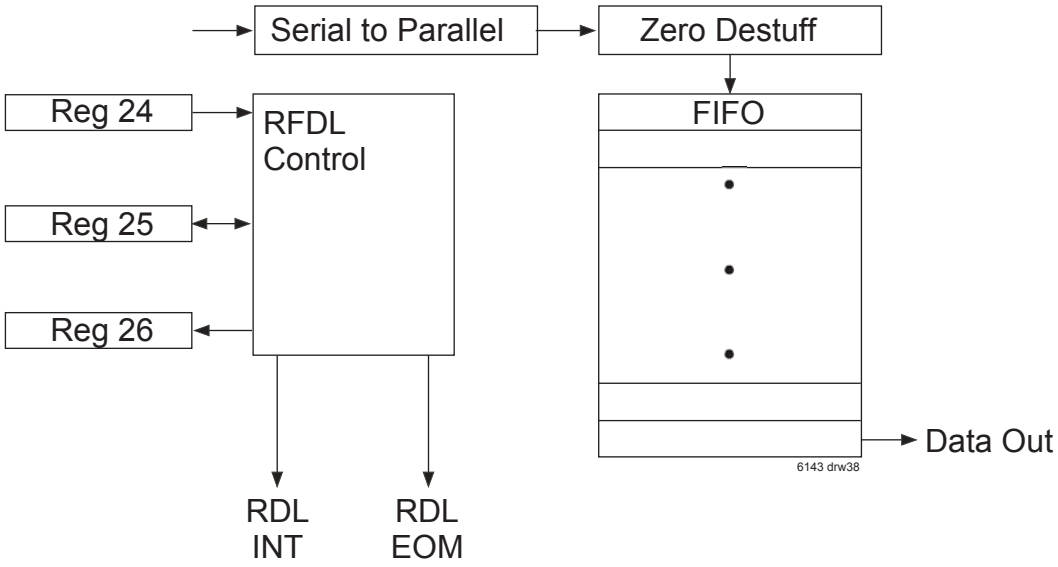


Figure 24. RFDL

Polled Mode:

In the polled mode the controlling microprocessor will periodically initiate a service routine and complete the following:

1) Read the RFDL Data Register

2) Read the RFDL Status Register

3) If the FIFO has underrun (0x00) then discard byte and wait for the next period/interrupt.

4) If the FIFO has overflowed (OVR = 1) then discard the last frame and wait for the next period/interrupt.

5) If FLG = 0 (i.e. abort) and the link was active discard the byte and wait for the next period/interrupt.

6) If FLG = 1 and the link was inactive, then set the link to active, discard the byte and wait for the next period/interrupt.

7) Save the byte.

8) If EOMR = 1, then check the CRC, NVB and process the frame

9) If FE = 0, then go to step 1, else wait for next period/interrupt.

Steps 1 and 2 may be reserved to avoid reading the Data Register unneccessarily.

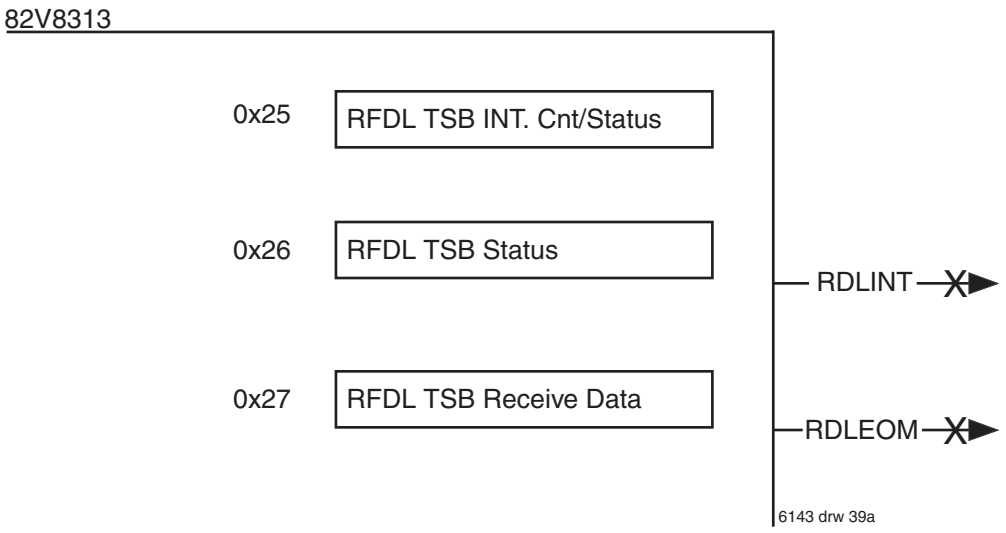


Figure 25. RFDL Polled Mode

Interrupt Driven Mode:

In the interrupt driven mode the microprocessor will service the M13 when the RFDL indicates when a data byte is ready or when an error condition occurs. The ISR will be the same as with the polled condition described above. The above flow (Steps 5 and 6) assumes that the link state is stored as a local variable. This is done to determine if the link state inactive, receiving all ones or BOC which contains all ones sequences, or active and thus receiving data and flags.

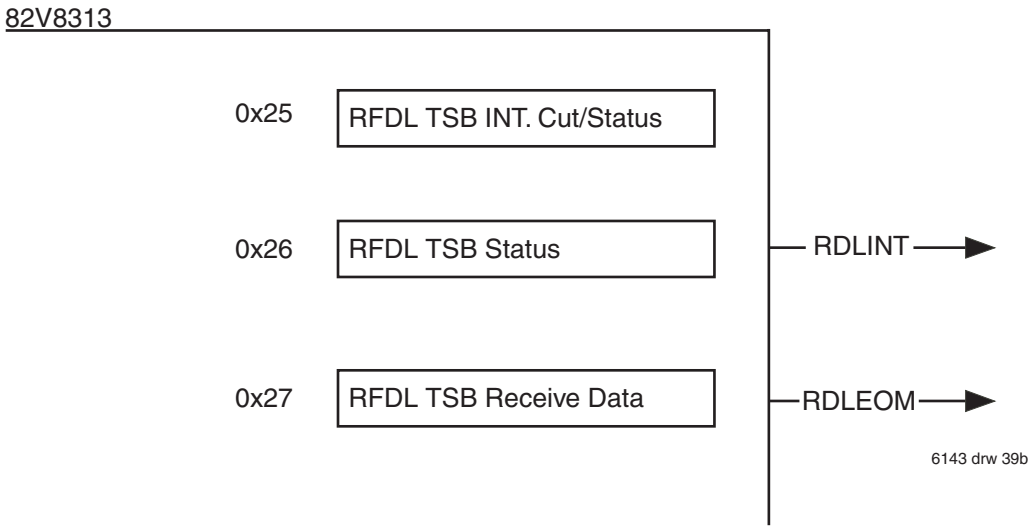


Figure 26. RFDL Interrupt Driven Mode

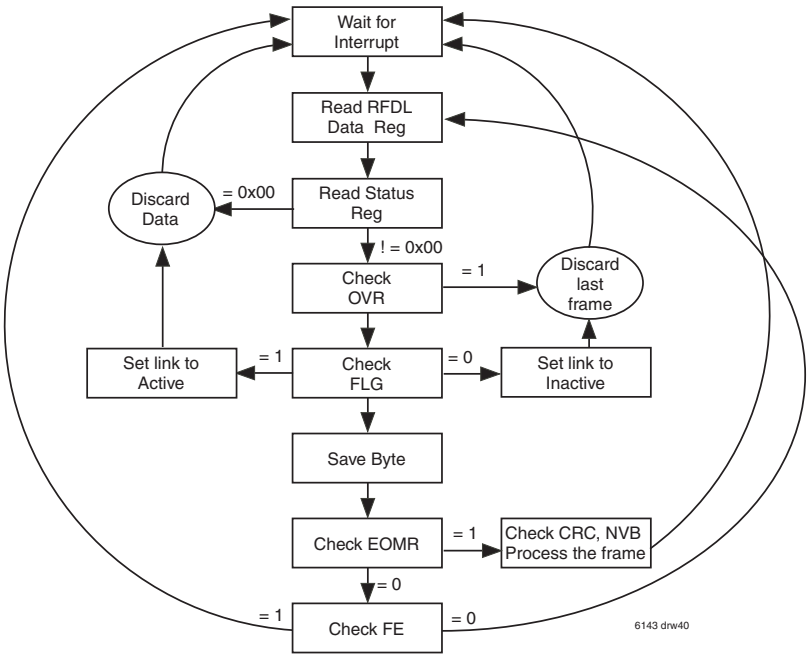


Figure 27. RFDL Interrupt Service Routine

DMA Mode:

The RFDL can also be used with a DMA controller. In this case the RDLEOM of the M13 is connected to the interrupt pin of the micro-controller. The RDLEOM is also routed to a gate, with the RDLINT, which will inhibit a DMA request if the RDLEOM output is high. In this way, if the RDLEOM is low, the RDLINT will control DMA requests. When the DMA controller reads the last byte (EOM or abort) or an overrun condition occurs the RDLEOM output goes high the DMA controller will be inhibited from reading more bytes and the processor is interrupted. When the processor takes over, the DMA can be halted and readied for the subsequent frame, and the frame processing initiated.

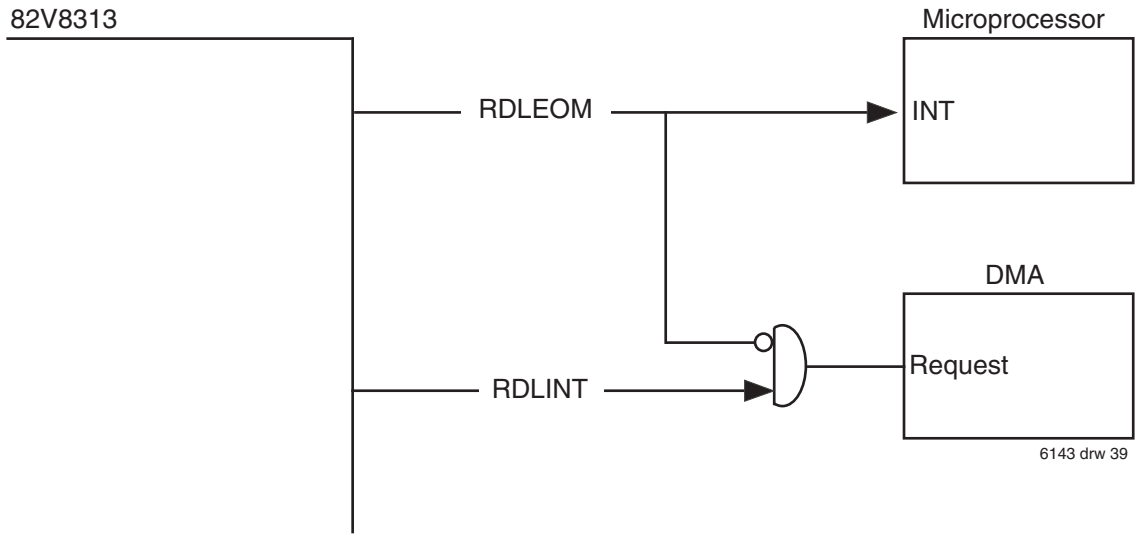


Figure 28. RFDL DMA Mode

RFDL Normal Data and Abort Sequence:

The above diagram shows the relationship between the incoming and extracted data link data and the RDLINT, RDLEOM, and microprocessor bus. To simplify the examples each microprocessor access is a composition of multiple accesses following the recommended handling sequence, where each incoming data byte of the farme is “handled” (read) in turn. As can be seen there is a short delay from the incoming data to RDLINT going high. It can also be seen that RDLINT will both be de-asserted until the microprocessor reads the data byte from the RFDL Data Register. The assert/de-assert sequence is followed through the entire farme until Byte (n-2) when multiple bytes exist in the buffer. In this case it can be seen that the RDLINT is not de-asserted. At the end of an interrupt sequence the controlling microprocessor should realize that the interrupt has not been completely cleared and thus re-enter the ISR. At Byte (n-1) the interrupt is cleared and the RDLINT is de-asserted. In a data link frame, it is not necessary to have an integral number bytes. In the above example, this is one of those cases. The “R” represents the non-integral bits that remain at the end of the frame. The internal RFDL block will take in the remainder and the CRC and also register those into the RFDL Data Register. In this example B1 will contain the remainder of the farme data and the first part of the first byte of CRC data. B2 will contain the second part of the first byte of the CRC data plus the first part of the second byte of the CRC data. And finally, B3 will contain only the second part of the second byte of the CRC data. When the status register is read for B3, the EOM bit in the RFDL Status Register will also be set to indicate the end of the current frame (End of Message --EOM). The RFDL block parses data on byte boundaries until the RFDL receives the end flag. The RFDL block will indicate the size of the remainder by setting the NVB (Number of Vaild Bits) in the RFDL TSB Status register (0x26). The NVB information can be used by controlling microprocessor to properly parse, check, and handle the data.

In the above example, after B3 is read a new frame is started. Shortly after it starts, it is aborted. The microprocessor first reads Byte 1 and then reads the B1 byte. When B1 is read the Status Register will indicate FLG bit and EOM bit meaning all bytes up to the abort should be read.

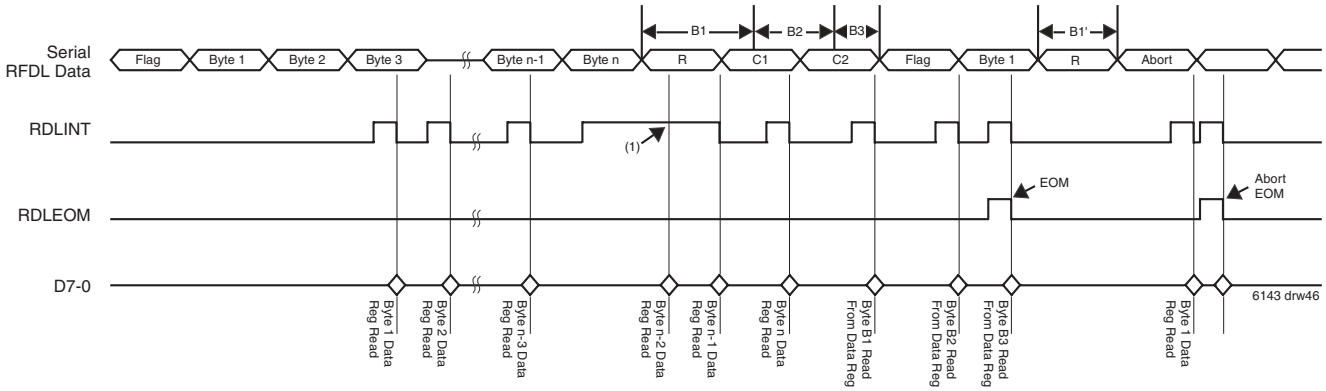


Figure 29. RFDL Normal Data And Abort Sequence

FUNCTIONAL TIMING:

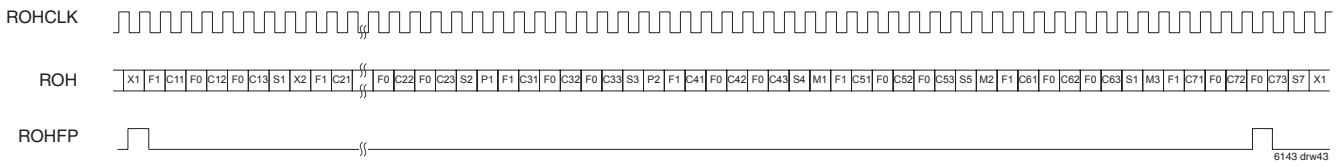


Figure 30. Receive DS3 OH Serial Stream

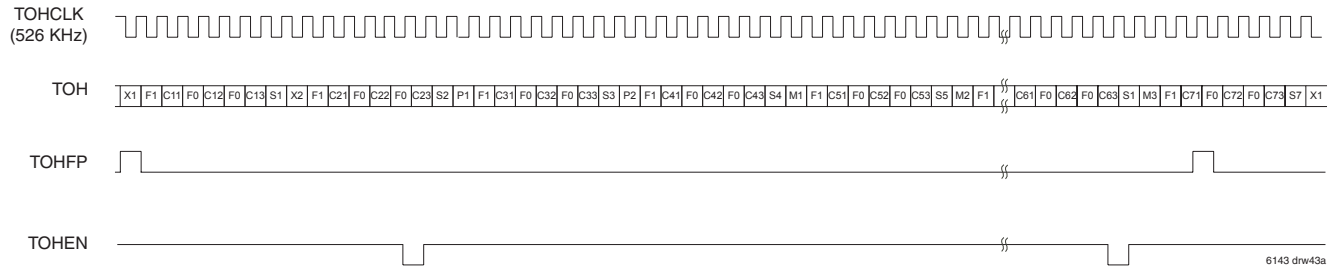


Figure 31. Transmit DS3 OH Serial Stream

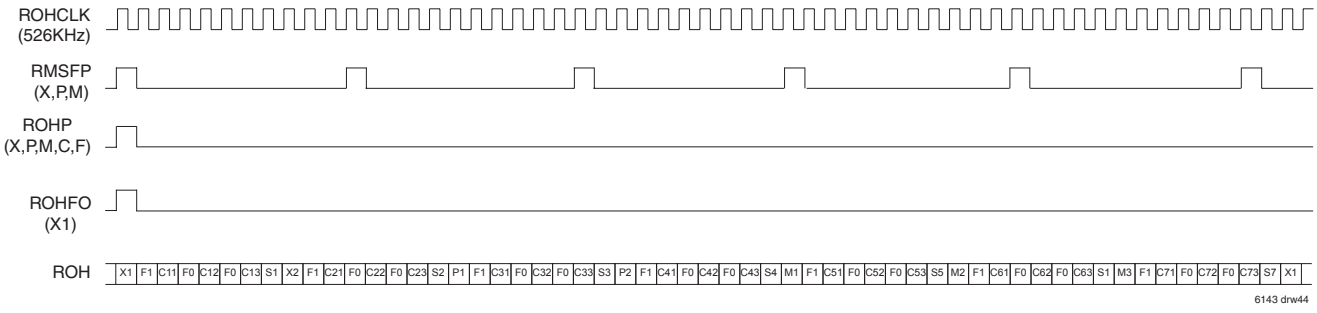


Figure 32. Functional Receive OH Timing Low Speed

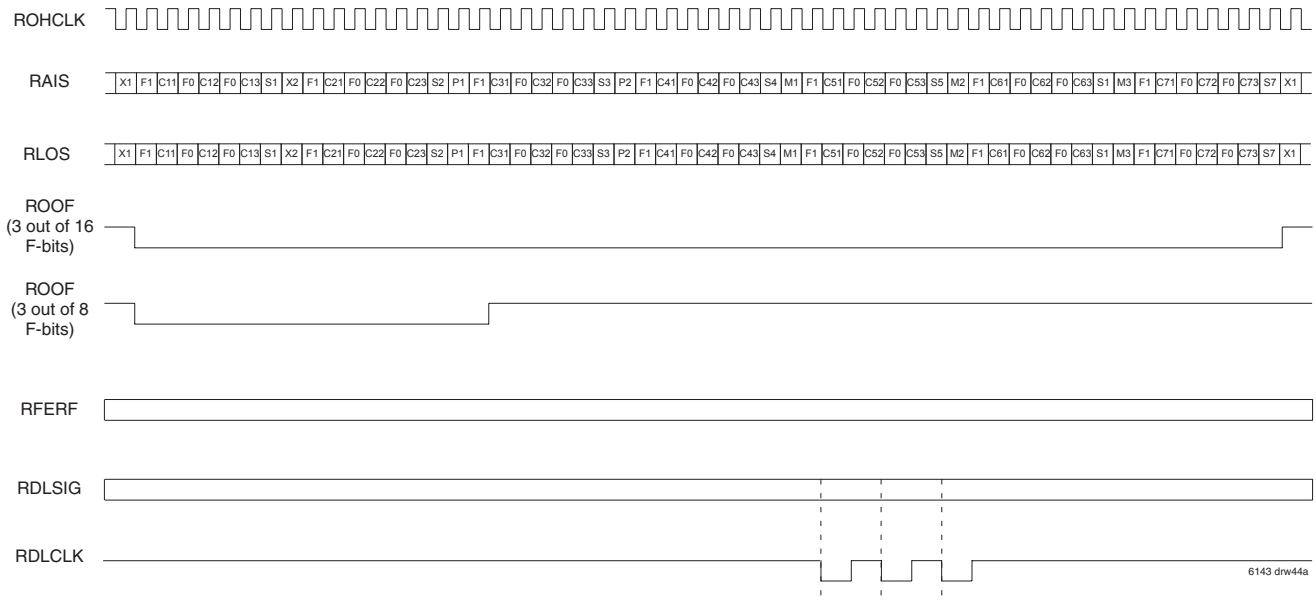


Figure 33. Functional Receive Timing PMON

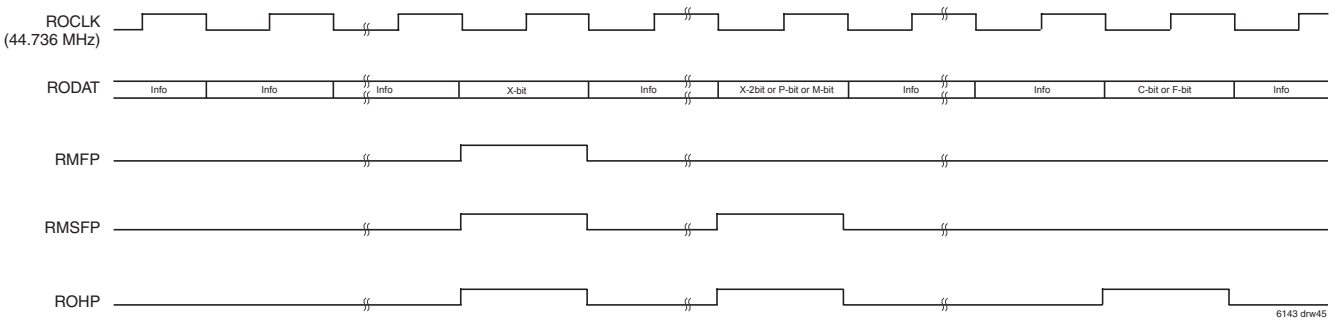


Figure 34. Functional Receive OH Timing High-Speed

Loopback Modes:

DS3 Diagnostic Loopback

For a DS3 Diagnostic Loopback, the transmitted DS3 stream will be looped back into the DS3 receive path and as a result the incoming DS3 will be ignored. As a result of the incoming DS3 being ignored, the receive path will use the transmit clock instead of the RPOS./RDAT and RNEG/RLCV.

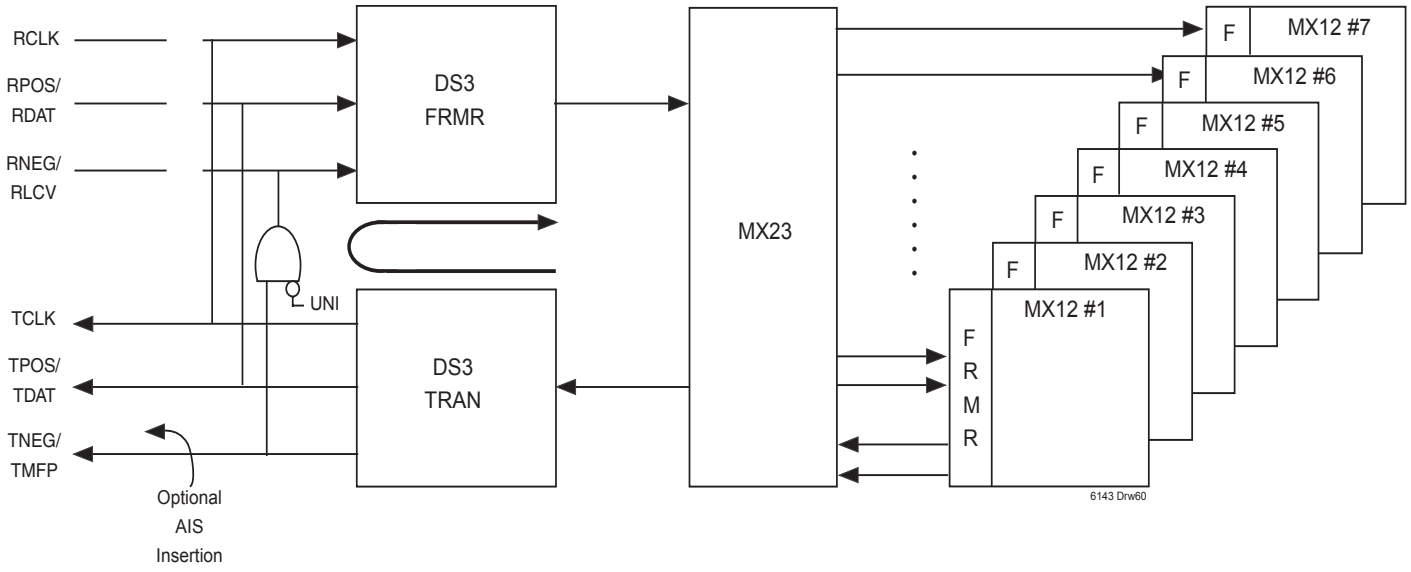


Figure 35. DS3 Diagnostic Loopback

DS3 Line Loopback

For a DS3 Line Loopback, the received DS3 stream will be looped back into the DS3 transmit path and as a result the internally generated DS3 will be ignored. Similar to the DS3 Diagnostic Loopback the transmit clock will be substituted with the receive clock.

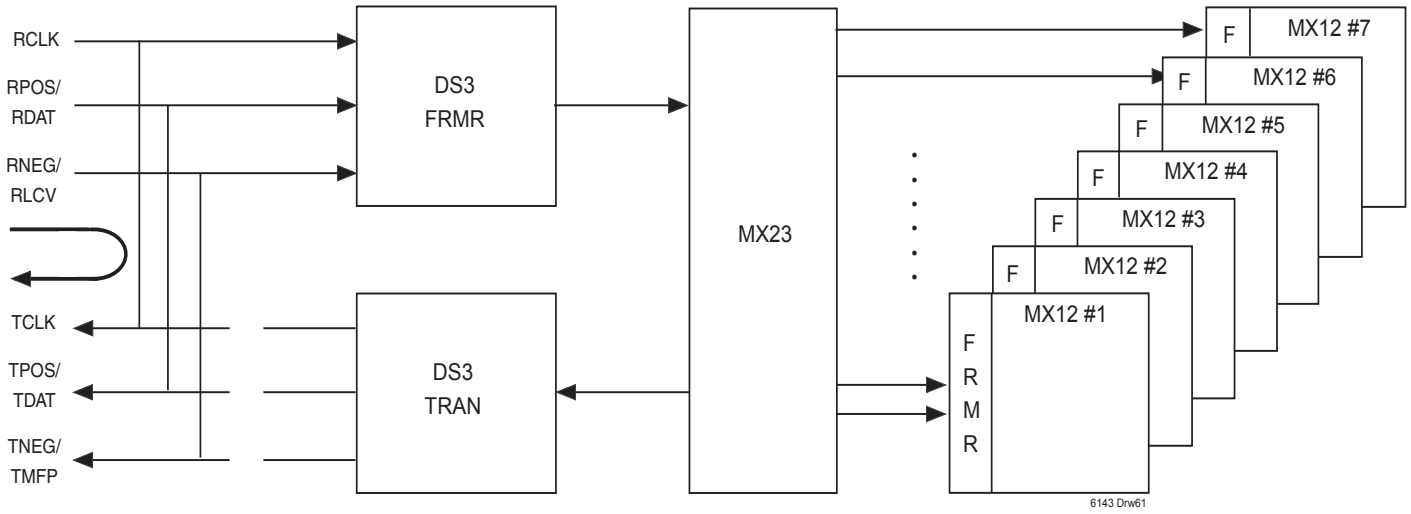


Figure 36. DS3 Line Loopback

DS2/G.747 Demultiplex Loopback

For a DS2/G.747 Demultiples Loopback individual DS2 or G.747 streams can be looped from the receive DS3 stream and be placed back on the transmit DS3 stream. As might be expected, the internally generated DS2 or G.747 DS2 will be ignored.

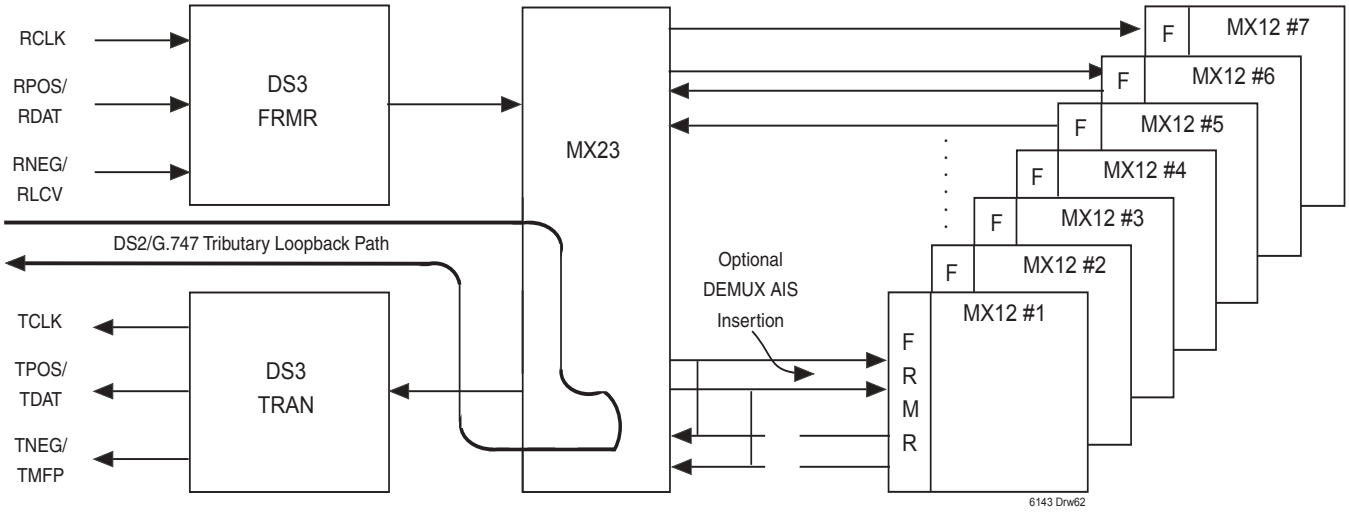


Figure 37. DS2 / G.747 Demultiplex Loopback

DS1/E1 Demultiplex Loopback

For a DS1/EI Demultiplex Loopback individual DS1 or E1 streams can be looped from the received DS3 stream and be placed back on the transmit DS3 stream. As with the DS2/G.747 Demultiplex loopback the corresponding incoming DS1 or E1 stream will be ignored.

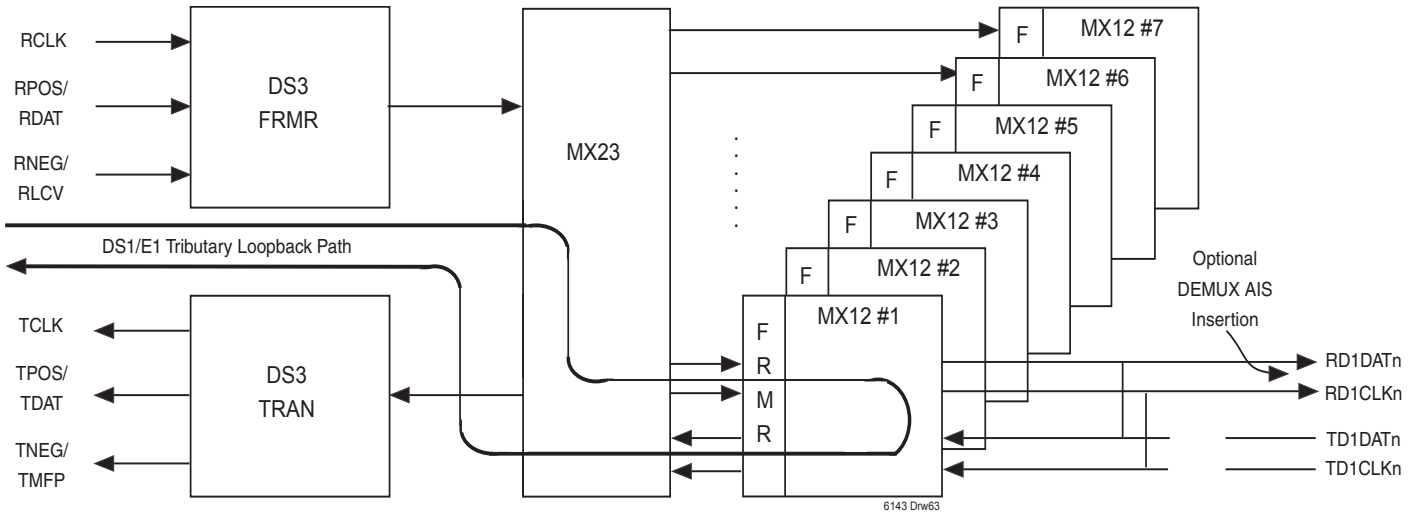


Figure 38. DS1/E1 Demultiplex Loopback6+

DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage	-0.5	+4.0	V
V_I	Voltage on Digital Inputs	GND -0.3	Vcc +0.3	V
Io	Current at Digital Outputs	-50	50	mA
Ts	Storage Temperature	-55	+125	°C
P_D	Package Power Dissipation	—	2	W

RECOMMENDED OPERATING CONDITIONS(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Positive Supply	3.0	3.3	3.6	V
V_{IH}(1)	Input HIGH Voltage	2.0	—	Vcc	V
V_{IL}	Input LOW Voltage	-0.3	—	0.8	V
T_{OP}	Operating Temperature Industrial	-40	25	+85	°C

Notes:

1. Inputs/Outputs are 5V tolerant.
2. Voltages are with respect to ground (GND) unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{CC}(1)	Supply Current	—	—	185	mA
I_{IL}(3.4)	Input Leakage (input pins)	-10	—	60	µA
I_{BL}(3.4)	Input Leakage (I/O pins)	-10		60	µA
I_{OZ}(3,4)	High-Impedance Leakage	—	—	60	µA
V_{OH}(5)	Output HIGH Voltage	2.4	—	—	V
V_{OL}(6)	Output LOW Voltage	—	—	0.4	V

Note:

1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Outputs unloaded.
3. $0 \leq V \leq Vcc$
4. Maximum leakage on pins (output or I/O in High-Impedance state) is over an applied voltage (V).
5. IOH = 10 mA
6. IOL = 10 mA

AC ELECTRICAL CHARACTERISTICS

MICROPROCESSOR INTERFACE TIMING CHARACTERICSTICS

MICROPROCESSOR READ ACCESS

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SAR}	Address to Valid Read Set-up Time	20		—	ns
t_{HAR}	Address to Valid Read Hold Time	20		—	ns
t_{SALR}	Address to Latch Set-up Time	20		—	ns
t_{HALR}	Address to Latch Hold Time	20		—	ns
t_{VL}	Valid Latch Pulse Width	20		—	ns
t_{HLR}	Latch to Read Hold	20		—	ns
t_{PRD}	Valid Read to Valid Data Propagation Delay	—		100	ns
t_{ZRD}	Valid Read Deserted to Output Tristate	—		20	ns
t_{PINTH}	Valid Read Deasserted to INTB Tristate	—		50	ns

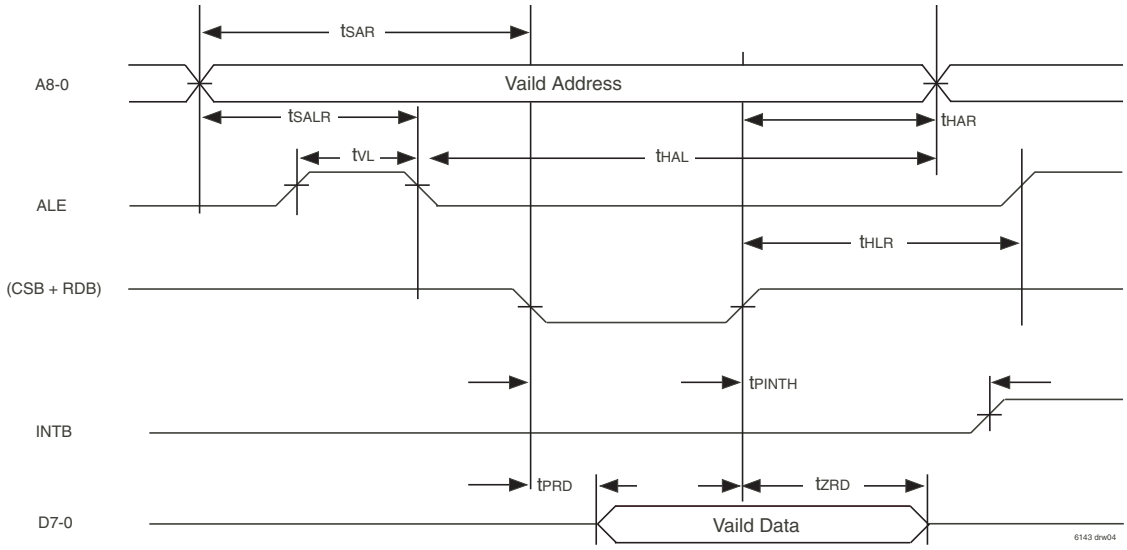


Figure 39 Microprocessor Read Access Timing

Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the microprocessor data bus, (D 7-0).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor timing applies to normal mode register accesses only.
5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
7. In non-multiplexed address/data bus architectures, ALE should be held high, parameters t_{SALR}, t_{HALR}, t_{VL}, t_{HLR} and t_{SLR} are not applicable.
8. Parameters t_{HAR} and t_{SAR} are not applicable of address latching is used.

MICROPROCESSOR WRITE ACCESS

Symbol	Parameter	Min.	Max.	Unit
t_{SAW}	Address to Valid Write Set-up Time	25	—	ns
t_{SDW}	Data to Valid Write Set-up Time	20	—	ns
t_{SALW}	Address to Latch Set-up Time	20	—	ns
t_{HALW}	Address to Latch Hold Time	20	—	ns
t_{VL}	Valid Latch Pulse Width	20	—	ns
t_{SLW}	Latch to Write Set-up	0	—	ns
t_{HLW}	Latch to Write Hold	20	—	ns
t_{HDW}	Data to Valid Write Hold Time	20	—	ns
t_{HAW}	Address Valid Write Hold Time	20	—	ns
t_{VWR}	Valid Write Pulse Width	40	—	ns

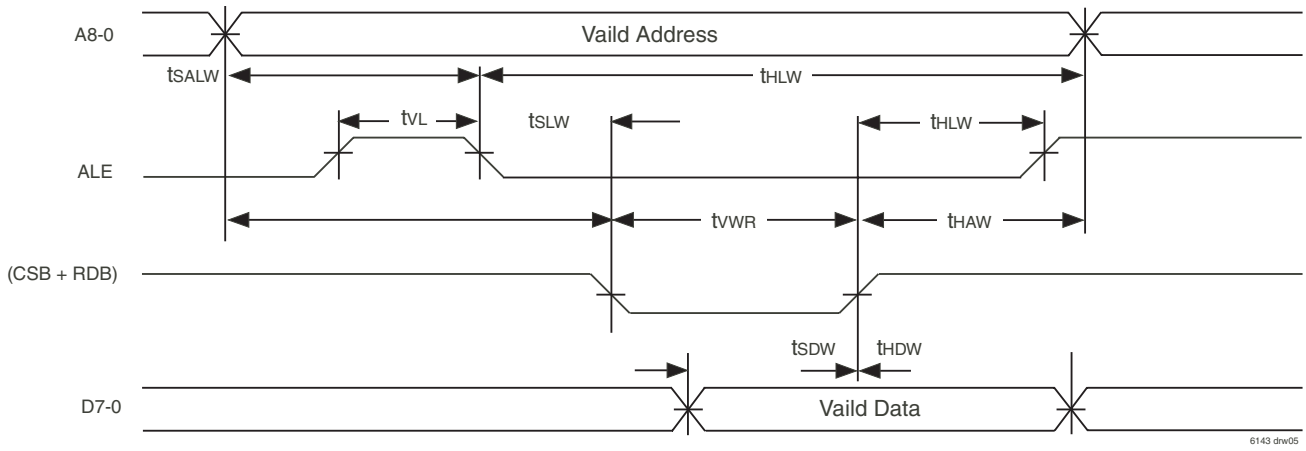


Figure 40 Microprocessor Write Access Timing

Notes on Microprocessor Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WDB signals.
2. Microprocessor timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters t_{SALW}, t_{HALW}, t_{VL}, t_{HLW} and t_{SLW} are not applicable.
4. Parameters t_{HAW} and t_{SAW} are not applicable of address latching is used.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

TIMING CHARACTERISTICS

RECEIVE DS3 INPUT

Symbol	Parameter	Min.	Max.	Unit
	RCLK Frequency (nominally 44.736 MHz)	-20	+20	ppm
	RCLK Duty Cycle	40	60	%
t_{SRPOS}	RPOS/RDAT Set-up Time	4	—	ns
t_{HRPOS}	RPOS/RDAT Hold Time	6	—	ns
t_{SRNEG}	RNEG/RLCV Set-up Time	4	—	ns
t_{HRNEG}	RNEG/RLCV Hold Time	6	—	ns

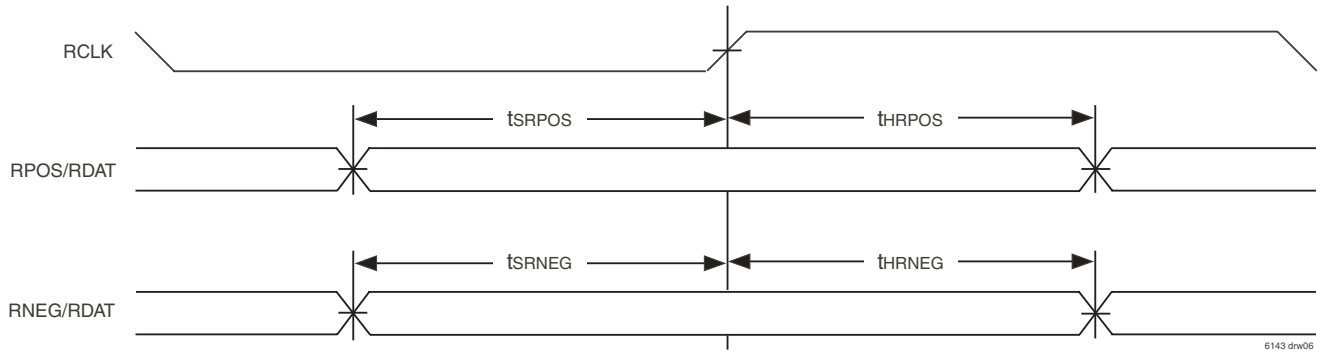


Figure 41 Receive DS3 Input Timing

TRANSMIT DS3 INPUT

Symbol	Parameter	Min.	Max.	Unit
	TICLK Frequency (nominally 44.736 MHz)	20	—	ppm
	TICLK Duty Cycle	20	—	%
t_{STIMFP}	TIMFP Set-up Time	20	—	ns
t_{HTIMFP}	TIMFP Hold Time	20	—	ns

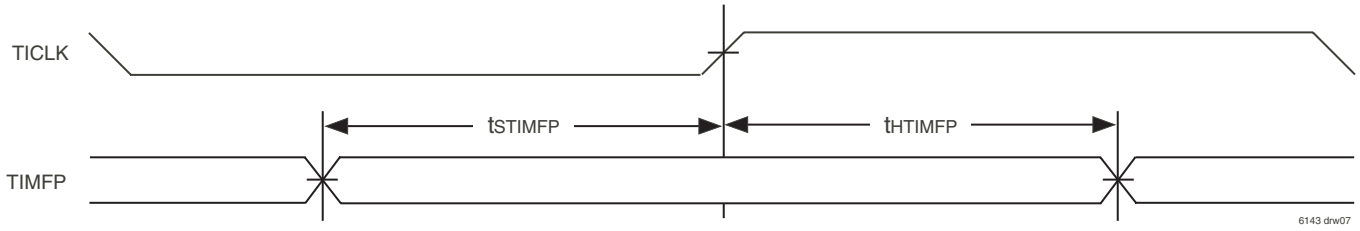


Figure 42 Transmit DS3 Input Timing

TRANSMIT OVERHEAD INPUT

Symbol	Parameter	Min.	Max.	Unit
t_{STOH}	TOH Set-up Time	20	—	ns
t_{HTOH}	TOH Hold Time	20	—	ns
t_{STOHEN}	TOHEN Set-up Time	20	—	ns
t_{HTOHEN}	TOHEN Hold Time	20	—	ns

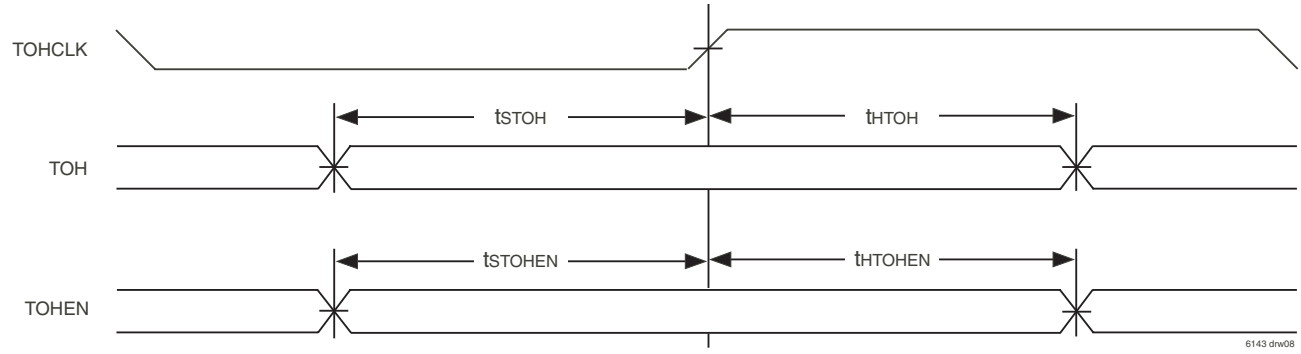


Figure 43 Transmit Overhead Input Timing

TRANSMIT TRIBUTARY INPUT

Symbol	Parameter	Min.	Max.	Unit
	TD1CLKn Frequency (nominally 1.544 MHz, when configured for DS1 rate operation)	-130	+130	ppm
	TD1CLKn Frequency (nominally 2.048 MHz, when configured for E1 rate operation; not applicable for n = 4, 8, 12, 16, 20, 24, 28)	-50	+50	ppm
	TD1CLKn Frequency (nominally 6.312 MHz, when configured for DS2 rate operation; only applicable for n = 4, 8, 12, 16, 20, 24, 28)	-33	+33	ppm
	TD1CLK Duty Cycle (all configurations)	33	67	%
	TD2CLK Frequency (nominally 6.312 MHz)	-33	+33	ppm
	TD2CLK Duty Cycle	33	67	%
$t_{STD1DAT}$	TD1DAT Set-up Time	20	—	ns
$t_{HTD1DAT}$	TD1DAT Hold Time	20	—	ns

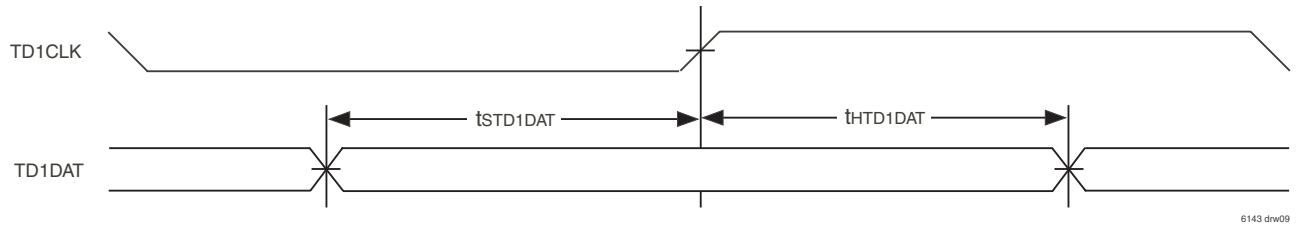


Figure 44 Transmit Tributary Input Timing

TRANSMIT DATA LINK INPUT

Symbol	Parameter	Min.	Max.	Unit
$t_{STDLSIG}$	TDLSIG to TDLCLK Set-up Time	20	—	ns
$t_{HTDLSIG}$	TDLSIG to TDLCLK Hold Time	20	—	ns

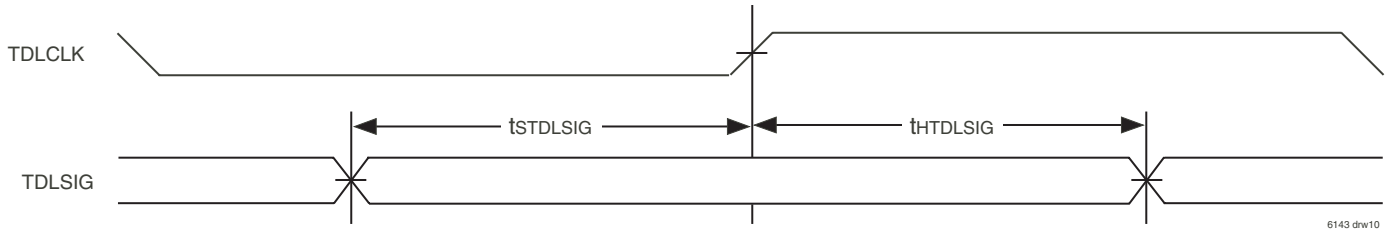


Figure 45 Transmit Data Link Input Timing

TRANSMIT DATA LINK EOM INPUT

Symbol	Parameter	Min.	Max.	Unit
t_{VTEOMI}	TDLEMOI Pulse Width[3]	5	—	ns
$t_{S1TEOMI}$	TDLEMOI Pulse to Falling Edge of WFDL[3] Transmit Data Register Write Set-up Time	0	—	ns
$t_{S2TEOMI}$	TDLEMOI Pulse to Next Falling Edge of XFDL[3] Transmit Data Register Write Set-up Time	0	—	ns
$t_{S3TEOMI}$	TDLEMOI Pulse After TDLINT Assertion[3]	—	210	µs

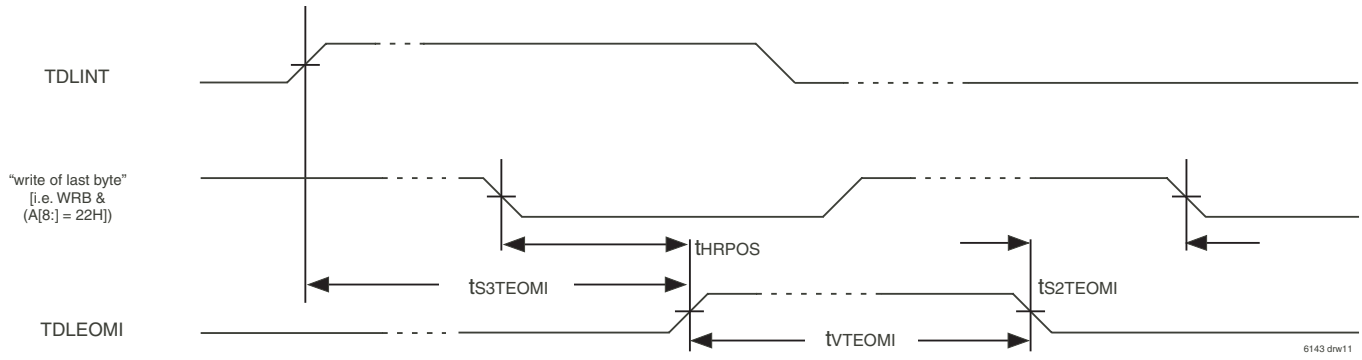


Figure 46 Transmit Data Link EOM Input Timing

Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.
3. TD1CLK frequency, TD2CLK frequency, $t_{S1TEOMI}$, $t_{S2TEOMI}$, $t_{S3TEOMI}$ and t_{VTEOMI} values are guaranteed by design - not measured.

TRANSMIT DS3 OUTPUT

Symbol	Parameter	Min.	Max.	Unit
	TCLK Duty Cycle	TICLK -5	TICLK +5	%
t_{PTPOS}	TCLK Low to TPOS/TDAT Valid Prop. Delay	-2	5	ns
t_{PTNEG}	TCLK Low to TNEG/TMFP Valid Prop. Delay	-2	5	ns

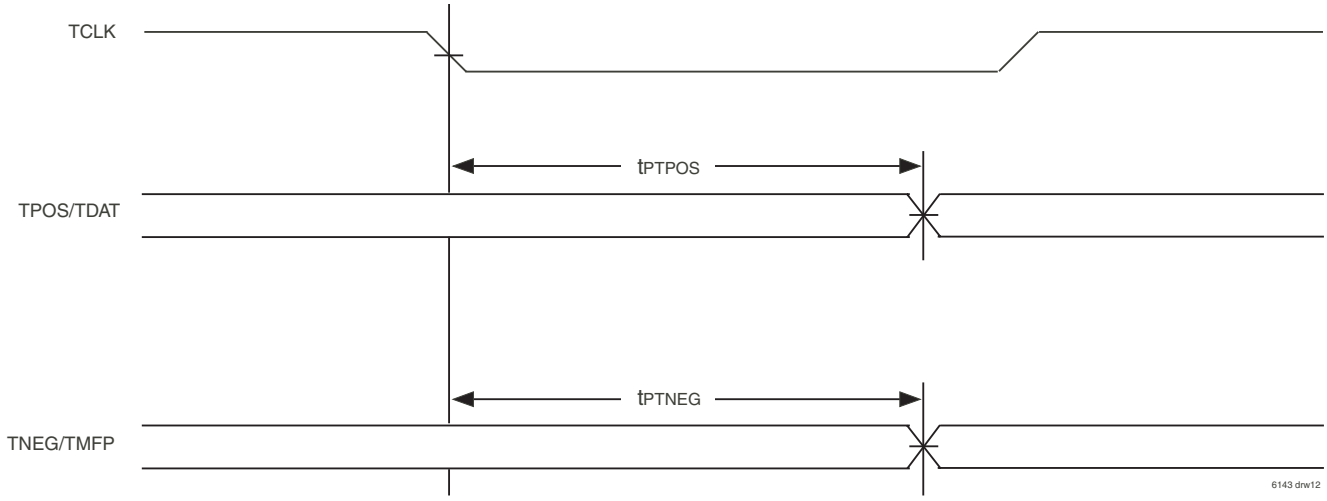


Figure 47 Transmit DS3 Output Timing

RECEIVE DS3 OUTPUT

Symbol	Parameter	Min.	Max.	Unit
tPRODAT	ROCLK Low to RODAT Valid Prop. Delay	-3	3	ns
tPRMFP	ROCLK Low to RMFP Valid Propagation Delay	-3	3	ns
tPRMSFP	ROCLK Low to RMSFP Valid Prop. Delay	-3	3	ns
tPROHP	ROCLK Low to ROHP Valid Propagation Delay	-3	3	ns
tPRLOS	ROCLK Low to RLOS Valid Propagation Delay	-3	3	ns

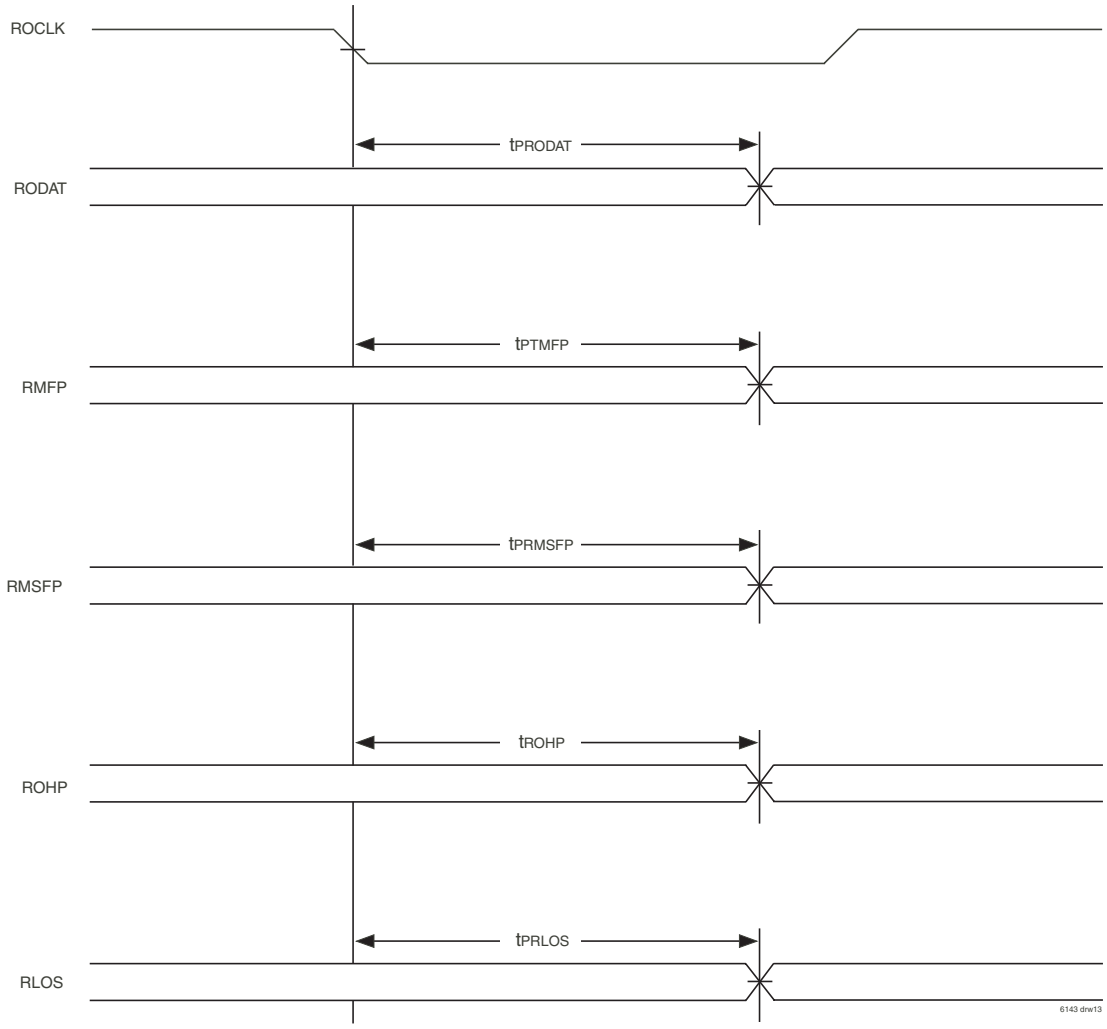


Figure 48 Receive DS3 Output Timing

RECEIVE OVERHEAD OUTPUT

Symbol	Parameter	Min.	Max.	Unit
t_{PROH}	ROHCLK Low to ROH Valid Propagation Delay	-5	20	ns
t_{PROHFP}	ROHCLK Low to ROHFP Valid Prop. Delay	-5	20	ns
t_{PRAIS}	ROHCLK Low to RAIS Valid Propagation Delay	-5	20	ns
t_{PROOF}	ROHCLK Low to ROOF Valid Prop. Delay	-5	20	ns
t_{PRFERF}	ROHCLK Low to RFERF Valid Prop. Delay	-5	20	ns

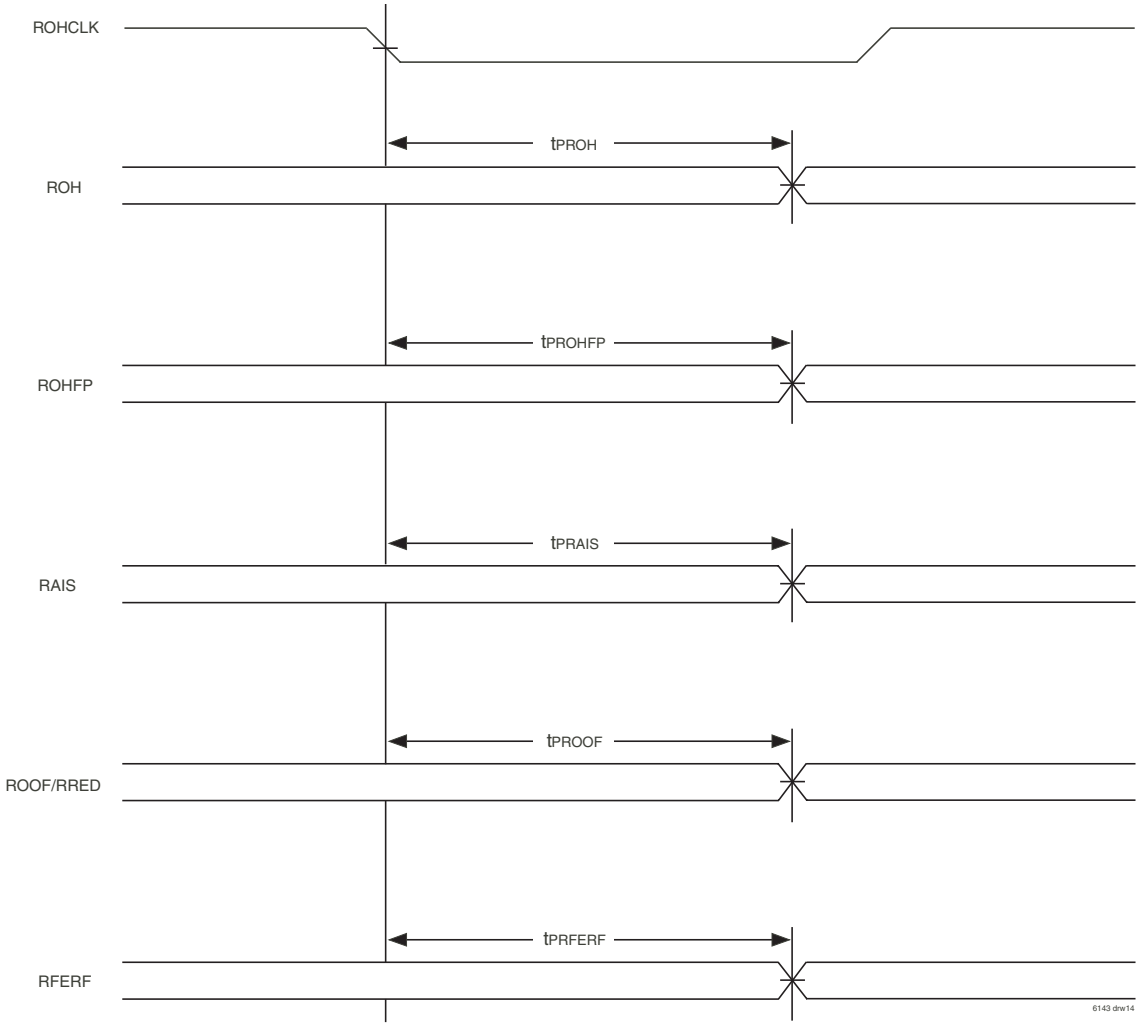


Figure 49 Receive Overhead Output Timing

TRANSMIT OVERHEAD OUTPUT

Symbol	Parameter	Min.	Max.	Unit
t_{PTOHFP}	TOHCLK Low to TOHFP Valid Prop. Delay	-10	20	ns

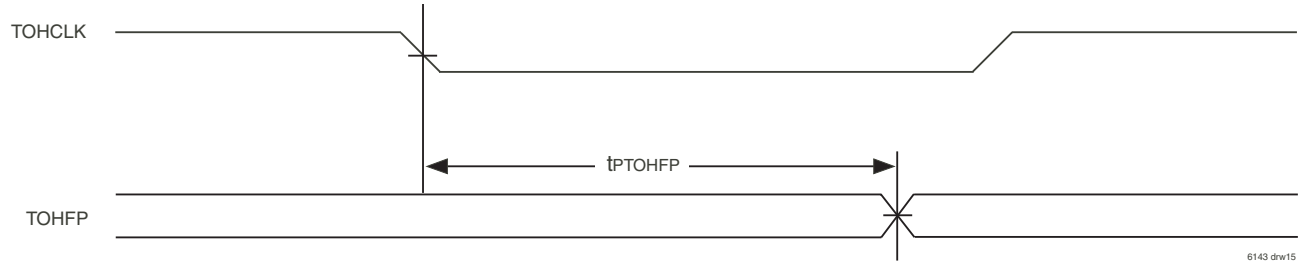


Figure 50 Transmit Overhead Output Timing

RECEIVE TRIBUTARY OUTPUT

Symbol	Parameter	Min.	Max.	Unit
$t_{PRD1DAT}$	RD1CLK Low to RD1DAT Valid Prop. Delay	-10	20	ns

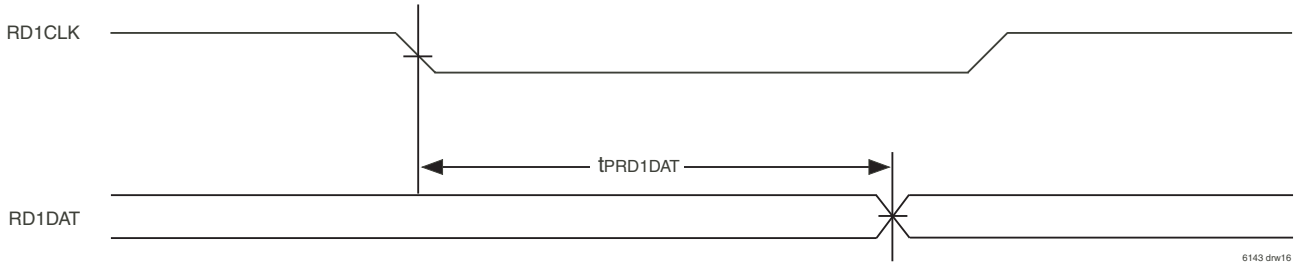


Figure 51 Receive Tributary Output Timing

RECEIVE DATA LINK OUTPUT

Symbol	Parameter	Min.	Max.	Unit
$t_{PRD1DAT}$	RD1CLK Low to RD1DAT Valid Prop. Delay	-10	20	ns

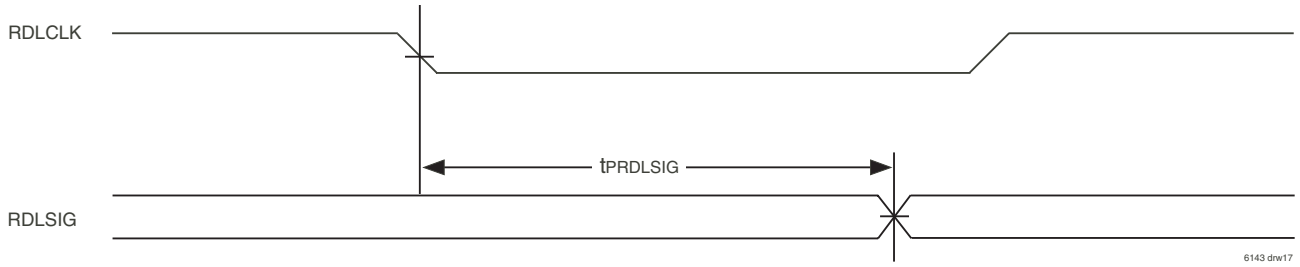


Figure 52 Receive Data Link Output Timing

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 20 pF load on the high-speed DS3 outputs (TCLK, TPOS/TDAT, TNEG/TMFP, ROCLK, RODAT, RMFP, RMSFP, and ROHP) and a 50 pF load on the remaining outputs.

JTAG Timing Specifications

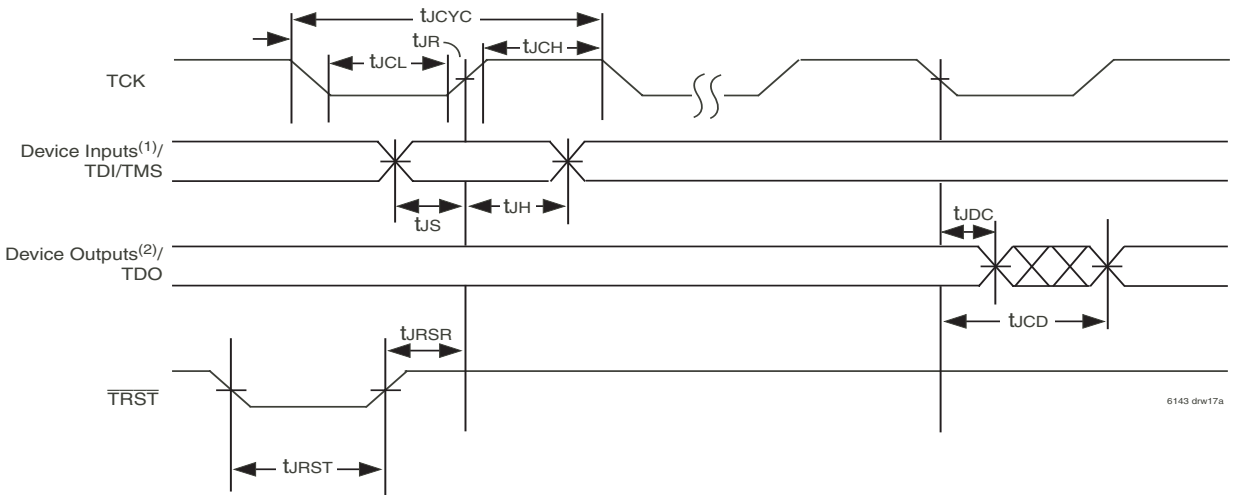


Figure 53 Standard JTAG Timing

Notes:

1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO

JTAG AC Electrical Characteristics (1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
tJCYC	JTAG Clock Input Period	100	-	ns
tJCH	JTAG Clcok HIGH	40	-	ns
tJCL	JTAG Clock LOW	40	-	ns
tJR	JTAG Clock Rise Time	-	3(1)	ns
tJF	JTAG Clock Fall Time	-	3(1)	ns
tJRST	JTAG Reset	50	-	ns
tJRSR	JTAG Reset Recovery	50	-	ns
tJCD	JTAG Data Output	-	25	ns
tJDC	JTAG Data Output Hold	0	-	ns
tJS	JTAG Setup	15	-	ns
tJH	JTAG Hold	15	-	ns

Notes:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x0312(1)	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

Note:

1. Device ID forIDT82V8313 is 0x0313.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

JTAG Information

All fourteen even T1 data inputs (TD1DAT2, 4, 6...28) are inverted before JTAG scan registers. So during JTAG preload/sample operation, the inverted values will be shifted out in TDO output. In other words if 0 is applied to the pin a 1 will be read out on TDO for that corresponding pin.

All fourteen even T1 data outputs (D1DAT2,4,6...28) are inverted after JTAG scan registers. So during JTAG EXTEST operation, their iverted values will be output on the output pads. In other words if a 0 is loaded into the pad, a 1 will be seen on the pin when looked at externally.

System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGH-Z	0011	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a HIGH-Z state.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device input(2) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those indentified above.

Notes:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$
3. The Boundary Scan Description Language (BSDL) file for this device is available on the IDT website (www.idt.com), or b y contacting you local IDT sales representative.

JTAG SCAN ORDER

Name	In	Out	High-Z
TD1CLK27	0		
RD1DAT27		1	2
TD1DAT27	3		
RD1CLK26		4	5
TD1CLK26	6		
RD1DAT26		7	8
TD1DAT26	9		
RD1CLK25		10	11
TD1CLK25	12		
RD1DAT25		13	14
TD1DAT25	15		
RD1CLK24		16	17
TD1CLK24	18		
RD1DAT24		19	20
TD1DAT24	21		
RD1CLK23		22	23
TD1CLK23	24		
RD1DAT23		25	26
TD1DAT23	27		
RD1CLK22		28	29
TD1CLK22	30		
RD1DAT22		31	32
TD1DAT22	33		
RD1CLK21		34	35
TD1CLK21	36		
RD1DAT21		37	38
TD1DAT21	39		
RD1CLK20		40	41
TD1CLK20	42		
RD1DAT20		43	44
TD1DAT20	45		
RD1CLK19		46	47
TD1CLK19	48		
RD1DAT19		49	50
TD1DAT19	51		
RD1CLK18		52	53
TD1CLK18	54		

JTAG SCAN ORDER

Name	In	Out	High-Z
RD1DAT18		55	56
TD1DAT18	57		
RD1CLK17		58	59
TD1CLK17	60		
RD1DAT17		61	62
TD1DAT17	63		
RD1CLK16		64	65
TD1CLK16	66		
RD1DAT16		67	68
TD1DAT16	69		
RD1CLK15		70	71
TD1CLK15	72		
RD1DAT15		73	74
TD1DAT15	75		
RD1CLK14		76	77
TD1CLK14	78		
RD1DAT14		79	80
TD1DAT14	81		
RD1CLK13		82	83
TD1CLK13	84		
RD1DAT13		85	86
TD1DAT13	87		
RD1CLK12		88	89
TD1CLK12	90		
RD1DAT12		91	92
TD1DAT12	93		
RD1CLK11		94	95
TD1CLK11	96		
RD1DAT11		97	98
TD1DAT11	99		
RD1CLK10		100	101
TD1CLK10	102		
RD1DAT10		103	104
TD1DAT10	105		
RD1CLK9		106	107
TD1CLK9	108		

Name	In	Out	High-Z
RD1DAT9		109	110
TD1DAT9	111		
RD1CLK8		112	113
TD1CLK8	114		
RD1DAT8		115	116
TD1DAT8	117		
RD1CLK7		118	119
TD1CLK7	120		
RD1DAT7		121	122
TD1DAT7	123		
RD1CLK6		124	125
TD1CLK6	126		
RD1DAT6		127	128
TD1DAT6	129		
RD1CLK5		130	131
TD1CLK5	132		
RD1DAT5		133	134
TD1DAT5	135		
RD1CLK4		136	137
TD1CLK4	138		
RD1DAT4		139	140
TD1DAT4	141		
RD1CLK3		142	143
TD1CLK3	144		
RD1DAT3		145	146
TD1DAT3	147		
RD1CLK2		148	149
TD1CLK2	150		
RD1DAT2		151	152
TD1DAT2	153		
RD1CLK1		154	155
TD1CLK1	156		
RD1DAT1		157	158
TD1DAT1	159		
TDLEMOI	160		
TDLSIG	161	162	163
TD2CLK	164		

Name	In	Out	High-Z
TDLCLK_INT		165	166
TIMFP		167	
TICLK	168		
TCLK	169	170	
TPOS_DAT	171	172	
RAIS	173	174	
TNEG_MFP	175	176	
GD2CLK	177	178	
RODAT	179	180	
ROCLK	181	182	
RMFP	183	184	
ROHP	185	186	
TOHCLK	187	188	
TOHFP	189	190	
RMSFP	191	192	
TOH	193		
TOHEN	194		
ROHFP	195	196	
ROH	197	198	
ROHCLK	199	200	
RLOS	201	202	
RFERF	203	204	
ROOF_RED	205	206	
REXZ	207	208	
RCLK	209		
RPOS_DAT	210		
RNEG_LCV	211		
RDCLK_INT	212	213	
RDLSIG_EOM	214	215	
$\overline{INT}$	216	217	
D0	218	219	220
D1	221	222	223
D2	224	225	226
D3	227	228	229

Name	In	Out	High-Z
D4	230	231	232
D5	233	234	235
D6	236	237	238
D7	239	240	241
$\overline{CS}$	242		
ALE	243		
A0	244		
A1	245		
A2	246		
A3	247		
A4	248		
A5	249		
A6	250		

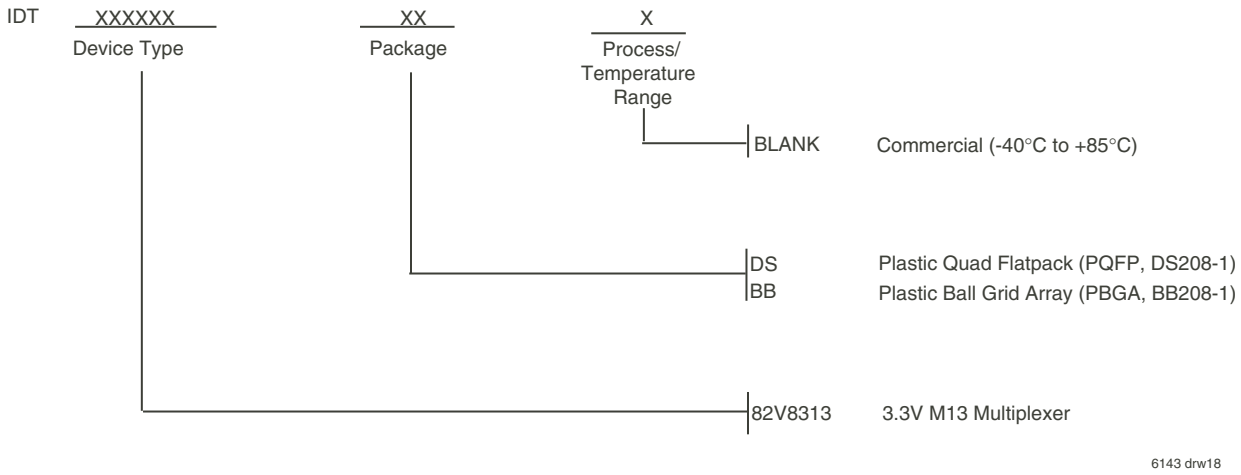
Name	In	Out	High-Z
A7	251		
A8	252		
$\overline{WR}$	253		
$\overline{RD}$	254		
$\overline{RST}$	255		
RD1CLK28		256	257
TD1CLK28	258		
RD1DAT28		259	260
TD1DAT28	261		
RD1CL27		262	263

Note:

All fourteen even T1 data inputs (TS1DAT2,4,6...28) are inverted before JTAG scan registers. So during JTAG preload/sample operation, the inverted values will be shifted out in TDO output. In other words if a 0 is applied to the pin 1 will be read out on TDO for that corresponding pin.

All fourteen even T1 data outputs (RD1DAT2,4,6...28) are inverted after JTAG scan registers. So during JTAG EXTEST operation, their inverted values will be output on the output pads. In other words if a 0 is loades into the pad, a 1 will be seen on the pin when looked at externally.

ORDERING INFORMATION



Datasheet Document History

12/15/2003 **Pgs. 1 thru 130**
03/15/2004 **Pgs. 3 and 121.**
06/03/2004 **Pgs. 101, 102 and 121.**

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American National Standards Institute (ANSI)

ANSI T1.101 1994: Synchronization Interface Standard.

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TR-NWT-000170 Issue 2, 01/1993: Digital Cross-Connect System Generic Requirements and Objectives.

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International Telecommunication Union (ITU-T)

Recommendation G.703 04/91: Physical/electrical characteristics oh hierarchical digitalinterfaces

Recommendation G.704 07/95: Synchronous frame structures used at 1544, 6312, 2048, 8488 and 44 736 kbit/s hierarchical levels

Recommendation G.706 04/91: Frame alignment and cyclic redundancy check (CGC) procedures relating to basic frame structures defined in Recommendation G.704

Recommendation G.747 1988: Second order digital multiplex equipment operating at 6312 kbit/s and multiplexing three tributaries at 2048 kbit/s

Recommendation G.752 1988: Characteristics of digital multiplex equipment based on a second order bit rate of 6312 kbit/s and using positive justification

Recommendation G.824 03/93: The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

Recommendation M.20 10/92: Maintenance and Philosophy for telecommunication networks

Recommendation O.150 05/96: General requirements for instrumentation for performance measurements on digital transmission equipment

Recommendation O.151 10/92: Error performance measuring equipment operating at the primary rate and above

Recommendation O.152 10/92: Error performance measuring equipment for bit rates of 64 kbit/s and N x 64 kbit/s signals

Recommendation O.153 10/92: Basic parameters for the measurement of error performance at bit rates below the primary rate

Recommendation Q.921 03/93: ISDN user-network interface Data link layer specification

Network Working Group

RFC 2495 01/99: Definitions of Managed Objects for the Ds1, E1, Ds2 and E2 Interface Types.

Other documents

T1 Basics (Telecommunications Techniques Corporation - TTC)

The Fundamentals of Ds3 1992 (Telecommunications Techniques Corporation - TTC)

ADM	Add / Drop Multiplexer
AIC	Application Identification
AIS	Alarm Indication Singnal
AIS-CI	Alarm Indication Signal - Customer Installation
AISS	AIS Second
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
B-DCS	Broadband DCS
BER	Bit Error Rate
BERT	Bit Error Rate Testing
BITS	Building Integrated Timing Source (or Supply)
BnZS	Bipolar with n zero Substitution (n = 3 for Ds3 and 8 for Ds1 level)
BOC	Bit Oriented Code
BPV	Bipolar Violation
C/R	Command / Response
CAS-BR	Channel Associated Signaling - Bit Robbing (signaling distributed in each Ds0)
CAS-CC	Channel Associated Signaling - Common Channel (in timeslot 24 in T1 channel)
CC	Composite Clock
CCS	Common Channel Signaling
CFA	Carrier Failure Alarm
CGA	Carrier Group Alarm
CI	Customer Installation
COFA	Change of Frame Alignment
CP	Parity bit instead of stuffing indicator in Ds3 C-bit parity mode
CRC	Cyclical Redundancy Check
CS	Controlled Slip
CSS	Controlled Slip Second
CSU	Customer Service Unit
CV	Code Violation

CVCP	"Code Violation, CP-bit"
CVP	"Code Violation, P-bit"
DCS	Digital Cross-connect System
Dsx	"Digital Signal hierarchy, level x"
EA	Extension Address (field)
EDF	Extended Superframe Format
EIC	Equipment Identification Channel
EOM	End of Message
ERR	Error
ES	Errored Second
ESA	"Errored Second, type A"
ESACP	"Errored Second, type A, CP-bit"
ESAP	"Errored Second, type A, P-bit"
ESB	"Errored Second, type B"
ESBCP	"Errored Second, type B, CP-bit"
ESBP	"Errored Second, type B, P-bit"
ESCP	"Errored Second, CP-bit"
ESP	"Errored Second, P-bit"
EXZ	Excessive Zeros
EXZS	Excessive Zero Suppression
FAS	Frame Alignment Signal
FC	Failure Count
FCS	Frame Check Sequence
FDL	Facility Data Link
FEAC	Far End Alarm and Control Channel
FEBE	Far End Block Error
FEPR	Far End Performance Report
FERF	Far End Receive Failure
FIC	Fast Information Channel
GPS	General Positioning System
HDB3	High Density Bipolar Three
HDLC	High Level Data Link Control
HSSL	High Speed Serial Link
IDL	Idle Pattern

ISDN	Integrated Services Digital Network
ISID	Idle Signal Identification
ITU	International Telecommunication Union
L	Line
LAPD	Link Access Protocol on the D Channel
LCV	Line Code Violation
LFE	Line Far End
LIC	Location Identification Channel
LIU	Line Interface Unit
LOD	Loss of Data
LOF	Loss of Frame
LOS	Loss of Signal
MART	Maximum Average Reframe Time
MDL	Maintenance Data Link
MOP	Message Oriented Protocol
NE	Network Element
NP	Network Path
NPFE	Network Path
NPRM	Network Performance Report Message
OC-n	Optical Carrier level n
OOF	Out of Frame
P	Path
PER	Parity Error Ratio
PFE	Path Far End
PID	Path Identification
PM	Performance Monitoring
POL	Polarity
PRM	Performance Report Message
PRS	Primary Reference Source
PS	Protection Switching
PSC	Protection Switching Count
PSD	Protection Switching Duration
PTE	Path Terminating Equipment
RAI	Remote Alarm Indication

RAI-CI	Remote Alarm Indication - Customer Installation
RDI	Remote Defect Indication
RED	Red Alarm
SAPI	Service Access Point Identifier
SAS	Severely Errored Frame / Alarm Indication Signal (SEF/AIS) Second
SEF	Severely Errored Frame
SES	Severely Errored Second
SESCP	"Severely Errored Second, CP-bit"
SESP	"Severely Errored Second, P-bit"
SF	Superframe Format Signal
SLC96	Subscriber Loop Carrier (96 subscriber access line)
SONET	Synchronous Optical Network
SPRM	Supplement Performance Report Message
STS-n	Synchronous Transport Signal Level n (STS-1: transmission rate of 51.84 Mbit/s)
TCA	Threshold Crossing Alert
TEI	Terminal Endpoint Identifier
TSID	Test Signal Identification
UAS	Unavailable Second
UASCP	"Unavailable Second, CP-bit"
UASP	"Unavailable Second, P-bit"
UDR	Underrun
UI	Unit Interval
VT	Virtual Tributary (VT1.5: 1.544 Mbit/s signal encapsulated in a higher rate)
W-DCS	Wideband DCS
ZBTSI	Zero-byte time slot interchange

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