



# 3.3V CMOS 16-BIT BUS TRANSCIVER/REGISTER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

**IDT74LVCHR16646A**

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$ , Normal Range
- $V_{cc} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

## DRIVE FEATURES:

- Balanced Output Drivers:  $\pm 12mA$
- Low switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

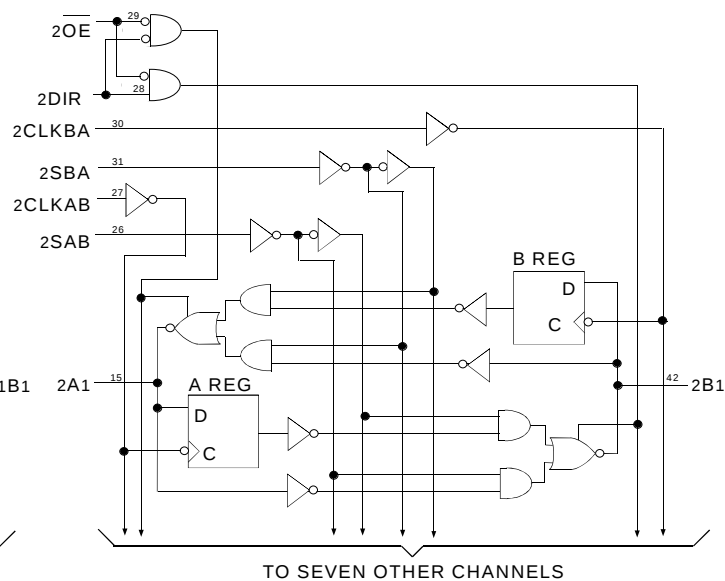
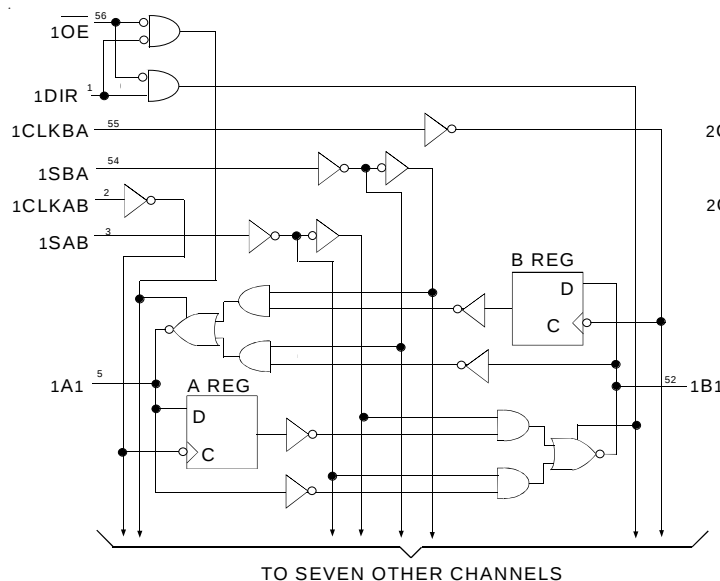
The LVCHR16646A 16-bit transceiver/register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type transceivers with 3-state D-type registers. The controls circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (DIR), over-riding Output Enable control ( $\overline{OE}$ ) and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the low-to-high transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

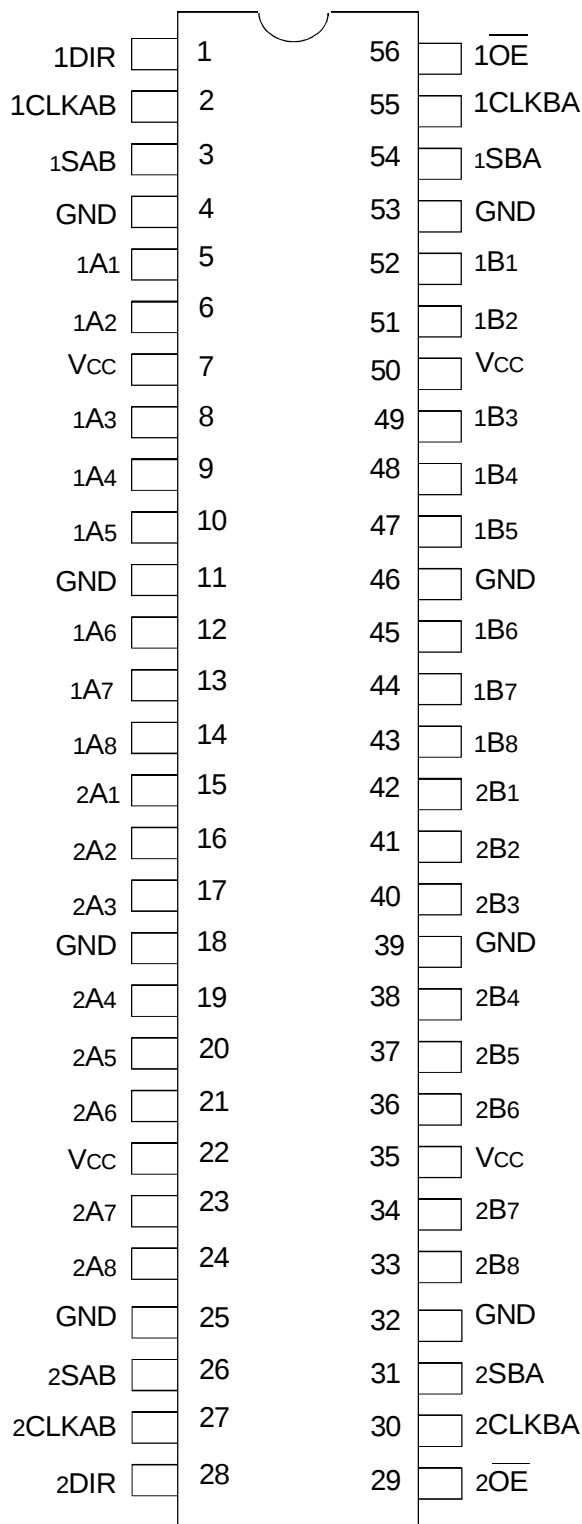
The LVCHR16646A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive  $\pm 12mA$  at the designated threshold levels.

The LVCHR16646A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                             | Description                                                           | Max          | Unit |
|------------------------------------|-----------------------------------------------------------------------|--------------|------|
| V <sub>TERM</sub>                  | Terminal Voltage with Respect to GND                                  | -0.5 to +6.5 | V    |
| T <sub>STG</sub>                   | Storage Temperature                                                   | -65 to +150  | °C   |
| I <sub>OUT</sub>                   | DC Output Current                                                     | -50 to +50   | mA   |
| I <sub>IK</sub><br>I <sub>OK</sub> | Continuous Clamp Current,<br>V <sub>I</sub> < 0 or V <sub>O</sub> < 0 | -50          | mA   |
| I <sub>CC</sub><br>I <sub>SS</sub> | Continuous Current through each<br>V <sub>CC</sub> or GND             | ±100         | mA   |

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 4.5  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 6.5  | 8    | pF   |
| C <sub>I/O</sub> | I/O Port Capacitance     | V <sub>IN</sub> = 0V  | 6.5  | 8    | pF   |

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

| Pin Names         | Description                                                      |
|-------------------|------------------------------------------------------------------|
| x A x             | Data Register A Inputs <sup>(1)</sup><br>Data Register B Outputs |
| x B x             | Data Register B Inputs <sup>(1)</sup><br>Data Register A Outputs |
| xCLKAB, xCLKBA    | Clock Pulse Inputs                                               |
| xSAB, xSBA        | Output Data Source Select Inputs                                 |
| x $\overline{OE}$ | Output Enable Inputs (Active LOW)                                |
| xDIR              | Direction Control Inputs                                         |

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE<sup>(1)</sup>

| Inputs           |        |          |          |        |        | Data I/O <sup>(2)</sup> |             | Operation or Function                 |
|------------------|--------|----------|----------|--------|--------|-------------------------|-------------|---------------------------------------|
| $\overline{xOE}$ | $xDIR$ | $xCLKAB$ | $xCLKBA$ | $xSAB$ | $xSBA$ | $xAx$                   | $xBx$       |                                       |
| X                | X      | ↑        | X        | X      | X      | Input                   | Unspecified | Store A, B unspecified <sup>(2)</sup> |
| X                | X      | X        | ↑        | X      | X      | Unspecified             | Input       | Store B, A unspecified <sup>(2)</sup> |
| H                | X      | ↑        | ↑        | X      | X      | Input                   | Input       | Store A and B data                    |
| H                | X      | H or L   | H or L   | X      | X      | Input                   | Input       | Isolation, hold storage               |
| L                | L      | X        | X        | X      | L      | Output                  | Input       | Real time B data to A bus             |
| L                | L      | X        | H or L   | X      | H      | Output                  | Input       | Stored B data to A bus                |
| L                | H      | X        | X        | L      | X      | Input                   | Output      | Real time A data to B bus             |
| L                | H      | H or L   | X        | H      | X      | Input                   | Output      | Stored A data to B bus                |

### NOTES:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
↑ = LOW-to-HIGH transition
- The data output functions may be enabled or disabled by various signals at  $\overline{OE}$  or  $DIR$ . Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

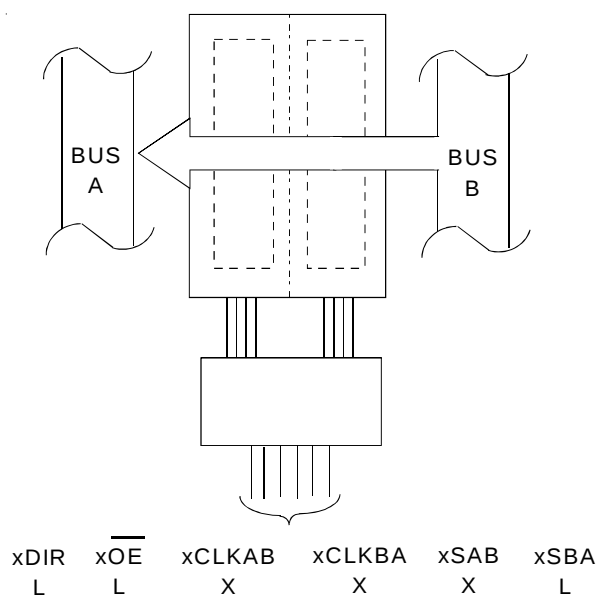
Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

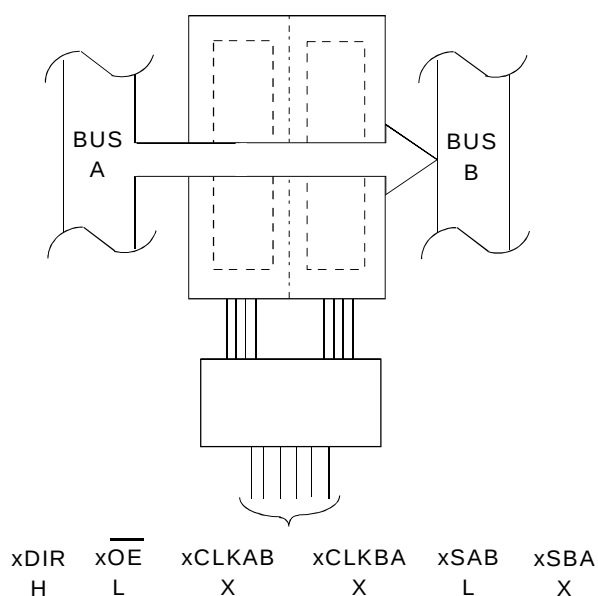
| Symbol                     | Parameter                                              | Test Conditions                                                       |                                          | Min. | Typ. <sup>(1)</sup> | Max.     | Unit          |
|----------------------------|--------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------|------|---------------------|----------|---------------|
| $V_{IH}$                   | Input HIGH Voltage Level                               | $V_{CC} = 2.3\text{V}$ to $2.7\text{V}$                               |                                          | 1.7  | —                   | —        | V             |
|                            |                                                        | $V_{CC} = 2.7\text{V}$ to $3.6\text{V}$                               |                                          | 2    | —                   | —        |               |
| $V_{IL}$                   | Input LOW Voltage Level                                | $V_{CC} = 2.3\text{V}$ to $2.7\text{V}$                               |                                          | —    | —                   | 0.7      | V             |
|                            |                                                        | $V_{CC} = 2.7\text{V}$ to $3.6\text{V}$                               |                                          | —    | —                   | 0.8      |               |
| $I_{IH}$<br>$I_{IL}$       | Input Leakage Current                                  | $V_{CC} = 3.6\text{V}$                                                | $V_I = 0$ to $5.5\text{V}$               | —    | —                   | $\pm 5$  | $\mu\text{A}$ |
| $IOZH$<br>$IOZL$           | High Impedance Output Current<br>(3-State Output pins) | $V_{CC} = 3.6\text{V}$                                                | $V_O = 0$ to $5.5\text{V}$               | —    | —                   | $\pm 10$ | $\mu\text{A}$ |
| $IOFF$                     | Input/Output Power Off Leakage                         | $V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$             |                                          | —    | —                   | $\pm 50$ | $\mu\text{A}$ |
| $V_{IK}$                   | Clamp Diode Voltage                                    | $V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$                      |                                          | —    | -0.7                | -1.2     | V             |
| $V_H$                      | Input Hysteresis                                       | $V_{CC} = 3.3\text{V}$                                                |                                          | —    | 100                 | —        | mV            |
| $ICCL$<br>$ICCH$<br>$ICCZ$ | Quiescent Power Supply Current                         | $V_{CC} = 3.6\text{V}$                                                | $V_{IN} = \text{GND}$ or $V_{CC}$        | —    | —                   | 10       | $\mu\text{A}$ |
|                            |                                                        |                                                                       | $3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$ | —    | —                   | 10       |               |
| $\Delta I_{CC}$            | Quiescent Power Supply Current Variation               | One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND |                                          | —    | —                   | 500      | $\mu\text{A}$ |

### NOTES:

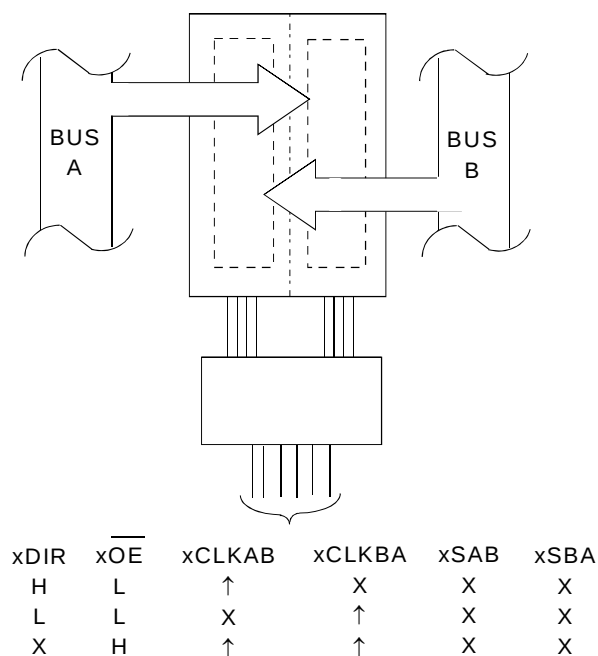
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.



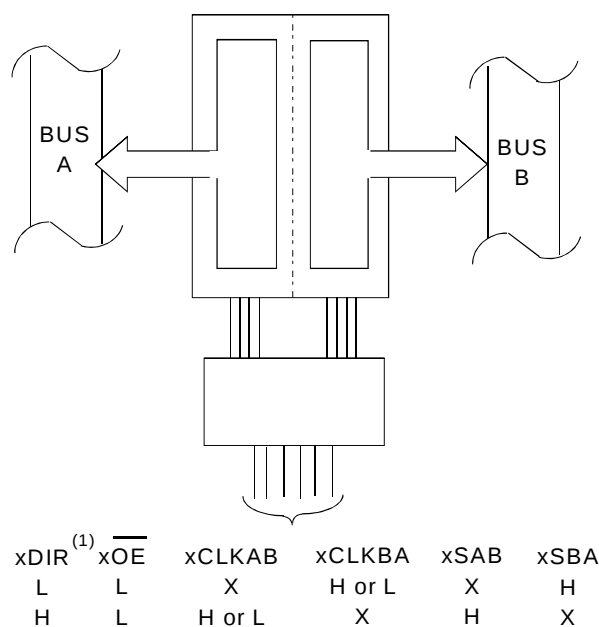
**Real-Time Transfer  
Bus B to A**



**Real-Time Transfer  
Bus A to B**



**Storage from  
A, B, or A and B**



**Transfer Stored  
Data to A and/or B**

**NOTE:**

1. Cannot transfer data to A Bus and B Bus simultaneously.

## BUS-HOLD CHARACTERISTICS

| Symbol         | Parameter <sup>(1)</sup>         | Test Conditions        |                            | Min. | Typ. <sup>(2)</sup> | Max. | Unit |
|----------------|----------------------------------|------------------------|----------------------------|------|---------------------|------|------|
| IBHH<br>IBHL   | Bus-Hold Input Sustain Current   | V <sub>CC</sub> = 3V   | V <sub>I</sub> = 2V        | -75  | —                   | —    | μA   |
|                |                                  |                        | V <sub>I</sub> = 0.8V      | 75   | —                   | —    |      |
| IBHH<br>IBHL   | Bus-Hold Input Sustain Current   | V <sub>CC</sub> = 2.3V | V <sub>I</sub> = 1.7V      | —    | —                   | —    | μA   |
|                |                                  |                        | V <sub>I</sub> = 0.7V      | —    | —                   | —    |      |
| IBHHO<br>IBHLO | Bus-Hold Input Overdrive Current | V <sub>CC</sub> = 3.6V | V <sub>I</sub> = 0 to 3.6V | —    | —                   | ±500 | μA   |

### NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter           | Test Conditions <sup>(1)</sup> |                          | Min.                  | Max. | Unit |
|--------|---------------------|--------------------------------|--------------------------|-----------------------|------|------|
| VOH    | Output HIGH Voltage | V <sub>CC</sub> = 2.3V to 3.6V | I <sub>OH</sub> = -0.1mA | V <sub>CC</sub> - 0.2 | —    | V    |
|        |                     | V <sub>CC</sub> = 2.3V         | I <sub>OH</sub> = -4mA   | 1.9                   | —    |      |
|        |                     |                                | I <sub>OH</sub> = -6mA   | 1.7                   | —    |      |
|        |                     | V <sub>CC</sub> = 2.7V         | I <sub>OH</sub> = -4mA   | 2.2                   | —    |      |
|        |                     |                                | I <sub>OH</sub> = -8mA   | 2                     | —    |      |
|        |                     | V <sub>CC</sub> = 3V           | I <sub>OH</sub> = -6mA   | 2.4                   | —    |      |
|        |                     |                                | I <sub>OH</sub> = -12mA  | 2                     | —    |      |
| VOL    | Output LOW Voltage  | V <sub>CC</sub> = 2.3V to 3.6V | I <sub>OL</sub> = 0.1mA  | —                     | 0.2  | V    |
|        |                     | V <sub>CC</sub> = 2.3V         | I <sub>OL</sub> = 4mA    | —                     | 0.4  |      |
|        |                     |                                | I <sub>OL</sub> = 6mA    | —                     | 0.55 |      |
|        |                     | V <sub>CC</sub> = 2.7V         | I <sub>OL</sub> = 4mA    | —                     | 0.4  |      |
|        |                     |                                | I <sub>OL</sub> = 8mA    | —                     | 0.6  |      |
|        |                     | V <sub>CC</sub> = 3V           | I <sub>OL</sub> = 6mA    | —                     | 0.55 |      |
|        |                     |                                | I <sub>OL</sub> = 12mA   | —                     | 0.8  |      |

### NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range.  
T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 25°C

| Symbol | Parameter                                                      | Test Conditions                 | Typical | Unit |
|--------|----------------------------------------------------------------|---------------------------------|---------|------|
| CPD    | Power Dissipation Capacitance per Transceiver Outputs enabled  | C <sub>L</sub> = 0pF, f = 10Mhz | —       | pF   |
| CPD    | Power Dissipation Capacitance per Transceiver Outputs disabled |                                 | —       |      |

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

| Symbol                               | Parameter                                                           | V <sub>CC</sub> = 2.7V |      | V <sub>CC</sub> = 3.3V ± 0.3V |      | Unit |
|--------------------------------------|---------------------------------------------------------------------|------------------------|------|-------------------------------|------|------|
|                                      |                                                                     | Min.                   | Max. | Min.                          | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>xAx to xBx or xBx to xAx                       | 2                      | 6.3  | 2                             | 5.3  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>xCLK to xAx or xBx                             | 2                      | 7.3  | 2                             | 6.3  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>xSBA or xSAB to xAx or xBx                     | 2                      | 7.3  | 2                             | 6.3  | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>x $\overline{OE}$ or xDIR to xAx or Bx        | 2                      | 8.5  | 2                             | 7.5  | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>x $\overline{OE}$ or xDIR to xAx or Bx       | 2                      | 7    | 2                             | 6    | ns   |
| t <sub>su</sub>                      | Set-up Time HIGH or LOW before CLKAB $\uparrow$ or CLKBA $\uparrow$ | 2.5                    | —    | 2.5                           | —    | ns   |
| t <sub>h</sub>                       | Hold Time HIGH or LOW after CLKAB $\uparrow$ or CLKBA $\uparrow$    | 1.5                    | —    | 1.5                           | —    | ns   |
| t <sub>w</sub>                       | Clock Pulse Width HIGH or LOW                                       | 3                      | —    | 3                             | —    | ns   |
| t <sub>sk(0)</sub>                   | Output Skew <sup>(2)</sup>                                          | —                      | —    | —                             | 500  | ps   |

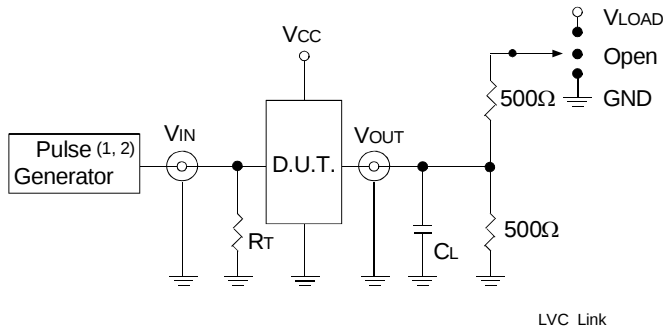
### NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T<sub>A</sub> = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

| Symbol            | V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V | V <sub>CC</sub> <sup>(1)</sup> =2.7V | V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V | Unit |
|-------------------|-------------------------------------------|--------------------------------------|-------------------------------------------|------|
| V <sub>LOAD</sub> | 6                                         | 6                                    | 2 x V <sub>CC</sub>                       | V    |
| V <sub>IH</sub>   | 2.7                                       | 2.7                                  | V <sub>CC</sub>                           | V    |
| V <sub>T</sub>    | 1.5                                       | 1.5                                  | V <sub>CC</sub> / 2                       | V    |
| V <sub>LZ</sub>   | 300                                       | 300                                  | 150                                       | mV   |
| V <sub>HZ</sub>   | 300                                       | 300                                  | 150                                       | mV   |
| C <sub>L</sub>    | 50                                        | 50                                   | 30                                        | pF   |



Test Circuit for All Outputs

#### DEFINITIONS:

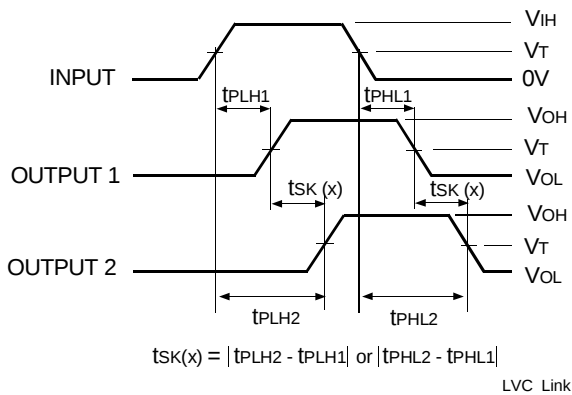
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

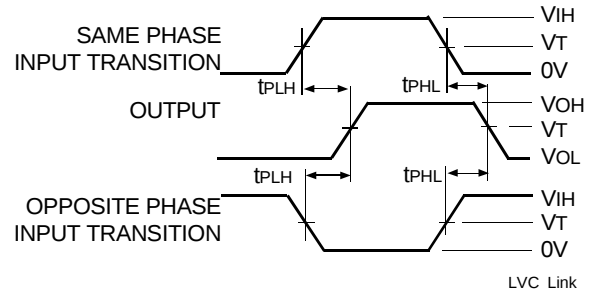
| Test                                    | Switch            |
|-----------------------------------------|-------------------|
| Open Drain<br>Disable Low<br>Enable Low | V <sub>LOAD</sub> |
| Disable High<br>Enable High             | GND               |
| All Other Tests                         | Open              |



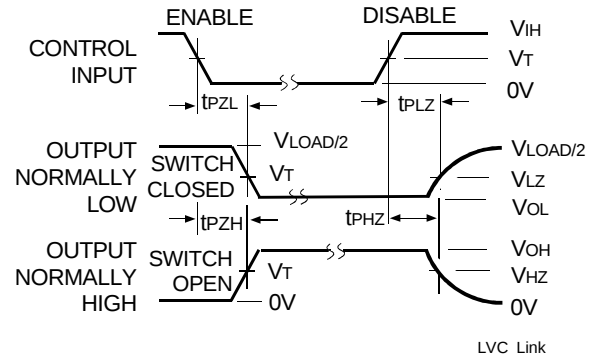
Output Skew - t<sub>sk</sub>(x)

#### NOTES:

1. For t<sub>sk</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>sk</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.



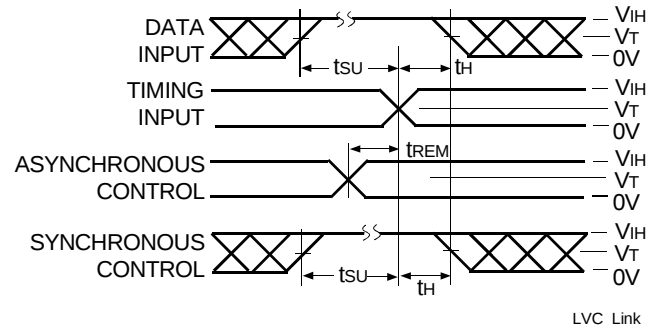
Propagation Delay



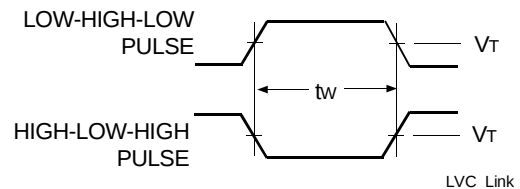
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

| IDT         | XX | LVC | X        | XX     | XXXX        | XX      |                                                                       |
|-------------|----|-----|----------|--------|-------------|---------|-----------------------------------------------------------------------|
| Temp. Range |    |     | Bus-Hold | Family | Device Type | Package |                                                                       |
|             |    |     |          |        |             | PV      | Shrink Small Outline Package                                          |
|             |    |     |          |        |             | PA      | Thin Shrink Small Outline Package                                     |
|             |    |     |          |        |             | PF      | Thin Very Small Outline Package                                       |
|             |    |     |          |        | 646A        |         | 16-Bit Transceiver/Register with 3-State Outputs, 5 Volt Tolerant I/O |
|             |    |     |          |        | R16         |         | Double-Density, $\pm 12\text{mA}$                                     |
|             |    |     |          |        | H           |         | Bus-hold                                                              |
|             |    |     |          |        | 74          |         | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$                        |



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