FEATURES:

- 3V to 3.6V operating voltage
- 48MHz to 160MHz output frequency range
- Input from fundamental crystal oscillator or external source
- Internal PLL feedback (loading the feedback output relative to the other outputs, will adjust the propagation delay between REF inputs and outputs)
- Select inputs ($S_{[1:0]}$) for FB divide selection (multiply ratio of 2, 3, 4, 4.25, 5, 6, 6.25, and 8)
- Low jitter
- PLL bypass for testing and power-down control (S1 = H, S0 = H, powers part down <500µA)
- Available in TSSOP package
- Pin and function compatible to IDT5V926

APPLICATIONS:

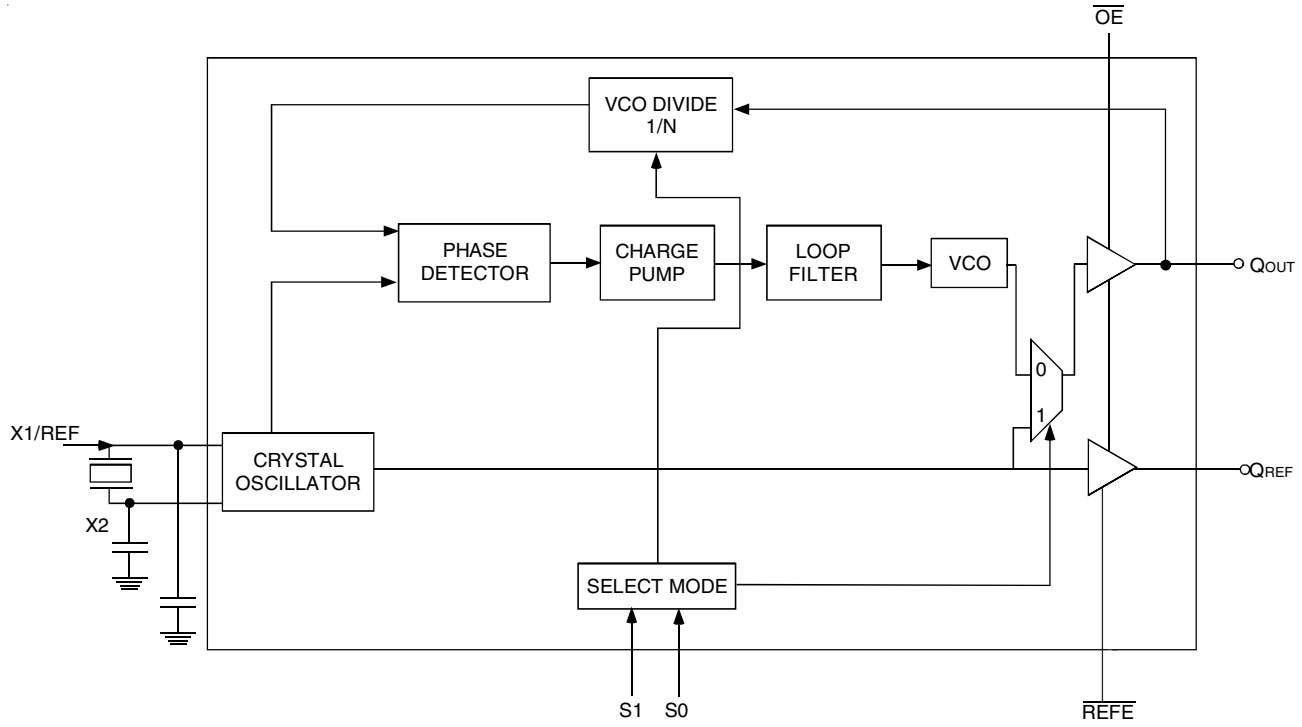
- Gigabit ethernet
- Router
- Network switches
- SAN
- Instrumentation
- Fibre channel

DESCRIPTION:

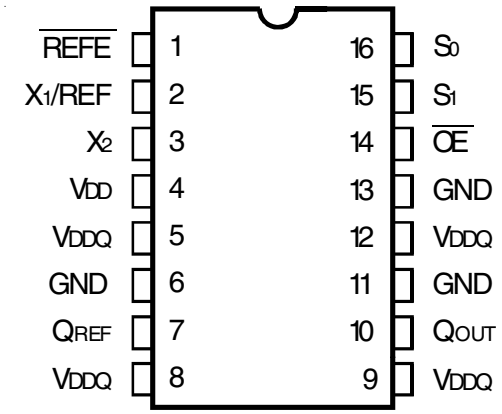
The IDT5V926A is a low-cost, low skew, low jitter, and high-performance clock multiplier with a reference clock from either a lower frequency crystal or clock input. It has been specially designed to interface with Gigabit Ethernet and Fast Ethernet applications by providing a 125MHz clock from 25MHz input. It can be programmed to provide output frequencies ranging from 48MHz to 160MHz, with input frequencies ranging from 6MHz to 80MHz.

The IDT5V926A includes an internal RC filter that provides excellent jitter characteristics and eliminates the need for external components. When using the optional crystal input, the device accepts a 10 - 40MHz fundamental mode crystal with a maximum equivalent series resistance of 50Ω.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Max.	Unit
V_{DD}/V_{DDQ}	Supply Voltage to Ground	-0.5 to +4.6	V
V_I	Input Voltage	-0.5 to +4.6	V
I_O	Output Current	±50	mA
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Name	Type	Description
S[1:0]	I	Three level divider/mode select pins. Float to MID.
$\overline{OE}$	I	Output enable bar. Outputs Qout and QREF are in a high-impedance state when HIGH. Set $\overline{OE}$ LOW for normal operation (has internal pull-down).
$\overline{REFE}$	I	QREF enable input. QREF stopped LOW when HIGH. When set $\overline{REFE}$ LOW, the QREF is enabled (has internal pull-down).
X1/REF	I	Crystal oscillator input or clock input.
X2	I	Crystal oscillator output. Leave unconnected for clock input.
QOUT	O	Output at N*REF frequency.
QREF	O	Output at REF frequency.
VDDQ	PWR	Power supply for the device outputs. Connect to VDD on PCB.
VDD	PWR	Power supply for the device core and inputs. Connect to VDD on PCB.
GND	PWR	Ground supply.

CRYSTAL SPECIFICATION

The crystal oscillators should be fundamental mode quartz crystals: overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. Crystal tuning capacitors should be connected from X1/REF to GND and from X2 to GND.

DIVIDE SELECTION TABLE(1)

S1	S0	Divide-by-N Value	Mode
L	L	2	PLL
L	M	3	PLL
L	H	4	PLL
M	L	4.25	PLL
M	M	5	PLL
M	H	6	PLL
H	L	6.25	PLL
H	M	8	PLL
H	H	TEST	TEST (2)

NOTES:
1. H = HIGH, M = MID, L = LOW
2. Test mode for low frequency testing. In this mode, REF clock bypasses the VCO (VCO powered down) and the crystal oscillator is powered down.

COMMON OUTPUT FREQUENCY EXAMPLES (MHz)

Output	48	60	64	72	75	80	90	100
Input	24	10	16	12	25	10	15	20
FB Divide Selection S[1:0]	LL	MH	LH	MH	LM	HM	MH	MM

Output	106.25	106.25	120	125	125	125	150	155.52
Input	17	25	15	20	25	62.5	25	19.44
FB Divide Selection S[1:0]	HL	ML	HM	HL	MM	LL	MH	HM

OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}/V_{DDQ}	Power Supply Voltage	3	3.3	3.6	V
T_A	Operating Temperature	- 40	25	+85	°C
C_{IN}	Input Capacitance, OE, F = 1MHz, V_{IN} = 0V, T_A = 25°C	—	5		pF

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{DD}/V_{DDQ} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max	Unit
V_{IL}	Input LOW Voltage			—	—	0.8	V
V_{IH}	Input HIGH Voltage			2	—	—	V
V_{IHH}	Input HIGH Voltage	3-level input only		V_{DD} - 0.6	—	—	V
V_{IMM}	Input MID Voltage	3-level input only		$V_{DD}/2$ - 0.3	—	$V_{DD}/2$ + 0.3	V
V_{ILL}	Input LOW Voltage	3-level input only		—	—	0.6	V
I_3	3-Level Input DC Current, S[1:0]	$V_{IN} = V_{DD}$	HIGH Level	—	—	+200	µA
		$V_{IN} = V_{DD}/2$	MID Level	- 50	—	+50	
		V_{IN} = GND	LOW Level	- 200	—	—	
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	$\overline{OE}$, $\overline{REFE}$	—	—	100	µA
		$V_{IN} = V_{DD}$, S[1:0] = HH	X1/REF	—	2	4	mA
V_{OL}	Output LOW Voltage	I_{OL} = 12mA		—	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA		2.4	—	—	V

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min.	Typ.	Max	Unit
I_{DD_PD}	Power Down Current	V_{DD} = Max. $S_{[1:0]}$ = HH $\overline{OE}$ = L; X_1/REF = L All outputs unloaded	—	—	500	µA
ΔI_{DD}	Supply Current per Input	V_{DD} = Max., V_{IN} = 3V	—	—	30	µA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.6V $S_{[1:0]}$ = LL $\overline{OE}$ = L F_{OUT} = 160MHz All outputs unloaded	—	—	50	mA

NOTE:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
t_R, t_F	Rise Time, Fall Time	0.8V to 2V	Q_{OUT}		0.7	1.5	ns
			Q_{REF}		0.7	2.0	
d_T	Output/Duty Cycle	$V_T = V_{DDQ}/2$	$Q_{OUT \le 125MHz}$	45		55	%
			$Q_{OUT > 125MHz}$	44		56	
			Q_{REF}	40		60	
t_J	Cycle - Cycle Jitter	F_{OUT} = 106.25MHz				100	ps
		F_{OUT} = 125MHz				90	
		F_{OUT} = 155.52MHz				125	
f_{OUT}	Output Frequency			48		160	MHz

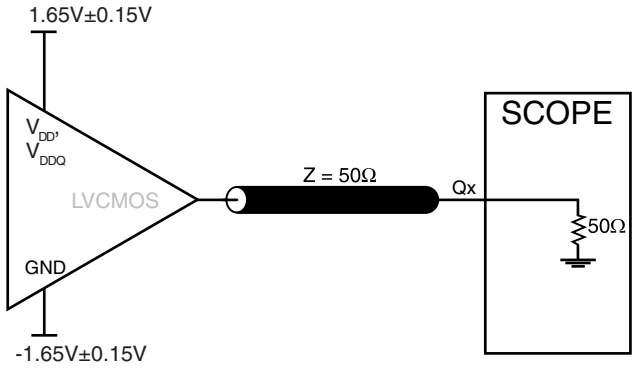
INPUT TIMING REQUIREMENTS

Symbol	Description(1)	Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall time, 0.8V to 2V(2)	—	10	ns/V
t_{PWC}	Input clock pulse, HIGH or LOW(2)	2	—	ns
D_H	Input duty cycle(2)	10	90	%
f_{OSC}	XTAL oscillator frequency	10	40	MHz
f_{IN}	Input frequency(2)	48/N	160/N	MHz

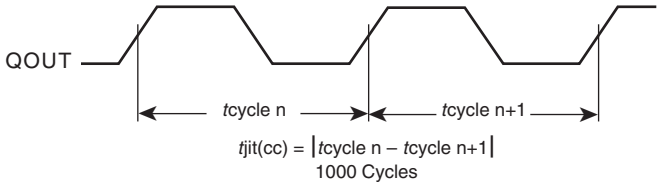
NOTES:

1. Where pulse width implied by D_H is less than the t_{PWC} limit, t_{PWC} limit applies.
2. When using a clock input.

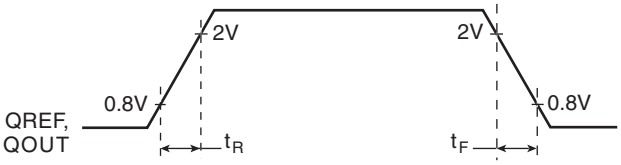
PARAMETER MEASUREMENT INFORMATION



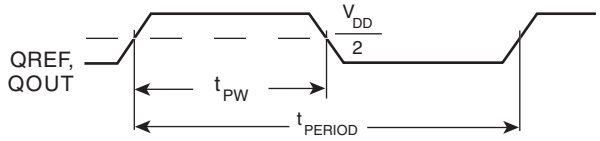
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



CYCLE-TO-CYCLE JITTER



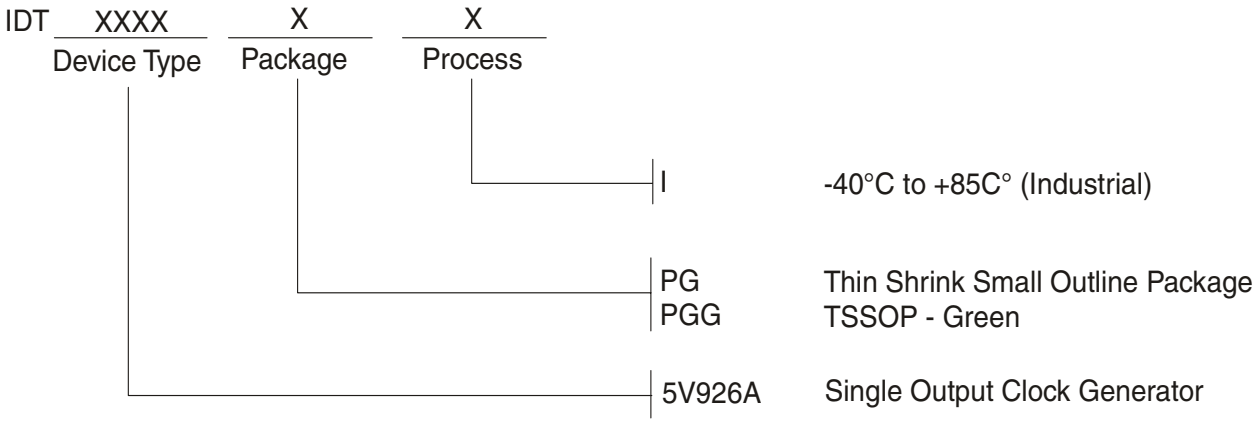
OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

ORDERING INFORMATION



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For Sales
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Fax: 408-284-2775
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For Tech Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)