SPREAD SPECTRUM CLOCK GENERATOR IDT5V50009

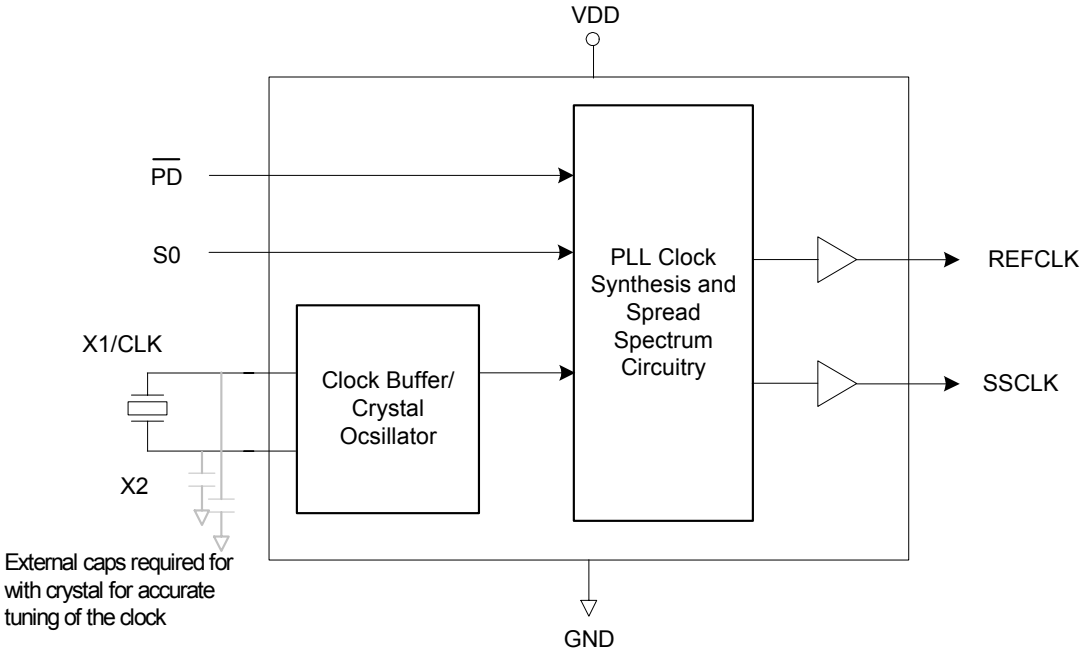
Description

The IDT5V50009 generates a low EMI output clock and a reference clock from a clock or crystal input. The part is designed to lower EMI through the application of spreading a clock. Using IDT's proprietary mix of analog and digital Phase-Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output, reducing the frequency amplitude peaks by several dB depending on spread range. The IDT5V50009 offers a range of down spread from a high speed clock or crystal input. The IDT5V50009 generates one modulated (SSCLK) and unmodulated (REFCLK) clock. The modulated clock is controlled by the select pin, and the unmodulated clock has the same frequency as the input clock or crystal.

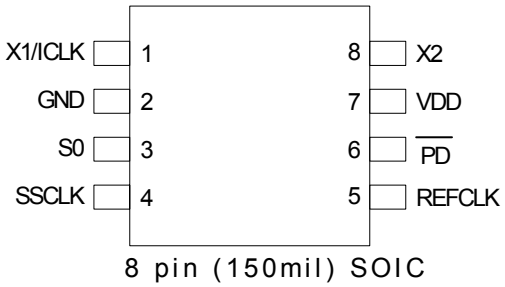
Features

- Packaged in 8-pin SOIC
- Available in Pb (lead) free package
- Input frequency range 20- 40 MHz
- Provides modulated and unmodulated clocks
- Accepts a clock or crystal input
- Provides down spread modulation
- Provides power down function
- Reduce electromagnetic interference (EMI) by 8-16 db
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



8 pin (150mil) SOIC

Spread Percentage Select Table

S0	Spread Direction	Spread Percentage (%)
0	Down	-1.25
1	Down	-1.75

0 = connect to GND

1 = connect directly to VDD
* Default has internal pull up resistor to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Connect to a 20 to 40 MHz crystal or clock.
2	GND	Power	Connect to ground.
3	S0	Input	Select spread percentage per table above. Weak Internal pull-up.
4	SSCLK	Output	Spread spectrum clock output per table above. Weak Internal Pull down
5	REFCLK	Output	CMOS level clock output matches the nominal frequency of the input crystal or clock. Weak Internal Pull down
6	$\overline{PD}$	Input	Power down tri-state. This pin powers down entire chip and tri-state the outputs when low. Weak Internal pull-up.
7	VDD	Power	Connect to 3.3 V.
8	X2	Input	Connect to a 20 to 40 MHz crystal or leave unconnected.

External Components

The IDT5V50009 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT5V50009. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

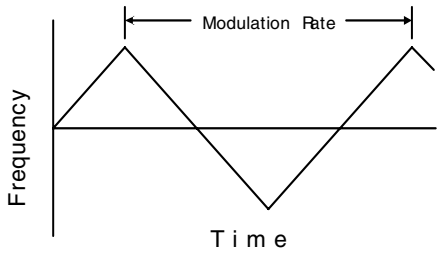
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Spread Spectrum Profile

The IDT5V50009 low EMI clock generator uses an optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices. The frequency modulation amplitude is constant with variations of the input frequency.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V50009. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+2.97		3.63	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Power Supply Range	V_{DD}		2.97	3.3	3.63	V
Input High Voltage	V_{IH}	S0 Input	2.0			V
Input Low Voltage	V_{IL}	S0 Input	0.0	0.0	0.8	V
Output High Voltage	V_{OH}	I_{OH} =-12 ma, SSCLK and REFCLK	2.4			V
Output Low Voltage	V_{OL}	I_{OL} =12ma, SSCLK			0.4	V
Power Supply Current. Operating	I_{DD}	F_{IN} =32 MHz, no load		19.0	23.0	mA
Power Supply Current Stand by	I_{DD}	$\overline{PD}$ = GND		150	250	µA
Input Capacitance	C_{IN}			5		pF
Clock Output Impedance				20		ohms
Internal Pull-up Resistor	R_{PU}	So, $\overline{PD}$		550		kΩ
Internal Pull-down Resistor	R_{Pd}	SSCLK		240		kΩ

AC Electrical Characteristics

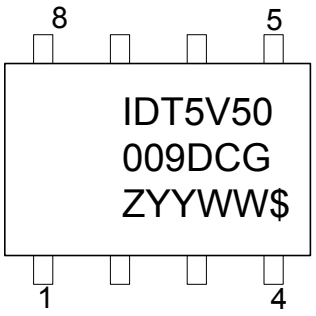
Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency			20		40	MHz
Output Clock Frequency			20		40	MHz
Clock Rise Time	trise1	SSCLK and REFCLK, 0.8 V to 2.0 V		0.75		ns
Clock Fall Time	tfall1	SSCLK and REFCLK, 0.8 V to 2.0 V		0.75		ns
Output Clock Duty Cycle		SSCLK and REFCLK @1.65V	45	50	55	%
Cycle-to-Cycle Jitter		SSCLK, Fin=27MHz, Fout=27MHz		250	350	ps
Cycle-to-Cycle Jitter		REFCLK, Fin=27MHz, Fout=27MHz		275	375	ps
Modulation rate		Input/512	39		78	kHz
EMI Peak Frequency Reduction				8 to 16		dB

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		°C/W
	θ_{JA}	1 m/s air flow		100		°C/W
	θ_{JA}	3 m/s air flow		80		°C/W
Thermal Resistance Junction to Case	θ_{JC}			35		°C/W

Marking Diagram (Pb free)

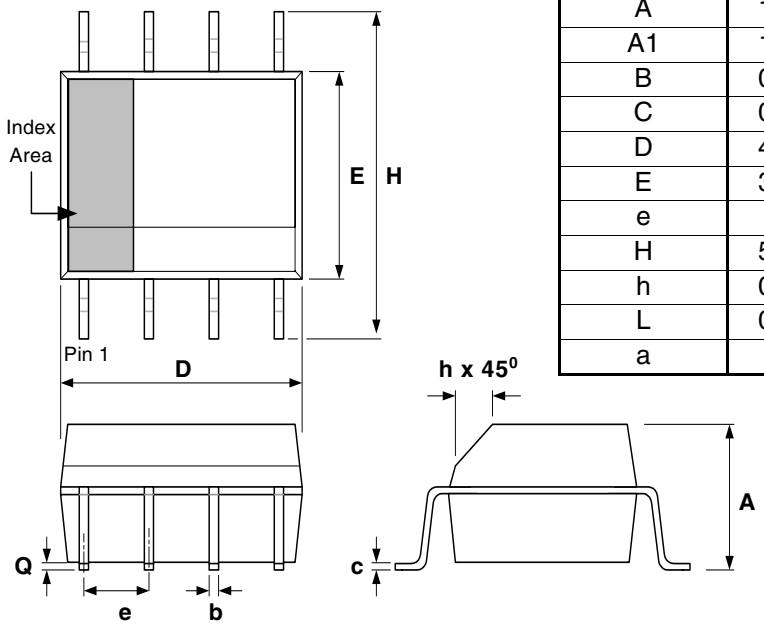


Notes:

1. “Z” is the device step (1 to 2 characters).
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “$” is the assembly mark code.
4. “G” after the two-letter package code designates RoHS compliant package.
5. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	1.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	0.1497	0.1574
e	1.27 Basic		0.050 Basic	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
a	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V50009DCG	See page 6	Tubes	8-pin SOIC	0 to +70° C
5V50009DCG8		Tape and Reel	8-pin SOIC	0 to +70° C

Parts that are ordered with a "G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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