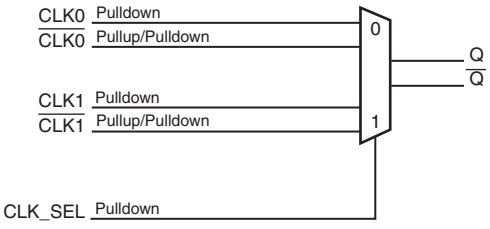
Description

The ICS85401 is a high performance 2:1 Differential-to-LVDS Multiplexer and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS. The ICS85401 can also perform differential translation because the differ-ential inputs accept LVPECL, CML as well as LVDS levels.
The ICS85401 is packaged in a small 3mm x 3mm 16 VFQFN package, making it ideal for use on space constrained boards.

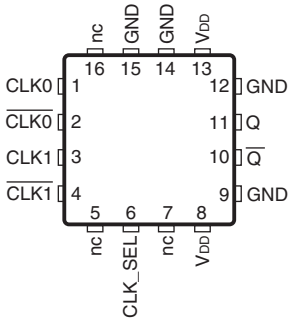
Features

- 2:1 LVDS MUX
- One LVDS output pair
- Two differential clock inputs can accept: LVPECL, LVDS, CML
- Maximum input/output frequency: 2.5GHz
- Translates LVCMOS/LVTTL input signals to LVDS levels by using a resistor bias network on nCLK0, nCLK1
- Propagation delay: 460ps (maximum)
- Part-to-part skew: 100ps (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS85401

16-Lead VFQFN
3mm x 3mm x 0.95mm
package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK0	Input	Pulldown	Non-inverting differential clock input.
2	$\overline{CLK0}$	Input	Pullup/ Pulldown	Inverting differential clock input. VDD/2 default when left floating.
3	CLK1	Input	Pulldown	Non-inverting differential clock input.
4	$\overline{CLK1}$	Input	Pullup/ Pulldown	Inverting differential clock input. VDD/2 default when left floating.
5, 7, 16	nc	Unused		No connect.
6	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, $\overline{CLK1}$ inputs. When LOW, selects CLK0, $\overline{CLK0}$ inputs. LVCMOS / LVTTL interface levels.
8, 13	V_{DD}	Power		Power supply pins.
9, 12, 14, 15	GND	Power		Power supply ground.
10, 11	$\overline{Q}$, Q	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to intenal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			1		pF
R_{PULLUP}	Input Pullup Resistor			37		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			37		kΩ

Function Tables

Table 3. Control Input Function Table

Input	CLK_OUT
CLK_SEL	CLK
0	CLK0, $\overline{CLK0}$
1	CLK1, $\overline{CLK1}$

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characterisitcs* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	51.5°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				40	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1	V_{DD} = V_{IN} = 3.465V			150	µA
		$\overline{CLK0}$, $\overline{CLK}$	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		$\overline{CLK0}$, $\overline{CLK}$	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15	0.8	1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for CLKx, $\overline{CLKx}$ is V_{DD} + 0.3V.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200	350	500	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.05	1.15	1.25	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

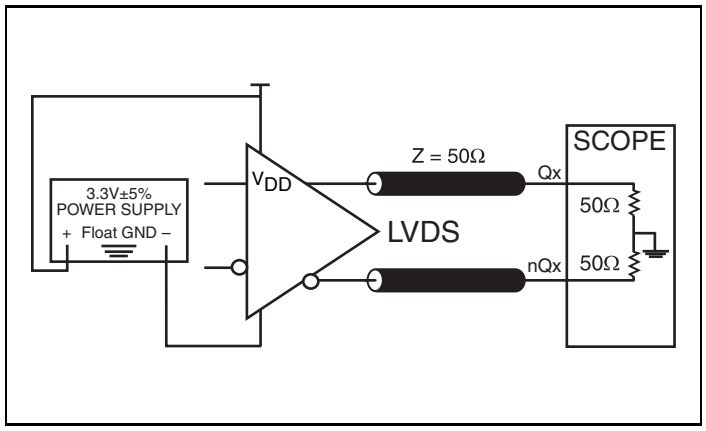
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

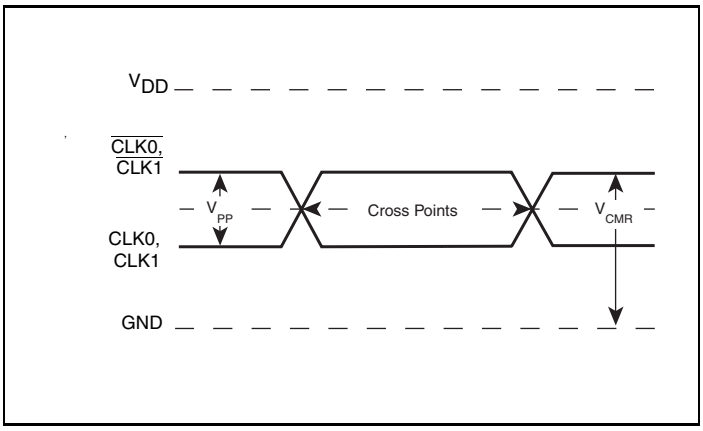
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		260	360	460	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				100	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	125	160	200	ps
odc	Output Duty Cycle		49		51	%
$MUX_{\_ISOLATION}$	MUX Isolation			-55		

All parameters measured at £ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.Typical Phase Noise at 156.25MHz

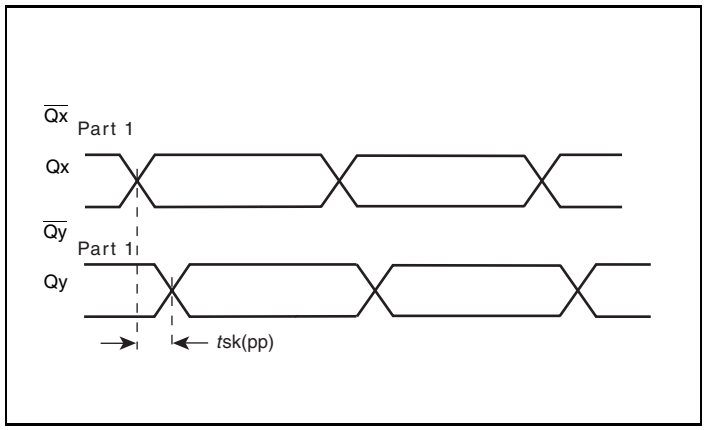
Parameter Measurement Information



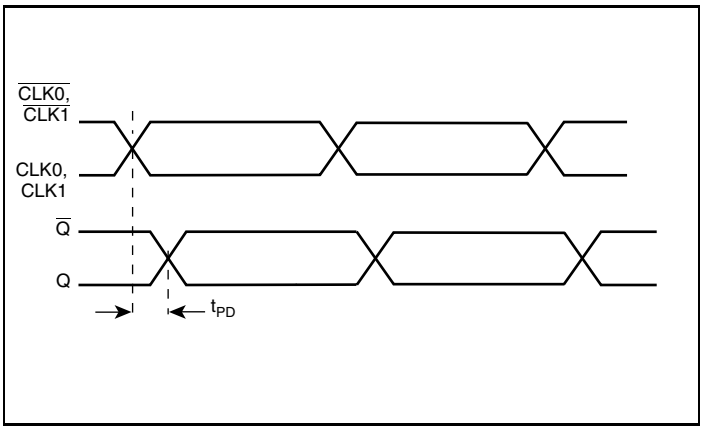
3.3V LVDS Output Load AC Test Circuit



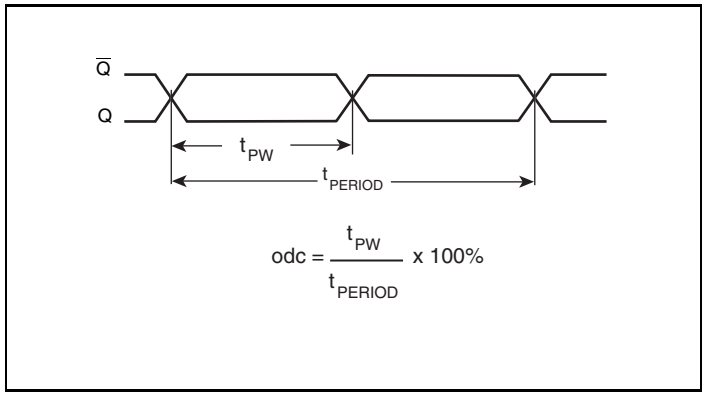
Differential Input Level



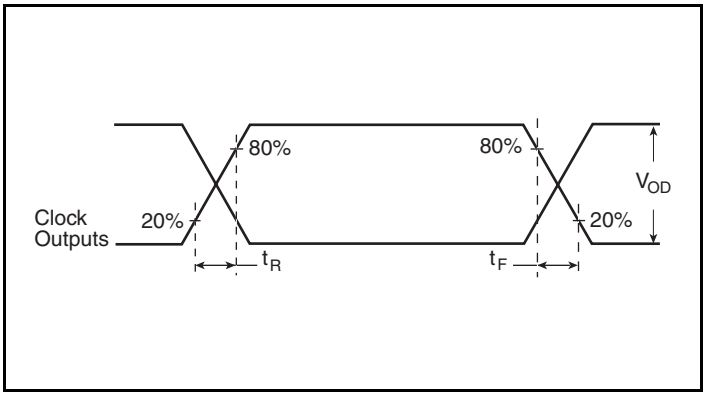
Part-to-Part Skew



Propagation Delay

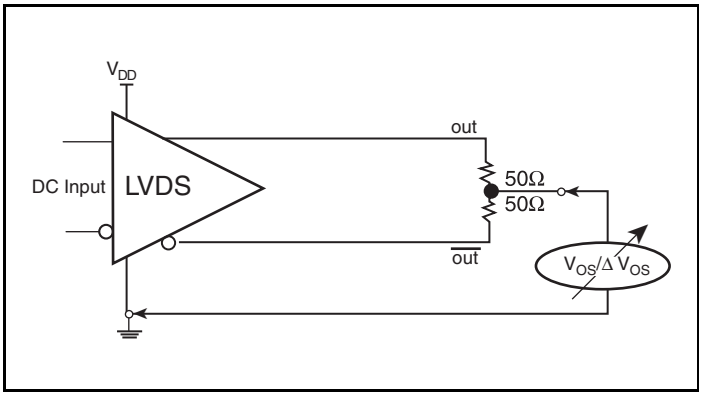


Output Duty Cycle/Pulse Width/Period

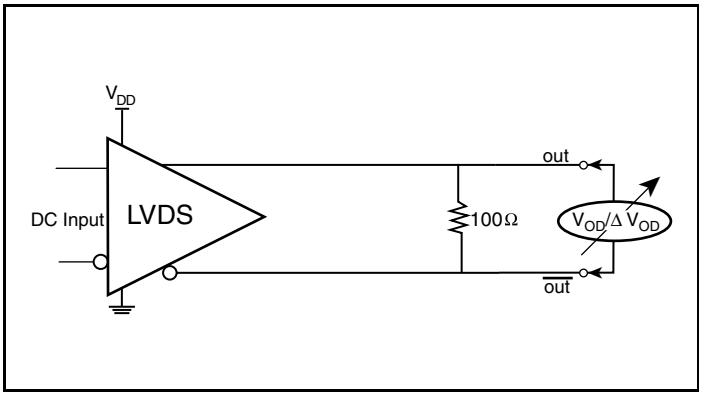


Output Rise/Fall Time

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

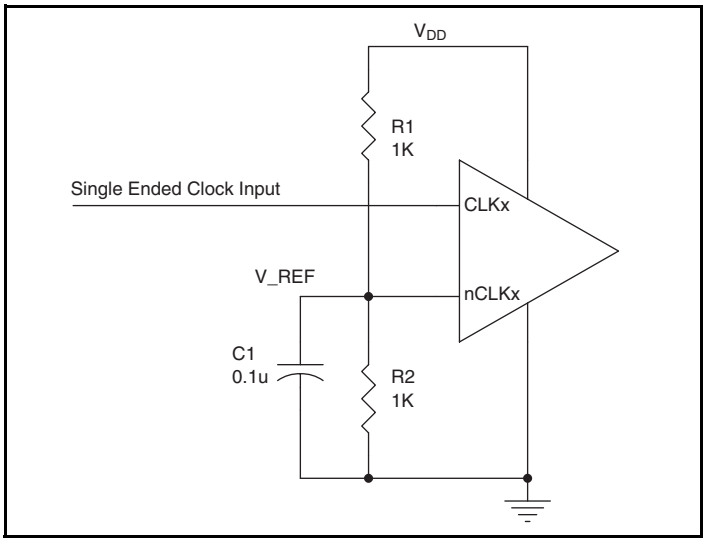


Figure 1. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLKx /$\overline{CLKx}$ accepts LVPECL, LVDS, CML and other differential signals. The signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS CLKx/$\overline{CLKx}$ input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

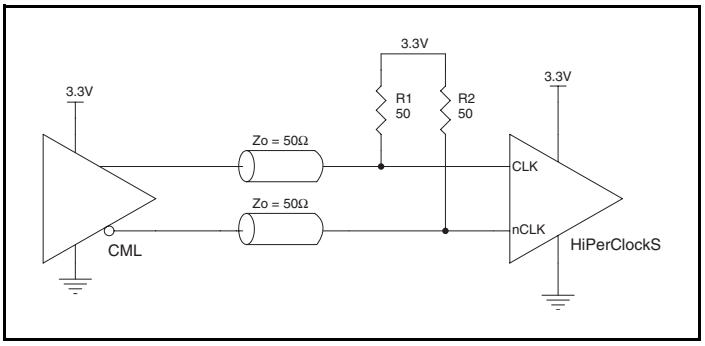


Figure 2A. HiPerClockS CLK/$\overline{CLK}$ Input Driven by an IDT Open Collector CML Driver

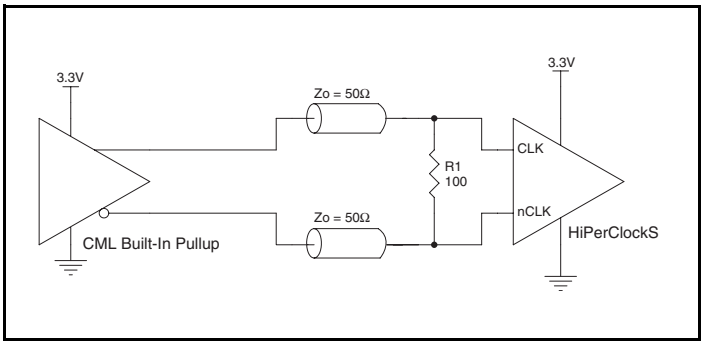


Figure 2B. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a Built-In Pullup CML Driver

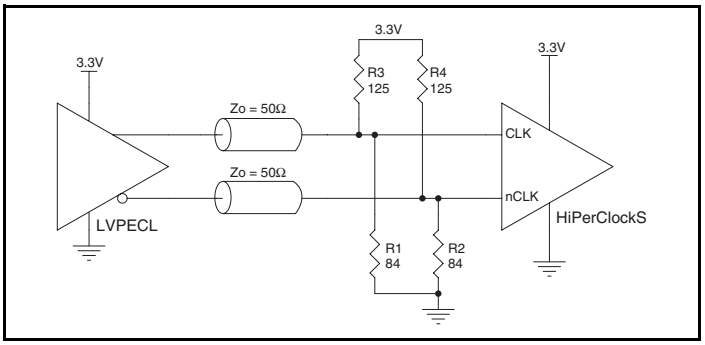


Figure 2C. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

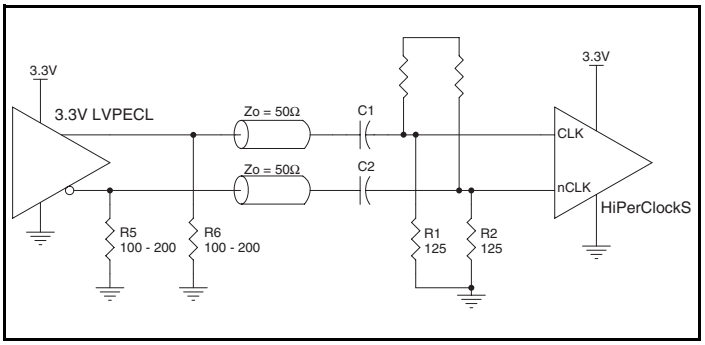


Figure 2D. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver with AC Couple

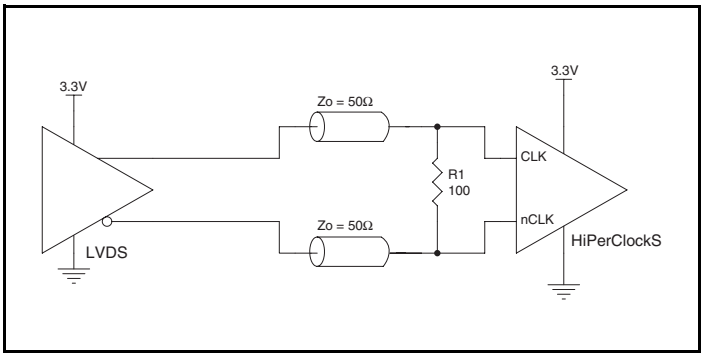


Figure 2E. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVDS Drive

Recommendations for Unused Input Pins

Inputs:

CLK/$\overline{CLK}$ Inputs:

For applications not requiring the use of the differential input, both CLK and $\overline{CLK}$ can be left floating. Though not required, but for additional protection, a 1kW resistor can be tied from CLK to ground.

Application Schematic Example

Figure 3 shows an example of ICS85401 application schematic. This device can accept different types of input signal. In this example, the input is driven by a LVDS driver. The decoupling capacitor should be located as close as possible to the power pin.

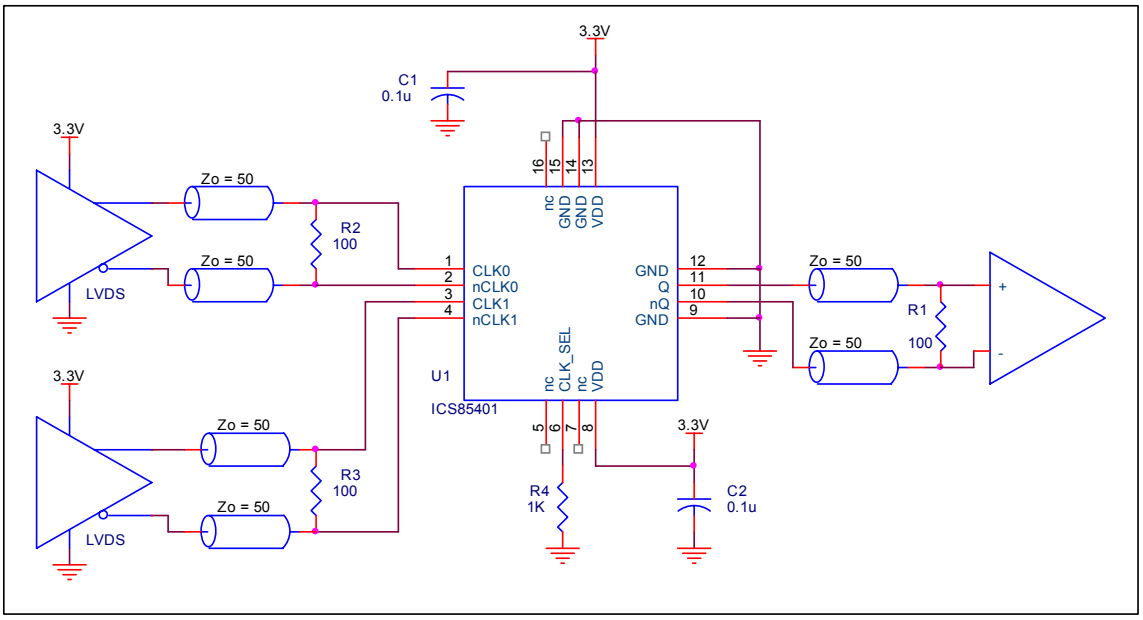


Figure 3. ICS85401 Application Schematic Example

Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 4.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

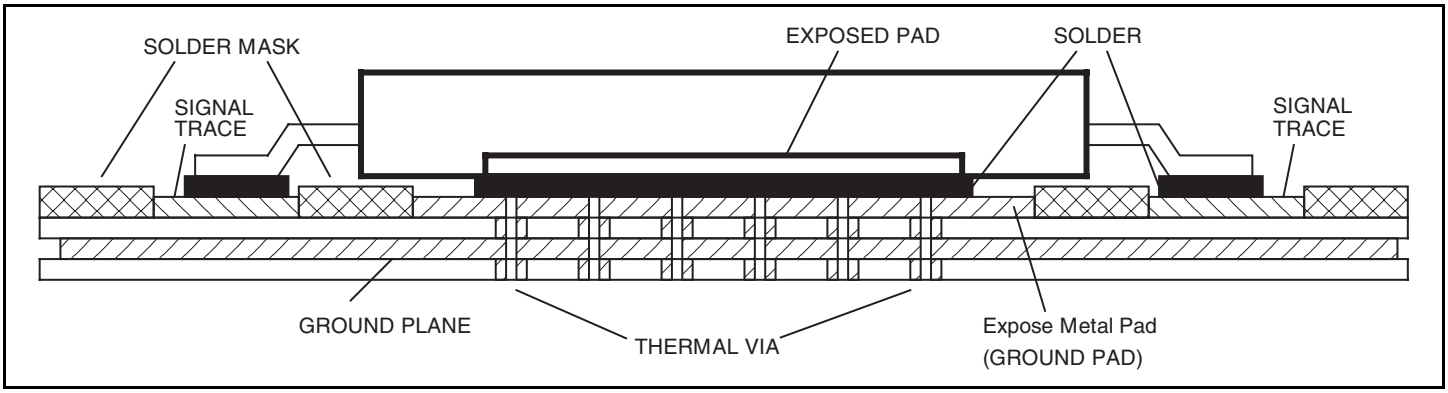


Figure 4. P.C. Board for Exposed Pad Thermal Release Path Example

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 5* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

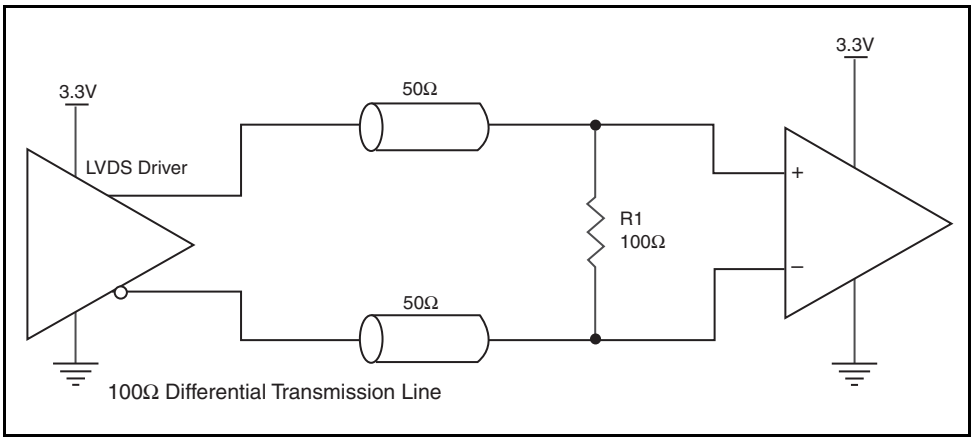


Figure 5. Tyical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS85401.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85401 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power$_{_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 40mA = **138.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.139W * 51.5°C/W = 92.2°C. This iswell below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resitance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} **by Velocity**			
Linear Feet per Minute	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W		

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Linear Feet per Minute	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W		

Transistor Count

The transistor count for ICS85401 is: 132

Package Outline and Package Dimension

Package Outline - K Suffix for 16 Lead VFQFN

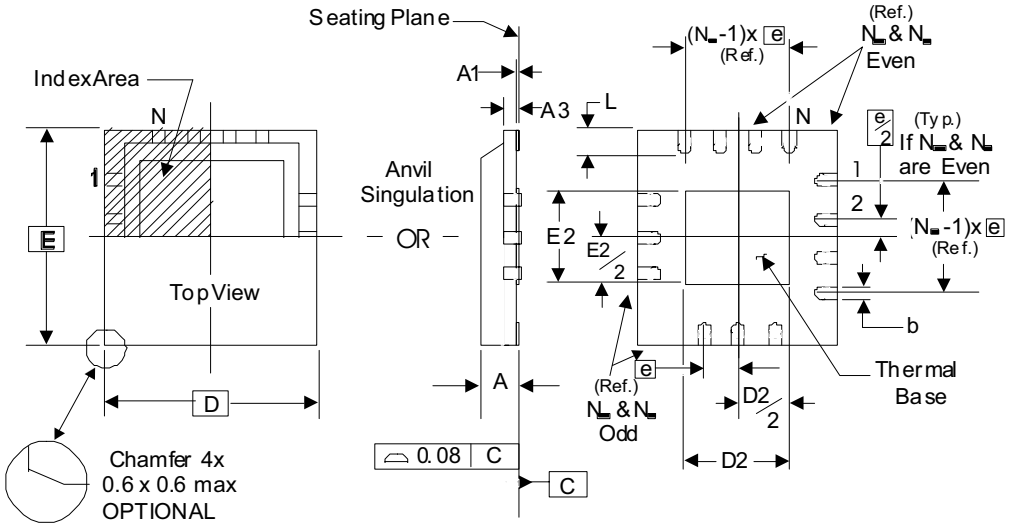


Table 8. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85401AK	401A	16 Lead VFQFN	Tube	-40°C to 85°C
85401AKT	401A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
85401AKLF	01AL	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
85401AKLFT	01AL	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		8	Add Schematic Layout.	8/23/04
A	T8	10	Corrected count in Ordering Information Table.	11/17/04
A		1	Pin Assignment - corrected label on pin 2.	2/22/05
A	T8	1 11	Features section - added Lead-Free bullet. Ordering Information Table - corrected Shipping Packaging from Tray to Tube, and added Lead-Free part number and note.	3/14/06
A	T9	7 10 13	Corrected *Differential Clock Input Interface.* Added *Power Considerations* Section. Ordering Information Table - added Lead-Free marking. Updated format throughout the datasheet.	3/6/07

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