

# FEMTOCLOCKS™ VCXO BASED FREQUENCY TRANSLATOR/JITTER ATTENUATOR

ICS843002-31

## GENERAL DESCRIPTION



The ICS843002-31 is a member of the HiPerClockS™ family of high performance clock solutions from IDT. This monolithic device is a high-performance, PLL-based synchronous clock generator and jitter attenuation circuit. The ICS843002-31 contains two clock multiplication stages that are cascaded in series. The first stage is a VCXO-based PLL that is optimized to provide reference clock jitter attenuation, to be jitter tolerant, and to provide a stable reference clock for the second multiplication stage. The second stage is the proprietary IDT FemtoClock™ circuit which is a high-frequency, sub-picosecond clock multiplier.

The VCXO PLL has an on-chip VCXO circuit that uses an external, inexpensive pullable crystal in the 17.5 to 25MHz range. The PLL includes 13 bit reference and feedback dividers supporting complex PLL multiplication ratios and input reference clock rates as low as 2.3kHz. External loop filter components are used (two resistors and two capacitors) to achieve the low loop bandwidth needed for jitter attenuation of a recovered data clock.

The FemtoClock circuit can multiply the VCXO crystal frequency by a factor of 28 or 32 (selectable) and provide a clock output of up to 700MHz.

### Clock Input/Output Configuration:

- Clock Inputs - one differential pair, two singled ended (mux selected)
  - Differential input pair can support LVPECL, LVDS, LVHSTL, SSTL, HCSL or single-ended LVCMOS or LVTTTL levels
  - Singled ended inputs can support LVCMOS or LVTTTL levels
- Clock Outputs, FemtoClockS two LVPECL pairs (selectable output dividers)
- Clock Output, VCXO – one single ended output (at VCXO crystal frequency)
- Clock Output, other – VCXO reference clock

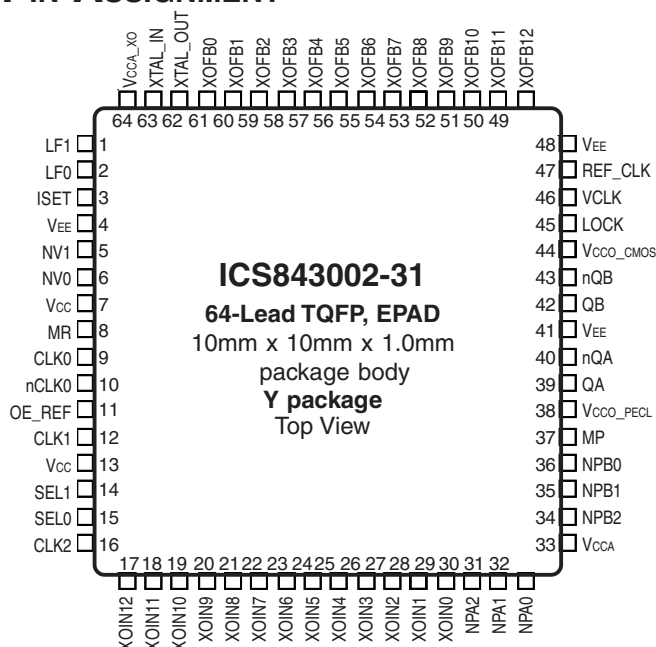
### Example Applications:

- SONET/SDH line card clock generator (up to 622.08MHz for OC-48) using 8kHz frame clock as input reference
- Jitter attenuation of a recovered communications clock
- Complex-ratio clock frequency translation between various communication protocols, such as:
  - For telecom, OC-12 to E3 rate conversion, 622.08MHz to 34.368MHz, PLL ratio of 179/32
  - For digital video, ITU-R601 to SMPTE 252M/59.94, 27MHz to 74.17582MHz, PLL ratio of 250/91

## FEATURES

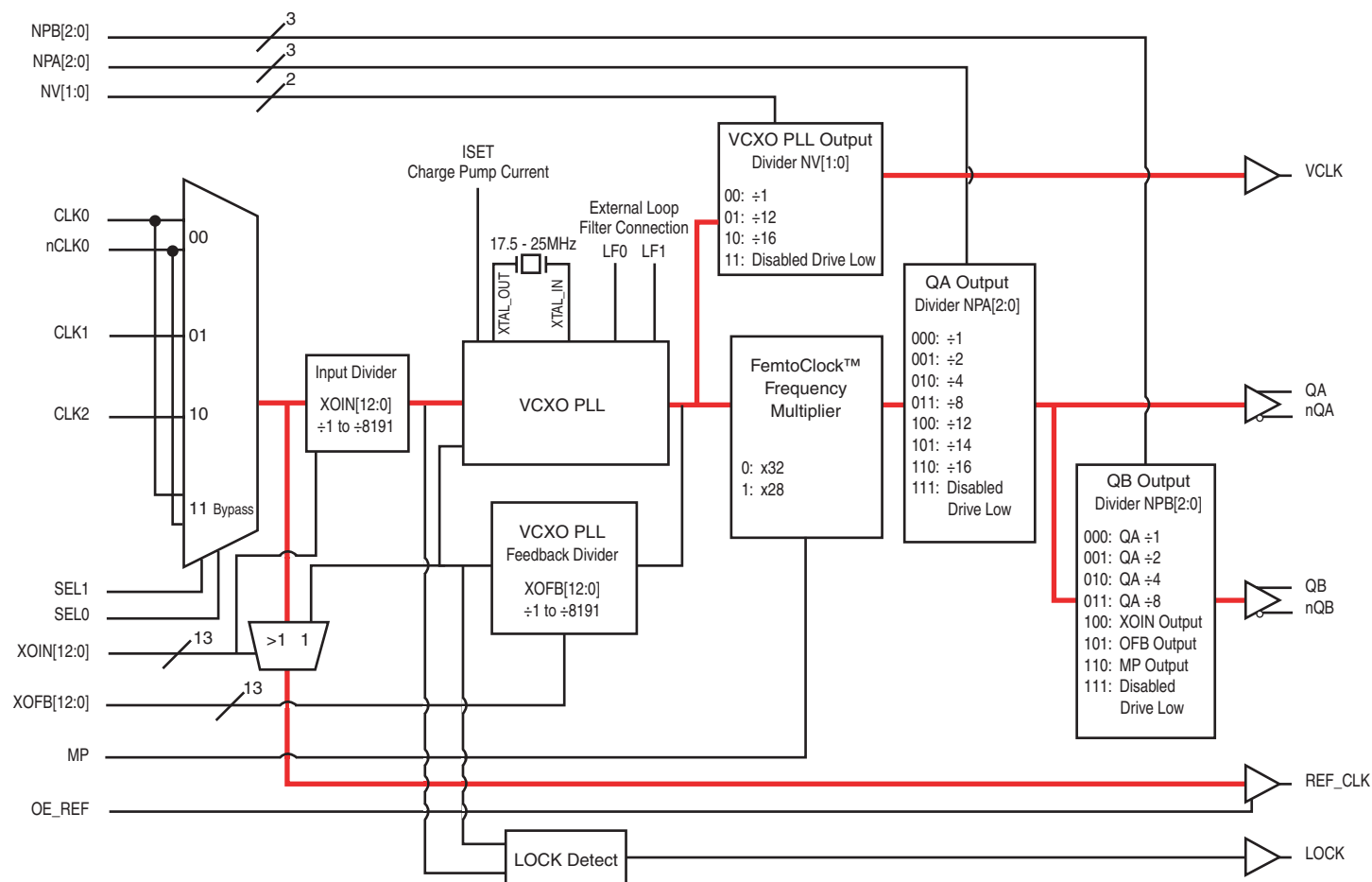
- Outputs:
  - Two high frequency differential LVPECL outputs  
Output frequency: up to 700MHz
  - One LVCMOS/LVTTL VCXO PLL output with output enable
  - One Reference clock output with output enable
  - One LOCK detect output
- Input mux supports 3 selectable inputs: one differential input pair and two LVCMOS/LVTTL input clocks
- 13-bit VCXO PLL feedback and reference dividers provide wide range of frequency translation ratio options
- FemtoClock frequency multiplier supports rate of: 560MHz - 700MHz
- 'Lock Detect' output reports lock status of VCXO PLL
- VCXO PLL circuit provides jitter attenuation with loop bandwidth of 250Hz and below (user adjustable)
- RMS phase jitter, random at 12kHz to 20MHz: <1ps (design target)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## PIN ASSIGNMENT



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

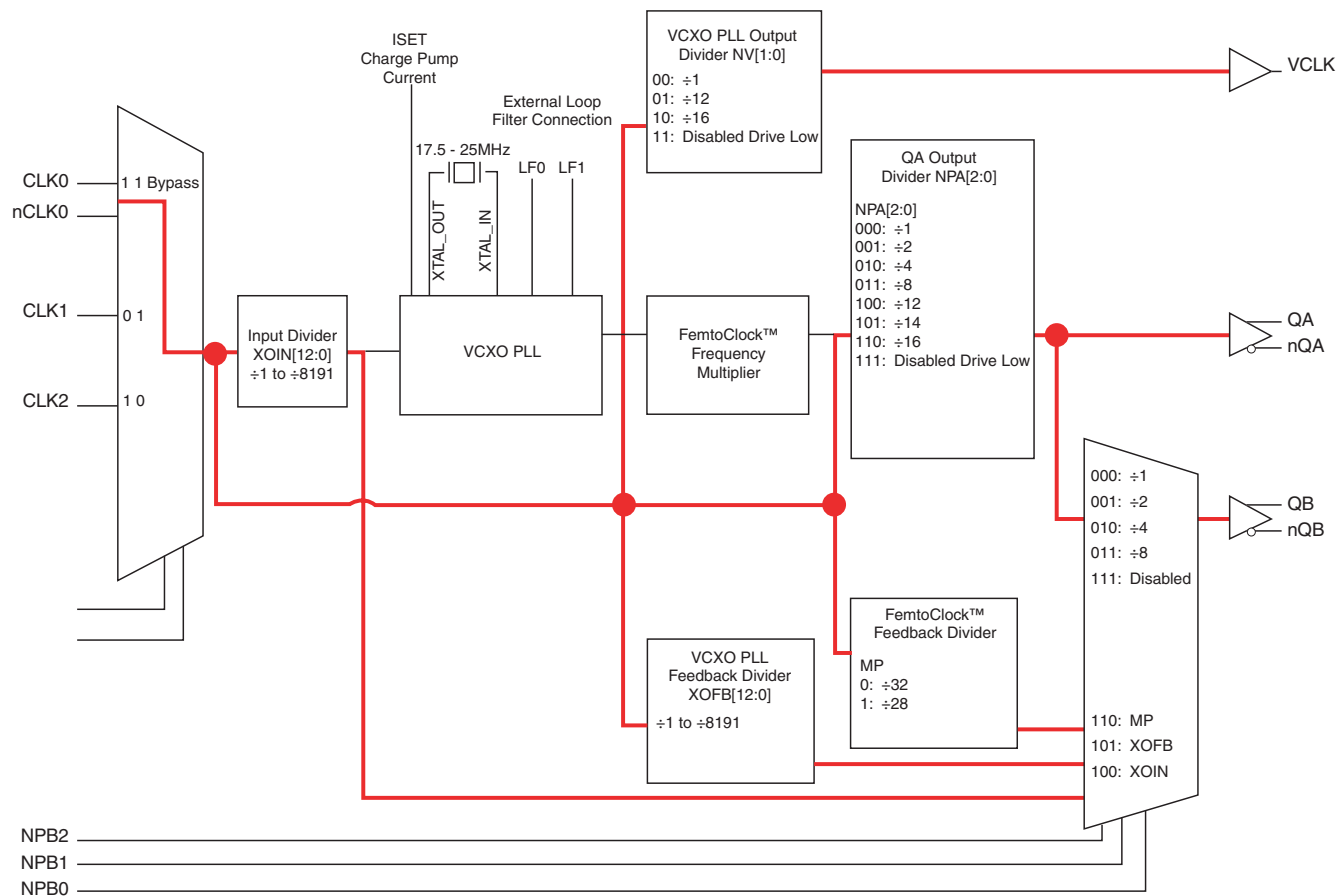
## BLOCK DIAGRAM - NOMINAL SYSTEM CONFIGURATION



NOTE 1: For application configuration (non-test/bypass modes).

NOTE 2: Bold lines — are primary clock paths (non-control/non-feedback lines). Not all control lines and signal paths are shown in this simplified block diagram.

## SIMPLIFIED BLOCK DIAGRAM - CLOCK SIGNAL PATHS IN BYPASS MODE



NOTE 1: Setting SEL1:SEL0 = 11 enables bypass mode. Only clock signals on the CLK0/nCLK0 input pair are routed to the device in bypass mode.

NOTE 2: Bold lines **—** show clock bypass paths. Not all control lines and signal paths are shown in this simplified block diagram.

TABLE 1. PIN DESCRIPTIONS (CONTINUED ON NEXT PAGE)

| Number                                                        | Name                  | Type                |                     | Description                                                                                                                                                                                |
|---------------------------------------------------------------|-----------------------|---------------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2                                                          | LF1, LF0              | Analog Input/Output |                     | Loop filter connection pins.                                                                                                                                                               |
| 3                                                             | ISSET                 | Analog Input/Output |                     | Charge pump current setting pin.                                                                                                                                                           |
| 4, 41, 48                                                     | V <sub>EE</sub>       | Power               |                     | Negative supply pins. Normally connected to ground.                                                                                                                                        |
| 5, 6                                                          | NV1, NV0              | Input               | Pullup              | VCXO PLL output divider control pins. LVC MOS/LVTTL interface levels.                                                                                                                      |
| 7, 13                                                         | V <sub>CC</sub>       | Power               |                     | Core power supply pins.                                                                                                                                                                    |
| 8                                                             | MR                    | Input               | Pulldown            | Master Reset. When HIGH, resets all internal dividers and LVC MOS outputs are in high impedance. LVC MOS / LVTTL interface levels.                                                         |
| 9                                                             | CLK0                  | Input               | Pulldown            | Non-inverting differential clock input.                                                                                                                                                    |
| 10                                                            | nCLK0                 | Input               | Pullup/<br>Pulldown | Inverting differential clock input. V <sub>CC</sub> /2 bias voltage when left floating.                                                                                                    |
| 11                                                            | OE_REF                | Input               | Pulldown            | Output enable control for reference clock output. When logic LOW, the reference clock output is in high impedance. When logic HIGH, the output is enabled. LVC MOS/LVTTL interface levels. |
| 12                                                            | CLK1                  | Input               | Pulldown            | Clock input. LVC MOS/LVTTL interface levels.                                                                                                                                               |
| 14, 15                                                        | SEL1, SEL0            | Input               | Pulldown            | Input clock select. LVC MOS/LVTTL interface levels.                                                                                                                                        |
| 16                                                            | CLK2                  | Input               | Pulldown            | Clock input. LVC MOS/LVTTL interface levels.                                                                                                                                               |
| 17, 18,<br>19, 20,<br>21, 22,<br>23, 24,<br>25, 26,<br>27, 28 | XOIN12:XOIN1          | Input               | Pulldown            | VCXO PLL input divider control input. LVC MOS/LVTTL interface levels.                                                                                                                      |
| 29                                                            | XOIN0                 | Input               | Pullup              | VCXO PLL input divider control input. LVC MOS/LVTTL interface levels.                                                                                                                      |
| 30, 31,<br>32                                                 | NPA2, NPA1,<br>NPA0   | Input               | Pulldown            | LVPECL output divider control for QA/nQA outputs. LVC MOS/LVTTL interface levels.                                                                                                          |
| 33                                                            | V <sub>CCA</sub>      | Power               |                     | Analog supply pin.                                                                                                                                                                         |
| 34, 35,<br>36                                                 | NPB2, NPB1,<br>NPB0   | Input               | Pulldown            | LVPECL output divider control for QB/nQB outputs. LVC MOS/LVTTL interface levels.                                                                                                          |
| 37                                                            | MP                    | Input               | Pulldown            | FemtoClock™ circuit clock multiplication control input. When HIGH, selects 28. When LOW, selects 32. LVC MOS/LVTTL interface levels.                                                       |
| 38,                                                           | V <sub>CCO_PECL</sub> | Power               |                     | Output power supply pin for LVPECL clock outputs.                                                                                                                                          |
| 39, 40                                                        | QA, nQA               | Output              |                     | Differential clock output pair. LVPECL interface levels.                                                                                                                                   |
| 42, 43                                                        | QB, nQB               | Output              |                     | Differential clock output pair. LVPECL interface levels.                                                                                                                                   |
| 44                                                            | V <sub>CCO_CMOS</sub> | Power               |                     | Output power supply pin for LVC MOS outputs.                                                                                                                                               |
| 45                                                            | LOCK                  | Output              |                     | Lock detect output. LVC MOS/LVTTL interface levels.                                                                                                                                        |
| 46                                                            | VCLK                  | Output              |                     | VCXO PLL clock output. LVC MOS/LVTTL interface levels.                                                                                                                                     |
| 47                                                            | REF_CLK               | Output              |                     | Reference clock output. LVC MOS/LVTTL interface levels.                                                                                                                                    |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 1. PIN DESCRIPTIONS (CONTINUED FROM PREVIOUS PAGE)

| Number                                                        | Name                 | Type  |          | Description                                                                         |
|---------------------------------------------------------------|----------------------|-------|----------|-------------------------------------------------------------------------------------|
| 49, 50,<br>51, 52,<br>53, 54,<br>55, 56,<br>57, 58,<br>59, 60 | XOFB12:XOFB1         | Input | Pulldown | VCXO feedback divider control input.<br>LVCMOS/LVTTL interface levels.              |
| 61                                                            | XOFB0                | Input | Pullup   | VCXO feedback divider control input.<br>LVCMOS/LVTTL interface levels.              |
| 62, 63                                                        | XTAL_OUT,<br>XTAL_IN | Input |          | VCXO crystal oscillator interface. XTAL_IN is the input.<br>XTAL_OUT is the output. |
| 64                                                            | V <sub>CCA_XO</sub>  | Power |          | Analog power supply pin for VCXO.                                                   |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol                | Parameter                                            | Test Conditions                                                                                                      | Minimum | Typical | Maximum | Units |
|-----------------------|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                                    |                                                                                                                      |         | 4       |         | pF    |
| C <sub>PD</sub>       | Power Dissipation Capacitance<br>(per LVCMOS output) | V <sub>CC</sub> , V <sub>CCA</sub> , V <sub>CCA_XO</sub> , V <sub>CCO_CMOS</sub> ,<br>V <sub>CCO_PECL</sub> = 3.465V |         | TBD     |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                                |                                                                                                                      |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                              |                                                                                                                      |         | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance                                     |                                                                                                                      |         | 7       |         | Ω     |

## SECTION 1. FREQUENCY TRANSLATION

The ICS843002-31 is a two stage device, a VCXO PLL stage followed by a low phase noise FemtoClock multiplier stage. The VCXO uses a pullable crystal to lock to the reference clock and can provide an output frequency up to 25MHz on the single-ended VCLK output. For higher frequencies, the low phase noise FemtoClock can multiply the VCXO PLL output clock up to 700MHz on 2 differential LVPECL output pairs (QA/nQA, QB/nQB).

The VCXO PLL stage has a 13-bit input divider and a 13-bit feedback divider to generate large integer ratios needed for some frequency translation applications. When configuring the device is to use pullable crystals in the 17.5MHz – 25MHz range on the VCXO PLL stage, and ensure that the FemtoClock PLL is kept within its range of 560MHz to 700MHz.

Below are 3 examples:

### 1. 8kHz to 622.08MHz and 155.52MHz

This frequency translation requires use of both the VCXO PLL and the FemtoClock circuit. The VCXO PLL can be used to multiply up to 19.44MHz for use as a reference clock for the FemtoClock which will do the multiplication from 19.44MHz to 622.08MHz.

- ➔ Using a 19.44MHz pullable crystal on XTAL\_IN/XTAL\_OUT, set the VCXO PLL feedback divider pins, XOFB[12:0], to 2430. This multiplies the 8kHz reference clock to 19.44MHz.
- ➔ Set the FemtoClock multiplication control pin, MP, to 0 which sets the multiplication factor to 32. This sets the FemtoClock VCO to 622.08MHz.
- ➔ Set the QA/nQA output divider control pins, NPA[2:0] = 000 for divide by 1. This sets the QA/nQA LVPECL output pair for 622.08MHz.

- ➔ Set the QB/nQB output divider control pins, NPB[2:0] = 010 for divide by 4. This sets the QB/nQB LVPECL output pair for 155.52MHz.

### 2. T1 to T3. (1.544MHz to two 44.736MHz outputs)

Since 44.736MHz is slightly higher than the maximum VCXO output frequency, the FemtoClock circuit will have to be used.

- ➔ Using a pullable 22.368MHz on XTAL\_IN/XTAL\_OUT, set the VCXO PLL feedback divider pins, XOFB[12:0] to 2796 and the input divider pins, XOIN[12:0] to 193. This multiplies the 1.544MHz reference to 22.368MHz ( $1.544\text{MHz} * 2796/193 = 22.368\text{MHz}$ ).
- ➔ Set the FemtoClock multiplication control pin, MP, to 28 which sets the VCO at 626.304MHz.
- ➔ Set the QA/nQA output divider control pins, NPA[2:0] = 101 for divide by 14. This sets the QA/nQA LVPECL output pair for 44.736MHz.
- ➔ Set the QB/nQB output divider control pins, NPB[2:0] = 000 for divide by 1. This sets the QB/nQB LVPECL output pair for 44.736MHz.

### 3. T1 to E1. (1.544MHz to two 2.048MHz outputs)

The 2.048MHz output frequency requirement is low enough that the FemtoClock circuit is not required. Only the VCXO stage is used for this frequency translation.

- ➔ Using a pullable 24.576MHz on XTAL\_IN/XTAL\_OUT, set the VCXO PLL feedback divider pins, XOFB[12:0] to 3072 and the input divider pins, XOIN[12:0] to 193. This multiplies the 1.544MHz reference to 2.048MHz ( $1.544\text{MHz} * 3072/193 = 2.048\text{MHz}$ ).
- ➔ Set the VCXO PLL Output Divider control pins, NV[1:0] = 01 for /12. This divides the 24.576MHz VCXO PLL frequency down to 2.048MHz.

## SECTION 2. FREQUENCY CONFIGURATION

The Frequency Configuration Table Examples (see the following pages) are intended to show the most common frequency translation requirements. It is sorted in order of descending input frequency. It is not intended to be an exhaustive configuration table because that would be impractical with almost 3 billion possible configurations. As far as configuration is concerned, frequencies  $\leq 25\text{MHz}$  can be generated with the VCXO PLL while frequencies  $> 25\text{MHz}$  require the use of the downstream FemtoClock which can multiply the VCXO PLL output up to 700MHz. Complex integer ratios are handled with the VCXO PLL stage and the FemtoClock circuit can be configured to multiply the VCXO PLL output by 32 or 28. The following example will illustrate the configuration process.

Assume you have a 1.544MHz T1 clock which needs to be multiplied up to 622.08MHz (OC12). Obviously, the FemtoClock multiplier will be needed to achieve 622.08MHz. Since the FemtoClock has a selectable multiplication factor of 28 or 32,

this means there are 2 viable VCXO PLL crystal choices which fall within its 17.5MHz – 15MHz range: 22.217143MHz (/28 feedback divider) or 19.44MHz (/32 feedback divider). Use of the /28 feedback divider for the FemtoClock multiplier will give slightly better phase noise, but in this case 22.217143/1.544 cannot be exactly achieved with the 13-bit input and feedback VCXO PLL dividers. Using the x32 setting of the FemtoClock allows a ratio of  $19.44/1.544 = 2430/193$  which is easily achievable. So the FemtoClock would be set for x32 and a 19.44MHz crystal would be used. The VCXO PLL input divider would be set for 193 and the VCXO PLL feedback divider would be set for 2430. To double check the solution, perform the following calculation:  $1.544 * 2430 * 32/193 = 622.08\text{MHz}$ .

The 2<sup>nd</sup> FemtoClock multiplier output, QB/nQB, can be set to equal the QA/nQA output frequency or a fraction of its frequency. The following fractional values are available: /1, /2, /4, /8.

TABLE 3A. FREQUENCY CONFIGURATION EXAMPLES, CONTINUED ON NEXT PAGE

| Input Frequency (MHz) | Output Frequency (MHz) | VCXO or FemtoClock Output | Required VCXO Crystal Frequency (MHz) | VCXO Input Divider | VCXO Feedback Divider | VCXO Output Divider | FemtoClock Multiplication Factor | FemtoClock Output Frequency (MHz) | FemtoClock Output Divider | Application                      |
|-----------------------|------------------------|---------------------------|---------------------------------------|--------------------|-----------------------|---------------------|----------------------------------|-----------------------------------|---------------------------|----------------------------------|
| 622.08                | 622.08                 | FemtoClock Output         | 19.44                                 | 32                 | 1                     | N/A                 | 32                               | 622.08                            | 1                         | 622.08 -> 622.08 (OC12)          |
| 622.08                | 311.04                 | FemtoClock Output         | 19.44                                 | 32                 | 1                     | N/A                 | 32                               | 622.08                            | 2                         | 622.08 -> 311.04 (SONET)         |
| 622.08                | 155.52                 | FemtoClock Output         | 19.44                                 | 32                 | 1                     | N/A                 | 32                               | 622.08                            | 4                         | 622.08 -> 155.52 (OC12 to OC3)   |
| 622.08                | 77.76                  | FemtoClock Output         | 19.44                                 | 32                 | 1                     | N/A                 | 32                               | 622.08                            | 8                         | 622.08 -> 77.76 (SONET)          |
| 622.08                | 51.84                  | FemtoClock Output         | 19.44                                 | 32                 | 1                     | N/A                 | 32                               | 622.08                            | 12                        | 622.08 -> 51.84 (OC12 to OC1)    |
| 622.08                | 38.88                  | FemtoClock Output         | 19.44                                 | 32                 | 1                     | N/A                 | 32                               | 622.08                            | 16                        | 622.08 -> 38.88 (SONET)          |
| 622.08                | 19.44                  | VCXO Output               | 19.44                                 | 32                 | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 622.08 -> 19.44 (SONET)          |
| 622.08                | 44.736                 | FemtoClock Output         | 22.368                                | 6480               | 233                   | N/A                 | 28                               | 626.304                           | 14                        | 622.08 -> 44.736 (OC12 to T3)    |
| 622.08                | 34.368                 | VCXO Output               | 34.368                                | 3240               | 179                   | 1                   | N/A                              | N/A                               | N/A                       | 622.08 -> 34.368 (OC12 to E3)    |
| 622.08                | 32.064                 | VCXO Output               | 32.064                                | 3240               | 167                   | 1                   | N/A                              | N/A                               | N/A                       | 622.08 -> 32.064 (OC12 to J3)    |
| 622.08                | 2.048                  | VCXO Output               | 24.576                                | 405                | 16                    | 12                  | N/A                              | N/A                               | N/A                       | 622.08 -> 2.048 (OC12 to E1)     |
| 622.08                | 1.544                  | VCXO Output               | 24.704                                | 4860               | 193                   | 16                  | N/A                              | N/A                               | N/A                       | 622.08 -> 1.544 (OC12 to T1/J1)  |
| 311.04                | 311.04                 | FemtoClock Output         | 19.44                                 | 16                 | 1                     | N/A                 | 32                               | 622.08                            | 2                         | 311.04 -> 311.04 (SONET)         |
| 311.04                | 155.52                 | FemtoClock Output         | 19.44                                 | 16                 | 1                     | N/A                 | 32                               | 622.08                            | 4                         | 311.04 -> 155.52 (SONET)         |
| 311.04                | 77.76                  | FemtoClock Output         | 19.44                                 | 16                 | 1                     | N/A                 | 32                               | 622.08                            | 8                         | 311.04 -> 77.76 (SONET)          |
| 311.04                | 51.84                  | FemtoClock Output         | 19.44                                 | 16                 | 1                     | N/A                 | 32                               | 622.08                            | 12                        | 311.04 -> 51.84 (SONET)          |
| 311.04                | 38.88                  | FemtoClock Output         | 19.44                                 | 16                 | 1                     | N/A                 | 32                               | 622.08                            | 16                        | 311.04 -> 38.88 (SONET)          |
| 311.04                | 19.44                  | VCXO Output               | 19.44                                 | 16                 | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 311.04 -> 19.44 (SONET)          |
| 311.04                | 622.08                 | FemtoClock Output         | 19.44                                 | 16                 | 1                     | 1                   | 32                               | 622.08                            | 1                         | 311.04 -> 622.08 (SONET)         |
| 311.04                | 622.08                 | FemtoClock Output         | 19.44                                 | 16                 | 1                     | 1                   | 32                               | 622.08                            | 1                         | 311.04 -> 622.08 (SONET)         |
| 311.04                | 44.736                 | FemtoClock Output         | 22.368                                | 3240               | 233                   | 1                   | 28                               | 626.304                           | 14                        | 311.04 -> 44.736 (SONET to T3)   |
| 311.04                | 34.368                 | VCXO Output               | 34.368                                | 1620               | 179                   | 1                   | N/A                              | N/A                               | N/A                       | 311.04 -> 34.368 (SONET to E3)   |
| 311.04                | 32.064                 | VCXO Output               | 32.064                                | 1620               | 167                   | 1                   | N/A                              | N/A                               | N/A                       | 311.04 -> 32.064 (SONET to J3)   |
| 311.04                | 2.048                  | VCXO Output               | 24.576                                | 405                | 32                    | 12                  | N/A                              | N/A                               | N/A                       | 311.04 -> 2.048 (SONET to E1)    |
| 311.04                | 1.544                  | VCXO Output               | 24.704                                | 2430               | 193                   | 16                  | N/A                              | N/A                               | N/A                       | 311.04 -> 1.544 (SONET to T1/J1) |
| 155.52                | 155.52                 | FemtoClock Output         | 19.44                                 | 8                  | 1                     | N/A                 | 32                               | 622.08                            | 4                         | 155.52 -> 155.52 (OC3)           |
| 155.52                | 77.76                  | FemtoClock Output         | 19.44                                 | 8                  | 1                     | N/A                 | 32                               | 622.08                            | 8                         | 155.52 -> 77.76 (SONET)          |
| 155.52                | 51.84                  | FemtoClock Output         | 19.44                                 | 8                  | 1                     | N/A                 | 32                               | 622.08                            | 12                        | 155.52 -> 51.84 (OC3 to OC1)     |
| 155.52                | 38.88                  | FemtoClock Output         | 19.44                                 | 8                  | 1                     | N/A                 | 32                               | 622.08                            | 16                        | 155.52 -> 38.88 (SONET)          |
| 155.52                | 19.44                  | VCXO Output               | 19.44                                 | 8                  | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 155.52 -> 19.44 (SONET)          |
| 155.52                | 311.04                 | FemtoClock Output         | 19.44                                 | 8                  | 1                     | N/A                 | 32                               | 622.08                            | 2                         | 155.52 -> 311.04 (SONET)         |

TABLE 3A. FREQUENCY CONFIGURATION EXAMPLES, CONTINUED ON NEXT PAGE

| Input Frequency (MHz) | Output Frequency (MHz) | VCXO or FemtoClock Output | Required VCXO Crystal Frequency (MHz) | VCXO Input Divider | VCXO Feedback Divider | VCXO Output Divider | FemtoClock *Multiplication Factor | FemtoClock Output Frequency (MHz) | FemtoClock Output Divider | Application                     |
|-----------------------|------------------------|---------------------------|---------------------------------------|--------------------|-----------------------|---------------------|-----------------------------------|-----------------------------------|---------------------------|---------------------------------|
| 155.52                | 622.08                 | FemtoClock Output         | 19.44                                 | 8                  | 1                     | N/A                 | 32                                | 622.08                            | 1                         | 155.52 -> 622.08 (OC3 to OC12)  |
| 155.52                | 44.736                 | FemtoClock Output         | 22.368                                | 1620               | 233                   | N/A                 | 28                                | 626.304                           | 14                        | 155.52 -> 44.736 (OC3 to T3)    |
| 155.52                | 34.368                 | VCXO Output               | 34.368                                | 810                | 179                   | 1                   | N/A                               | N/A                               | N/A                       | 155.52 -> 34.368 (OC3 to E3)    |
| 155.52                | 32.064                 | VCXO Output               | 32.064                                | 810                | 167                   | 1                   | N/A                               | N/A                               | N/A                       | 155.52 -> 32.064 (OC3 to J3)    |
| 155.52                | 2.048                  | VCXO Output               | 24.576                                | 405                | 64                    | 12                  | N/A                               | N/A                               | N/A                       | 155.52 -> 2.048 (OC3 to E1)     |
| 155.52                | 1.544                  | VCXO Output               | 24.704                                | 1215               | 193                   | 16                  | N/A                               | N/A                               | N/A                       | 155.52 -> 1.544 (OC3 to T1/J1)  |
| 77.76                 | 77.76                  | FemtoClock Output         | 19.44                                 | 4                  | 1                     | N/A                 | 32                                | 622.08                            | 8                         | 77.76 -> 77.76 (SONET)          |
| 77.76                 | 51.84                  | FemtoClock Output         | 19.44                                 | 4                  | 1                     | N/A                 | 32                                | 622.08                            | 12                        | 77.76 -> 51.84 (SONET)          |
| 77.76                 | 38.88                  | FemtoClock Output         | 19.44                                 | 4                  | 1                     | N/A                 | 32                                | 622.08                            | 16                        | 77.76 -> 38.88 (SONET)          |
| 77.76                 | 19.44                  | VCXO Output               | 19.44                                 | 4                  | 1                     | 1                   | N/A                               | N/A                               | N/A                       | 77.76 -> 19.44 (SONET)          |
| 77.76                 | 155.52                 | FemtoClock Output         | 19.44                                 | 4                  | 1                     | N/A                 | 32                                | 622.08                            | 4                         | 77.76 -> 155.52 (SONET)         |
| 77.76                 | 311.04                 | FemtoClock Output         | 19.44                                 | 4                  | 1                     | N/A                 | 32                                | 622.08                            | 2                         | 77.76 -> 311.04 (SONET)         |
| 77.76                 | 622.08                 | FemtoClock Output         | 19.44                                 | 4                  | 1                     | N/A                 | 32                                | 622.08                            | 1                         | 77.76 -> 622.08 (SONET)         |
| 77.76                 | 44.736                 | FemtoClock Output         | 22.368                                | 810                | 233                   | N/A                 | 28                                | 626.304                           | 14                        | 77.76 -> 44.736 (SONET to T3)   |
| 77.76                 | 34.368                 | VCXO Output               | 34.368                                | 405                | 179                   | 1                   | N/A                               | N/A                               | N/A                       | 77.76 -> 34.368 (SONET to E3)   |
| 77.76                 | 32.064                 | VCXO Output               | 32.064                                | 405                | 167                   | 1                   | N/A                               | N/A                               | N/A                       | 77.76 -> 32.064 (SONET to J3)   |
| 77.76                 | 2.048                  | VCXO Output               | 24.576                                | 405                | 128                   | 12                  | N/A                               | N/A                               | N/A                       | 77.76 -> 2.048 (SONET to E1)    |
| 77.76                 | 1.544                  | VCXO Output               | 24.704                                | 1215               | 386                   | 16                  | N/A                               | N/A                               | N/A                       | 77.76 -> 1.544 (SONET to T1/E1) |
| 51.84                 | 51.84                  | FemtoClock Output         | 19.44                                 | 8                  | 3                     | N/A                 | 32                                | 622.08                            | 12                        | 51.84 -> 51.84 (SONET)          |
| 51.84                 | 38.88                  | FemtoClock Output         | 19.44                                 | 8                  | 3                     | N/A                 | 32                                | 622.08                            | 16                        | 51.84 -> 38.88 (SONET)          |
| 51.84                 | 19.44                  | VCXO Output               | 19.44                                 | 8                  | 3                     | 1                   | N/A                               | N/A                               | N/A                       | 51.84 -> 19.44 (SONET)          |
| 51.84                 | 77.76                  | FemtoClock Output         | 19.44                                 | 8                  | 3                     | N/A                 | 32                                | 622.08                            | 8                         | 51.84 -> 77.76 (SONET)          |
| 51.84                 | 155.52                 | FemtoClock Output         | 19.44                                 | 8                  | 3                     | N/A                 | 32                                | 622.08                            | 4                         | 51.84 -> 155.52 (OC1 to OC3)    |
| 51.84                 | 311.04                 | FemtoClock Output         | 19.44                                 | 8                  | 3                     | N/A                 | 32                                | 622.08                            | 2                         | 51.84 -> 311.04 (SONET)         |
| 51.84                 | 622.08                 | FemtoClock Output         | 19.44                                 | 8                  | 3                     | N/A                 | 32                                | 622.08                            | 1                         | 51.84 -> 622.08 (OC1 to OC12)   |
| 51.84                 | 44.736                 | FemtoClock Output         | 22.368                                | 540                | 233                   | N/A                 | 28                                | 626.304                           | 14                        | 51.84 -> 44.736 (OC1 to T3)     |
| 51.84                 | 34.368                 | VCXO Output               | 34.368                                | 270                | 179                   | 1                   | N/A                               | N/A                               | N/A                       | 51.84 -> 34.368 (OC1 to E3)     |
| 51.84                 | 32.064                 | VCXO Output               | 32.064                                | 270                | 167                   | 1                   | N/A                               | N/A                               | N/A                       | 51.84 -> 32.064 (OC1 to J3)     |
| 51.84                 | 2.048                  | VCXO Output               | 24.576                                | 135                | 64                    | 12                  | N/A                               | N/A                               | N/A                       | 51.84 -> 2.048 (OC1 to E1)      |
| 51.84                 | 1.544                  | VCXO Output               | 24.704                                | 405                | 193                   | 16                  | N/A                               | N/A                               | N/A                       | 51.84 -> 1.544 (OC1 to T1/J1)   |
| 44.736                | 44.736                 | FemtoClock Output         | 22.368                                | 2                  | 1                     | 1                   | 28                                | 626.304                           | 14                        | 44.736 -> 44.736 (T3)           |

TABLE 3A. FREQUENCY CONFIGURATION EXAMPLES, CONTINUED ON NEXT PAGE

| Input Frequency (MHz) | Output Frequency (MHz) | VCXO or FemtoClock Output | Required VCXO Crystal Frequency (MHz) | VCXO Input Divider | VCXO Feedback Divider | VCXO Output Divider | FemtoClock Multiplication Factor | FemtoClock Output Frequency (MHz) | FemtoClock Output Divider | Application                      |
|-----------------------|------------------------|---------------------------|---------------------------------------|--------------------|-----------------------|---------------------|----------------------------------|-----------------------------------|---------------------------|----------------------------------|
| 44.736                | 1.544                  | VCXO Output               | 24.704                                | 699                | 386                   | 16                  | N/A                              | N/A                               | N/A                       | 44.736 -> 1.544 (T3 to T1/J1)    |
| 44.736                | 2.048                  | VCXO Output               | 24.576                                | 233                | 128                   | 12                  | N/A                              | N/A                               | N/A                       | 44.736 -> 2.048 (T3 to E1)       |
| 44.736                | 19.44                  | VCXO Output               | 19.44                                 | 932                | 405                   | 1                   | N/A                              | N/A                               | N/A                       | 44.736 -> 19.44 (T3 to SONET)    |
| 44.736                | 32.064                 | VCXO Output               | 32.064                                | 233                | 167                   | 1                   | N/A                              | N/A                               | N/A                       | 44.736 -> 32.064 (T3 to J3)      |
| 44.736                | 34.368                 | VCXO Output               | 34.368                                | 233                | 179                   | 1                   | N/A                              | N/A                               | N/A                       | 44.736 -> 34.368 (T3 to E3)      |
| 44.736                | 38.88                  | FemtoClock Output         | 19.44                                 | 932                | 405                   | N/A                 | 32                               | 622.08                            | 16                        | 44.736 -> 38.88 (T3 to SONET)    |
| 44.736                | 51.84                  | FemtoClock Output         | 19.44                                 | 932                | 405                   | N/A                 | 32                               | 622.08                            | 12                        | 44.736 -> 51.84 (T3 to OC1)      |
| 44.736                | 77.76                  | FemtoClock Output         | 19.44                                 | 932                | 405                   | N/A                 | 32                               | 622.08                            | 8                         | 44.736 -> 77.76 (T3 to SONET)    |
| 44.736                | 155.52                 | FemtoClock Output         | 19.44                                 | 932                | 405                   | N/A                 | 32                               | 622.08                            | 4                         | 44.736 -> 155.52 (T3 to OC3)     |
| 44.736                | 311.04                 | FemtoClock Output         | 19.44                                 | 932                | 405                   | N/A                 | 32                               | 622.08                            | 2                         | 44.736 -> 311.04 (T3 to SONET)   |
| 44.736                | 622.08                 | FemtoClock Output         | 19.44                                 | 932                | 405                   | N/A                 | 32                               | 622.08                            | 1                         | 44.736 -> 622.08 (T3 to OC12)    |
| 38.88                 | 38.88                  | FemtoClock Output         | 19.44                                 | 2                  | 1                     | N/A                 | 32                               | 622.08                            | 16                        | 38.88 -> 38.88 (SONET)           |
| 38.88                 | 19.44                  | VCXO Output               | 19.44                                 | 2                  | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 38.88 -> 19.44 (SONET)           |
| 38.88                 | 77.76                  | FemtoClock Output         | 19.44                                 | 2                  | 1                     | N/A                 | 32                               | 622.08                            | 8                         | 38.88 -> 77.76 (SONET)           |
| 38.88                 | 155.52                 | FemtoClock Output         | 19.44                                 | 2                  | 1                     | N/A                 | 32                               | 622.08                            | 4                         | 38.88 -> 155.52 (SONET to OC3)   |
| 38.88                 | 311.04                 | FemtoClock Output         | 19.44                                 | 2                  | 1                     | N/A                 | 32                               | 622.08                            | 2                         | 38.88 -> 311.04 (SONET)          |
| 38.88                 | 622.08                 | FemtoClock Output         | 19.44                                 | 2                  | 1                     | N/A                 | 32                               | 622.08                            | 1                         | 38.88 -> 622.08 (SONET to OC12)  |
| 38.88                 | 44.736                 | FemtoClock Output         | 22.368                                | 405                | 233                   | N/A                 | 28                               | 626.304                           | 14                        | 38.88 -> 44.736 (SONET to T3)    |
| 38.88                 | 34.368                 | VCXO Output               | 34.368                                | 405                | 358                   | 1                   | N/A                              | N/A                               | N/A                       | 38.88 -> 34.368 (SONET to E3)    |
| 38.88                 | 32.064                 | VCXO Output               | 32.064                                | 405                | 334                   | 1                   | N/A                              | N/A                               | N/A                       | 38.88 -> 32.064 (SONET to J3)    |
| 38.88                 | 2.048                  | VCXO Output               | 24.576                                | 405                | 256                   | 12                  | N/A                              | N/A                               | N/A                       | 38.88 -> 2.048 (SONET to E1)     |
| 38.88                 | 1.544                  | VCXO Output               | 24.704                                | 1215               | 772                   | 16                  | N/A                              | N/A                               | N/A                       | 38.88 -> 1.544 (SONET to DS1/J1) |
| 34.368                | 34.368                 | VCXO Output               | 34.368                                | 1                  | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 34.368 -> 34.368 (E3)            |
| 34.368                | 44.736                 | FemtoClock Output         | 22.368                                | 358                | 233                   | N/A                 | 28                               | 626.304                           | 14                        | 34.368 -> 44.736 (E3 to T3)      |
| 34.368                | 32.064                 | VCXO Output               | 32.064                                | 179                | 167                   | 1                   | N/A                              | N/A                               | N/A                       | 34.368 -> 32.064 (E3 to J3)      |
| 34.368                | 19.44                  | VCXO Output               | 19.44                                 | 716                | 405                   | 1                   | N/A                              | N/A                               | N/A                       | 34.368 -> 19.44 (E3 to SONET)    |
| 34.368                | 2.048                  | VCXO Output               | 24.576                                | 179                | 128                   | 12                  | N/A                              | N/A                               | N/A                       | 34.368 -> 2.048 (E3 to E1)       |
| 34.368                | 1.544                  | VCXO Output               | 24.704                                | 537                | 386                   | 16                  | N/A                              | N/A                               | N/A                       | 34.368 -> 1.544 (E3 to T1)       |
| 32.064                | 32.064                 | VCXO Output               | 32.064                                | 1                  | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 32.064 -> 32.064 (J3)            |
| 32.064                | 34.368                 | VCXO Output               | 34.368                                | 167                | 179                   | 1                   | N/A                              | N/A                               | N/A                       | 32.064 -> 34.368 (J3 to E3)      |
| 32.064                | 44.736                 | FemtoClock Output         | 22.368                                | 334                | 233                   | N/A                 | 28                               | 626.304                           | 14                        | 32.064 -> 44.736 (J3 to T3)      |

TABLE 3A. FREQUENCY CONFIGURATION EXAMPLES, CONTINUED ON NEXT PAGE

| Input Frequency (MHz) | Output Frequency (MHz) | VCXO or FemtoClock Output | Required VCXO Crystal Frequency (MHz) | VCXO Input Divider | VCXO Feedback Divider | VCXO Output Divider | FemtoClock Multiplication Factor | FemtoClock Output Frequency (MHz) | FemtoClock Output Divider | Application                             |
|-----------------------|------------------------|---------------------------|---------------------------------------|--------------------|-----------------------|---------------------|----------------------------------|-----------------------------------|---------------------------|-----------------------------------------|
| 32.064                | 2.048                  | VCXO Output               | 24.576                                | 167                | 128                   | 12                  | N/A                              | N/A                               | N/A                       | 32.064 -> 2.048 (J3 to E1)              |
| 32.064                | 1.544                  | VCXO Output               | 24.704                                | 501                | 386                   | 16                  | N/A                              | N/A                               | N/A                       | 32.064 -> 1.544 (J3 to T1)              |
| 19.44                 | 19.44                  | VCXO Output               | 19.44                                 | 1                  | 1                     | 1                   | N/A                              | N/A                               | N/A                       | 19.44 -> 19.44 (SONET)                  |
| 19.44                 | 38.88                  | FemtoClock Output         | 19.44                                 | 1                  | 1                     | N/A                 | 32                               | 622.08                            | 16                        | 19.44 -> 38.88 (SONET)                  |
| 19.44                 | 51.84                  | FemtoClock Output         | 19.44                                 | 1                  | 1                     | N/A                 | 32                               | 622.08                            | 12                        | 19.44 -> 51.84 (SONET to OC1)           |
| 19.44                 | 77.76                  | FemtoClock Output         | 19.44                                 | 1                  | 1                     | N/A                 | 32                               | 622.08                            | 8                         | 19.44 -> 77.76 (SONET)                  |
| 19.44                 | 155.52                 | FemtoClock Output         | 19.44                                 | 1                  | 1                     | N/A                 | 32                               | 622.08                            | 4                         | 19.44 -> 155.52 (SONET to OC3)          |
| 19.44                 | 311.04                 | FemtoClock Output         | 19.44                                 | 1                  | 1                     | N/A                 | 32                               | 622.08                            | 2                         | 19.44 -> 311.04 (SONET)                 |
| 19.44                 | 622.08                 | FemtoClock Output         | 19.44                                 | 1                  | 1                     | N/A                 | 32                               | 622.08                            | 1                         | 19.44 -> 622.08 (SONET to OC12)         |
| 19.44                 | 44.736                 | FemtoClock Output         | 22.368                                | 405                | 466                   | N/A                 | 28                               | 626.304                           | 14                        | 19.44 -> 44.736 (SONET to T3)           |
| 19.44                 | 34.368                 | VCXO Output               | 34.368                                | 405                | 716                   | 1                   | N/A                              | N/A                               | N/A                       | 19.44 -> 34.368 (SONET to E3)           |
| 19.44                 | 32.064                 | VCXO Output               | 32.064                                | 405                | 668                   | 1                   | N/A                              | N/A                               | N/A                       | 19.44 -> 32.064 (SONET to J3)           |
| 19.44                 | 2.048                  | VCXO Output               | 24.576                                | 405                | 512                   | 12                  | N/A                              | N/A                               | N/A                       | 19.44 -> 2.048 (SONET to E1)            |
| 19.44                 | 1.544                  | VCXO Output               | 24.704                                | 1215               | 1544                  | 16                  | N/A                              | N/A                               | N/A                       | 19.44 -> 1.544 (SONET to T1/J1)         |
| 19.44                 | 666.5142857            | FemtoClock Output         | 20.82857143                           | 14                 | 15                    | N/A                 | 32                               | 666.5142857                       | 1                         | 19.44 -> 666.5142857 (255/238 FEC)      |
| 19.44                 | 669.3265823            | FemtoClock Output         | 20.9164557                            | 79                 | 85                    | N/A                 | 32                               | 669.3265823                       | 1                         | 19.44 -> 669.3265823 (255/237 FEC)      |
| 19.44                 | 672.1627119            | FemtoClock Output         | 21.00508475                           | 236                | 255                   | N/A                 | 32                               | 672.1627119                       | 1                         | 19.44 -> 672.1627119 (255/236 FEC)      |
| 2.048                 | 2.048                  | VCXO Output               | 24.576                                | 1                  | 12                    | 12                  | N/A                              | N/A                               | N/A                       | 2.048 -> 2.048 (E1)                     |
| 2.048                 | 1.544                  | VCXO Output               | 24.704                                | 16                 | 193                   | 16                  | N/A                              | N/A                               | N/A                       | 2.048 -> 1.544 (E1 to T1/J1)            |
| 2.048                 | 34.368                 | VCXO Output               | 34.368                                | 32                 | 537                   | 1                   | N/A                              | N/A                               | N/A                       | 2.048 -> 34.368 (E1 to E3)              |
| 2.048                 | 32.064                 | VCXO Output               | 32.064                                | 32                 | 501                   | 1                   | N/A                              | N/A                               | N/A                       | 2.048 -> 32.064 (E1 to J3)              |
| 2.048                 | 44.736                 | FemtoClock Output         | 22.368                                | 64                 | 699                   | N/A                 | 28                               | 626.304                           | 14                        | 2.048 -> 44.736 (E1 to T3)              |
| 1.544                 | 1.544                  | VCXO Output               | 24.704                                | 1                  | 16                    | 16                  | N/A                              | N/A                               | N/A                       | 1.544 -> 1.54 (T1/J1)                   |
| 1.544                 | 2.048                  | VCXO Output               | 24.576                                | 193                | 3072                  | 12                  | N/A                              | N/A                               | N/A                       | 1.544 -> 2.048 (T1 to E1)               |
| 1.544                 | 32.064                 | VCXO Output               | 32.064                                | 193                | 4008                  | 1                   | N/A                              | N/A                               | N/A                       | 1.544 -> 32.064 (T1/J1 to J3)           |
| 1.544                 | 34.368                 | VCXO Output               | 34.368                                | 193                | 4296                  | 1                   | N/A                              | N/A                               | N/A                       | 1.544 -> 34.368 (T1/J1 to E3)           |
| 1.544                 | 44.736                 | FemtoClock Output         | 22.368                                | 193                | 2796                  | N/A                 | 28                               | 626.304                           | 14                        | 1.544 -> 44.736 (T1/J1 to T3)           |
| 0.008                 | 1.544                  | VCXO Output               | 24.704                                | 1                  | 3088                  | 16                  | N/A                              | N/A                               | N/A                       | 8KHz -> 1.544MHz (Frame Clock to T1)    |
| 0.008                 | 2.048                  | VCXO Output               | 24.576                                | 1                  | 3072                  | 12                  | N/A                              | N/A                               | N/A                       | 8KHz -> 2.048MHz (Frame Clock to E1)    |
| 0.008                 | 19.44                  | VCXO Output               | 19.44                                 | 1                  | 2430                  | 1                   | N/A                              | N/A                               | N/A                       | 8KHz -> 19.44MHz (Frame Clock to SONET) |
| 0.008                 | 32.064                 | VCXO Output               | 32.064                                | 1                  | 4008                  | 1                   | N/A                              | N/A                               | N/A                       | 8KHz -> 32.064MHz (Frame Clock to J3)   |

TABLE 3A. FREQUENCY CONFIGURATION EXAMPLES

| Input Frequency (MHz) | Output Frequency (MHz) | VCXO or FemtoClock Output | Required VCXO Crystal Frequency (MHz) | VCXO Input Divider | VCXO Feedback Divider | VCXO Output Divider | FemtoClock Multiplication Factor | FemtoClock Output Frequency (MHz) | FemtoClock Output Divider | Application                              |
|-----------------------|------------------------|---------------------------|---------------------------------------|--------------------|-----------------------|---------------------|----------------------------------|-----------------------------------|---------------------------|------------------------------------------|
| 0.008                 | 34.368                 | VCXO Output               | 34.368                                | 1                  | 4296                  | 1                   | N/A                              | N/A                               | N/A                       | 8KHz -> 34.368MHz (Frame Clock to E3)    |
| 0.008                 | 44.736                 | FemtoClock Output         | 22.368                                | 1                  | 2796                  | 1                   | 28                               | 626.304                           | 14                        | 8KHz -> 44.736MHz (Frame Clock to T3)    |
| 0.008                 | 38.88                  | FemtoClock Output         | 19.44                                 | 1                  | 2430                  | N/A                 | 32                               | 622.08                            | 16                        | 8KHz -> 38.88MHz (Frame Clock to SONET)  |
| 0.008                 | 77.76                  | FemtoClock Output         | 19.44                                 | 1                  | 2430                  | N/A                 | 32                               | 622.08                            | 8                         | 8KHz -> 77.76MHz (Frame Clock to SONET)  |
| 0.008                 | 155.52                 | FemtoClock Output         | 19.44                                 | 1                  | 2430                  | N/A                 | 32                               | 622.08                            | 4                         | 8KHz -> 155.52MHz (Frame Clock to SONET) |
| 0.008                 | 311.04                 | FemtoClock Output         | 19.44                                 | 1                  | 2430                  | N/A                 | 32                               | 622.08                            | 2                         | 8KHz -> 311.04MHz (Frame Clock to SONET) |
| 0.008                 | 622.08                 | FemtoClock Output         | 19.44                                 | 1                  | 2430                  | N/A                 | 32                               | 622.08                            | 1                         | 8KHz -> 622.08MHz (Frame Clock to OC12)  |

**ABSOLUTE MAXIMUM RATINGS**

|                                          |                           |
|------------------------------------------|---------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{CC} + 0.5V$  |
| Outputs, $V_O$ (LVCMOS)                  | -0.5V to $V_{CCO} + 0.5V$ |
| Outputs, $I_O$ (LVPECL)                  |                           |
| Continuous Current                       | 50mA                      |
| Surge Current                            | 100mA                     |
| Package Thermal Impedance, $\theta_{JA}$ | 22.3°C/W (0 lfpm)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCA\_XO} = V_{CCO\_CMOS} = V_{CCO\_PECL} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

| Symbol                         | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------------------------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$                       | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{CCA}, V_{CCA\_XO}$         | Analog Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{CCO\_CMOS}, V_{CCO\_PECL}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$                       | Power Supply Current  |                 |         | 395     |         | mA    |
| $I_{CCA}$                      | Analog Supply Current |                 |         | 15      |         | mA    |

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCA\_XO} = V_{CCO\_CMOS} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

| Symbol   | Parameter           | Test Conditions                                                                    | Minimum                        | Typical | Maximum        | Units         |
|----------|---------------------|------------------------------------------------------------------------------------|--------------------------------|---------|----------------|---------------|
| $V_{IH}$ | Input High Voltage  |                                                                                    | 2                              |         | $V_{CC} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage   |                                                                                    | -0.3                           |         | 0.8            | V             |
| $I_{IH}$ | Input High Current  | MP, MR, OE_REF, SEL0, SEL1, XOIN[12:1], NPA[2:0], NPB[2:0], CLK1, CLK2, XOFB[12:1] | $V_{CC} = V_{IN} = 3.465V$     |         | 150            | $\mu\text{A}$ |
|          |                     | NV0, NV1, XOIN0, XOFB0                                                             | $V_{CC} = V_{IN} = 3.465V$     |         | 5              | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current   | MP, MR, OE_REF, SEL0, SEL1, XOIN[12:1], NPA[2:0], NPB[2:0], CLK1, CLK2, XOFB[12:1] | $V_{CC} = 3.465V, V_{IN} = 0V$ | -5      |                | $\mu\text{A}$ |
|          |                     | NV0, NV1, XOIN0, XOFB0                                                             | $V_{CC} = 3.465V, V_{IN} = 0V$ | -150    |                | $\mu\text{A}$ |
| $V_{OH}$ | Output High Voltage | REF_CLK, VCLK, LOCK; NOTE 1                                                        | 2.6                            |         |                | V             |
| $V_{OL}$ | Output Low Voltage  | REF_CLK, VCLK, LOCK; NOTE 1                                                        |                                |         | 0.5            | V             |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO\_CMOS}/2$ .

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCA\_XO} = V_{CCO\_CMOS} = V_{CCO\_PECL} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

| Symbol    | Parameter                            | Test Conditions | Minimum                        | Typical | Maximum         | Units   |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                   | CLK0            | $V_{IN} = V_{CC} = 3.465V$     |         | 150             | $\mu A$ |
|           |                                      | nCLK0           | $V_{IN} = V_{CC} = 3.465V$     |         | 5               | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | CLK0            | $V_{IN} = 0V, V_{CC} = 3.465V$ | -150    |                 | $\mu A$ |
|           |                                      | nCLK0           | $V_{IN} = 0V, V_{CC} = 3.465V$ | -5      |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage           |                 | 0.15                           |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                 | $V_{EE} + 0.5$                 |         | $V_{CC} - 0.85$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 is  $V_{CC} + 0.3V$ .**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCA\_XO} = V_{CCO\_PECL} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6             |         | 1.0             | V     |

NOTE 1: Outputs terminated with  $50\ \Omega$  to  $V_{CCO\_PECL} - 2V$ . See "Parameter Measurement Information" section, "3.3V Output Load Test Circuit".**TABLE 5. CRYSTAL CHARACTERISTICS**

| Symbol    | Parameter                    | Test Conditions | Minimum     | Typical | Maximum   | Units            |
|-----------|------------------------------|-----------------|-------------|---------|-----------|------------------|
| $f_N$     | Nominal Frequency            |                 |             | 19.44   |           | MHz              |
| $f_T$     | Frequency Tolerance          |                 |             |         | $\pm TBD$ | ppm              |
| $f_S$     | Frequency Stability          |                 |             |         | $\pm TBD$ | ppm              |
|           | Operating Temperature Range  |                 | 0           |         | 70        | $^\circ\text{C}$ |
| $C_L$     | Load Capacitance             |                 |             | 12      |           | pF               |
| $C_O$     | Shunt Capacitance            |                 |             | 4       |           | pF               |
| $C_O/C_1$ | Pullability Ratio            |                 |             | 220     | 240       |                  |
| ESR       | Equivalent Series Resistance |                 |             |         | 50        | $\Omega$         |
|           | Drive Level                  |                 |             |         | 1         | mW               |
|           | Mode of Operation            |                 | Fundamental |         |           |                  |

**TABLE 6. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCA\_XO} = V_{CCO\_CMOS} = V_{CCO\_PECL} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter             | Test Conditions                                                                           | Minimum              | Typical | Maximum | Units |
|-------------|-----------------------|-------------------------------------------------------------------------------------------|----------------------|---------|---------|-------|
| $f_{OUT}$   | Output Frequency      | QA/nQA                                                                                    | 35                   |         | 700     | MHz   |
|             |                       | QB/nQB                                                                                    | 4.375                |         | 700     | MHz   |
|             |                       | VCLK                                                                                      | 1.1875               |         | 25      | MHz   |
|             |                       | REF_CLK                                                                                   |                      |         | 200     | MHz   |
| $t(j)$      | Timing Jitter         | OC-48 mask (12kHz - 20MHz)<br>19.44MHz input, into CLK0<br>622.08MHz output;<br>NOTE 1, 2 | Random jitter        | 1.3     |         | ps    |
|             |                       |                                                                                           | Deterministic jitter | 0.75    |         | ps    |
|             |                       |                                                                                           | Total jitter         | 1.5     |         | ps    |
|             |                       |                                                                                           |                      | 3.5     |         | mUI   |
|             |                       | OC-12 mask (250kHz - 5MHz)<br>19.44MHz input, into CLK0<br>155.52MHz output;<br>NOTE 1, 3 | Random jitter        | 1       |         | ps    |
|             |                       |                                                                                           | Deterministic jitter | 0.5     |         | ps    |
|             |                       |                                                                                           | Total jitter         | 1.1     |         | ps    |
|             |                       |                                                                                           |                      | 0.7     |         | mUI   |
|             |                       | OC-48 mask (12kHz - 20MHz)<br>8kHz input, into CLK2<br>622.08MHz output;<br>NOTE 1, 2     | Random jitter        | 1       |         | ps    |
|             |                       |                                                                                           | Deterministic jitter | 0.3     |         | ps    |
|             |                       |                                                                                           | Total jitter         | 1.1     |         | ps    |
|             |                       |                                                                                           |                      | 2.7     |         | mUI   |
|             |                       | OC-12 mask (250kHz - 5MHz)<br>8kHz input, into CLK2<br>155.52MHz output;<br>NOTE 1, 3     | Random jitter        | 0.9     |         | ps    |
|             |                       |                                                                                           | Deterministic jitter | 0.19    |         | ps    |
|             |                       |                                                                                           | Total jitter         | 0.9     |         | ps    |
|             |                       |                                                                                           |                      | 0.6     |         | mUI   |
| $t_R / t_F$ | Output Rise/Fall Time | 20% to 80%                                                                                | 200                  |         | 700     | ps    |
| odc         | Output Duty Cycle     | QA/QB @ 622.08MHz                                                                         |                      | 50      |         | %     |
|             |                       | VCLK, REF_CLK @ 19.44MHz                                                                  |                      | 50      |         | %     |
| $t_{LOCK}$  | PLL Lock Time         |                                                                                           |                      | 100     |         | ms    |

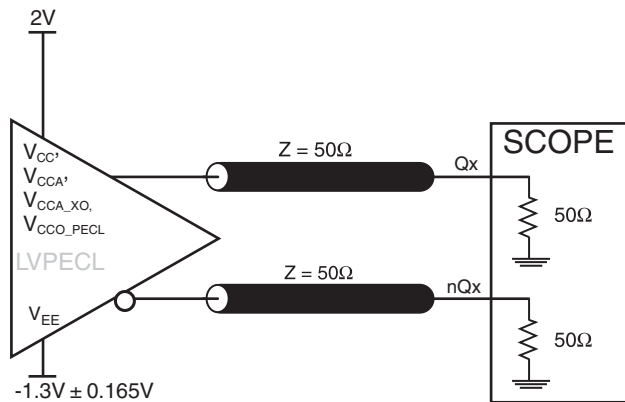
See Parameter Measurement Information section.

NOTE 1: External crystal is 19.44MHz Eliptek ECX-5451.

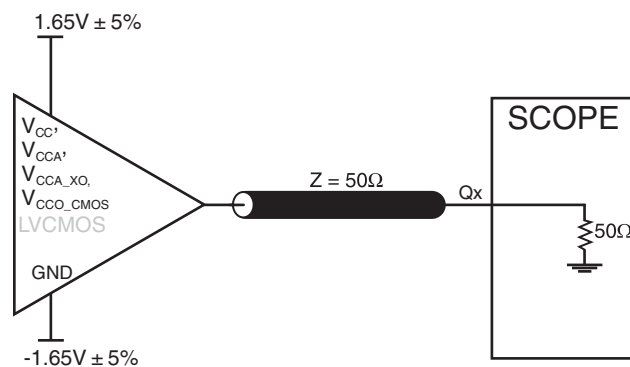
NOTE 2: Loop bandwidth (-3dB) = 180Hz; Loop Damping Factor = 5.3 (see Applications Section, Example Loop Filter Component Value, example case #4).

NOTE 3: Loop bandwidth (-3dB) = 19Hz; Loop Damping Factor = 2.8 (see Applications Section, Example Loop Filter Component Value example case #2).

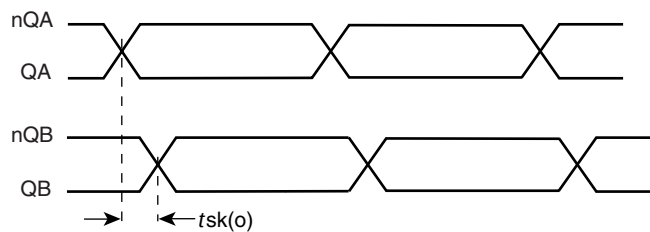
## PARAMETER MEASUREMENT INFORMATION



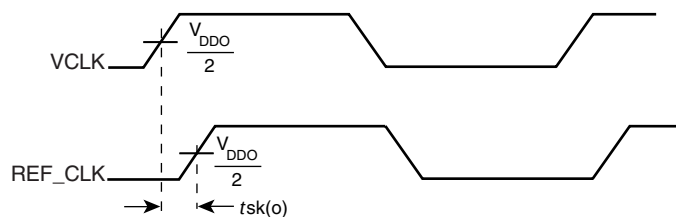
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



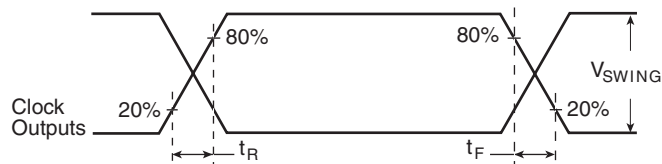
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



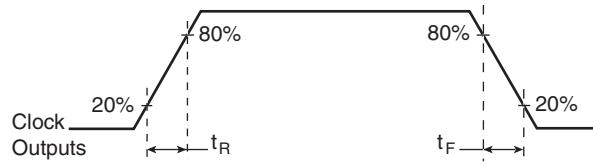
LVPECL OUTPUT SKEW



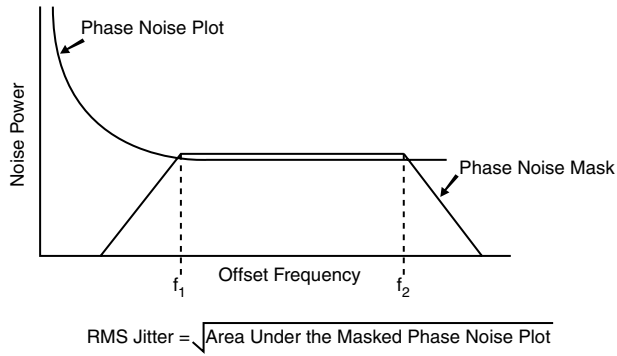
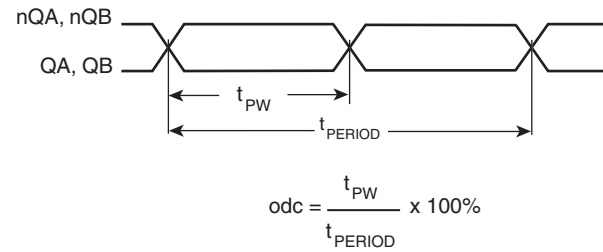
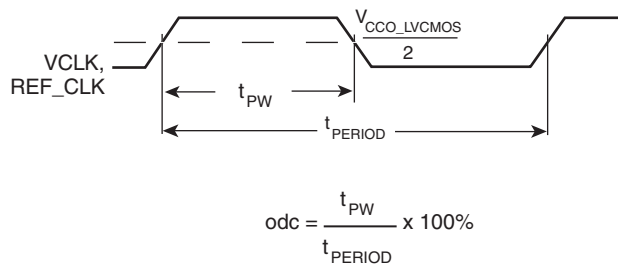
LVCMOS OUTPUT SKEW



LVPECL OUTPUT RISE/FALL TIME



LVCMOS OUTPUT RISE/FALL TIME

**PHASE JITTER****LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/ $t_{PERIOD}$** **LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/ $t_{PERIOD}$**

## APPLICATION INFORMATION

### DESCRIPTION OF THE PLL STAGES

The ICS843002-31 is a two stage frequency multiplication device, a VCXO PLL followed by a low phase noise FemtoClock frequency multiplier. The VCXO uses an external pullable crystal which can be pulled  $\pm 100$ ppm by the VCXO PLL circuitry to phase lock it to the input reference frequency. The output frequency of the VCXO PLL is equal to that of the external pullable crystal, which is in the range of 17.5MHz to 25MHz. The loop bandwidth VCXO PLL is typically set in the range of 10-250Hz which provides attenuation of input reference clock jitter. Since the VCXO is a high-Q oscillator circuit, it has low intrinsic output jitter and phase noise. The VCXO PLL output clock is available from the VCLK pin.

The FemtoClock frequency multiplier has an effective control bandwidth of about 800kHz which means it will track the VCXO PLL clock output.

### VCXO PLL LOOP RESPONSE CONSIDERATIONS

Loop response characteristics of the VCXO PLL is affected by the setting of the VCXO feedback divider value (XOFB) and by the external loop filter components. A practical range of loop bandwidth for many applications is 25Hz to 1kHz. A bandwidth of less than 10Hz requires careful component selection and possible metal shielding to prevent clock output wander. A damping factor of 0.7 or greater should be used to ensure loop stability. When a passband peaking of <0.1dB is desired for SONET/SDH loop timing application, the damping factor should be 6 or higher.

A PC base PLL bandwidth calculator is also under development. For assistance with loop filter bandwidth and component selection suggestions, please contact your IDT sales representative.

### SETTING THE VCXO PLL LOOP RESPONSE

The VCXO PLL loop response is determined both by fixed device characteristics and by other characteristics set by the user. This includes the values of  $R_S$ ,  $C_S$ ,  $C_P$  and  $R_{SET}$  as shown in the External VCXO PLL Components figure on this page.

The VCXO PLL loop bandwidth is approximated by:

$$NBW (VCXO PLL) = \frac{R_S \times I_{CP} \times K_O}{32}$$

#### WHERE:

$R_S$  = Value of resistor  $R_S$  in loop filter in Ohms

$I_{CP}$  = Charge pump current in amps (see table on page 17)

$K_O$  = VCXO Gain in Hz/V (see table on page 18)

XOFB Divider = 1 to 8191

The above equation calculates the “normalized” loop bandwidth (denoted as “NBW”) which is approximately equal to the -3dB bandwidth. NBW does not take into account the effects of damping factor or the second pole imposed by  $C_P$ . It does, however, provide a useful approximation of filter performance.

To prevent jitter on VCLK due to modulation of the VCXO PLL by the phase detector frequency, the following general rule should be observed:

$$NBW (VCXO PLL) \leq \frac{f (\text{Phase Detector})}{20}$$

$f (\text{Phase Detector}) = \text{Input Frequency} \div \text{XOIN}$

The PLL loop damping factor is determined by:

$$DF (VCLK) = \frac{R_S}{2} \times \sqrt{\frac{I_{CP} \times C_S \times K_O}{\text{XOFB Divider}}}$$

#### WHERE:

$C_S$  = Value of capacitor  $C_S$  in loop filter in Farads

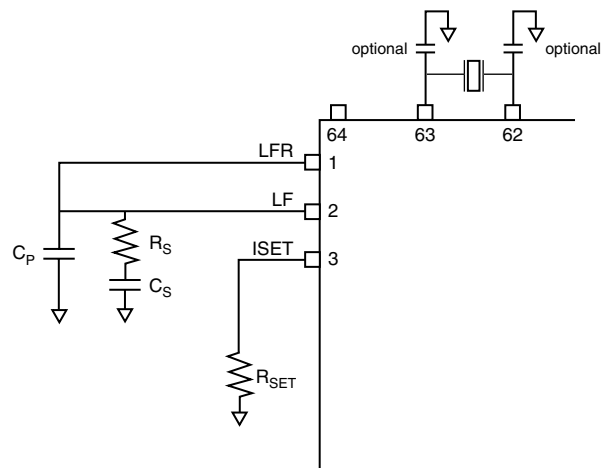


FIGURE 1. EXTERNAL VCXO PLL COMPONENTS

### NOTES ON SETTING THE VALUE OF $C_p$

As another general rule, the following relationship should be maintained between components  $C_s$  and  $C_p$  in the loop filter:

$$C_p = \frac{C_s}{20}$$

$C_p$  establishes a second pole in the VCXO PLL loop filter. For higher damping factors ( $> 1$ ), calculate the value of  $C_p$  based on a  $C_s$  value that would be used for a damping factor of 1. This will minimize baseband peaking and loop instability that can lead to output jitter.

$C_p$  also dampens VCXO PLL input voltage modulation by the charge pump correction pulses. A  $C_p$  value that is too low will result in increased output phase noise at the phase detector frequency due to this. In extreme cases where input jitter is high, charge pump current is high, and  $C_p$  is too small, the VCXO PLL input voltage can hit the supply or ground rail resulting in non-linear loop response.

The best way to set the value of  $C_p$  is to use the filter response software under development from ICS (please refer to the following section).  $C_p$  should be increased in value until it just starts affecting the passband peak.

### NOTES ON EXTERNAL CRYSTAL LOAD CAPACITORS

In the loop filter schematic diagram, capacitors are shown between pins 62 to ground and between pins 63 to ground. These are optional crystal load capacitors which can be used to center tune the external pullable crystal (the crystal frequency can only be lowered by adding capacitance, it cannot be raised). Note that the addition of external load capacitors will decrease the crystal pull range and the  $K_{vco}$  value.

### NOTES ON SETTING CHARGE PUMP CURRENT

The recommended range for the charge pump current is  $50\mu A$  to  $500\mu A$ . Below  $50\mu A$ , loop filter charge leakage, due to PCB or capacitor leakage, can become a problem. This loop filter leakage can cause locking problems, output clock cycle slips, or low frequency phase noise.

As can be seen in the loop bandwidth and damping factor equations or by using the filter response software available from ICS, increasing charge pump current ( $I_{CP}$ ) increases both bandwidth and damping factor.

### CHARGE PUMP CURRENT, EXAMPLE SETTINGS

| $R_{SET}$ | Charge Pump Current ( $I_{CP}$ ) |
|-----------|----------------------------------|
| 17.6K     | $62.5\mu A$                      |
| 8.8K      | $125\mu A$                       |
| 4.4K      | $250\mu A$                       |
| 2.2K      | $500\mu A$                       |

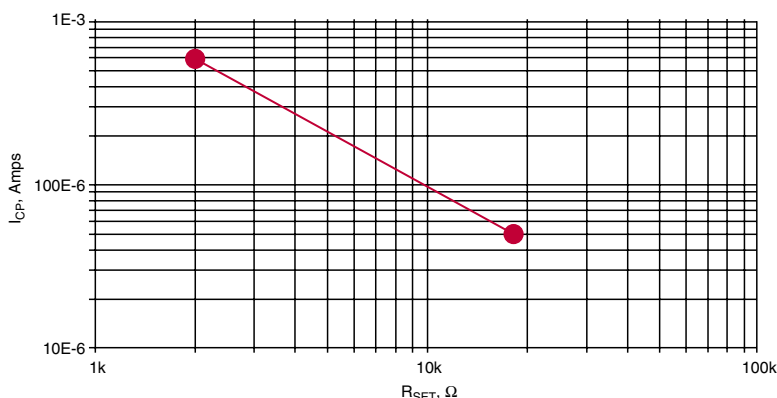
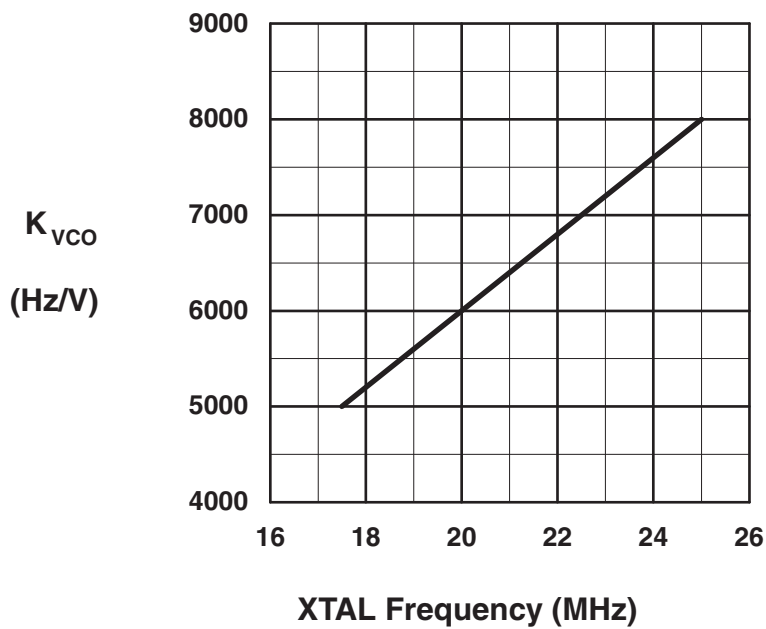


FIGURE 2. CHARGE PUMP CURRENT VS. VALUE OF  $R_{SET}$   
(EXTERNAL RESISTOR) GRAPH

**VCXO GAIN ( $K_O$ ) VS. XTAL FREQUENCY****EXAMPLE LOOP FILTER COMPONENT VALUE**

| Example Case Number | Device Configuration  |                      |              |              |            | Loop Filter Component Selection  |                              |                       |                       | VCXO PLL Performance |                     |                       |
|---------------------|-----------------------|----------------------|--------------|--------------|------------|----------------------------------|------------------------------|-----------------------|-----------------------|----------------------|---------------------|-----------------------|
|                     | Input Reference Clock | XTAL Frequency (MHz) | XOIN Divider | XOFB Divider | MP Divider | $R_{SET}$ Resistor ( $k\Omega$ ) | $R_S$ Resistor ( $k\Omega$ ) | $C_S$ Cap ( $\mu F$ ) | $C_P$ Cap ( $\mu F$ ) | Loop BW (-3dB) (MHz) | Loop Damping Factor | Passband Peaking (dB) |
| 1                   | 8kHz                  | 19.44                | 1            | 2430         | 0          | 4.5                              | 150                          | 10                    | 0.01                  | 18                   | 5.8                 | 0.1                   |
| 2                   | 8kHz                  | 19.44                | 1            | 2430         | 0          | 4.5                              | 150                          | 2.2                   | 0.01                  | 19                   | 2.8                 | 0.3                   |
| 3                   | 19.44kHz              | 19.44                | 32           | 32           | 0          | 9.09                             | 11                           | 10                    | 0.01                  | 65                   | 2.7                 | 0.3                   |
| 4                   | 19.44MHz              | 19.44                | 8            | 8            | 0          | 9.09                             | 11                           | 10                    | 0.01                  | 180                  | 5.3                 | 0.1                   |

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843002-31 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ ,  $V_{CCA\_XO}$ , and  $V_{CCO\_X}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a  $10\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

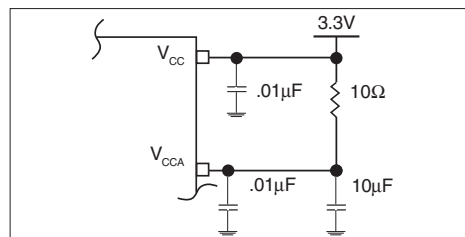


FIGURE 3. POWER SUPPLY FILTERING

## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK0/nCLK0 accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 4A to 4D* show interface examples for the HiPerClockS CLK0/nCLK0 input driven by the most common driver types. The input interfaces suggested here

are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

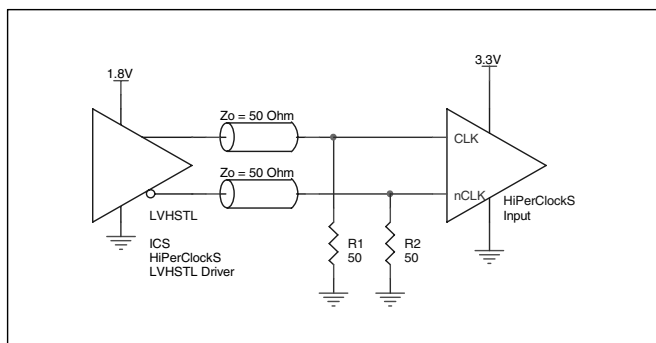


FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER

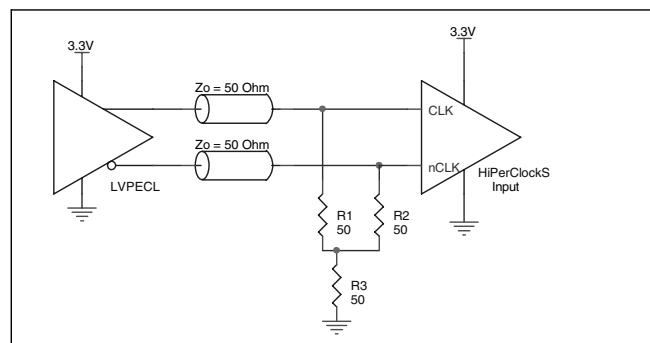


FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

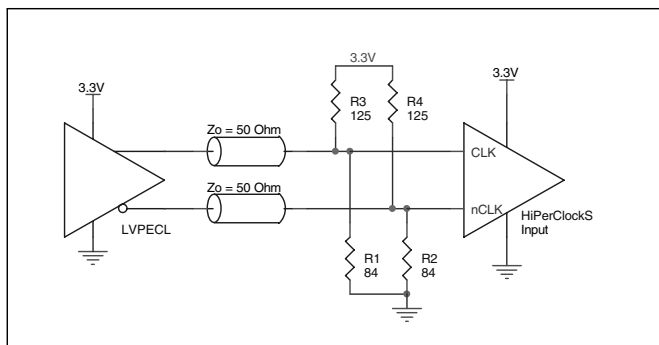


FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

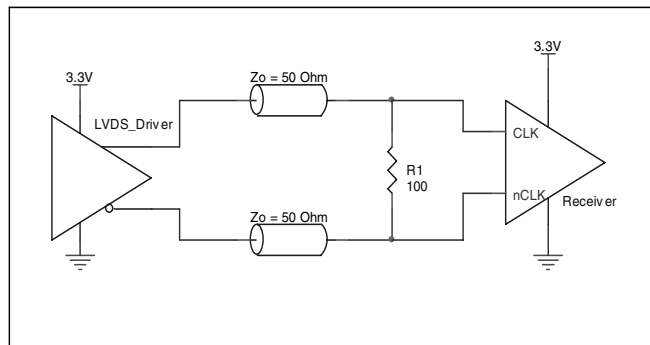


FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

## DIFFERENTIAL CLOCK INPUT CIRCUIT

### USING THE DIFFERENTIAL INTERFACE FOR SINGLE-ENDED CLOCKS

The differential interface (CLK0/nCLK0) can be used as a third single-ended input to support an LVCMOS or LVTTL clock driver. The clock input is connected to the CLK0 input pin, and the nCLK0 pin is left unconnected. To help reduce interference with the internal VCO circuits, an external resistor can be placed in series with the clock signal near the CLK0 input pin.

Combined with the input pin capacitance, this resistor acts as a low pass signal filter. The typical value of this optional series filter resistor is 100Ω. This will lower both the amplitude and edge rate of the clock input signal. In the case of a very short clock trace a series termination register may not be needed.

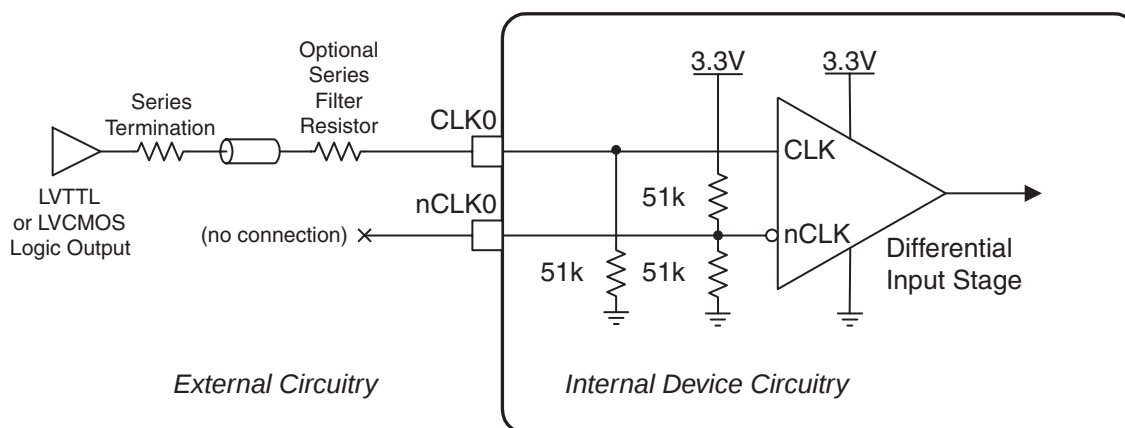


FIGURE 5. SINGLE-ENDED CLOCK INPUT INTERFACE

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL\_IN to ground.

#### CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

#### CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### OUTPUTS:

#### LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

#### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## THERMAL RELEASE PATH

The exposed metal pad provides heat transfer from the device to the P.C. board. The exposed metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted

through solder as shown in *Figure 6*. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

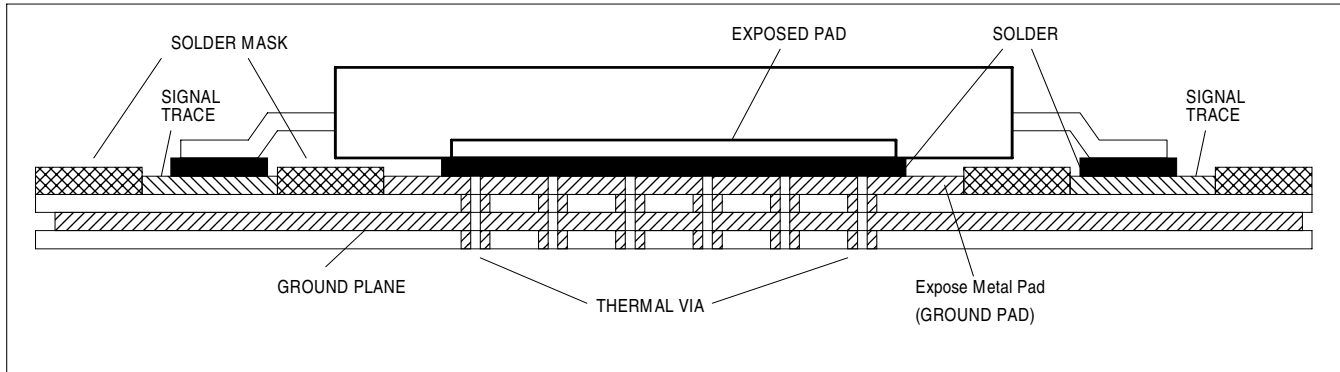


FIGURE 6. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE

## TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

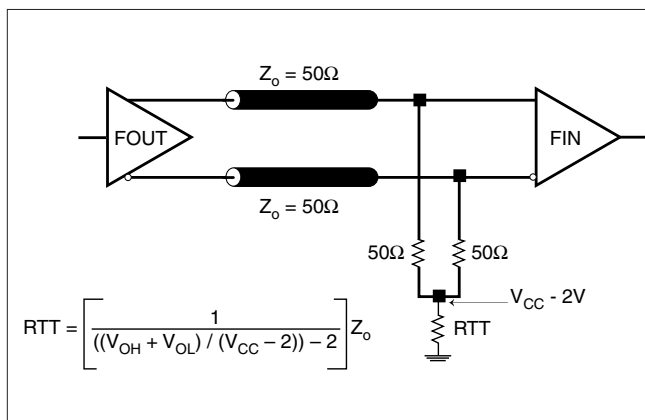


FIGURE 7A. LVPECL OUTPUT TERMINATION

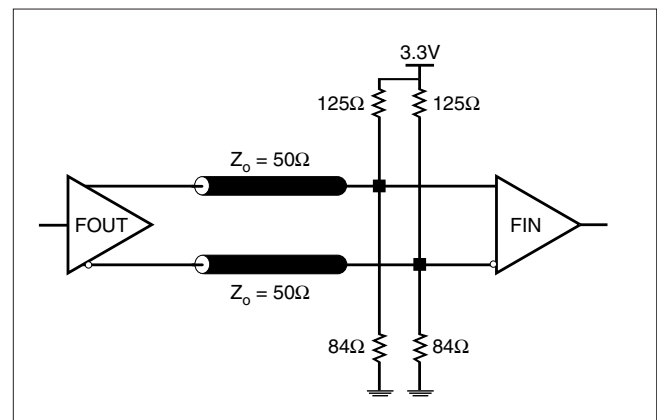


FIGURE 7B. LVPECL OUTPUT TERMINATION

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843002-31. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS843002-31 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 395mA = 1368.67mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30mW = 60mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 1368.67mW + 60mW = 1428.67mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 17.2°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 1.429W * 17.2^\circ C/W = 94.6^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

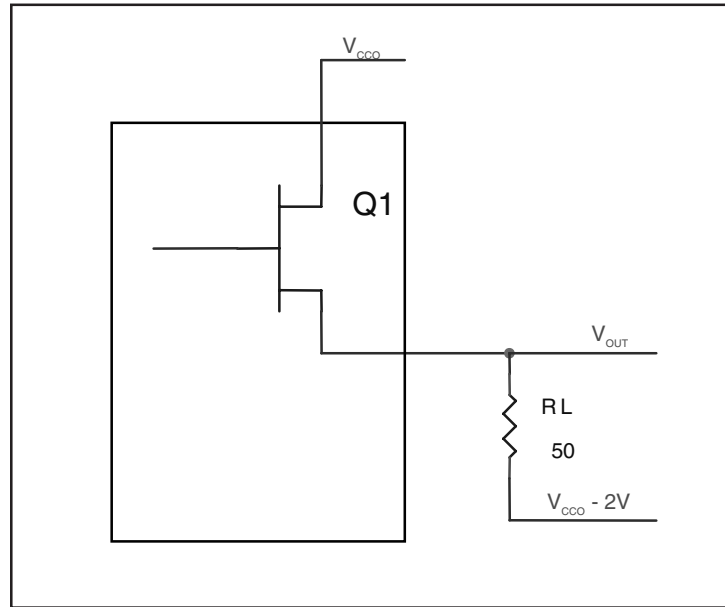
**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 64-PIN TQFP, E-PAD FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|----------------------------------------------------|----------|----------|----------|
|                                                    | 0        | 200      | 500      |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 22.3°C/W | 17.2°C/W | 15.1°C/W |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8*.



**FIGURE 8. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

## RELIABILITY INFORMATION

**TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 64 LEAD TQFP, E-PAD**

| <b><math>\theta_{JA}</math> vs. 0 Air Flow (Linear Feet per Minute)</b> |          |            |            |
|-------------------------------------------------------------------------|----------|------------|------------|
|                                                                         | <b>0</b> | <b>200</b> | <b>500</b> |
| Multi-Layer PCB, JEDEC Standard Test Boards                             | 22.3°C/W | 17.2°C/W   | 15.1°C/W   |

### TRANSISTOR COUNT

The transistor count for ICS843002-31 is: 10,095

PACKAGE OUTLINE - Y SUFFIX FOR 64 LEAD TQFP, EPAD (32 pin package depicted to define Table 9 dimension symbols)

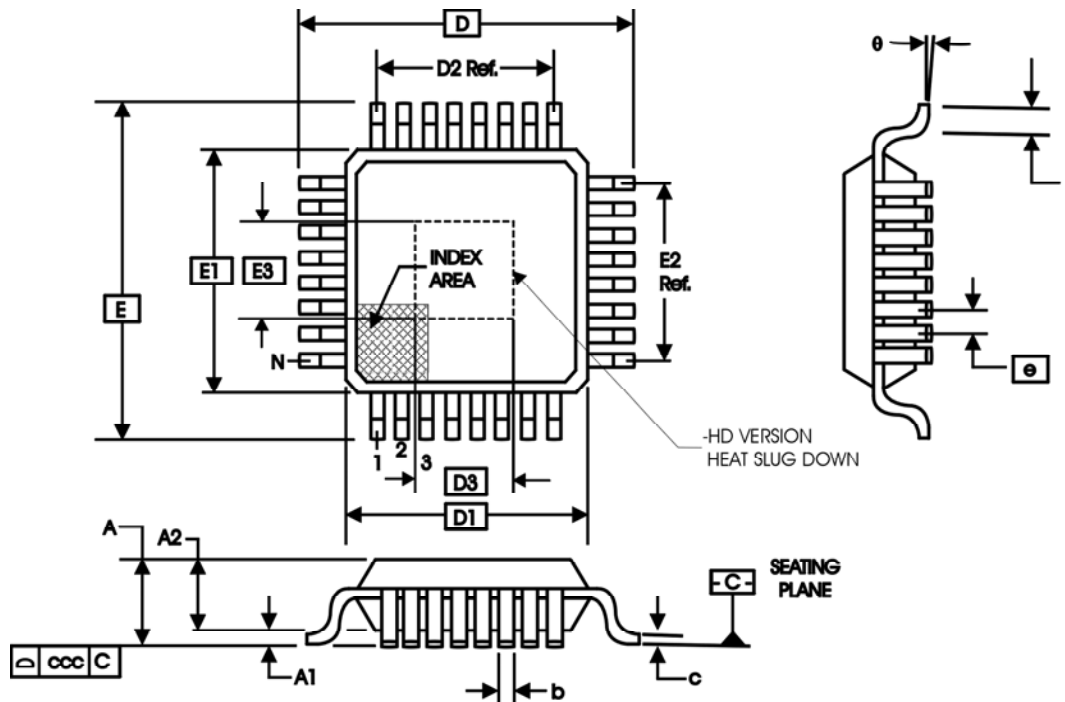


TABLE 9. PACKAGE DIMENSIONS FOR 64 LEAD TQFP, EPAD

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |             |         |         |
|--------------------------------------------------|-------------|---------|---------|
| SYMBOL                                           | ACD-HD      |         |         |
|                                                  | MINIMUM     | NOMINAL | MAXIMUM |
| N                                                | 64          |         |         |
| A                                                | --          | --      | 1.20    |
| A1                                               | 0.05        | 0.10    | 0.15    |
| A2                                               | 0.95        | 1.0     | 1.05    |
| b                                                | 0.17        | 0.22    | 0.27    |
| c                                                | 0.09        | --      | 0.20    |
| D                                                | 12.00 BASIC |         |         |
| D1                                               | 10.00 BASIC |         |         |
| D2                                               | 7.50 Ref.   |         |         |
| E                                                | 12.00 BASIC |         |         |
| E1                                               | 10.00 BASIC |         |         |
| E2                                               | 7.50 Ref.   |         |         |
| e                                                | 0.50 BASIC  |         |         |
| L                                                | 0.45        | 0.60    | 0.75    |
| θ                                                | 0°          | --      | 7°      |
| ccc                                              | --          | --      | 0.08    |
| D3 & E3                                          | 4.5         | 5.0     | 5.5     |

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking       | Package                        | Shipping Packaging | Temperature |
|-------------------|---------------|--------------------------------|--------------------|-------------|
| ICS843002CY-31    | ICS843002CY31 | 64 Lead TQFP, EPAD             | tray               | 0°C to 70°C |
| ICS843002CY-31T   | ICS843002CY31 | 64 Lead TQFP, EPAD             | 500 tape & reel    | 0°C to 70°C |
| ICS843002CY-31LF  | TBD           | 64 Lead "Lead-Free" TQFP, EPAD | tray               | 0°C to 70°C |
| ICS843002CY-31LFT | TBD           | 64 Lead "Lead-Free" TQFP, EPAD | 500 tape & reel    | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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800-345-7015  
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netcom@idt.com  
480-763-2056

---

**Corporate Headquarters**

Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road  
San Jose, CA 95138  
United States  
800 345 7015  
+408 284 8200 (outside U.S.)

**Asia Pacific and Japan**

Integrated Device Technology  
Singapore (1997) Pte. Ltd.  
Reg. No. 199707558G  
435 Orchard Road  
#20-03 Wisma Atria  
Singapore 238877  
+65 6 887 5505

**Europe**

IDT Europe, Limited  
321 Kingston Road  
Leatherhead, Surrey  
KT22 7TU  
England  
+44 (0) 1372 363 339  
Fax: +44 (0) 1372 378851



www.IDT.com