

HDTV CLOCK SYNTHESIZER

ICS667-01

Description

The ICS667-01 is a low-cost, low jitter, high-performance PLL clock synthesizer designed to produce the 74.176 MHz clock necessary for HDTV systems. Using IDT's patented analog Phase-Locked Loop (PLL) techniques, the device accepts a 27 MHz crystal or clock input. The zero ppm synthesis error exactly locks the display to the digital stream.

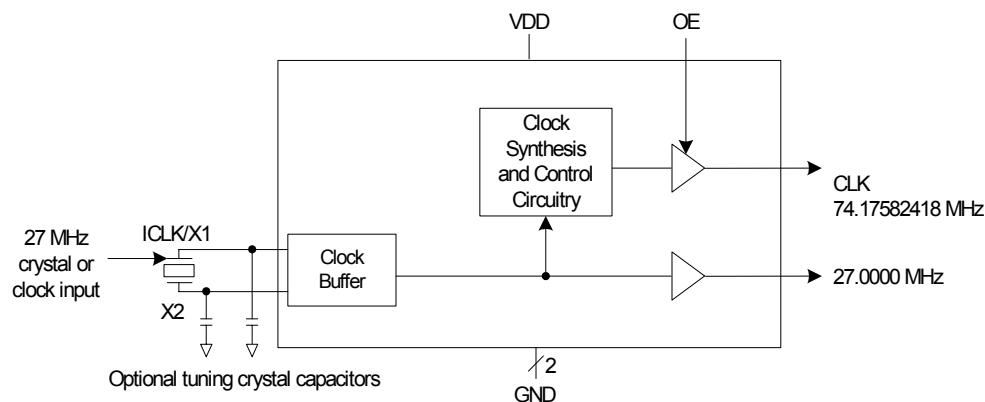
IDT manufactures the largest variety multimedia clock synthesizers for all applications. Consult IDT to eliminate crystals and oscillators from your board.

Features

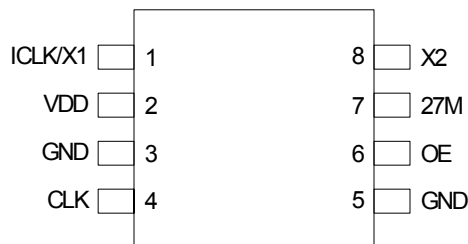
- Packaged in 8-pin SOIC
- Available in Pb (lead) free package
- Input frequency of 27 MHz
- Zero ppm synthesis error in output clock
- 3.3 V $\pm 5\%$ operating supply
- Ideal for HDTV applications and oscillator manufacturers
- Advanced, low power, sub-micron CMOS process

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | ICLK/X1 | XI | Crystal connection. Connect to a 27 MHz fundamental crystal or clock. |
| 2 | VDD | Power | Connect to +3.3 V. |
| 3 | GND | Power | Connect to ground. |
| 4 | CLK | Output | 74.17582418 MHz. |
| 5 | GND | Power | Connect to ground. |
| 6 | OE | Input | Output enable. Tri-states CLK output when low. Internal pull-up to VDD. |
| 7 | 27M | Output | 27 MHz buffered clock or crystal oscillator output. |
| 8 | X2 | XO | Crystal connection. Connect to a 27 MHz crystal, or leave unconnected for clock input. |

External Components

Decoupling Capacitor

A decoupling capacitor of 0.01 μ F must be connected between VDD and GND on pins 2 and 3. It must be connected close to the ICS667-01 to minimize lead inductance. Pin 5 can be connected to pin 3. No external power supply filtering is required for the ICS667-01.

Series Termination Resistor

A 33 Ω terminating resistor can be used next to the clock outputs for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 18 pF. A parallel resonant, fundamental mode, AT cut 27 MHz crystal should be used. The device crystal connections should

include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 16 \text{ pF}) \times 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with an 18 pF load capacitance, each crystal capacitor would be 4 pF $[(18 - 16) \times 2] = 4$.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS667-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|--------|------|--------|-------|
| Ambient Operating Temperature | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.150 | 3.3 | +3.465 | V |

DC Electrical Characteristics

VDD=3.3 V \pm 5% unless otherwise noted, Ambient temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|-------------------------|---------|----------|-------|-------|
| Operating Voltage | VDD | | 3.15 | 3.3 | 3.465 | V |
| Input High Voltage | V _{IH} | ICLK, OE | 2.0 | | | V |
| Input Low Voltage | V _{IL} | ICLK, OE | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -4 mA | VDD-0.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 4 mA | | | 0.4 | V |
| Operating Supply Current | IDD | No load | | 30 | | mA |
| Short Circuit Current | | Each output | | \pm 50 | | mA |
| Input Capacitance | C _{IN} | | | 7 | | pF |

AC Electrical Characteristics

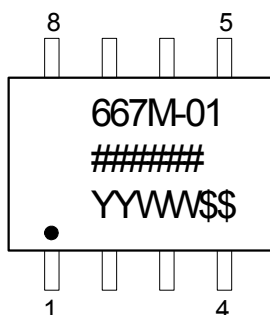
VDD = 3.3V ± 5%, CL = 15pF unless otherwise noted, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|------------------|---------------------------|------|------|------|-------|
| Input Frequency | F _{IN} | | | 27 | | MHz |
| Frequency Error, Output Clock | | | | | 0 | ppm |
| Output Clock Rise Time | t _{OR} | 0.8 to 2.0 V | | | 1.5 | ns |
| Output Clock Fall Time | t _{OF} | 2.0 to 8.0 V | | | 1.5 | ns |
| Output Clock Duty Cycle | | at 1.4 V | 40 | 50 | 60 | % |
| Maximum Absolute Jitter, short term | t _{ja} | Deviation from mean | | 200 | | ps |
| Maximum Absolute Jitter, Long term term over 1μs | t _{jl} | Deviation from mean | | 500 | | ps |
| Output Enable Time | | OE going from Low to High | | 20 | | ns |
| Internal Pull-up Resistor | R _{PUP} | OE pin | | 750 | | kΩ |

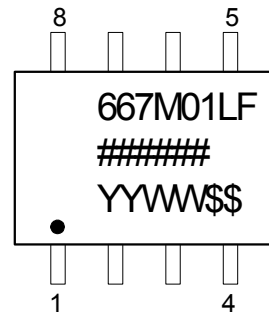
Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ _{JA} | Still air | | 150 | | °C/W |
| | θ _{JA} | 1 m/s air flow | | 140 | | °C/W |
| | θ _{JA} | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | θ _{JC} | | | 40 | | °C/W |

Marking Diagram



Marking Diagram (Pb free)

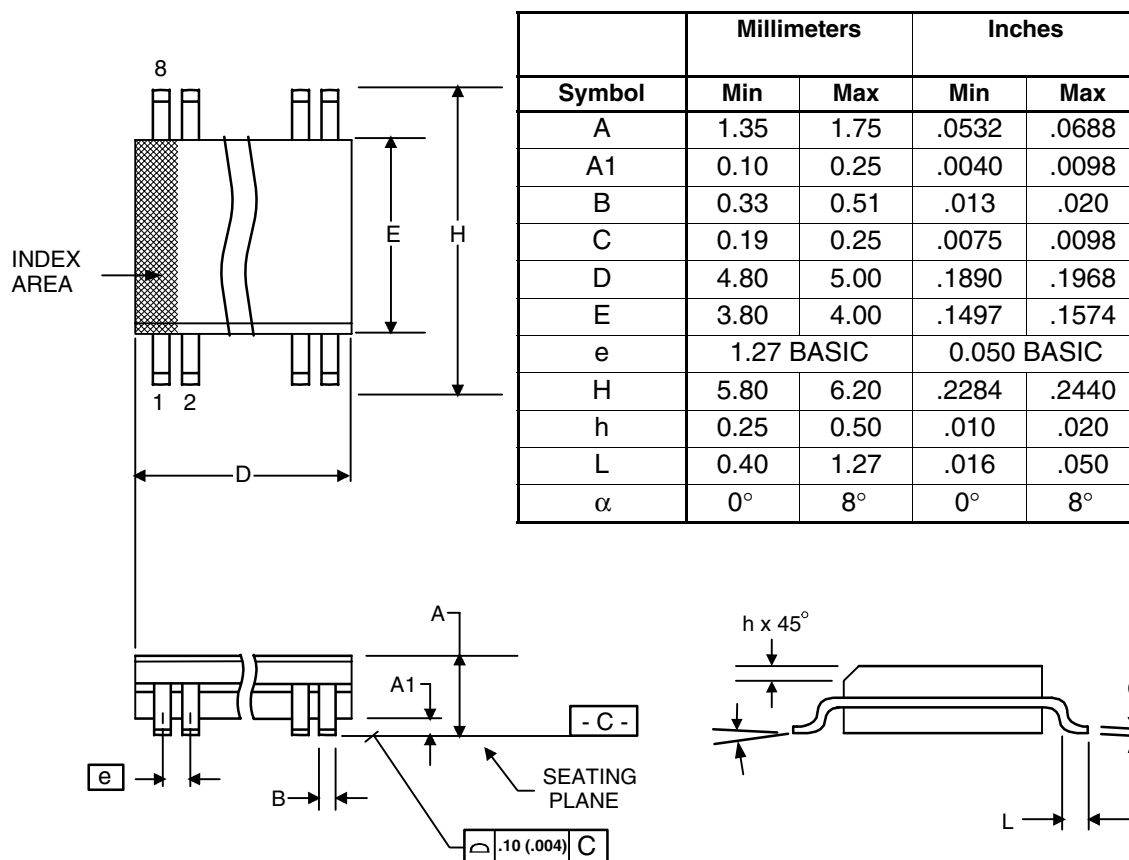


Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. Bottom marking: (origin)
Origin = country of origin if other than USA.
4. "LF" denotes Pb (lead) free package.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|------------|-------------|
| 667M-01* | see page 5 | Tubes | 8-pin SOIC | 0 to +70° C |
| 667M-01T* | | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 667M-01LF | see page 5 | Tubes | 8-pin SOIC | 0 to +70° C |
| 667M-01LFT | | Tape and Reel | 8-pin SOIC | 0 to +70° C |

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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