LOW PHASE NOISE CLOCK MULTIPLIER ICS601-02

Description

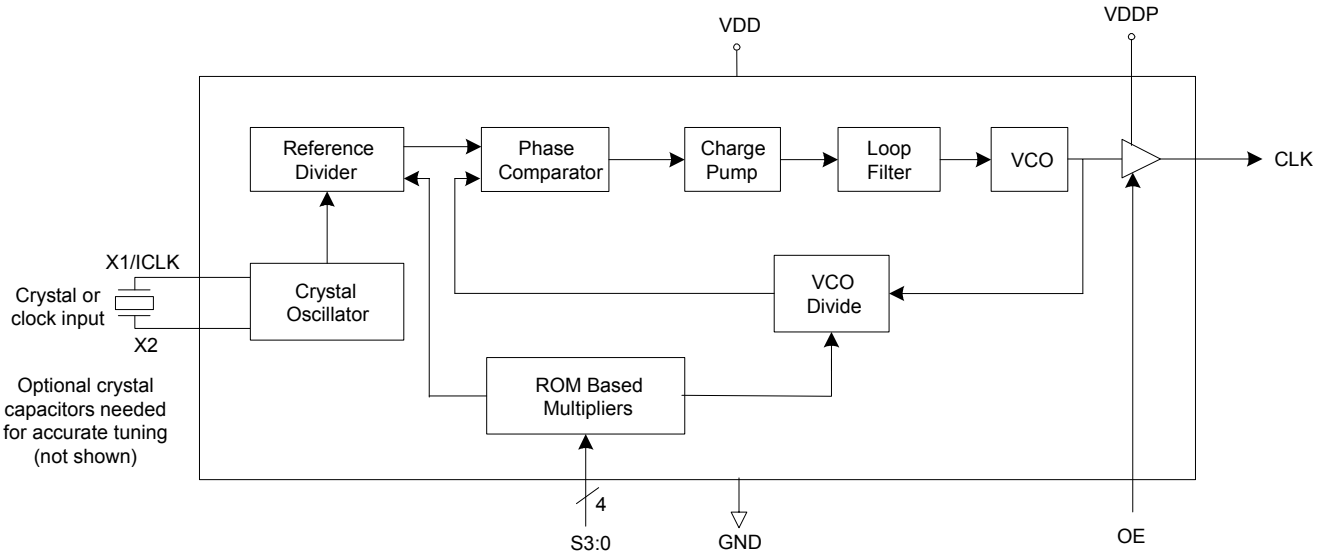
The ICS601-02 is a low cost, low phase noise, high performance clock synthesizer for any application that requires low phase noise and low jitter. The ICS601 is IDT's lowest phase noise multiplier. Using IDT's patented analog and digital Phase Locked Loop (PLL) techniques, the chip accepts a 10–27 MHz crystal or clock input, and produces output clocks up to 170 MHz at 3.3 V. A separate supply pin is provided so that the output can be 2.5 V.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed. For applications which require defined input to output timing, use the ICS670-01.

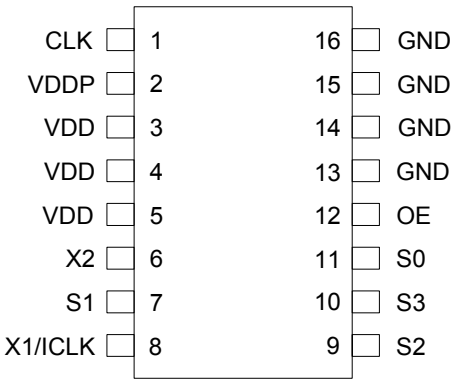
Features

- Packaged in 16-pin SOIC (Pb free)
- Uses fundamental 10 - 27 MHz crystal or clock
- Patented PLL with the lowest phase noise
- Output clocks up to 170 MHz at 3.3 V
- Output Enable function tri-states outptus
- Low phase noise: -132 dBc/Hz at 10 kHz
- Low jitter - 18 ps one sigma
- Full swing CMOS outputs with 25 mA drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- Industrial temperature range (-40 to +85°C)
- 3.3 V or 5 V core VDD. Output clock can operate down to 2.5 V.

Block Diagram



Pin Assignment



16-pin SOIC

Multiplier Select Table

S3	S2	S1	S0	CLK
0	0	0	0	Input x4/3
0	0	0	1	Input x4
0	0	1	0	Input x25/4
0	0	1	1	Input x3
0	1	0	0	Input x7.5
0	1	0	1	Input x5
0	1	1	0	Input x6
0	1	1	1	Input x8
1	0	0	0	Input x8/3
1	0	0	1	Input x8
1	0	1	0	Input x12.5
1	0	1	1	Input x6
1	1	0	0	Input x15
1	1	0	1	Input x10
1	1	1	0	Input x12
1	1	1	1	Input x16

0 = connect directly to ground
1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLK	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
2	VDDP	Power	Supply pin for CLK output buffer. Sets output clock amplitude. Connect to 2.5V or 3.3V.
3	VDD	Power	Connect to +3.3V or +5V. Must match other VDDs.
4	VDD	Power	Connect to +3.3V or +5V. Must match other VDDs.
5	VDD	Power	Connect to +3.3V or +5V. Must match other VDDs.
6	X2	XO	Crystal connection. Connect to a 10 - 27 MHz fundamental parallel mode crystal.
7	S1	Input	Multiplier select pin 1. Determines CLK output per table above. Internal pull-up.
8	X1/ICLK	XI	Crystal connection. Connect to a 10-27 MHz fundamental parallel mode crystal, or clock.
9	S2	Input	Multiplier select pin 2. Determines CLK output per table above. Internal pull-up.
10	S3	Input	Multiplier select pin 3. Determines CLK output per table above. Internal pull-up.
11	S0	Input	Multiplier select pin 0. Determines CLK output per table above. Internal pull-up.
12	OE	Input	Output Enable. Tri-states the output clock when low. Internal pull-up.
13	GND	Power	Connect to ground.
14	GND	Power	Connect to ground.
15	GND	Power	Connect to ground.
16	GND	Power	Connect to ground.

Achieving Low Phase Noise

Figure 1 shows a typical phase noise measurement in a 125 MHz system. There are a few simple steps that can be taken to achieve these levels of phase noise from the ICS601-02. Variations in VDD will increase the phase noise, so it is important to have a stable, low noise supply voltage at the device. Use decoupling capacitors of 0.1 µF in parallel with 0.01 µF. It is important to have these capacitors as close as possible to the ICS601-02 supply pins.

Disabling the REFOUT clock is also important for achieving low phase noise; lab tests have shown that this can reduce the phase noise by as much as 10 dBc/Hz.

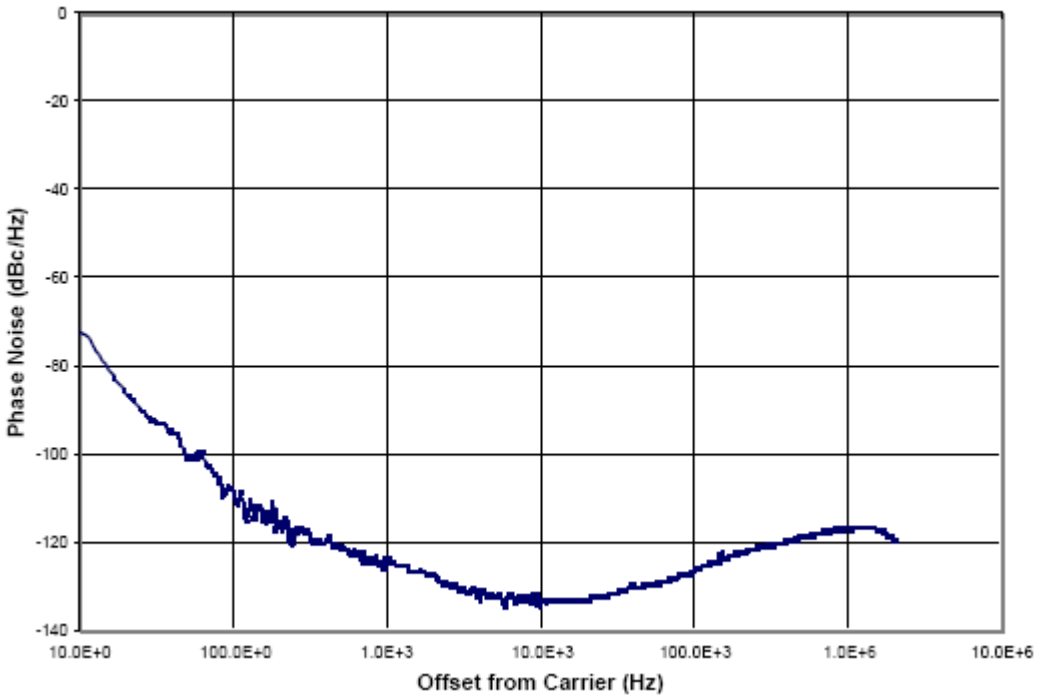


Figure 1: Phase Noise of ICS601-02 at 125 MHz out, 25 MHz crystal input, VDD=3.3 V.

External Components

The ICS601-02 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 µF and 0.1 µF should be connected between VDD and GND, as close to the part as possible. A series termination resistor of 33 Ω may be used for the clock output. The crystal must be connected as close to the chip as possible. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. In general, the value of these capacitors is given by the following equation, where CL is the crystal load capacitance: Crystal caps (pF) = (CL-5) x 2. So for a crystal with 16 pF load capacitance, two 22 pF caps can be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS601-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD (referenced to ground)	7 V
All Inputs and Outputs (referenced to ground)	-0.5 V to VDD+0.5 V
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C
Ambient Operating Temperature (industrial)	-40 to +85°C

DC Electrical Characteristics

Unless stated otherwise, **VDD = VDDP = 3.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Output Buffer Voltage	VDDP		2.375		VDD	V
Input High Voltage	V_{IH}	XI/ICLK pin only, Note 1	(VDD/2)+1			V
Input Low Voltage	V_{IL}	XI/ICLK pin only, Note 1			(VDD/2)-1	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Opertating Supply Current	IDD	No load, 125 MHz		9	20	mA
Short Circuit Current	I_{OS}	Each output	±40	±60		mA
Input Capacitance	C_{IN}	OE, select pins		5		pF

Note 1: Switching occurs nominally at VDD/2.

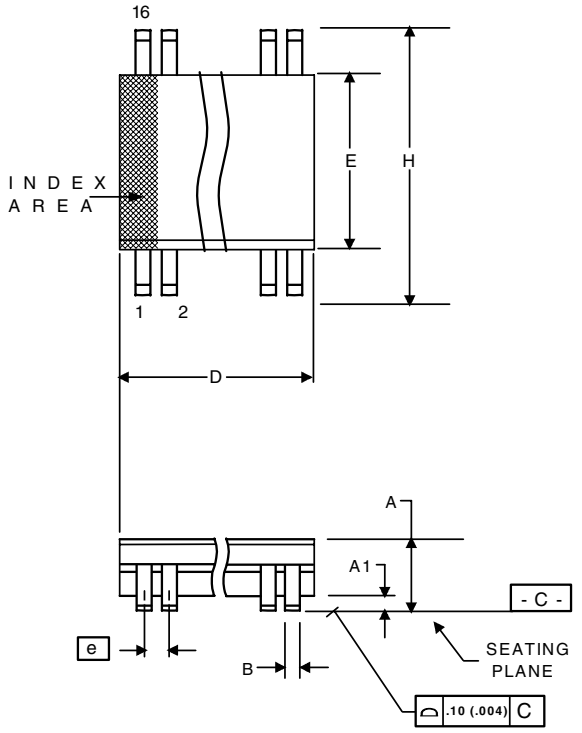
AC Electrical Characteristics

Unless stated otherwise, **VDD = VDDP = 3.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}		10		27	MHz
Output Frequency	f_{OUT}	At 3.3 V or 5 V			170	MHz
Output Clock Rise Time		0.8 to 2.0 V, no load			1.5	ns
Output Clock Fall Time		0.8 to 2.0 V, no load			1.5	ns
Output Clock Duty Cycle		At VDD/2	45	50	55	%
Maximum Absolute Jitter, short term, 125 MHz		No load		±50	±75	ps
Maximum Jitter, one sigma, 125 MHz (x5)		No load		18	25	ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset		-108		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		1 kHz offset		-123		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		10 kHz offset		-132		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		100 kHz offset		-125		dBc/Hz

Package Outline and Package Dimensions (16 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	SOIC	
Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
L	0.40	1.27
α	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS601M-02I	ICS601M-02I	Tubes	16-pin SOIC	-40 to +85° C
ICS601M-02IT	ICS601M-02I	Tape and Reel	16-pin SOIC	-40 to +85° C
ICS601M-02ILF	601M-02ILF	Tubes	16-pin SOIC	-40 to +85° C
ICS601M-02ILFT	601M-02ILF	Tape and Reel	16-pin SOIC	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
E		02/10/09	Converted to IDT document template.

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