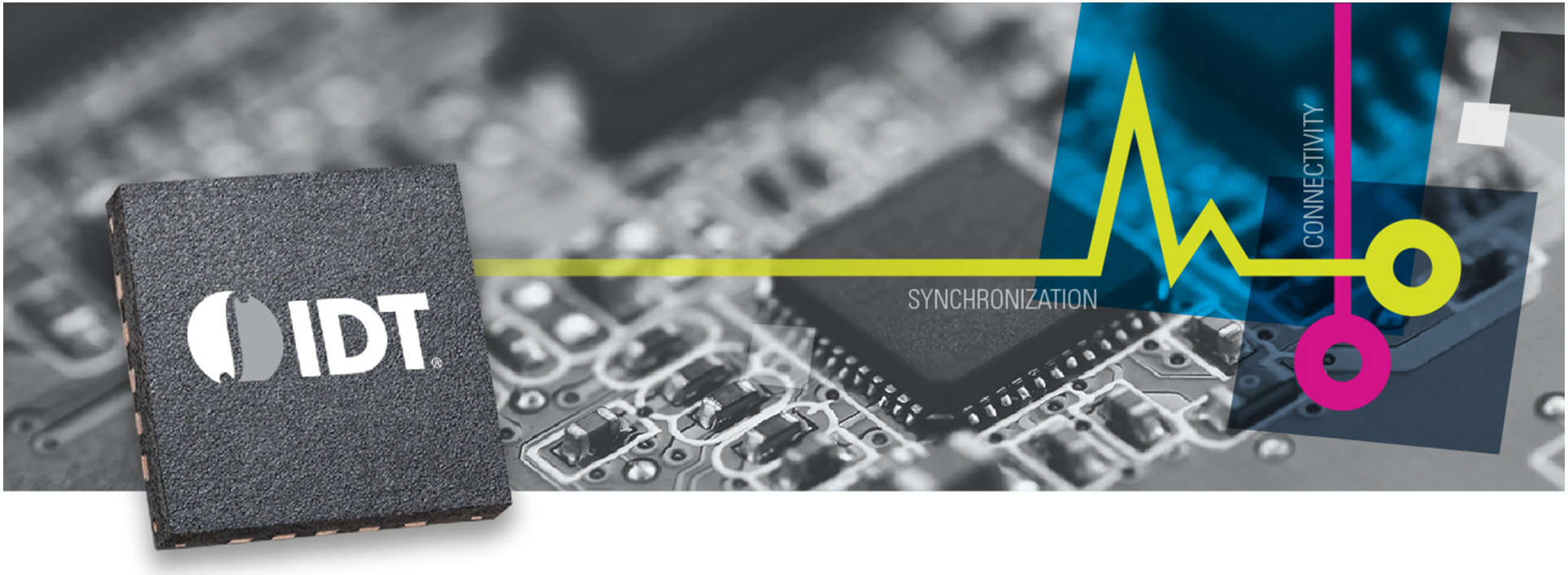


8V4xNS0x12 Clock Generators Channel NPI

November, 2017

8V4xNS0x12 Product Family Snapshot

80 fs Ultra-Low-Noise Clock Generators

Features

- 80 fs phase noise 156.25 Mhz
  - 12K to 20Mhz integration range
- 12 outputs in four banks with individual dividers
- Tight output skew less than 50 ps
- Fractional divider on Bank D
- Load configuration from EEPROM (412 only)
- Compact 9x9mm 64QFN package

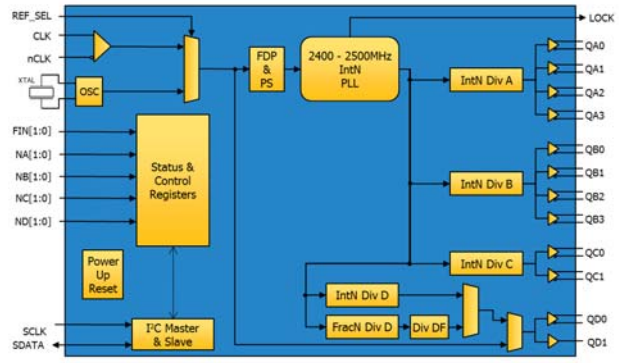
Benefits

- Ultra-low phase noise enables migration to 100/400G applications
- Eliminates need for individual clock domains and fanout buffer which reduces BOM and streamlines design
- Allows generation of one unrelated output frequency

Applications

- Integrated clock generator for 100 / 400Gbps interfaces
- Supports Ethernet, SONET or CPRI frequencies up to 2500MHz
- Also in many reference designs for high-speed SERDES applications

Block Diagram and Variants



Part Number	Features
8V49NS0312NLGI	LVDS / LVPECL output type
8V41NS0412NLGI	HCSL, 212.5MHz default
8V49NS0412NLGI	LVDS/LVPECL, 212.5MHz default