FEMTOCLOCKS™ LVCMOS/CRYSTAL-TO-SSTL_2 FREQUENCY SYNTHESIZER

ICS848004I

General Description

The ICS848004I is a 4 output SSTL_2 Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz and 53.125MHz. The ICS848004I uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The ICS848004I is packaged in a small 24-pin TSSOP package.

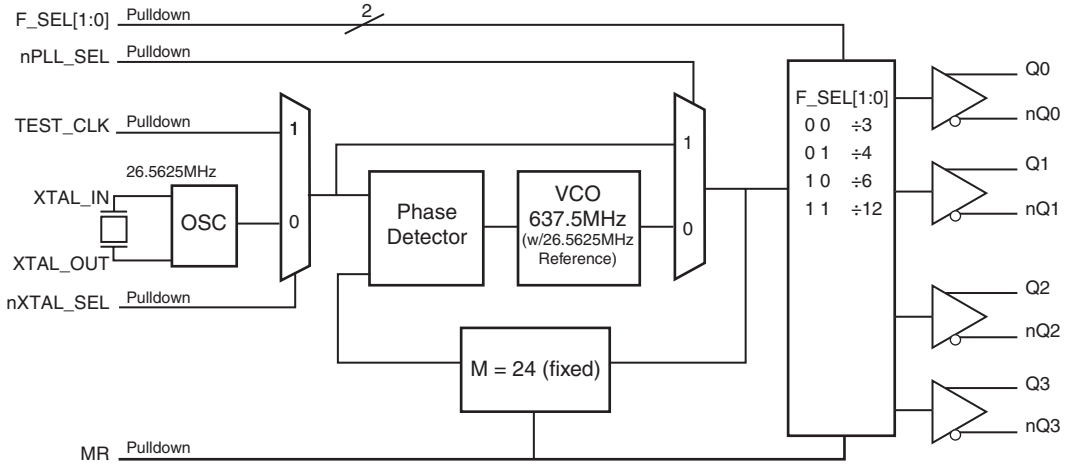
Features

- Four SSTL_2 differential clock output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, 53.125MHz
- VCO range: 560MHz – 680MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (637kHz – 10MHz): 0.80ps (typical)
- SSTL operating voltage supply ranges:
  V_{DD} / V_{DDO}
  3.0V – 3.6V / 3.0V to 3.6V
  2.3V – 3.6V / 2.3V – 2.7V
  2.3V – 3.6V / 1.7V – 1.9V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

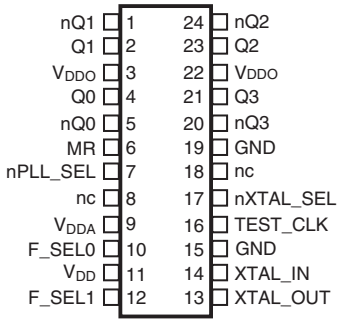
Frequency Select Function Table

Inputs						
Input Frequency (MHz)	F_SEL1	F_SEL0	M Div. Value	N Div. Value	M/N Div. Value	Output Frequency (MHz)
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25
23.4375	0	0	24	3	8	187.5

Block Diagram



Pin Assignment



ICS848004I

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. SSTL_2 interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	Q0, nQ0	Output		Differential output pair. SSTL_2 interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go LOW and the inverted outputs nQx to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL enabled). When HIGH, deselects the reference clock (PLL bypassed). LVCMOS/LVTTL interface levels.
8, 18	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10, 12	F_SEL0. F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	GND	Power		Power supply ground.
16	TEST_CLK	Input	Pulldown	Single-ended test clock input. LVCMOS/LVTTL interface levels.
17	nXTAL_SEL	Input	Pulldown	Selects between the single-ended TEST_CLK or crystal interface as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects crystal inputs. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. SSTL_2 interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. SSTL_2 interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to $V_{DD\ O}$ + 0.5V
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{DDO}	Output Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current			65		mA
I_{DDA}	Analog Supply Current			7		mA
I_{DDO}	Output Supply Current			12		mA

Table 3B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 10\%$ or $2.5V \pm 10\%$, $V_{DDO} = 2.5V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.25	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		2.25	3.3	3.63	V
V_{DDO}	Output Supply Voltage		2.25	2.5	2.75	V
I_{DD}	Power Supply Current			64		mA
I_{DDA}	Analog Supply Current			7		mA
I_{DDO}	Output Supply Current			12		mA

Table 3C. Power Supply DC Characteristics, V_{DD} = 3.3V ± 10% or 2.5V ± 10%, V_{DDO} = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.25	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		2.25	3.3	3.63	V
V_{DDO}	Output Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current			62		mA
I_{DDA}	Analog Supply Current			7		mA
I_{DDO}	Output Supply Current			12		mA

Table 3D. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{DD} = V_{IN} = 3.63V or 2.75V			150	µA
I_{IL}	Input Low Current	TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{DD} = 3.63V or 2.75V, V_{IN} = 0V	-5			µA

Table 3E. Differential DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Output Differential Voltage		0.7			V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		0.5		V_{DDO} – 0.85	V
V_{OH}	Output High Voltage; NOTE 2			>2.1		V
V_{OL}	Output Low Voltage; NOTE 2			<0.9		V

NOTE 1: V_{CMR}, V_{PP} defined for driving TEST_CLK input with differential levels other than SSTL_2.
NOTE 2: Outputs termination with 50Ω to GND.

Table 3F. Differential DC Characteristics, V_{DD} = 3.3V ± 10% or 2.5V ± 10%, V_{DDO} = 2.5V ± 10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Output Differential Voltage		0.7			V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		0.5		V_{DDO} – 0.85	V
V_{OH}	Output High Voltage; NOTE 2			>1.77		V
V_{OL}	Output Low Voltage; NOTE 2			<0.73		V

NOTE 1: V_{CMR}, V_{PP} defined for driving TEST_CLK input with differential levels other than SSTL_2.
NOTE 2: Outputs termination with 50Ω to GND.

Table 3G. Differential DC Characteristics, V_{DD} = 3.3V ± 10% or 2.5V ± 10%, V_{DDO} = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Output Differential Voltage		0.7			V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		0.5		V_{DDO} – 0.85	V
V_{OH}	Output High Voltage; NOTE 2			>1.19		V
V_{OL}	Output Low Voltage; NOTE 2			<0.615		V

NOTE 1: V_{CMR}, V_{PP} defined for driving TEST_CLK input with differential levels other than SSTL_2.
NOTE 2: Outputs termination with 50Ω to GND.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

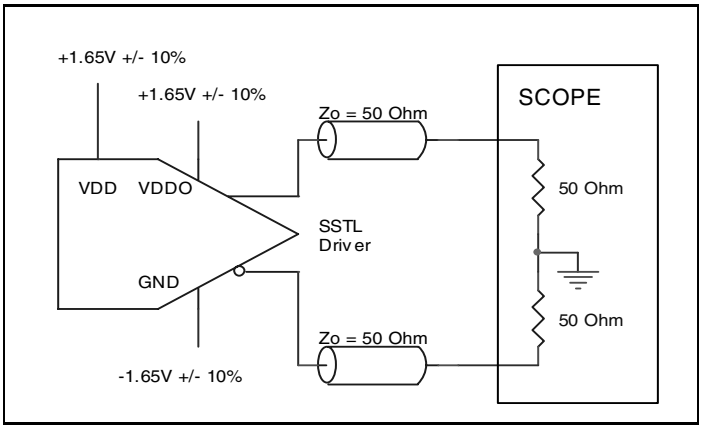
AC Electrical Characteristics

Table 5. AC Characteristics, T_A = -40°C to 85°C

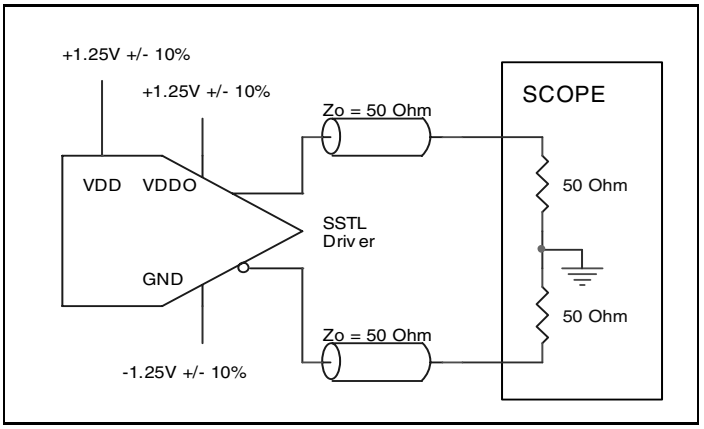
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 3	212.5MHz, (637kHz – 10MHz)		0.80		ps
		159.375MHz, (637kHz – 10MHz)		0.78		ps
		156.25MHz, (1.875MHz – 20MHz)		0.50		ps
		106.25MHz, (637kHz – 10MHz)		0.81		ps
		53.125MHz, (637kHz – 10MHz)		0.79		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		650		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plots.

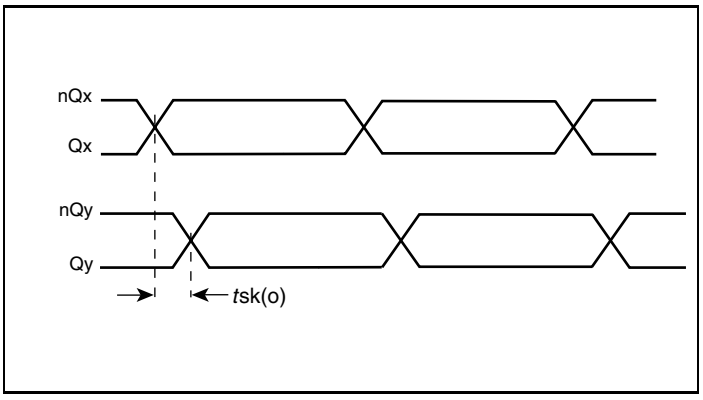
Parameter Measurement Information



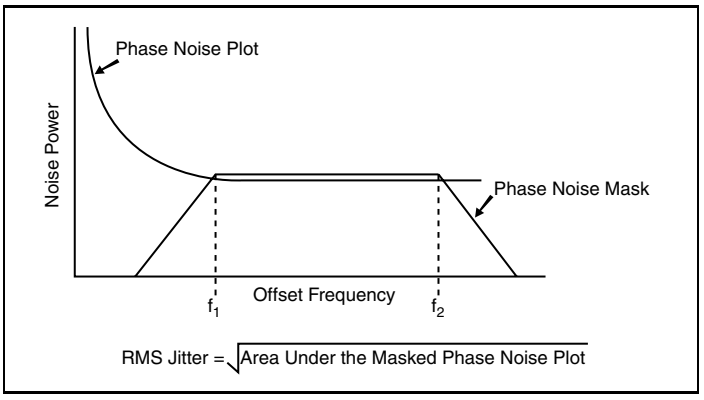
3.3V Core/3.3V Output Load AC Test Circuit



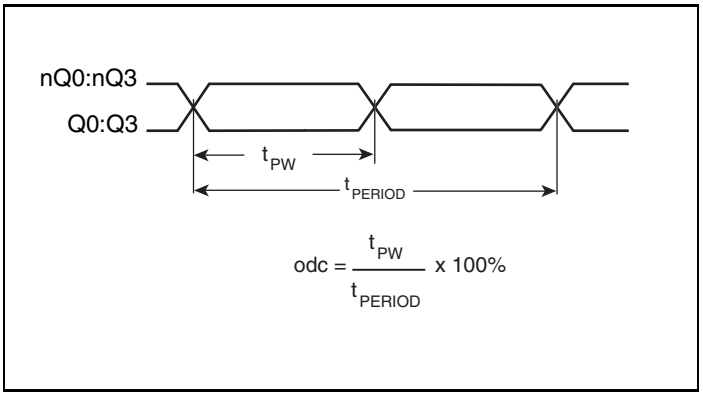
2.5V Core/2.5V Output Load AC Test Circuit



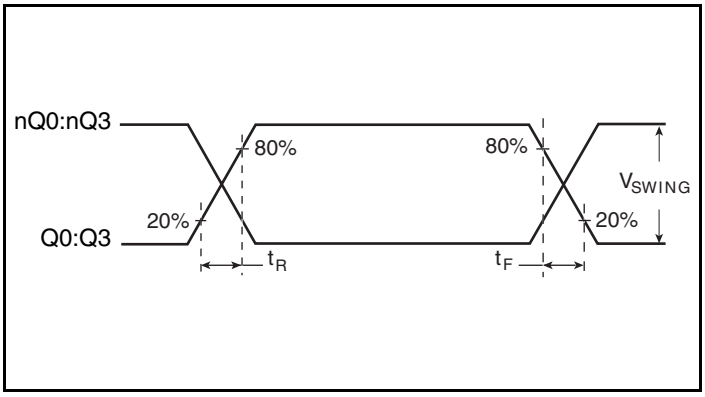
Output Skew



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS848004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD,}$ V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

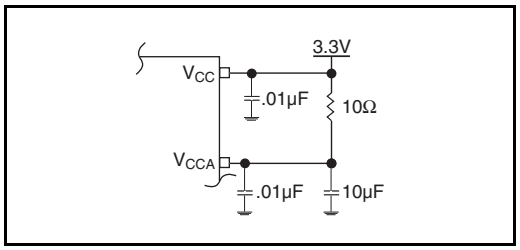


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

SSTL Outputs

All unused SSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS848004I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

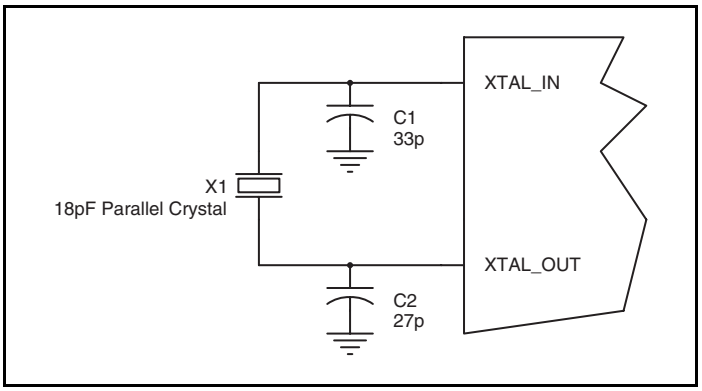


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

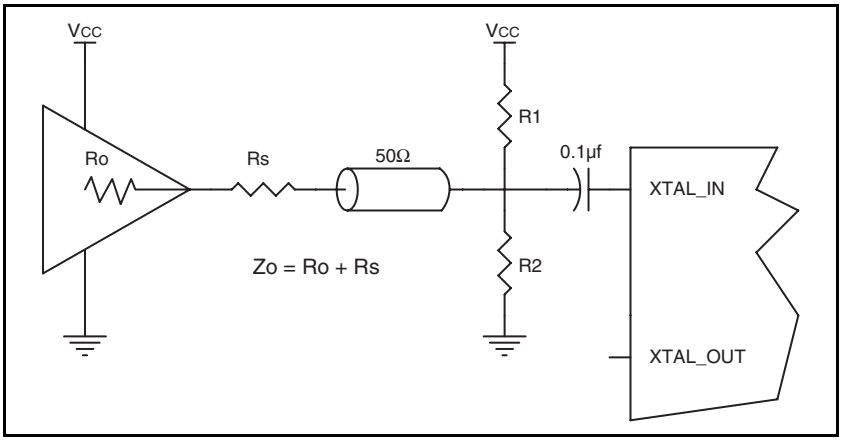


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

SSTL Interface

Figures 4A to *Figure 4C* show interface examples of ICS848004I SOCKET/nSOCKET input driven by an SSTL driver. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. The SSTL termination shown in these examples are also suitable for ICS848004I SSTL output drivers.

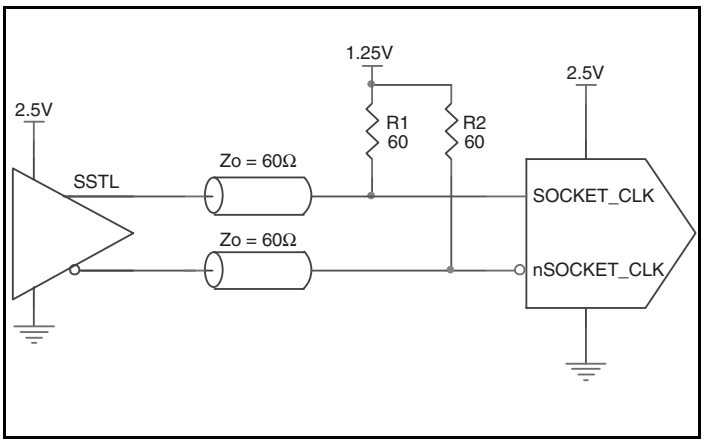


Figure 4A. Typical SSTL Interface for V_{DD}/2 = 1.25V being Available

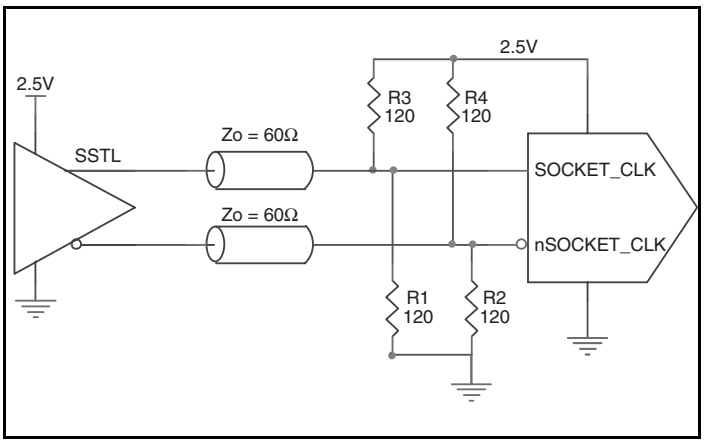


Figure 4B. SSTL Interface for V_{DD}/2 = 1.25V with No Available

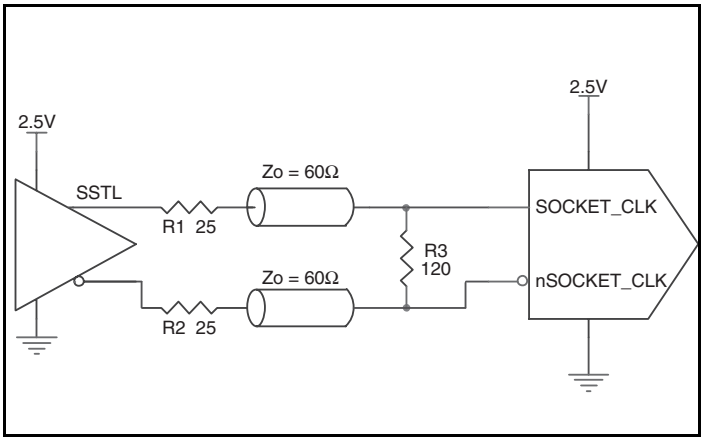


Figure 4C. Differential SSTL Interface

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0	75.9

Transistor Count

The transistor count for ICS848004I is: 2951

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

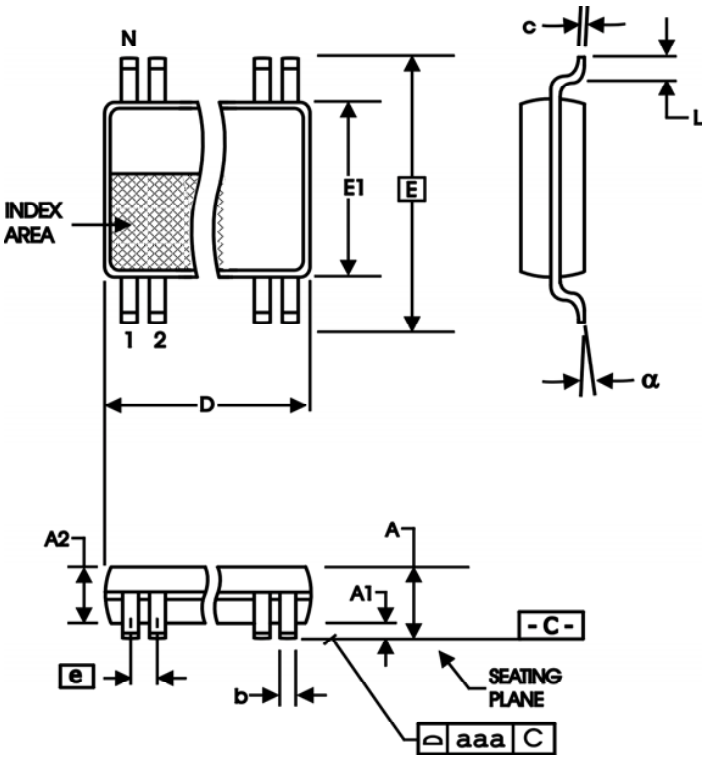


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS848004AGI	ICS848004AGI	24 Lead TSSOP	Tube	-40°C to 85°C
ICS848004AGIT	ICS848004AGI	24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
ICS848004AGILF	ICS848004AGIL	“Lead-Free” 24 Lead TSSOP	Tube	-40°C to 85°C
ICS848004AGILFT	ICS848004AGIL	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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