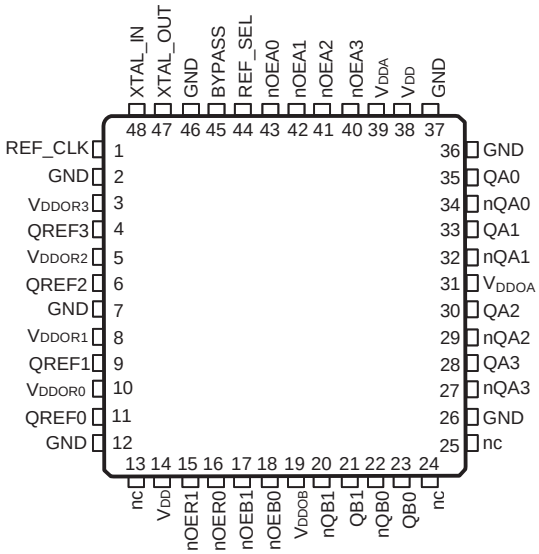
General Description

The ICS844S259I is a 10 LVDS/LVTTL output clock synthesizer designed for instrumentation and wireless applications. The device generates 4 copies of a 125MHz, and 2 copies of a 100MHz differential LVDS clock signal with excellent phase jitter performance. The PLL is optimized for a reference frequency of 25MHz. Both a crystal interface and a single-ended input are supported for the reference frequency. Four LVCMOS outputs duplicate the reference frequency and are provided for clock tree cascade purpose. Each of the four LVCMOS outputs can be supplied with either 3.3V, 2.5V or 1.8V, forming the respective LVCMOS output levels of 3.3V, 2.5V or 1.8V. The device uses IDT's third generation FemtoClock® technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption. The device supports a 3.3V voltage supply and is packaged in a small, lead-free (RoHS 6) 48-lead VFQFN package.

Features

- Third generation FemtoClock® technology
- 125MHz and 100MHz output clock synthesized from a 25MHz reference clock or fundamental mode crystal
- Six differential LVDS clock outputs
- QA[0:3] outputs (125MHz) are LVDS compatible
- QB[0:1] outputs (100MHz) are LVDS compatible
- Four single-ended LVCMOS-compatible reference clock outputs
- QREF[0:3] (25MHz) are 3.3V, 2.5V or 1.8V LVCMOS compatible
- Crystal interface designed for 25MHz XTAL (optional)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz - 20MHz): 0.583ps (typical)
- RMS phase jitter @ 100MHz, using a 25MHz crystal (12kHz - 20MHz): 0.570ps (typical)
- LVCMOS interface levels for the control input
- I/O supply voltage for LVCMOS:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
- I/O supply voltage for LVDS:
  Core/Output
  3.3V/2.5V
- Available in Lead-free (RoHS 6) compliant package
- -40°C to 85°C ambient operating temperature

Pin Assignment



ICS844S259I
48-lead VFQFN
7.0mm x 7.0mm x 0.925mm package body
K Package
Top View

Block Diagram

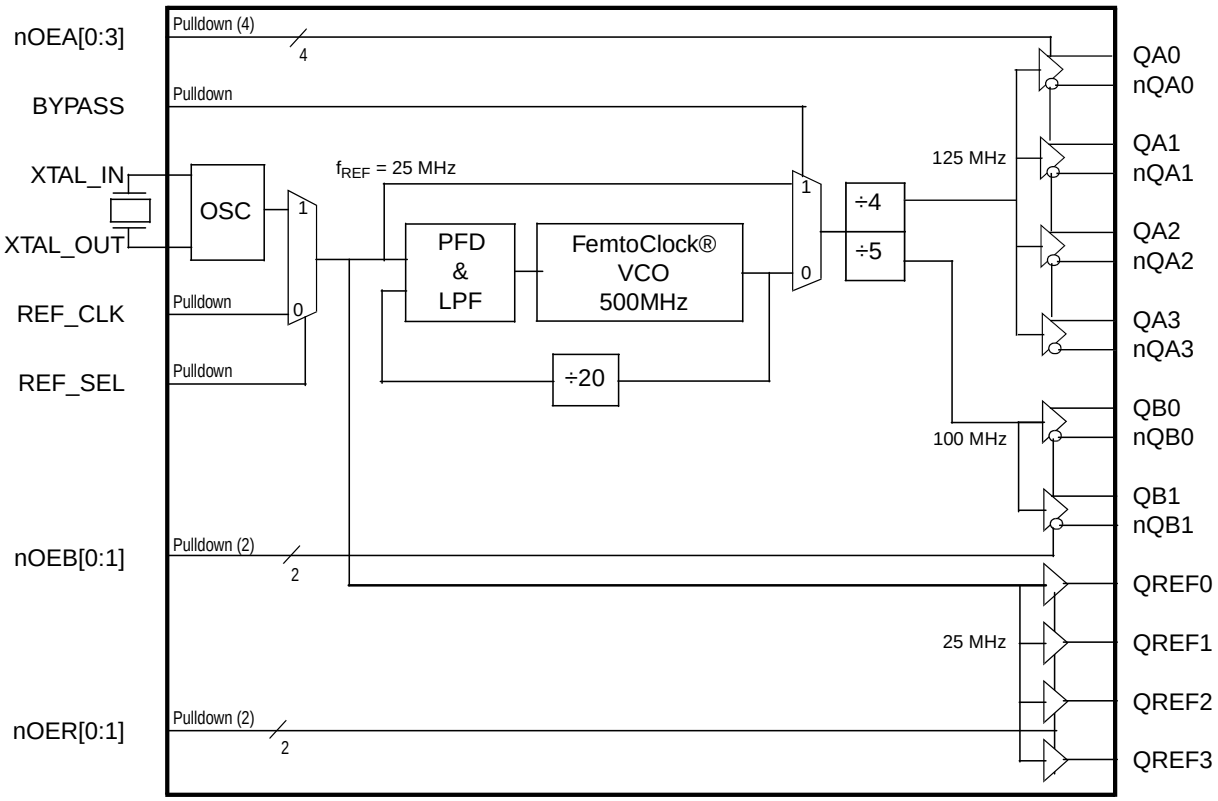


Table 1. Pin Descriptions

Number	Name	Type		Description
1	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
2, 7, 12, 26, 36, 37, 46	GND	Power		Power supply ground.
3	V_{DDOR3}	Power		Output supply pin for the output QREF3.
4, 6, 9, 11	QREF3, QREF2, QREF1, QREF0	Output		Single-ended reference clock outputs. LVCMOS/LVTTL interface levels.
5	V_{DDOR2}	Power		Output supply pin for the output QREF2.
8	V_{DDOR1}	Power		Output supply pin for the output QREF1.
10	V_{DDOR0}	Power		Output supply pin for the output QREF0.
13, 24, 25	nc	Unused		No connect.
14, 38	V_{DD}	Power		Core supply pins.
15, 16	nOER1, nOER0	Input	Pulldown	Output enable inputs for the QREFx outputs. See Table 3E for function. LVCMOS/LVTTL interface levels.
17, 18	nOEB1, nOEB0	Input	Pulldown	Output enable inputs for the individual QBn outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
19	V_{DDOB}	Power		Output supply pin for the Bank B outputs.
20, 21	nQB1, QB1	Output		Differential clock output pair (Bank B). LVDS interface levels.
22, 23	nQB0, QB0	Output		Differential clock output pair (Bank B). LVDS interface levels.
27, 28	nQA3, QA3	Output		Differential clock output pair (Bank A). LVDS interface levels.
29, 30	nQA2, QA2	Output		Differential clock output pair (Bank A). LVDS interface levels.
31	V_{DDOA}	Power		Output supply pin for the Bank A outputs.
32, 33	nQA1, QA1	Output		Differential clock output pair (Bank A). LVDS interface levels.
34, 35	nQA0, QA0	Output		Differential clock output pair (Bank A). LVDS interface levels.
39	V_{DDA}	Power		Analog power supply.
40, 41, 42, 43	nOEA3, nOEA2, nOEA1, nOEA0	Input	Pulldown	Output enable inputs for the individual QAn outputs. See Table 3C for function. LVCMOS/LVTTL interface levels.
44	REF_SEL	Input	Pulldown	Reference select pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
45	BYPASS	Input	Pulldown	PLL bypass mode select pin. See Table 3B for function. LVCMOS/LVTTL interface levels.
47, 48	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)		$V_{DDOR[0:3]}$ = 3.465V		7.5		pF
			V_{DDOA}, V_{DDOB}, $V_{DDOR[0:3]}$ = 2.625V		5.5		pF
			$V_{DDOR[0:3]}$ = 2.0V		4.5		pF
R_{OUT}	Output Impedance	QREF[0:3]	$V_{DDOR[0:3]}$ = 3.3V		25		Ω
		QREF[0:3]	$V_{DDOR[0:3]}$ = 2.5V		24		Ω
		QREF[0:3]	$V_{DDOR[0:3]}$ = 1.8V		35		Ω

Function Tables

Table 3A. PLL Reference Clock Select Function Table

Input	
REF_SEL	**Operation**
0 (default)	The REF_CLK input is selected as reference clock
1	The crystal interface is selected as reference clock

NOTE: REF_SEL is an asynchronous control input.

Table 3B. PLL Bypass Select Function Table

Input	
BYPASS	**Operation**
0 (default)	PLL mode
1	PLL bypass mode. The reference clock is routed to the output dividers. AC specifications do not apply in PLL bypass mode.

NOTE: BYPASS is an asynchronous control input.

Table 3C. Outputs QA[0:3] Enable Function Table

Input	
nOEAx	**Operation**
0 (default)	Outputs QA0 / nQA0, QA1 / nQA1, QA2 / nQA2, QA3 / nQA3 are enabled
1	Outputs QA0 / nQA0, QA1 / nQA1, QA2 / nQA2, QA3 / nQA3 are disabled in high-impedance state

NOTE: x = 0 to 3. Each QA[0:3], nQA[0:3] output is individually controlled by the corresponding nOEAx input.
Asynchronous control inputs.

Table 3D. Outputs QB[0:1] Enable Function Table

Input	
nOEBx	**Operation**
0 (default)	Outputs QB0 / nQB0, QB1 / nQB1 are enabled
1	Outputs QB0 / nQB0, QB1 / nQB1 are disabled in high-impedance state

NOTE: x = 0 to 1. Each QB[0:1], nQB[0:1] output is individually controlled by the corresponding nOEBx input.
Asynchronous control inputs.

Table 3E. Outputs QREF[0:3] Enable Function Table

Inputs		Operation	
nOER0	**nOER1**	**Outputs QREF[0:1]**	**Outputs QREF[2:3]**
0 (default)	0 (default)	Enabled	Enabled
0	1	Enabled	Disabled in high-impedance state
1	0	Disabled in high-impedance state	Enabled
1	1	Disabled in high-impedance state	Disabled in high-impedance state

NOTE: nOER[0:1] are asynchronous control inputs.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DDORx} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	29°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDORx} = 1.8V±5% to 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage			3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage			V_{DD} – 0.16	3.3	V_{DD}	V
V_{DDORx}	Output Supply Voltage; NOTE 1			3.135	3.3	3.465	V
V_{DDORx}, V_{DDOA}, V_{DDOB}				2.375	2.5	2.625	V
V_{DDORx}				1.6	1.8	2.0	V
I_{DD}	Core Supply Current					96	mA
I_{DDOA} + I_{DDOB}	LVDS Output Supply Current					150	mA
I_{DDA}	Analog Supply Current					16	mA
I_{DDORx}	Output Supply Current	QREF[0:3]	Static Current			2	mA

NOTE 1: Each V_{DDORx} V_{DDORx} denotes V_{DDOR0}, V_{DDOR1}, V_{DDOR2}, V_{DDOR3}. Supply voltage pin may be left open, connected to GND or supplied by 3.3V.

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 3.3V±5%, V_{DDORx} = 3.3V±5%, 2.5V±5% or 1.8V±0.2V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	REF_SEL, nOEA[0:3], nOEB[0:1], nOER[0:1], BYPASS, REF_CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	REF_SEL, nOEA[0:3], nOEB[0:1], nOER[0:1], BYPASS, REF_CLK	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage; NOTE 1	QREF[0:3]	V_{DDORx} = 3.465V	2.6			V
			V_{DDORx} = 2.625V	1.8			V
			V_{DDORx} = 2.0V	1.5			V
V_{OL}	Output Low Voltage; NOTE 1	QREF[0:3]	V_{DDORx} = 3.465V or 2.625V			0.5	V
			V_{DDORx} = 2.0V			0.4	V

NOTE: V_{DDORx} denotes V_{DDOR0}, V_{DDOR1}, V_{DDOR2}, V_{DDOR3}.

NOTE: nOEAx, nOEBx, nOERx, Bypass and REF_CLK are 3.3V tolerant.

NOTE 1: Output terminated with 50Ω to V_{DDORx} / 2. See Parameter Measurement Information Section.

Table 4C. LVDS DC Characteristics, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, V_{DDORx} = 3.3V±5%, 2.5V±5% or 1.8V±0.2V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency		BYPASS = 0		500		MHz
f_{OUT}	Output Frequency	QA[0:3], nQA[0:3]			125		MHz
		QB[0:1], nQB[0:1]			100		MHz
		QREF[0:3]			25		MHz
f_{REF}	Reference Frequency				25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1, 2	QA[0:3], nQA[0:3]	25MHz crystal, f_{OUT} = 125MHz, Integration Range: 12kHz – 20MHz		0.583	0.833	ps
		QB[0:1], nQB[0:1]	25MHz crystal, f_{OUT} = 100MHz, Integration Range: 12kHz – 20MHz		0.570	0.790	ps
		QREF[0:3]	25MHz crystal, f_{OUT} = 25MHz, Integration Range: 12kHz – 5MHz		0.576	0.676	ps
*t*jit(per)	RMS Period Jitter	QA[0:3], nQA[0:3]	125MHz		1.77	2.0	ps
		QB[0:1], nQB[0:1]	100MHz		1.86	2.5	ps
		QREF[0:3]	25MHz			3.3	ps
*t*jit(cc)	Cycle-to-Cycle Jitter	QA[0:3], nQA[0:3]	125MHz			20	ps
		QB[0:1], nQB[0:1]	100MHz			19	ps
		QREF[0:3]	25MHz			18	ps
tsk(b)	Bank Skew; NOTE 3, 4	QA[0:3], nQA[0:3]	f_{REF} = 25MHz			35	ps
		QB[0:1], nQB[0:1]	f_{REF} = 25MHz			23	ps
		QREF[0:3]	f_{REF} = 25MHz			40	ps
t_R / t_F	Output Rise/Fall Time	QA[0:3], nQA[0:3] QB[0:1], nQB[0:1]]	20% to 80%	35		285	ps
		QREF[0:3]	20% to 80%	135		675	ps
t_{LOCK}	PLL Lock Time					80	ms
odc	Output Duty Cycle	QA[0:3], nQA[0:3]	125MHz	48		52	%
		QB[0:1], nQB[0:1]	100MHz	48		52	%
		QREF[0:3]	25MHz	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

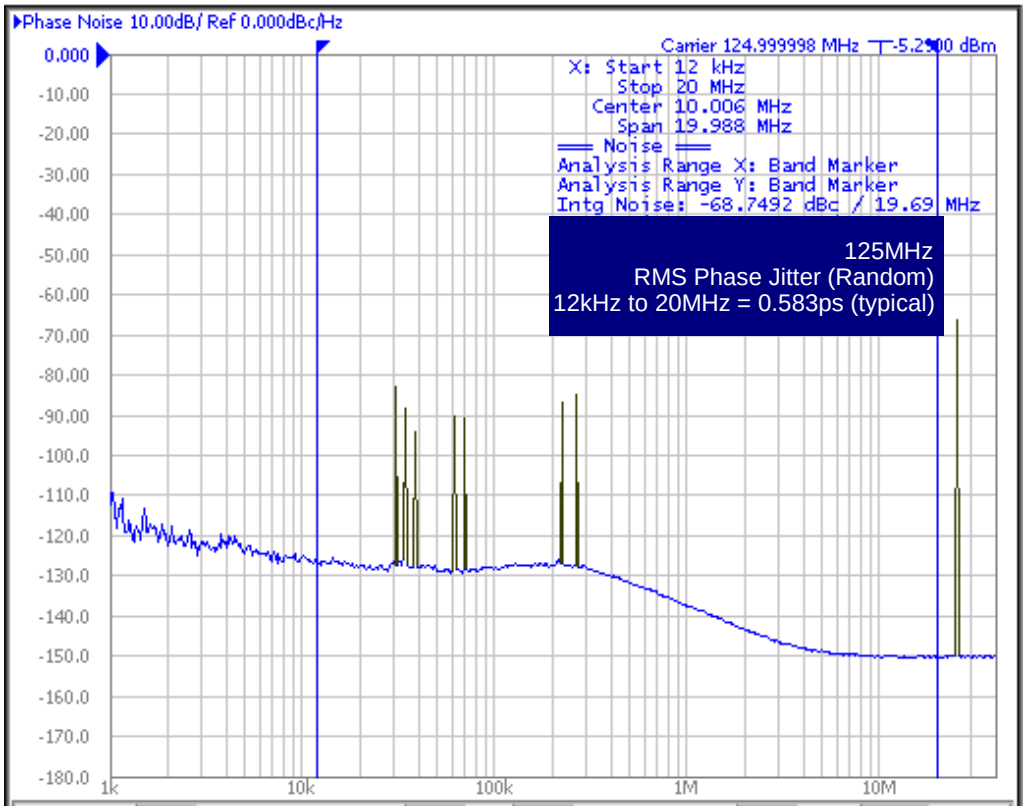
NOTE 1: Refer to the phase noise plots.

NOTE 2: Measured with REF_SEL = 0 using Rohde & Schwarz SMA100A Signal Generator 9kHz - 6GHz to drive HP8133A Pulse Generator as the reference source.

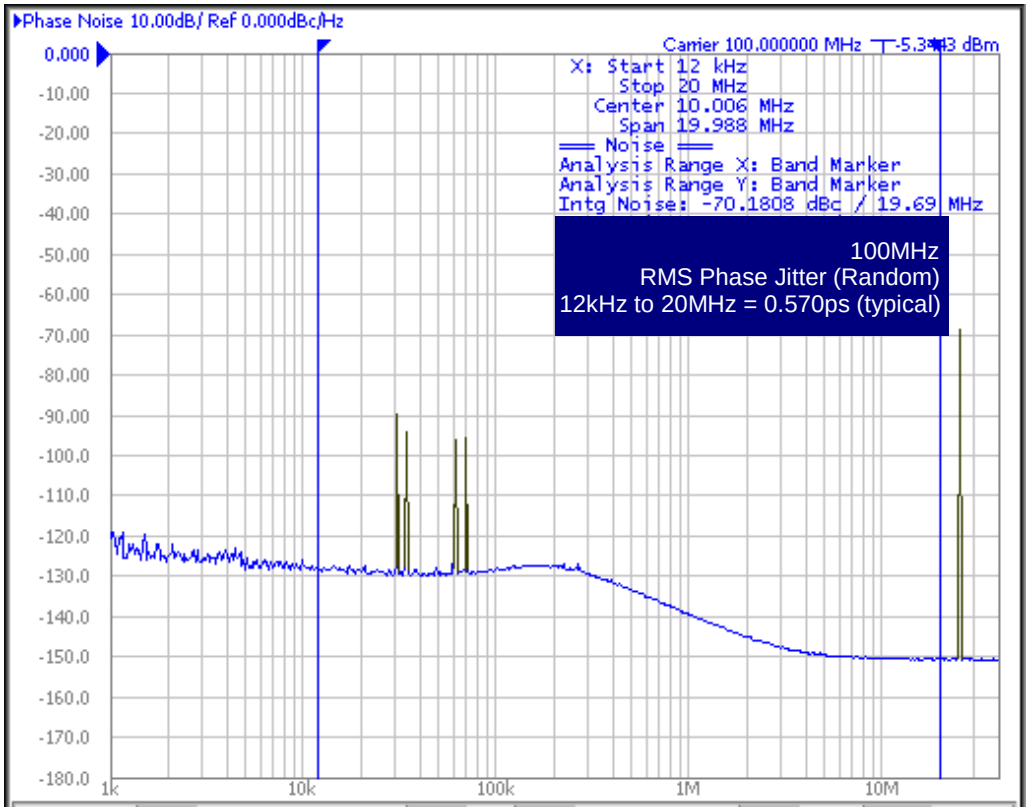
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

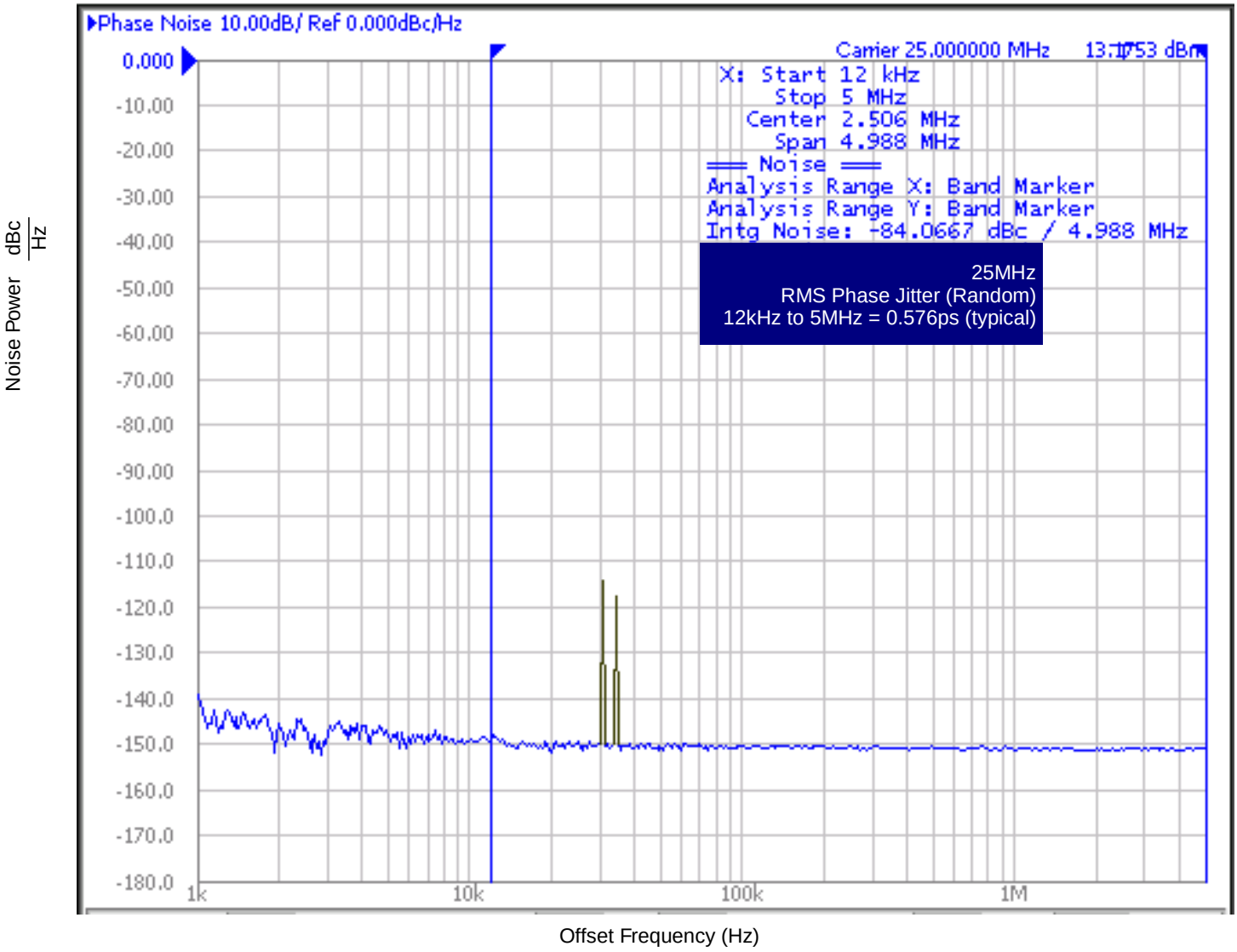
Typical Phase Noise at 125MHz (QAx Outputs)



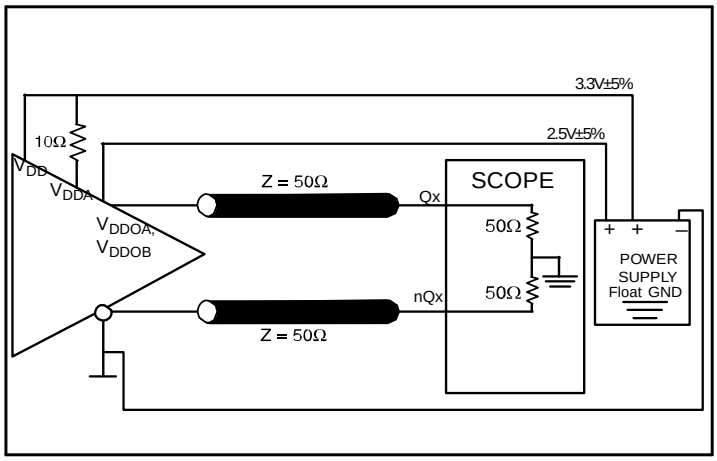
Typical Phase Noise at 100MHz (QBx Outputs)



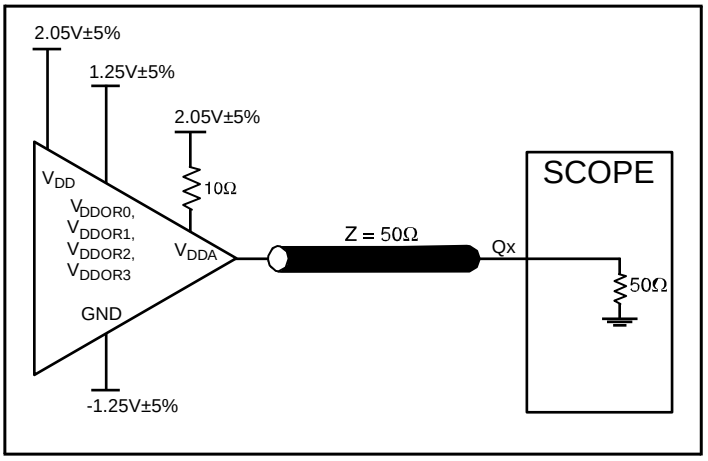
Typical Phase Noise at 25MHz (QREFx Outputs)



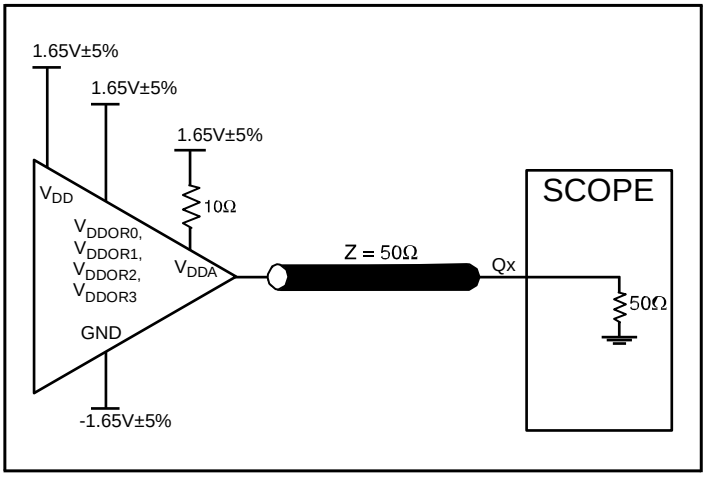
Parameter Measurement Information



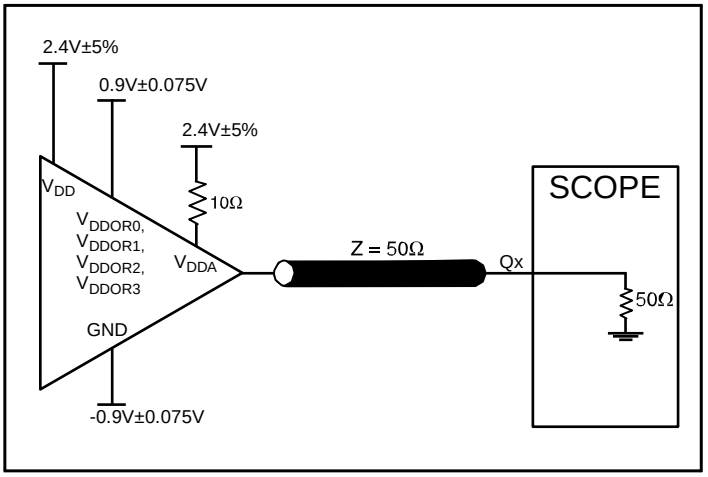
3.3V/2.5V LVDS Output Load AC Test Circuit



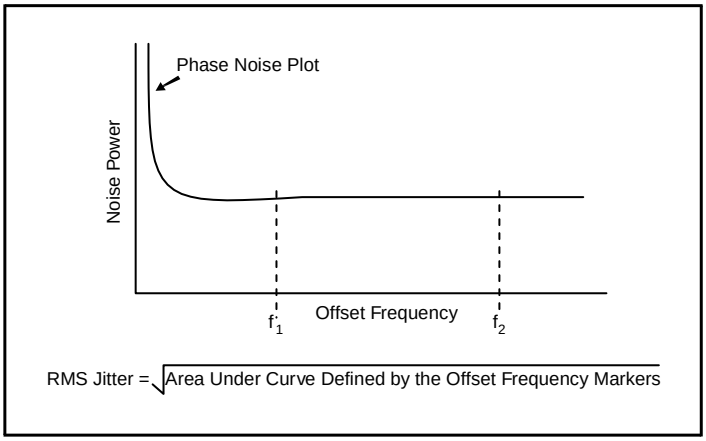
3.3V Core, 2.5V LVCMOS Output Load AC Test Circuit



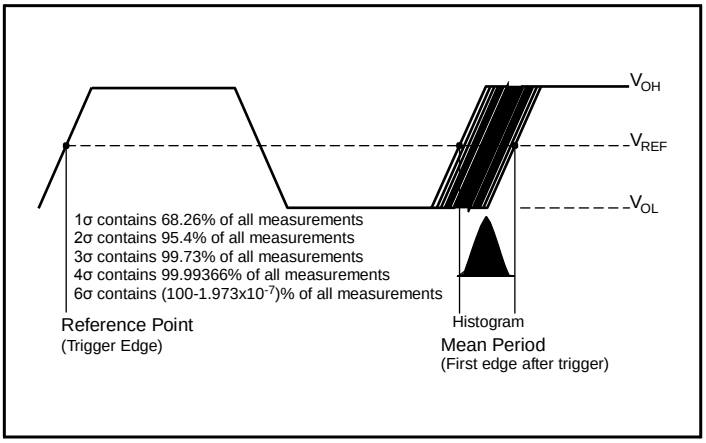
3.3V Core, 3.3V LVCMOS Output Load AC Test Circuit



3.3V Core, 1.8V LVCMOS Output Load AC Test Circuit

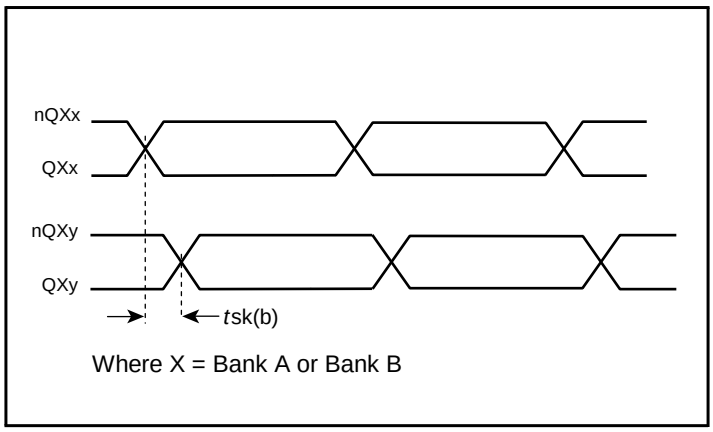


RMS Phase Jitter

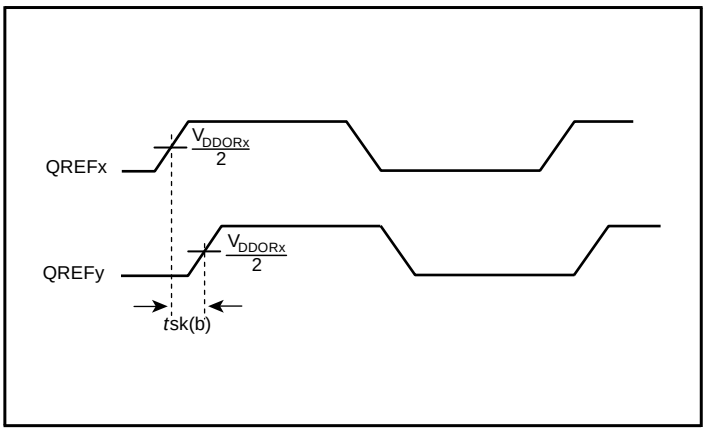


Period Jitter

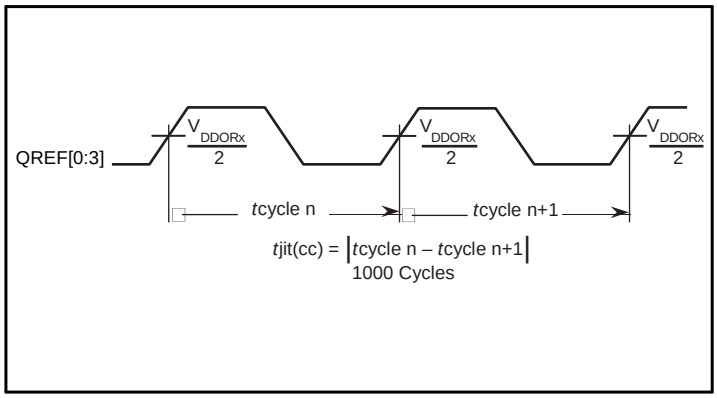
Parameter Measurement Information, continued



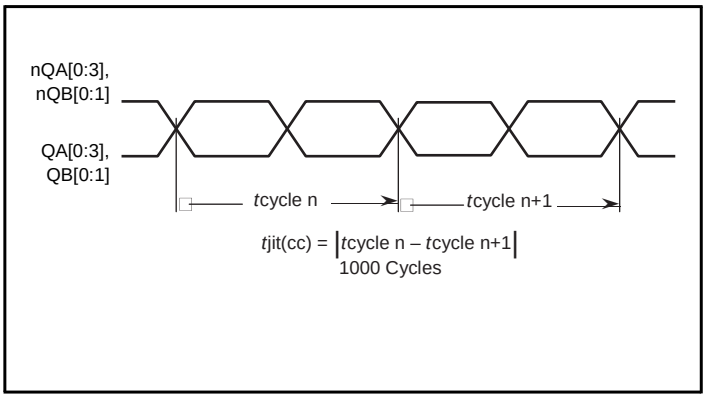
Differential Bank Skew



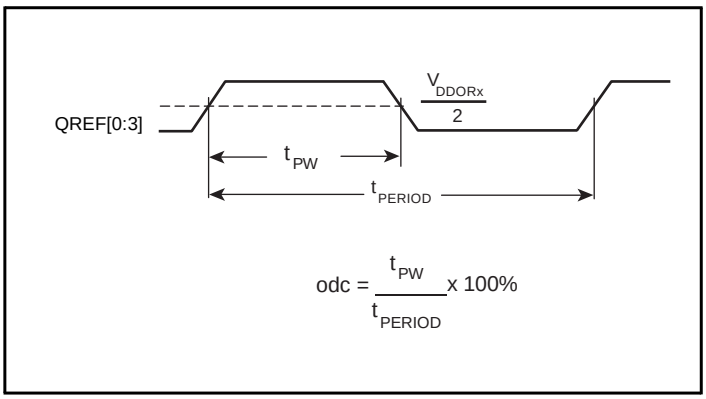
LVCMOS Bank Skew



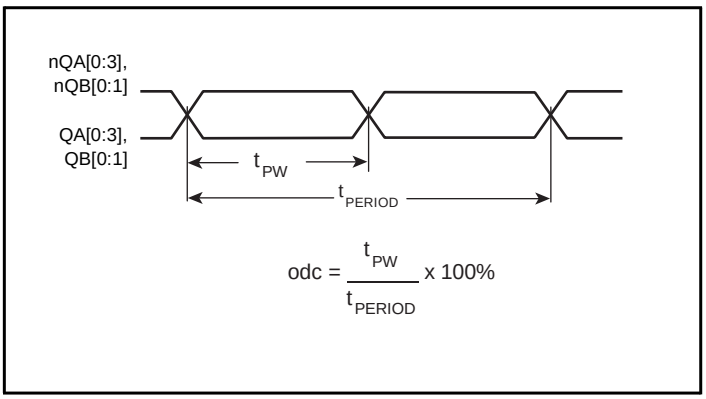
LVCMOS Cycle-to-Cycle Jitter



Differential Cycle-to-Cycle Jitter

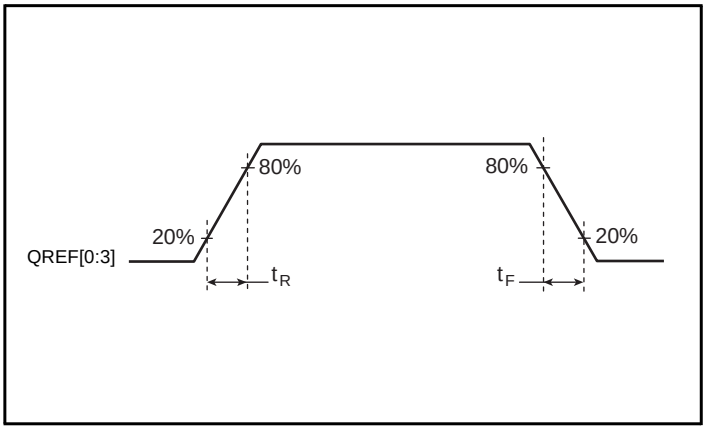


LVCMOS Output Duty Cycle/Pulse Width/Period

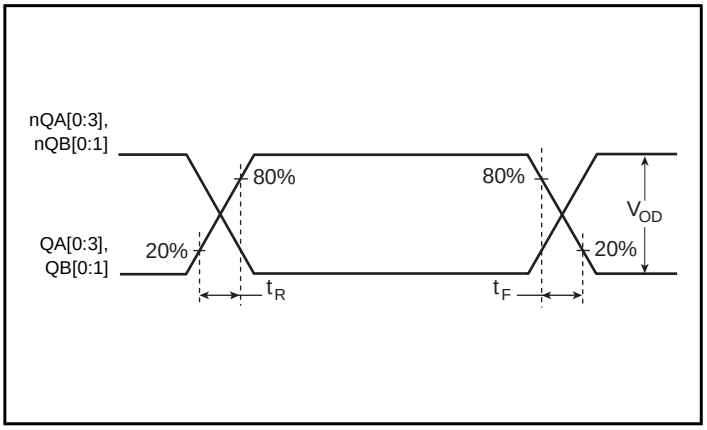


Differential Output Duty Cycle/Pulse Width/Period

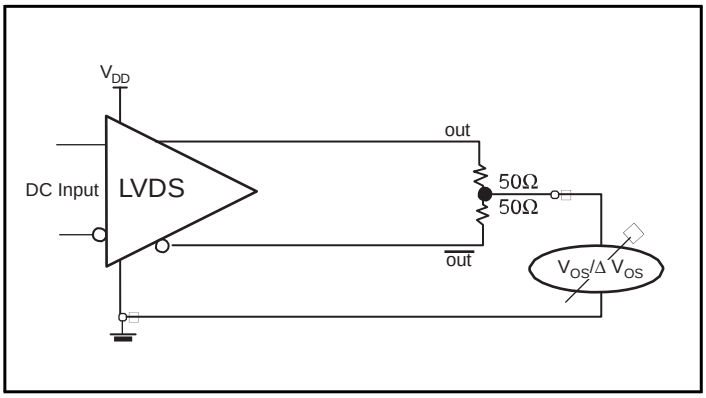
Parameter Measurement Information, continued



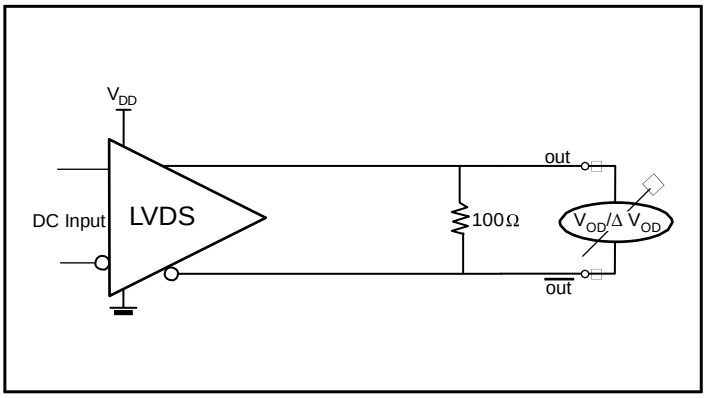
LVCMOS Rise/Fall Time



Differential Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

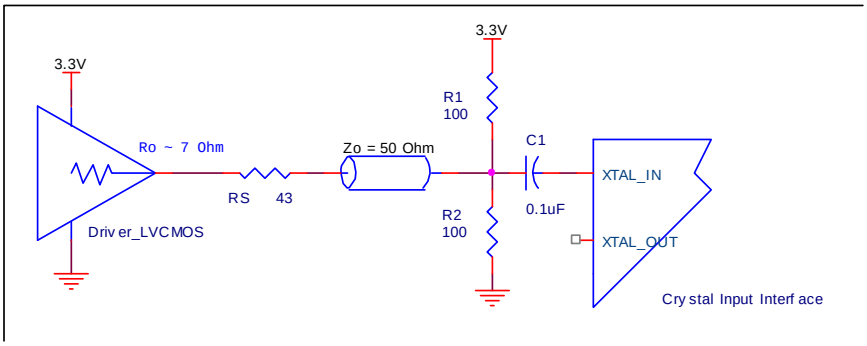


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

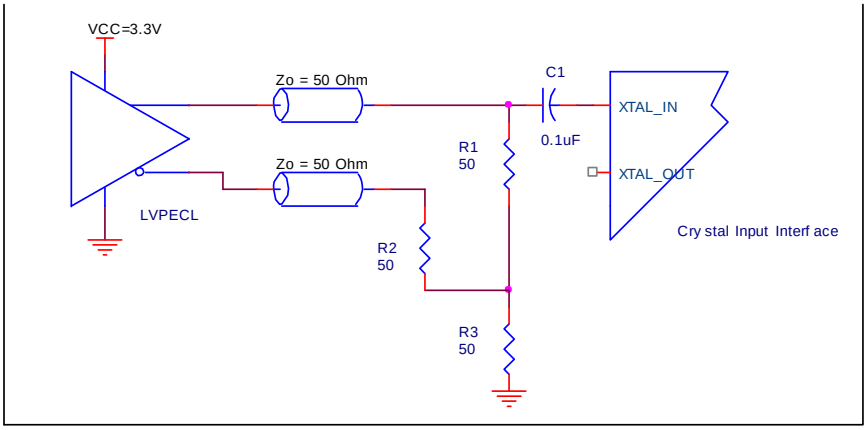


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

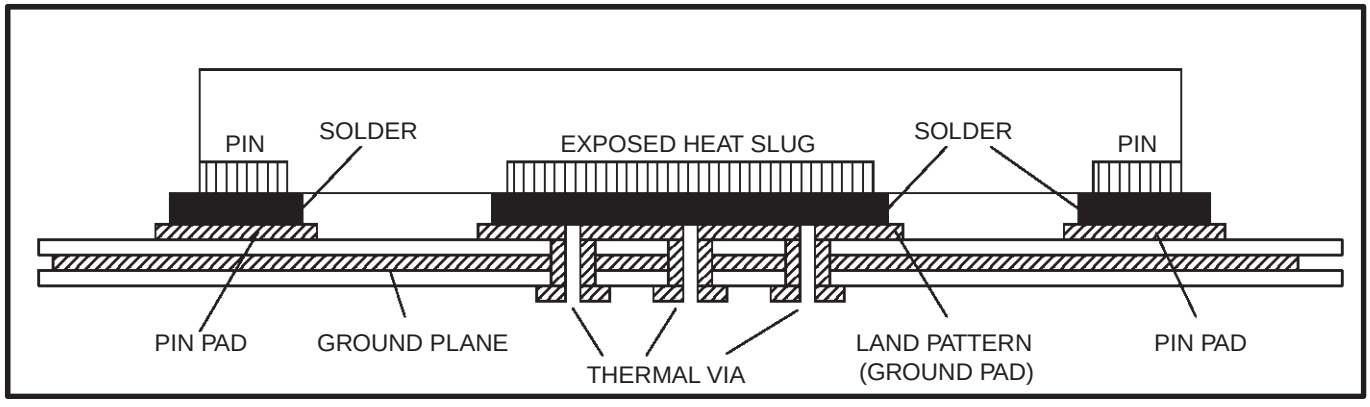


Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

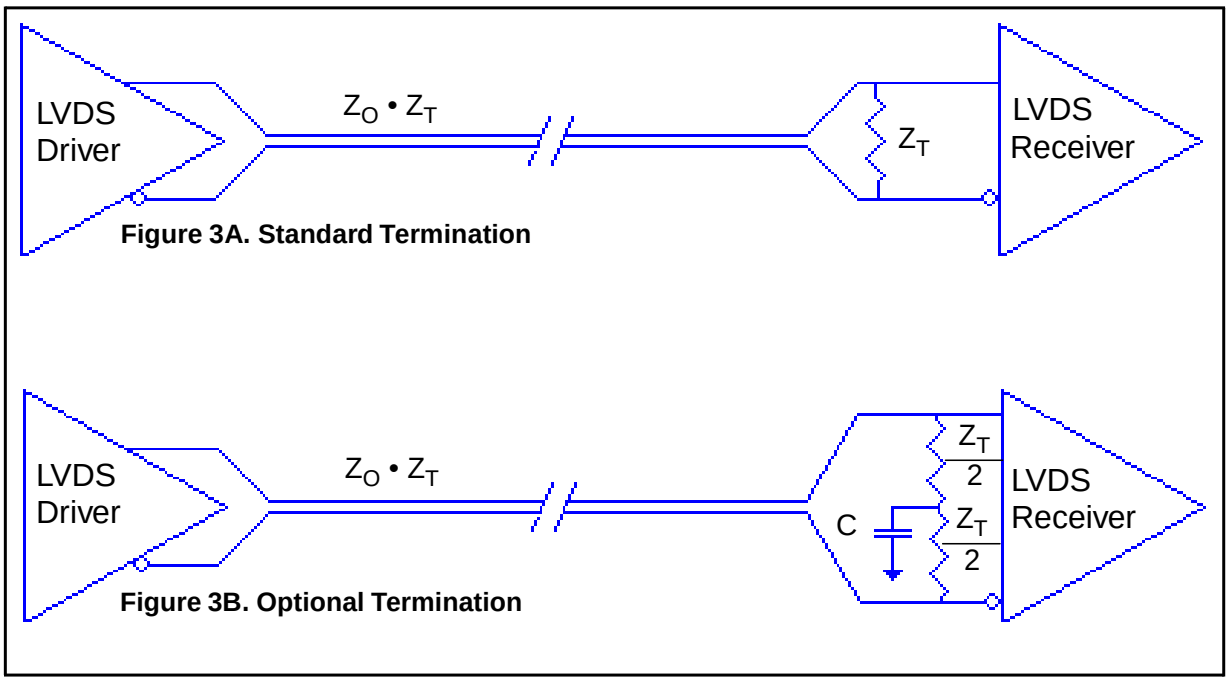


Figure 3A. Standard Termination

Figure 3B. Optional Termination

LVDS Termination

Schematic Layout

Figure 4 shows an example of ICS844S259I application schematic. In this example, the device is operated at V_{DD} = V_{DDORx} = V_{DDOA} = V_{CCOB} = 2.5V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 25pF and C2 = 27pF are recommended for frequency accuracy. Crystals with other load capacitance specifications can be used. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844S259I provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

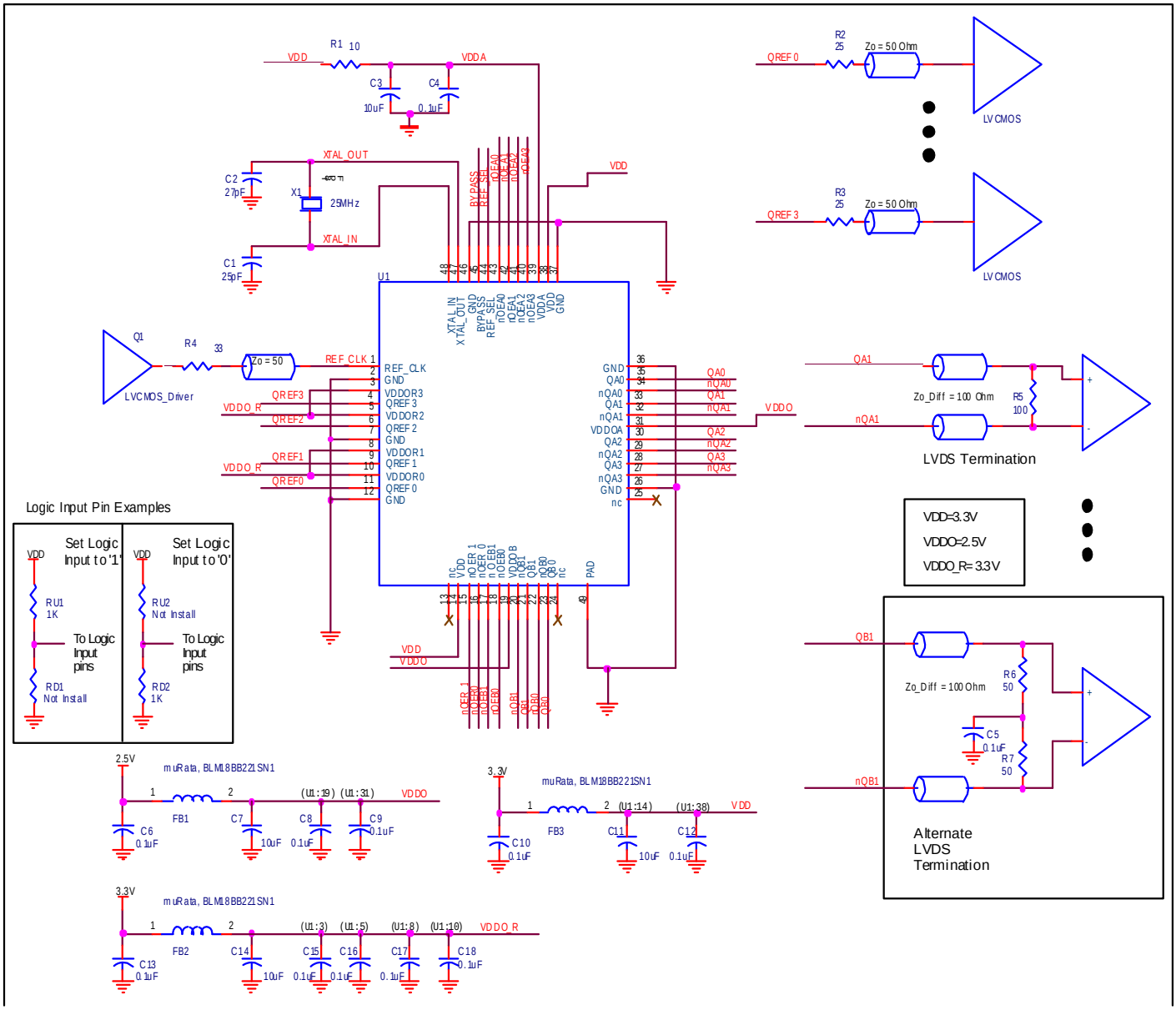


Figure 4. ICS844S259I Application Schematic

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844S259I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844S259I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, V_{DD_LVDS} = 2.5V + 5%, which gives worst case results.

The maximum current at 85°C is as follows:

I_{DD} = 89mA

I_{DD_LVDS} = 139mA

I_{DDA} = 15mA

NOTE: $V_{DD\_LVDS} = V_{DDOA} = V_{DDOB}$

$I_{DD\_LVDS} = I_{DDOA} + I_{DDOB}$

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = $(V_{DD} * I_{DD}) + (V_{DD\_LVDS} * I_{DD\_LVDS}) + (V_{DDA} * I_{DDA}) =$ (3.465V * 89mA) + (2.625V * 139mA) * (3.465V * 15mA)
  = 308.39mW + 364.88mW + 51.98mW = **725.25mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DDOR}/2$
  Output Current $I_{OUT} = V_{DDOR\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 25Ω)] = **23.1mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = $R_{OUT} * (I_{OUT})^2$ = 25Ω * $(23.1mA)^2$ = **13.34mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 13.34mW * 4 = **53.36mW**
- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * Frequency * $(V_{DDOR})^2$ = 7.5pF * 25MHz * $(3.465V)^2$ = **2.25mW per output**
  Total Power (25MHz) = **2.25mW * 4 = 9mW**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Total Power (R_{OUT}) + Total Power (25MHz)
  = 725.25mW + 53.36mW + 9mW
  = 787.61mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 29°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.788W * 29°C/W = 107.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48 Lead VFQFN, Forced Convection

θ_{JA} Vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.8°C/W	20.62°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 48-lead VFQFN

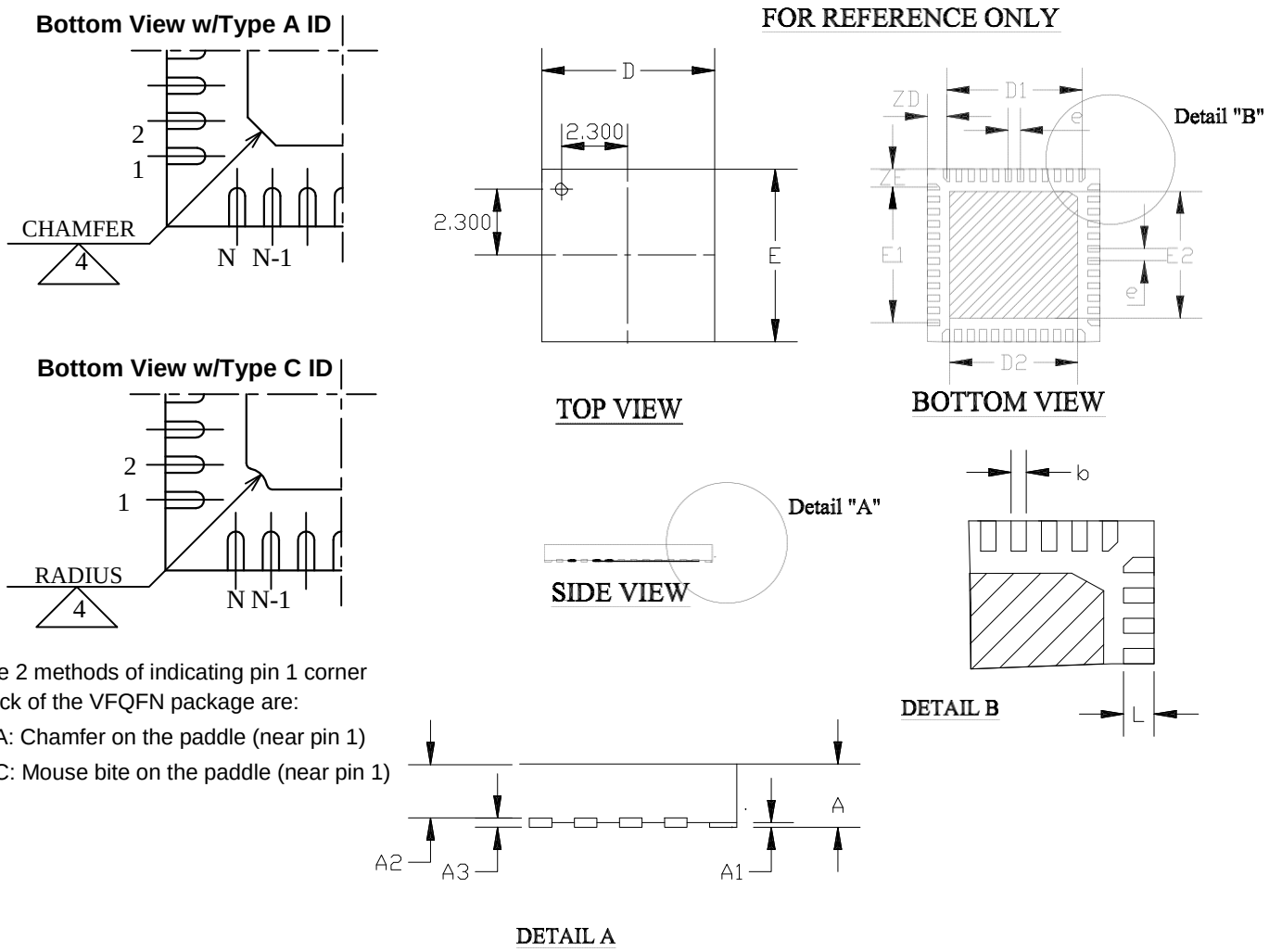
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.8°C/W	20.62°C/W

Transistor Count

The transistor count for ICS844S259I is: 9640

Package Outline and Package Dimensions

Package Outputline - K Suffix for 48 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions for 48 Lead VFQFN

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A		0.8	0.9
A1	0	0.02	0.05
A3		0.2 Ref.	
b	0.18	0.25	0.30
D & E		7.00 Basic	
D1 & E1		5.50 Basic	
D2 & E2	5.50	5.65	5.80
e		0.50 Basic	
R		0.20~0.25	
ZD & ZE		0.75 Basic	
L	0.35	0.40	0.45

Reference Document: IDT Drawing #PSC-4203

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844S259BKILF	ICS844S259BIL	Lead-Free, 48-lead VFQFN	Tray	-40°C to 85°C
844S259BKILFT	ICS844S259BIL	Lead-Free, 48-lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant

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