FEMTOCLOCK® NG CRYSTAL-TO-LVDS CLOCK SYNTHESIZER

ICS844N234I

PRELIMINARY DATA SHEET

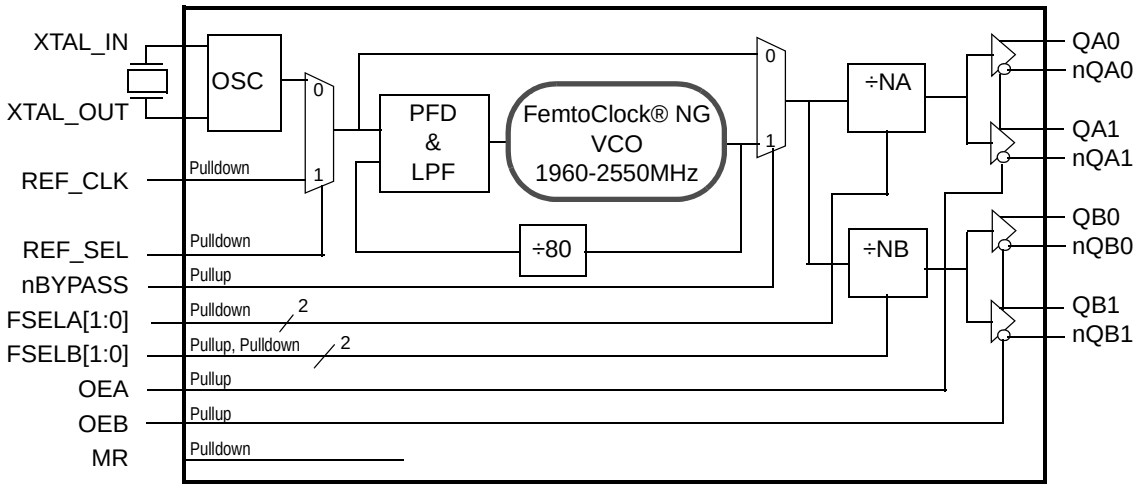
General Description

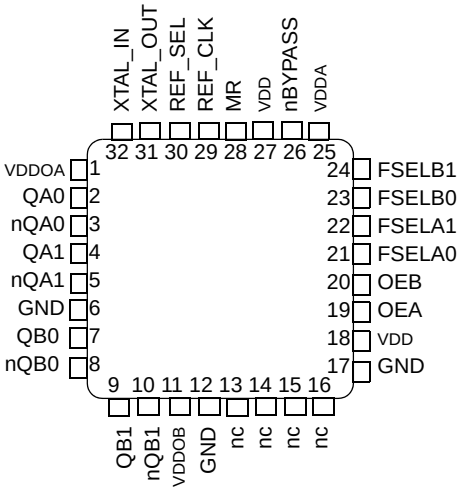
The ICS844N234I is a 4-output clock synthesizer designed for SRIO 1.3 and 2.0 reference clock applications. The device generates four copies of a selectable 100MHz, 312.5MHz, 156.25MHz or 125MHz clock signals with excellent phase jitter performance. The four outputs are organized in two banks of two LVDS ouputs.The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with low power consumption and high power supply noise rejection. The synthesized clock frequency and the phase-noise performance are optimized for driving SRIO 1.3 and 2.0 SerDes reference clocks. The device supports 3.3V and 2.5V voltage supplies and is packaged in a small, lead-free (RoHS 6) 32-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

Features

- 4TH generation FemtoClock® NG technology
- Selectable 100MHz, 312.5MHz, 156.25MHz or 125MHz output clock synthesized from a 31.25MHz fundamental mode crystal
- Four differential LVDS clock outputs
- Selectable 31.25MHz crystal interface or external reference clock
- RMS phase jitter @ 156.25MHz, using a 31.25MHz crystal (1MHz - 20MHz): 0.15ps (typical)
- RMS phase jitter @ 156.25MHz, using a 31.25MHz crystal (12kHz - 20MHz): 0.26ps (typical)
- LVCMOS interface levels for the frequency select input
- Full 3.3V or 2.5V supply voltage
- Lead-free (RoHS 6) 32-lead VFQFN package
- -40°C to 85°C ambient operating temperature

Block Diagram





Pin Assignment

ICS844N234I
32-lead VFQFN
5.0mm x 5.0mm x 0.925mm, package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice..

Pin Description and Characteristics

Table 1: Pin Descriptions

Number	Name	Type		Description
1	V_{DDOA}	Power		Output supply pin for Bank A outputs.
2, 3	QA0, nQA0	Output		Differential clock output. LVDS interface levels.
4, 5	QA1, nQA1	Output		Differential clock output. LVDS interface levels.
6, 12, 17	GND	Power		Power supply ground.
7, 8	QB0, nQB0	Output		Differential clock output. LVDS interface levels.
9, 10	QB1, nQB1	Output		Differential clock output. LVDS interface levels.
11	V_{DDOB}	Power		Output supply pin for Bank B outputs.
13, 14, 15, 16	nc	Unused		No connect.
18, 27	V_{DD}	Power		Core supply pins.
19	OEA	Input	Pullup	Output enable input. See Table 3E: for function. LVCMOS/LVTTL interface levels.
20	OEB	Input	Pullup	Output enable input. See Table 3F: for function. LVCMOS/LVTTL interface levels.
21, 22	FSELA0, FSELA1	Input	Pulldown	Frequency select pins. See Table 3A: for function. LVCMOS/LVTTL interface levels.
23	FSELB0,	Input	Pulldown	Frequency select pin. See Table 3B: for function. LVCMOS/LVTTL interface levels.
24	FSELB1	Input	Pullup	Frequency select pin. See Table 3B: for function. LVCMOS/LVTTL interface levels.
25	V_{DDA}	Power		Analog power supply.
26	nBYPASS	Input	Pullup	Bypass mode select pin. See Table 3D: for function. LVCMOS/LVTTL interface levels.
28	MR	Input	Pulldown	Master reset. See Table 3G: for function. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Alternative single-ended reference clock input. LVCMOS/LVTTL interface levels.
30	REF_SEL	Input	Pulldown	Reference select input. See Table 3C: for function. LVCMOS/LVTTL interface levels.
31, 32	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pulldown and Pullup* refer to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2: Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A: FSELA Output Frequency Selection

Input		Divider	Output Frequency with f_{XTAL} = 31.25MHz
FSELA1	FSELA0	NA	
0 (default)	0 (default)	25	100MHz
0	1	8	312.5MHz
1	0	16	156.25MHz
1	1	20	125MHz

NOTE: FSELA[1:0] are asynchronous controls.

Table 3B: FSELB Output Frequency Selection

Input		Divider	Output Frequency with f_{XTAL} = 31.25MHz
FSELB1	FSELB0	NB	
0	0	25	100MHz
0	1	8	312.5MHz
1 (default)	0 (default)	16	156.25MHz
1	1	20	125MHz

NOTE: FSELB[1:0] are asynchronous controls.

Table 3C: PLL Reference Clock Select Function Table

Input	
REF_SEL	Operation
0 (default)	The crystal interface is selected as reference clock
1	The REF_CLK input is selected as reference clock

NOTE: REF_SEL is an asynchronous control.

Table 3D: PLL BYPASS Function Table

Input	
nBYPASS	Operation
0	PLL is bypassed. The reference frequency f_{REF} is divided by the selected output dividers NA and NB. AC specifications do not apply in PLL bypass mode.
1 (default)	PLL is enabled. The reference frequency f_{REF} is multiplied by the PLL feedback divider of 80 and then divided by the selected output dividers NA and NB.

NOTE: nBYPASS is an asynchronous control.

Table 3E: OEA Output Enable Function Table

Input	
OEA	Operation
0	QA0, nQA0 and QA1, nQA1 outputs are disabled (high-impedance)
1 (default)	QA0, nQA0 and QA1, nQA1 outputs are enabled

NOTE: OEA is an asynchronous control.

Table 3F: OEB Output Enable Function Table

Input	
OEB	Operation
0	QB0, nQB0 and QB1, nQB1 outputs are disabled (high-impedance)
1 (default)	QB0, nQB0 and QB1, nQB1 outputs are enabled

NOTE: OEB is an asynchronous control.

Table 3G: MR Master Reset Function Table

Input	
MR	Operation
0 (default)	Internal dividers are enabled
1	Internal dividers are reset and outputs are in logic low state (Qx = L, nQx = H)

NOTE: MR is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V 0.5V to V_{DD}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A: Power Supply DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3V	3.465	V
			2.375	2.5V	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.30	3.3V	V_{DD}	V
			V_{DD} – 0.30	2.5V	V_{DD}	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		3.135	3.3V	3.465	V
			2.375	2.5V	2.625	V
I_{DD}	Power Supply Current			130		mA
I_{DDA}	Analog Supply Current			30		mA
I_{DDOA} + I_{DDOB}	Output Supply Current			110		mA

Table 4B: LVCMOS/LVTTL Input DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, REF_SEL, FSELA[1:0], FSELB0	V_{DD} = V_{IN} = 2.625V or 3.465V			150	µA
		OEA, OEB, FSELB1, nBYPASS	V_{DD} = V_{IN} = 2.625V or 3.465V			5	µA
I_{IL}	Input High Current	REF_CLK, MR, REF_SEL, FSELA[1:0], FSELB0	V_{DD} = 2.625V or 3.465V, V_{IN} = 0V	-5			µA
		OEA, OEB, FSELB1, nBYPASS	V_{DD} = 2.625V or 3.465V, V_{IN} = 0V	-150			µA

Table 4C: LVDS DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			335		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.28		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 4D: LVDS DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			330		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.27		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5: Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.6	31.25	31.875	MHz
Equivalent Series Resistance (ESR)				80	Ω
Shunt Capacitance				7	pF

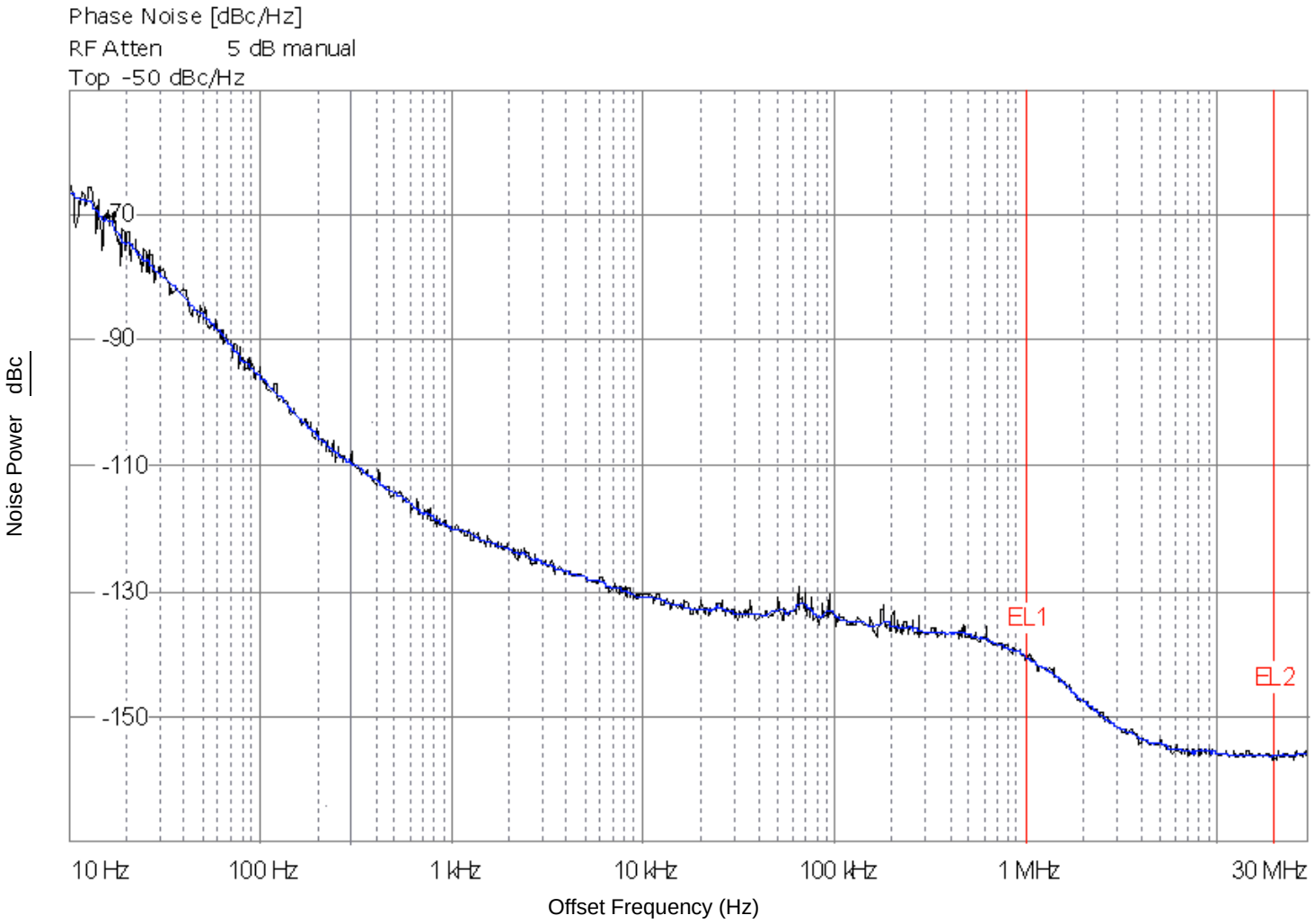
NOTE: Characterized using an 12pF parallel resonant crystal.

Table 6: AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = -40°C$ to $85°C$

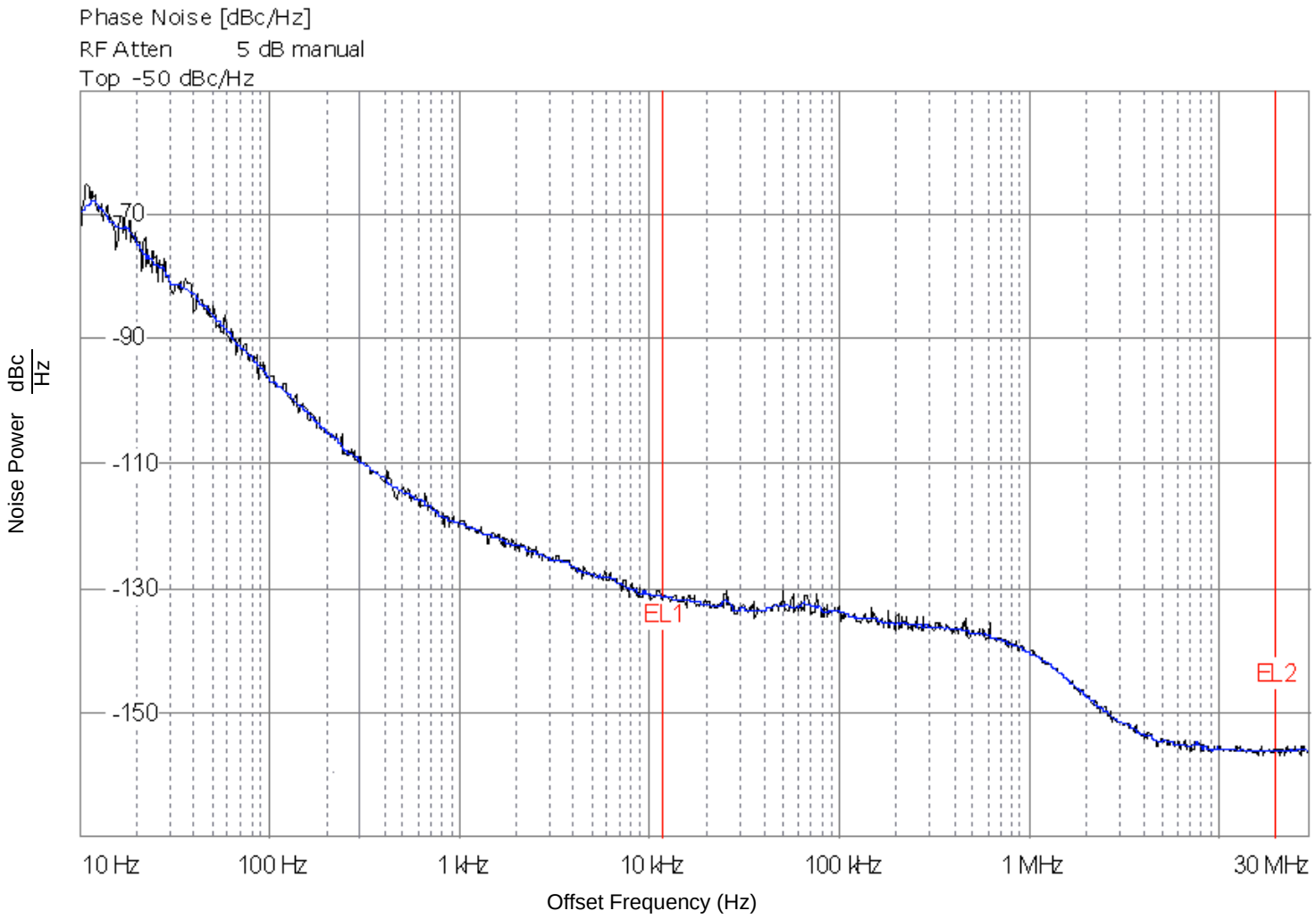
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		FSELx[1:0] = 00		100		MHz
			FSELx[1:0] = 01		312.5		MHz
			FSELx[1:0] = 10		156.25		MHz
			FSELx[1:0] = 11		125		MHz
f_{REF}	Reference Frequency		REF_CLK	19.6	31.25	31.875	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1		156.25MHz, Integration Range: 1MHz – 20MHz		0.15		ps
			156.25MHz, Integration Range: 12kHz – 20MHz		0.26		ps
Φ_N	Single-Side Band Noise Power		156.25MHz, Offset: 100Hz		-95		dBc/Hz
			156.25MHz, Offset: 1kHz		-120		dBc/Hz
			156.25MHz, Offset: 10kHz		-130		dBc/Hz
			156.25MHz, Offset: 100kHz		-134		dBc/Hz
tsk(o)	Output Skew; NOTE 2, 3, 4				45		ps
tsk(b)	Bank Skew; NOTE 2, 4, 5				5		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		290		ps
t_{LOCK}	PLL Lock Time				5		ms
odc	Output Duty Cycle	QB[0:1], nQB[0:1]			50		%
		QA[0:1], nQA[0:1]			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to the phase noise plots.
NOTE 2: f_{REF} = 31.25MHz.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

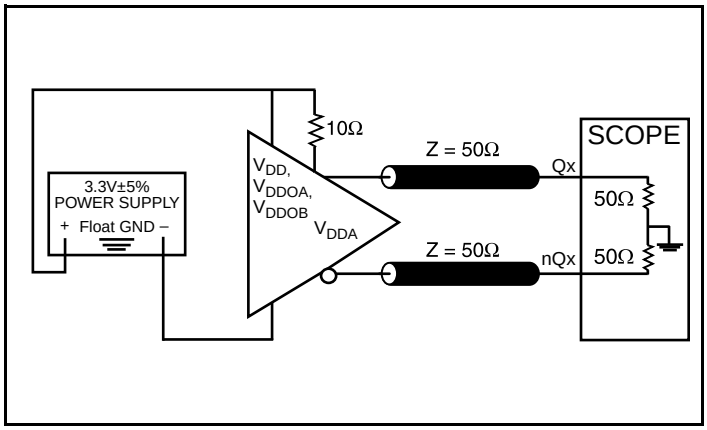
Typical Phase Noise at 156.25MHz (1MHz - 20MHz)



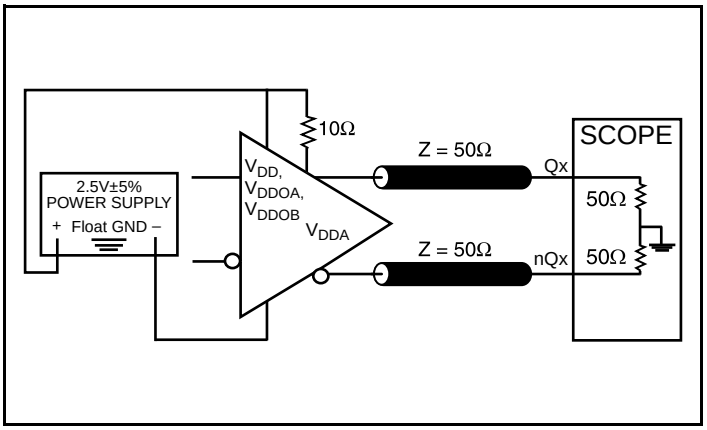
Typical Phase Noise at 156.25MHz (12MHz - 20MHz)



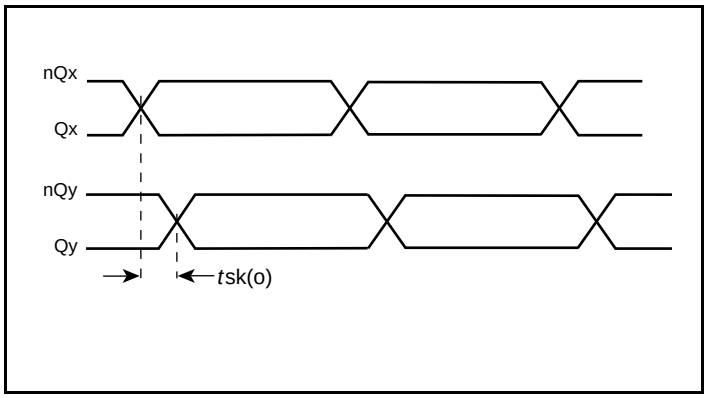
Parameter Measurement Information



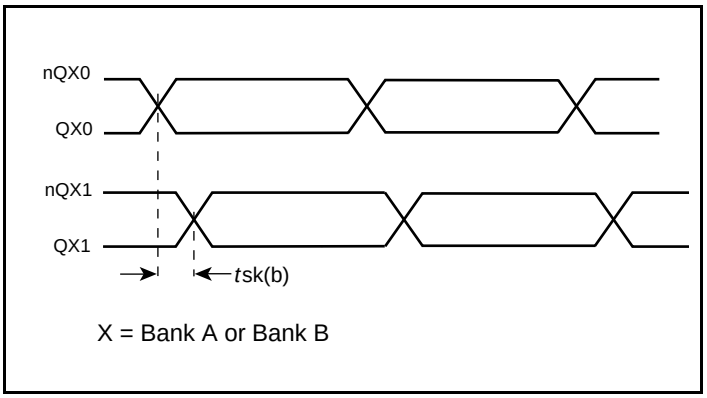
3.3V LVDS Output Load AC Test Circuit



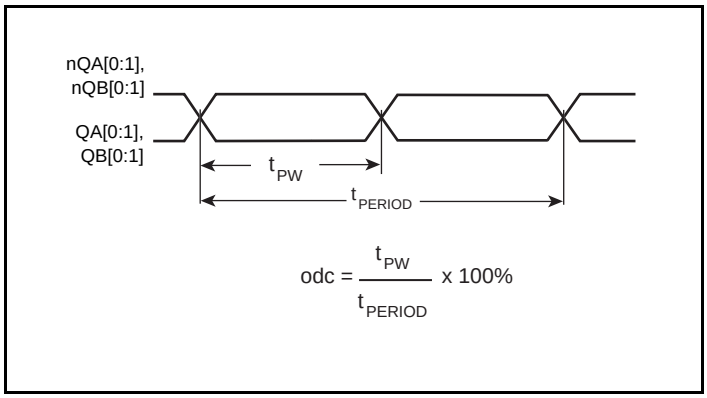
2.5V LVDS Output Load AC Test Circuit



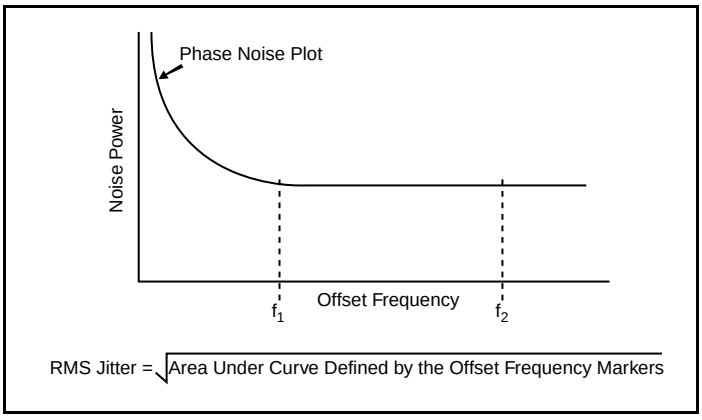
Output Skew



Bank Skew

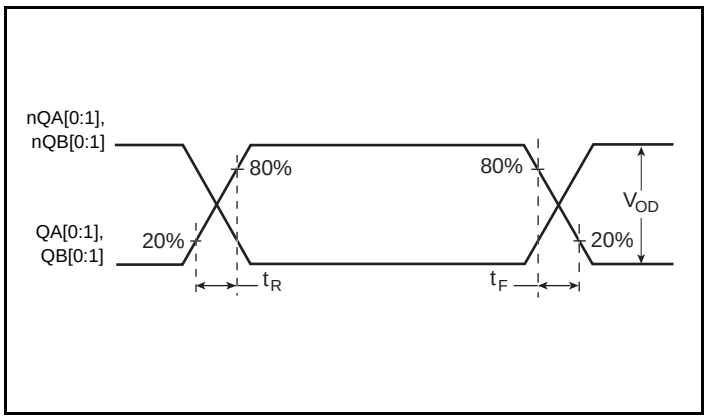


Output Duty Cycle/Pulse Width/Period

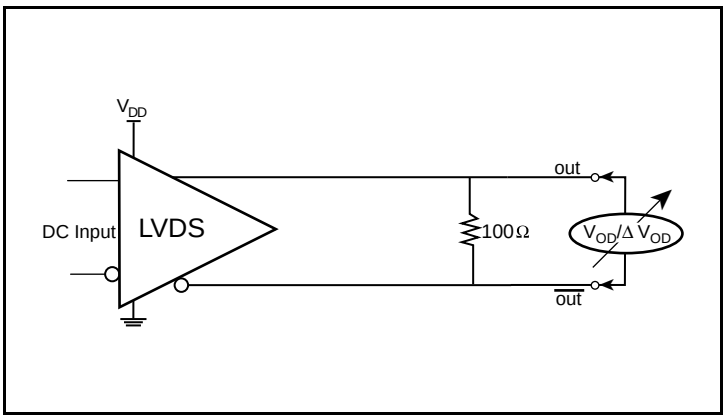


RMS Phase Jitter

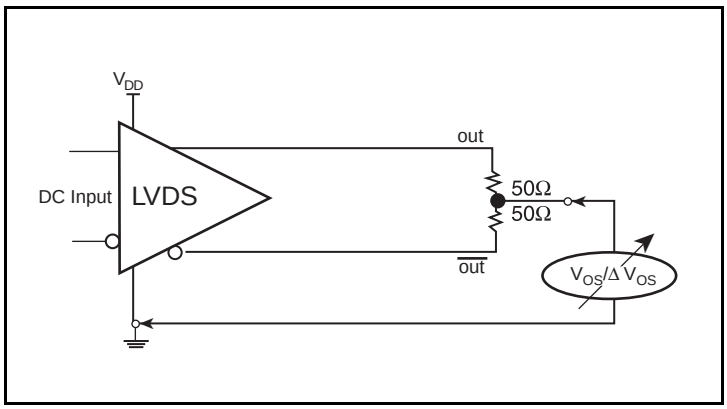
Parameter Measurement Information, continued



Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Interface to IDT SRIO Switches

The ICS844N234I is designed for driving the differential reference clock input (REF_CLK) of IDT's SRIO 1.3 and 2.0 switch devices. The LVDS outputs of the ICS844N234I have the low-jitter, differential voltage and impedance characteristics required to provide a high-quality 156.25MHz clock signal for both SRIO 1.3 and 2.0 switch devices. Please refer to *Figure 1* for suggested interfaces. In Figure 1, the AC-coupling capacitors are mandatory by the IDT SRIO switch devices. The differential REF_CLK_P/N input is internally re-biased and AC-terminated. Both interface circuits are optimized for 50Ω transmission lines and generate the voltage swing required to reliably drive the clock reference input of a IDT SRIO switch. Please refer to IDT's SRIO device datasheet for more details.

Figure 1 shows the recommended interface circuit for driving the 156.25MHz reference clock of an IDT SRIO 2.0 switch by a LVDS output (QA0, QA1, QB0 or QB1) of the ICS844N234I. The LVDS-to-differential interface as shown in Figure 1 does not require any external termination resistors: the ICS844N234I driver contains an internal source termination at all outputs. The differential REF_CLK input contains an internal AC-termination (R_L) and re-bias (V_{BIAS}). Use the LVDS Driver Termination (figure 5A and 5B) if the receiving device does not implement and internal termination.

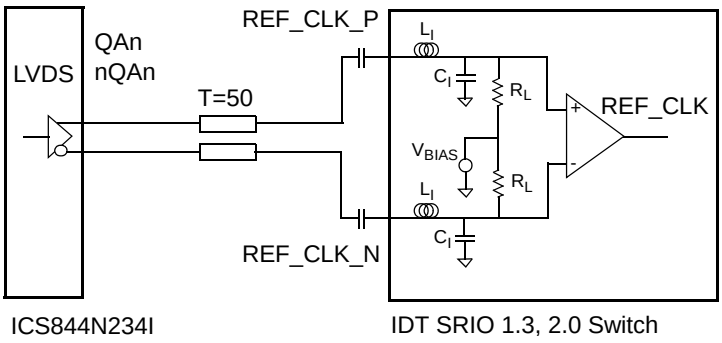


Figure 1. LVDS-to-SRIO 2.0 Reference Clock Interface

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844N234I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDOA} and V_{DDOB} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

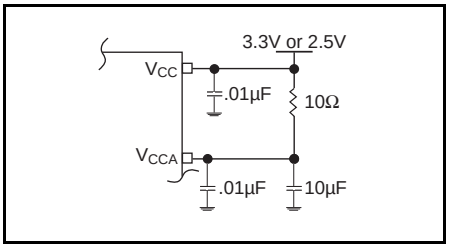


Figure 2. Power Supply Filtering

Crystal Input Interface

The ICS844N234I has been characterized with 12pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 31.25MHz, 12pF parallel resonant crystal and were chosen to minimize the ppm error.

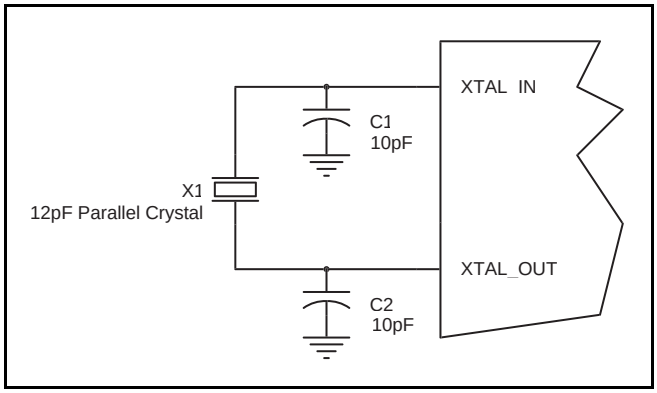


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 4A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 4B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

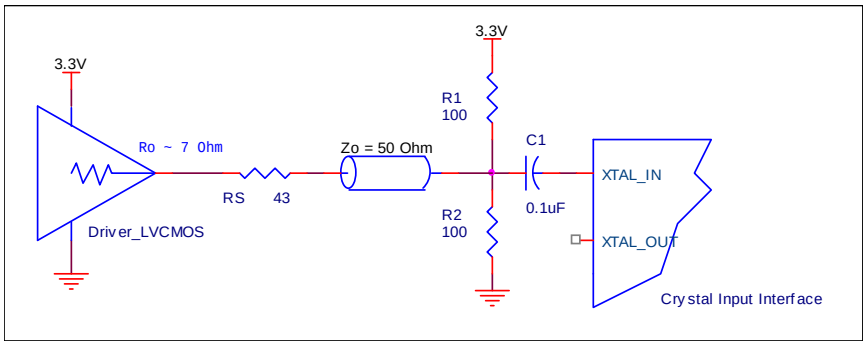


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

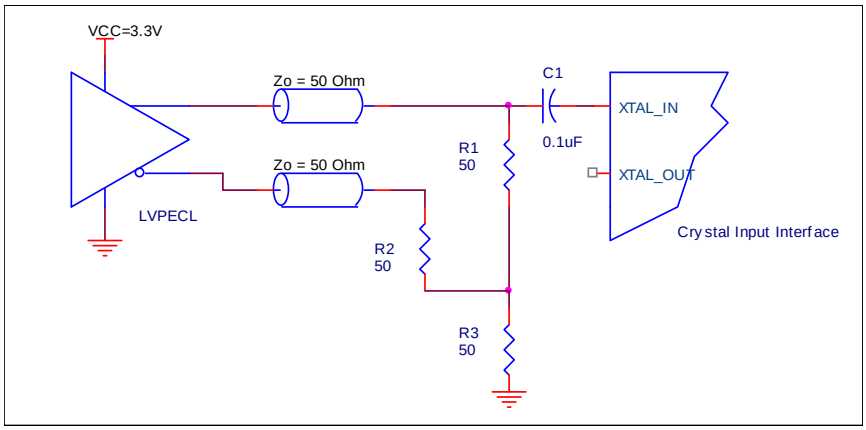


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of a reference clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

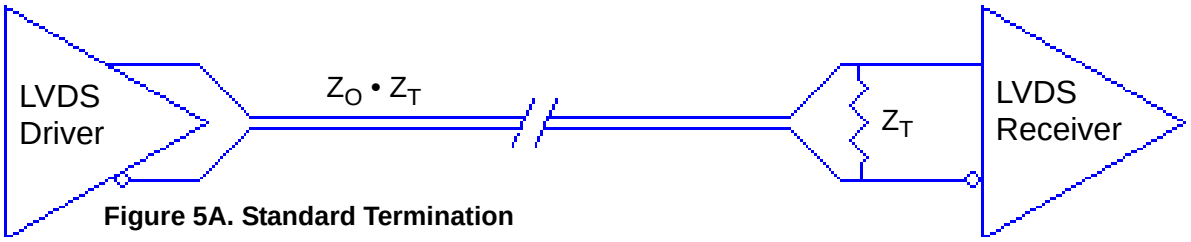


Figure 5A. Standard Termination

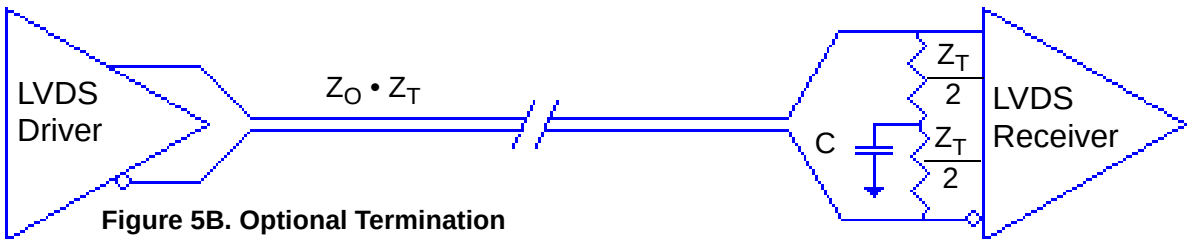


Figure 5B. Optional Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

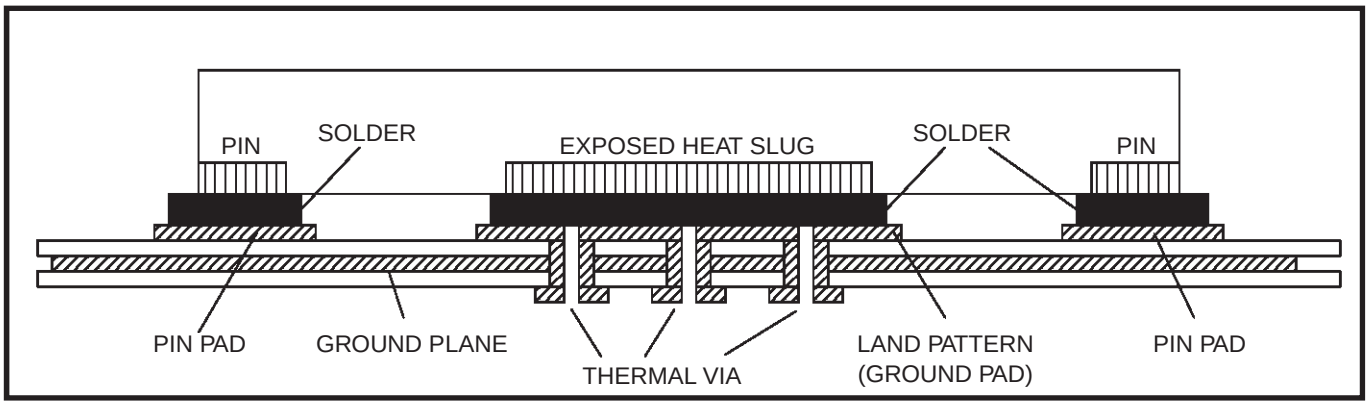


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844N234I for all outputs that are configured to LVDS (LEV_SEL = 0). Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844N234I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 159mA
I_{DDA_MAX} = 34mA
I_{DDO_MAX} = 134mA

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (159mA + 34mA) = **668.745mW**
- Power (output)$_{MAX}$ = V_{DDO_MAX} * (I_{DDOA} + I_{DDOB}) = 3.465V *134mA = **464.31mW**

Total Power$_{\_MAX}$ = 668.745mW + 464.31mW = **1133.055mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.133W * 33.1°C/W = 122.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 56 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 lead VFQFN

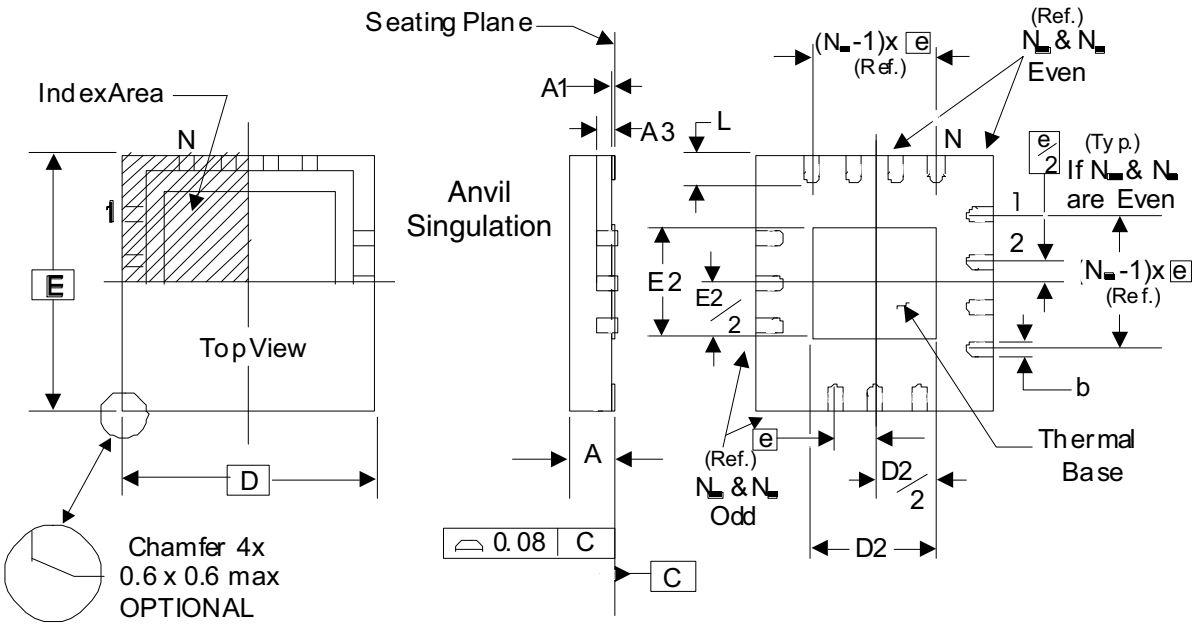
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Transistor Count

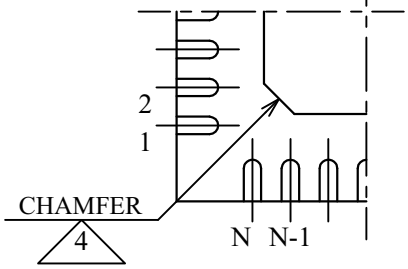
The transistor count for ICS844N234I is: 22,700

Package Outline and Package Dimensions

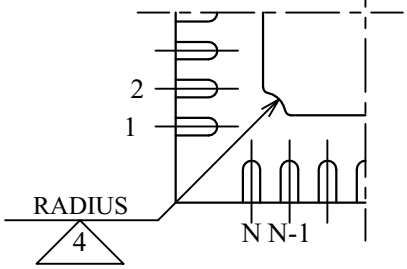
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844N234AKILF	ICS4N234AIL	Lead-Free, 32 Lead VFQFN	Tray	-40°C to 85°C
844N234AKILFT	ICS4N234AIL	Lead-Free, 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant

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