General Description

The ICS844625I is a high frequency clock generator. The ICS844625I uses an external 25MHz crystal to synthesize 312.5MHz, 156.25MHz and 125MHz clocks. The ICS844625I has excellent cycle-to-cycle and RMS period jitter performance.

The ICS844625I operates at full 3.3V, 2.5V or mixed 3.3V, 2.5V supply modes and is available in a fully RoHS compliant 48-lead TQFP, E-Pad package.

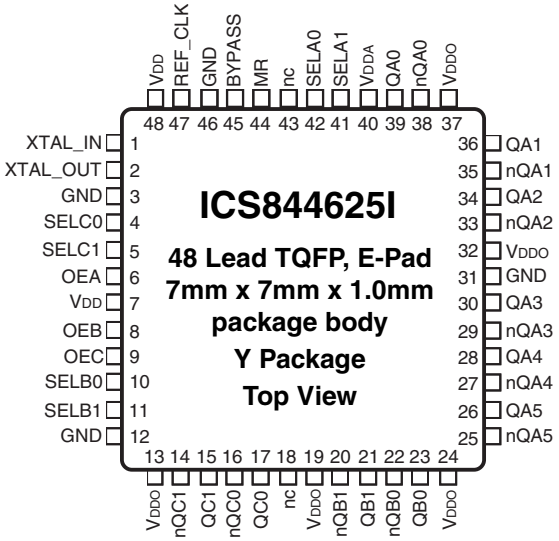
Features

- Ten selectable differential LVDS outputs
- Output frequencies of 312.5MHz, 156.25MHz or 125MHz using a 25MHz crystal.
- Crystal oscillator interface designed for 18pF, 25MHz parallel resonant crystal
- Cycle-to-cycle jitter: 13ps (typical)
- RMS phase jitter at 125MHz (1.875MHz - 20MHz): 0.417ps (typical), V_{DD} = 3.3V
- RMS phase jitter at 156.25MHz (1.875MHz - 20MHz): 0.387ps (typical), V_{DD} = 3.3V
- Output duty cycle: 50%, (typical)
- Supply modes:
  V_{DD} / V_{DDA} / V_{DDO}
  3.3V / 3.3V / 3.3V
  2.5V / 2.5V / 2.5V
  3.3V / 3.3V / 2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Frequency Table for Bank A, B and C Outputs

Crystal Frequency (MHz)	Feedback Divider	VCO Frequency (MHz)	Output Divider	Output Frequency (MHz)
25	25	625	÷2	312.5
25	25	625	÷4	156.25
25	25	625	÷5	125

Pin Assignment



Block Diagram

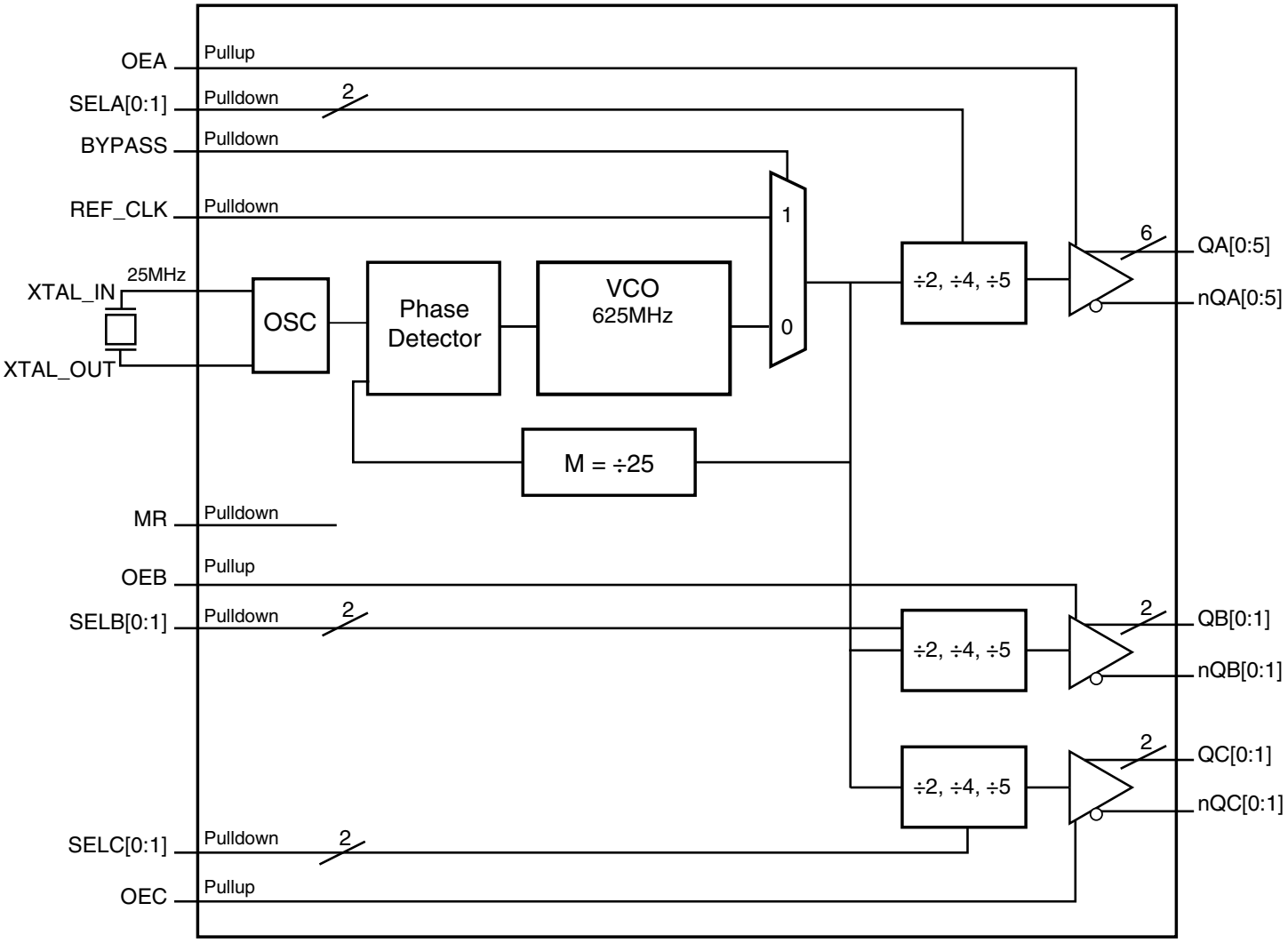


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
3, 12, 31, 46	GND	Power		Power supply pins.
4, 5	SELC0, SELC1	Input	Pulldown	Selects the output divider value. See Table 3C. LVCMOS/LVTTL interface levels.
6	OEA	Input	Pullup	Active high output enable. When logic HIGH, Bank A outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.
7, 48	V_{DD}	Power		Core supply pins.
8	OEB	Input	Pullup	Active high output enable. When logic HIGH, Bank B outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.
9	OEC	Input	Pullup	Active high output enable. When logic HIGH, Bank C outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.
10, 11	SELB0, SELB1	Input	Pulldown	Selects the output divider value. See Table 3B. LVCMOS/LVTTL interface levels.
13, 19, 24, 32, 37	V_{DDO}	Power		Output supply pins.
14, 15	nQC1, QC1	Output		Differential output pair. LVDS interface levels.
16, 17	nQC0, QC0	Output		Differential output pair. LVDS interface levels.
18, 43	nc	Unused		No connect.
20, 21	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
22, 23	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
25, 26	nQA5, QA5	Output		Differential output pair. LVDS interface levels.
27, 28	nQA4, QA4	Output		Differential output pair. LVDS interface levels.
29, 30	nQA3, QA3	Output		Differential output pair. LVDS interface levels.
33, 34	nQA2, QA2	Output		Differential output pair. LVDS interface levels.
35, 36	nQA1, QA1	Output		Differential output pair. LVDS interface levels.
38, 39	nQA0, QA0	Output		Differential output pair. LVDS interface levels.
40	V_{DDA}	Power		Analog supply pin.
41, 42	SELA1, SELA0	Input	Pulldown	Selects the output divider value. See Table 3A. LVCMOS/LVTTL interface levels.
44	MR	Input	Pulldown	Master Reset. LVCMOS/LVTTL interface levels.
45	BYPASS	Input	Pulldown	BYPASS signal allows to bypass the PLL. LVCMOS/LVTTL interface levels.
47	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. SELA Function Table

Input		
SELA0	SELA1	Bank A Output Divider
0	0	N/A
0	1	÷2
1	0	÷4
1	1	÷5

Table 3B. SELB Function Table

Input		
SELB0	SELB1	Bank B Output Divider
0	0	N/A
0	1	÷2
1	0	÷4
1	1	÷5

Table 3C. SELC Function Table

Input		
SELC0	SELC1	Bank C Output Divider
0	0	N/A
0	1	÷2
1	0	÷4
1	1	÷5

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, LVDS I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	29°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.31	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			101	125	mA
I_{DDA}	Analog Supply Current			25	31	mA
I_{DDO}	Output Supply Current			113	140	mA

Table 4B. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.21	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			96	120	mA
I_{DDA}	Analog Supply Current			17	21	mA
I_{DDO}	Output Supply Current			95	128	mA

Table 4C. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.31	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			100	125	mA
I_{DDA}	Analog Supply Current			25	31	mA
I_{DDO}	Output Supply Current			112.5	140	mA

Table 4D. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, BYPASS, SELA[1:0], SELB[1:0], SELC[1:0]	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		OEA, OEB, OEC	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, BYPASS, SELA[1:0], SELB[1:0], SELC[1:0]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OEA, OEB, OEC	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 4E. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		248	380	480	V
ΔV_{OD}	V_{OD} Magnitude Change				50	V
V_{OS}	Offset Voltage		1.30	1.43	1.52	V
ΔV_{OS}	V_{OS} Magnitude Change				50	V

Table 4F. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		205	329	420	V
ΔV_{OD}	V_{OD} Magnitude Change				50	V
V_{OS}	Offset Voltage		1.00	1.15	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	V

Table 4G. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		248	380	480	V
ΔV_{OD}	V_{OD} Magnitude Change				50	V
V_{OS}	Offset Voltage		1.30	1.43	1.52	V
ΔV_{OS}	V_{OS} Magnitude Change				50	V

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. LVDS AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Qx = ÷2		312.5		MHz
		Qx = ÷4		156.25		MHz
		Qx = ÷5		125		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); QAx = QBx = QCx	125MHz, (1.875MHz – 20MHz)		0.417	0.484	ps
		156.25MHz, (1.875MHz – 20MHz)		0.387	0.429	ps
		156.25MHz, (1MHz – 20MHz)		0.509	0.570	ps
		312.5MHz, (1.875MHz – 20MHz)		0.335	0.410	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			13	50	ps
t_R / t_F	Output Rise/Fall Time	f_{OUT} = 312.5MHz, 20% to 80%	350	600	1200	ps
		f_{OUT} = 125MHz, 156.25MHz, 20% to 80%	400	700	1200	ps
odc	Output Duty Cycle	f_{OUT} = 312.5MHz	35	48	60	%
		f_{OUT} = 125MHz, 156.25MHz	45	50	55	%
t_{LOCK}	PLL Lock Time				100	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

Table 6B. LVDS AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Qx = ÷2		312.5		MHz
		Qx = ÷4		156.25		MHz
		Qx = ÷5		125		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); QAx = QBx = QCx	125MHz, (1.875MHz – 20MHz)		0.498	0.633	ps
		156.25MHz, (1.875MHz – 20MHz)		0.454	0.552	ps
		156.25MHz, (1MHz – 20MHz)		0.646	0.768	ps
		312.5MHz, (1.875MHz – 20MHz)		0.350	0.429	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			13	50	ps
t_R / t_F	Output Rise/Fall Time	f_{OUT} = 312.5MHz, 20% to 80%	350	600	1200	ps
		f_{OUT} = 125MHz, 156.25MHz, 20% to 80%	400	700	1200	ps
odc	Output Duty Cycle	f_{OUT} = 312.5MHz	35	48	60	%
		f_{OUT} = 125MHz, 156.25MHz	45	50	55	%
t_{LOCK}	PLL Lock Time				100	ms

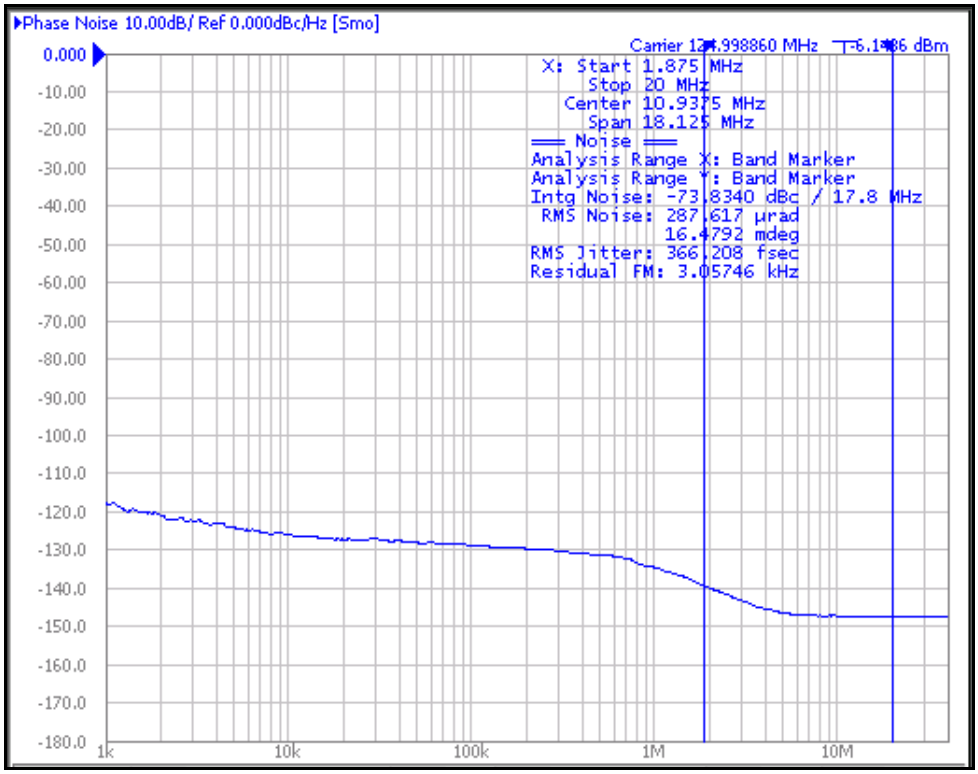
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

Table 6C. LVDS AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

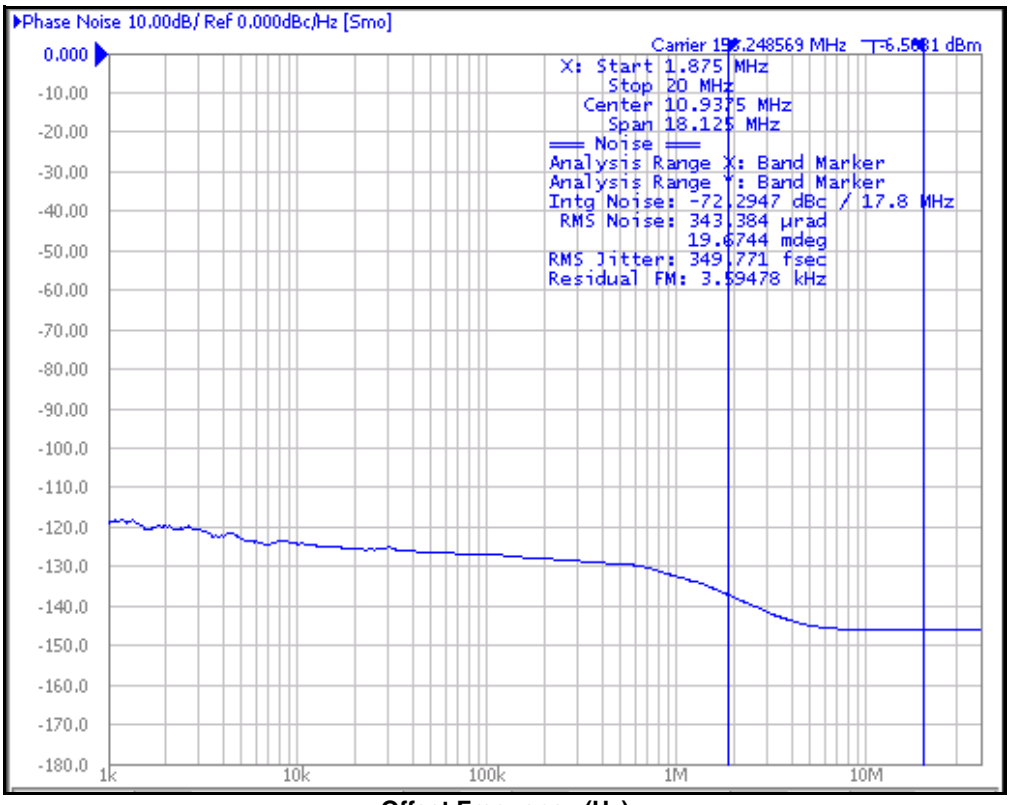
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Qx = ÷2		312.5		MHz
		Qx = ÷4		156.25		MHz
		Qx = ÷5		125		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); QAx = QBx = QCx	125MHz, (1.875MHz – 20MHz)		0.413	0.480	ps
		156.25MHz, (1.875MHz – 20MHz)		0.384	0.423	ps
		156.25MHz, (1MHz – 20MHz)		0.505	0.568	ps
		312.5MHz, (1.875MHz – 20MHz)		0.329	0.384	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			13	50	ps
t_R / t_F	Output Rise/Fall Time	f_{OUT} = 312.5MHz, 20% to 80%	350	600	1200	ps
		f_{OUT} = 125MHz, 156.25MHz, 20% to 80%	400	700	1200	ps
odc	Output Duty Cycle	f_{OUT} = 312.5MHz	35	48	60	%
		f_{OUT} = 125MHz, 156.25MHz	45	50	55	%
t_{LOCK}	PLL Lock Time				100	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

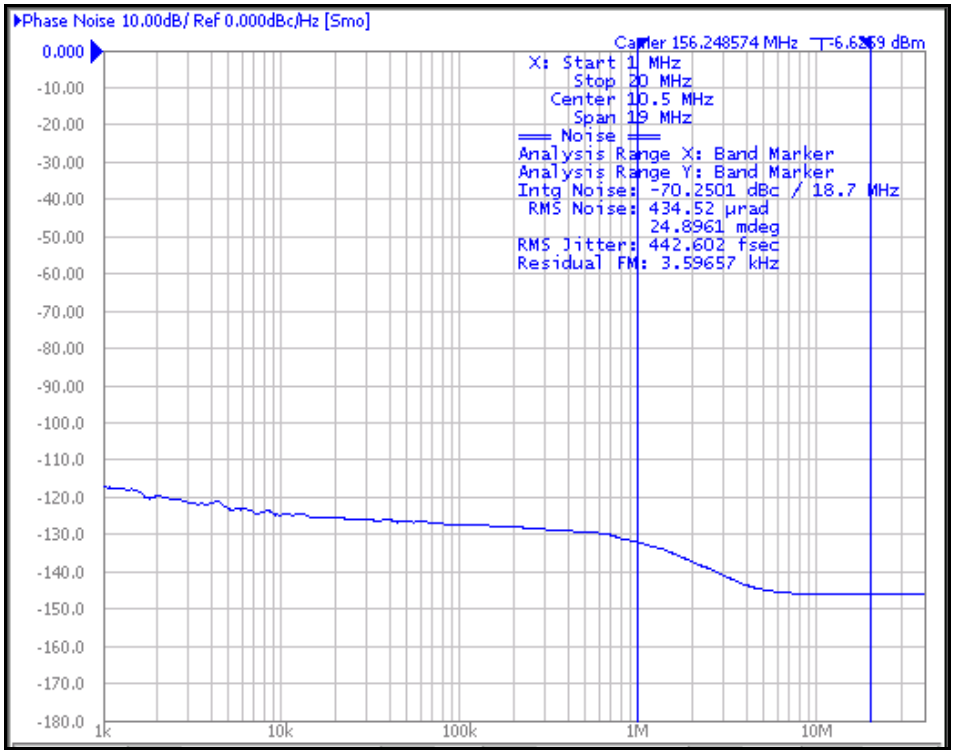
Typical Phase Noise at 125MHz, LVDS Output (V_{DD} = 3.3V, V_{DDO} = 3.3V)



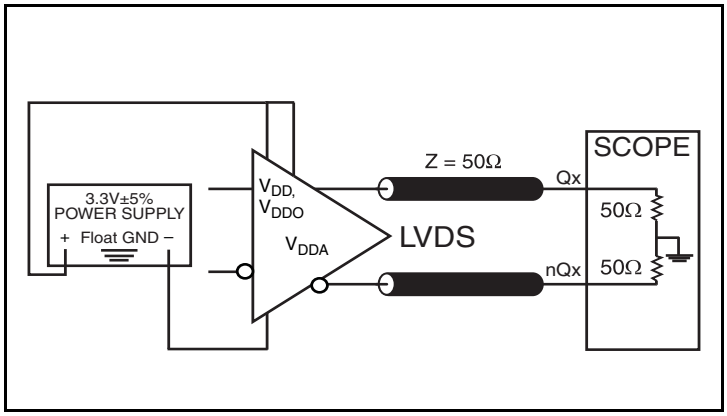
Typical Phase Noise at 156.25MHz, LVDS Output (V_{DD} = 3.3V, V_{DDO} = 3.3V)



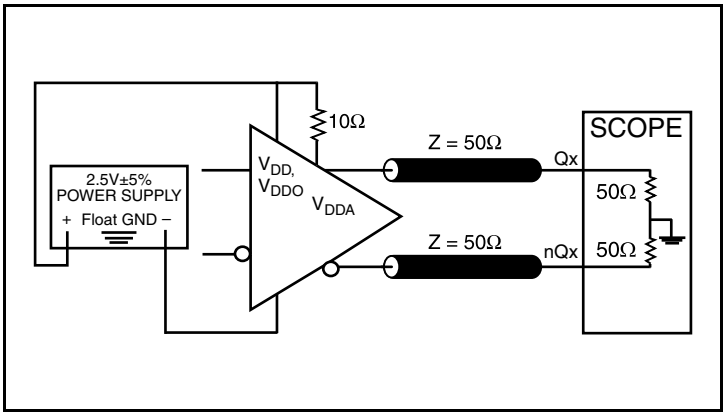
Typical Phase Noise at 156.25MHz, LVDS Output (V_{DD} = 3.3V, V_{DDO} = 3.3V)



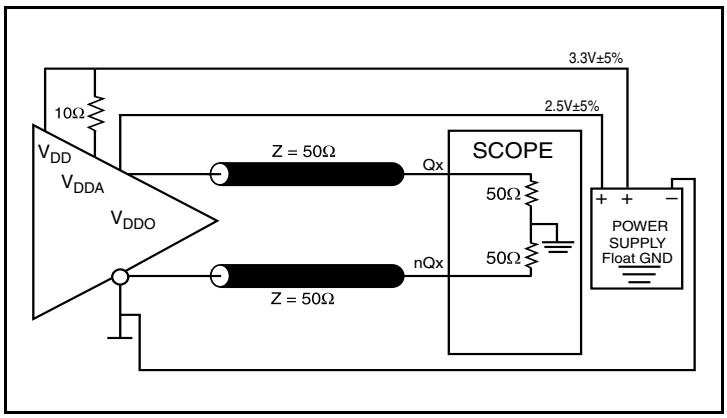
Parameter Measurement Information



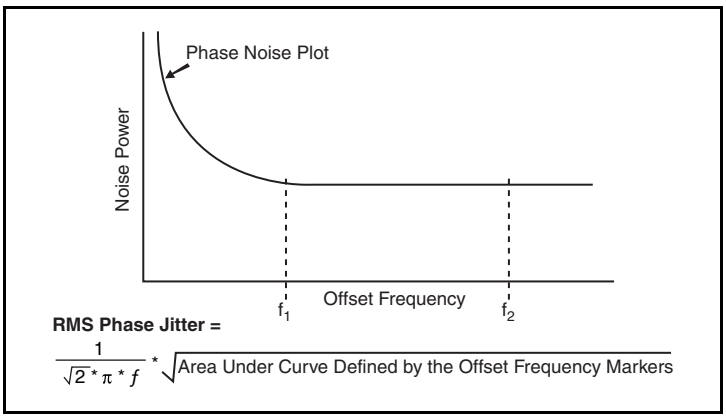
3.3V Core/ 3.3V LVDS Output Load AC Test Circuit



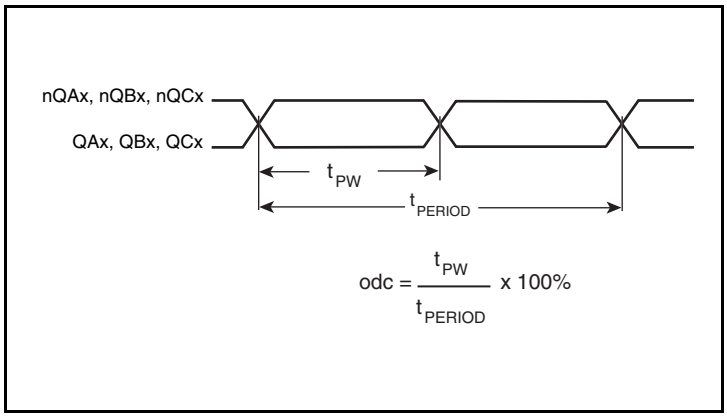
2.5V Core/ 2.5V LVDS Output Load AC Test Circuit



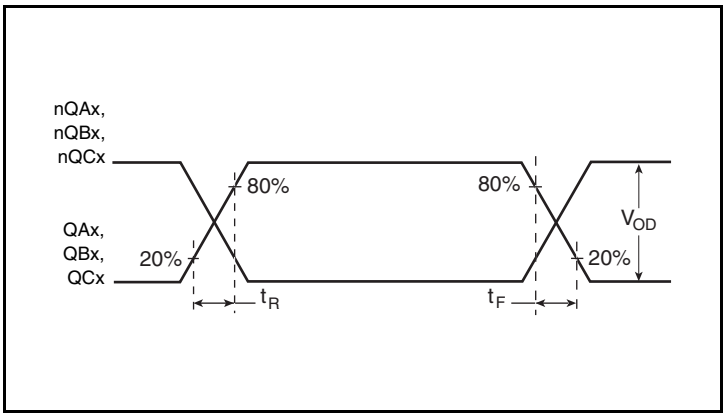
3.3V Core/ 2.5V LVDS Output Load AC Test Circuit



RMS Phase Jitter

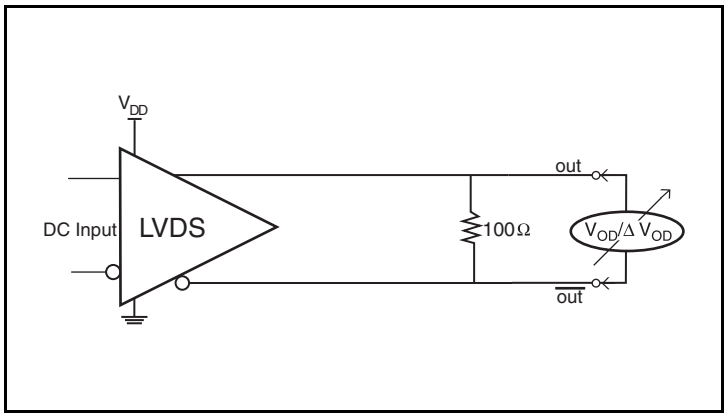


Output Duty Cycle/Pulse Width/Period

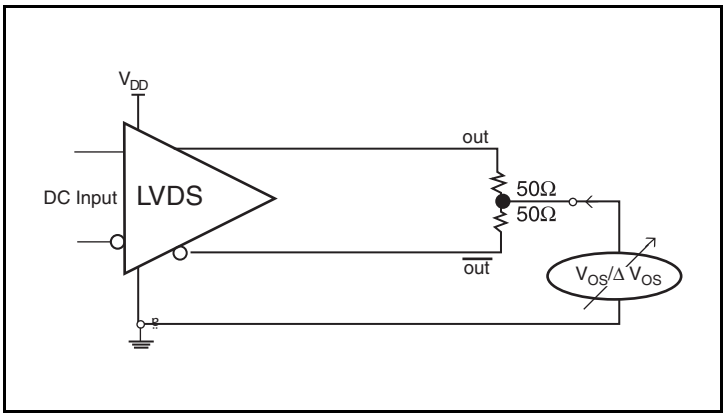


Output Rise/Fall Time

Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

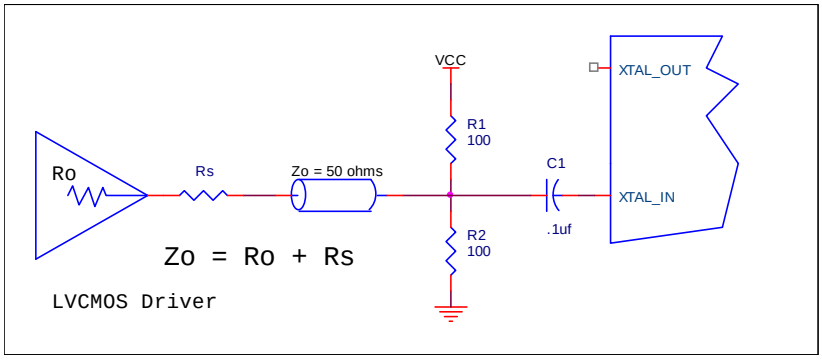


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

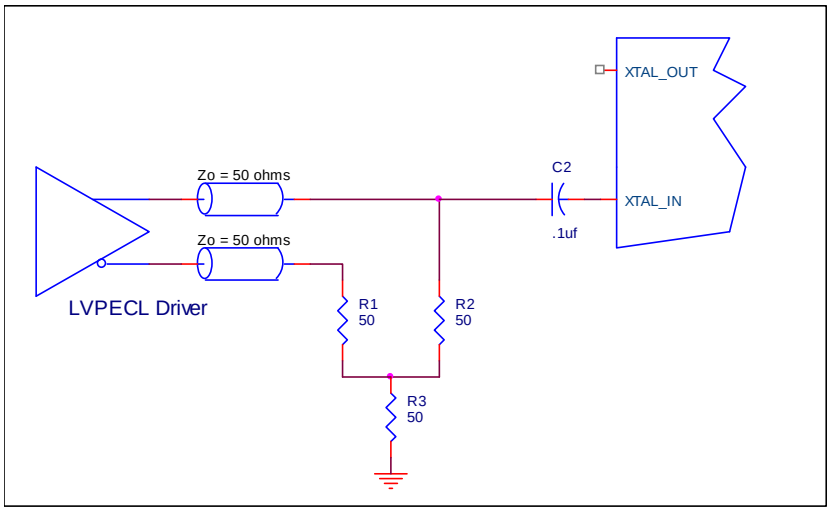


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

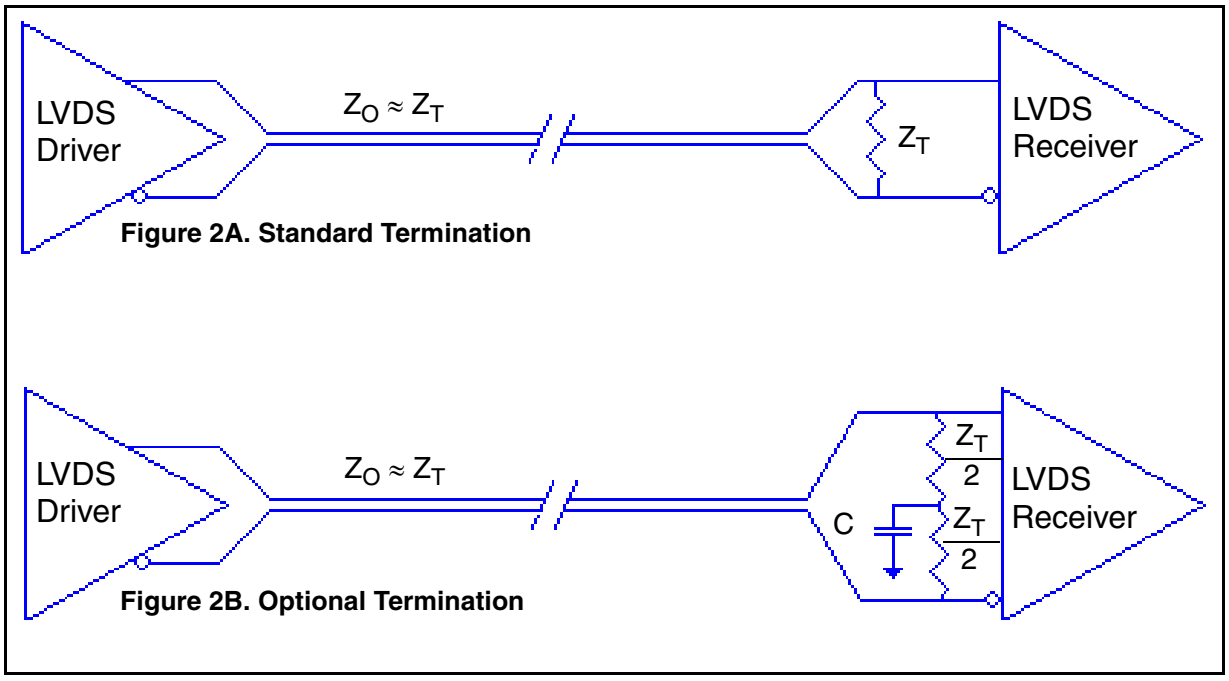


Figure 2A. Standard Termination

Figure 2B. Optional Termination

LVDS Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

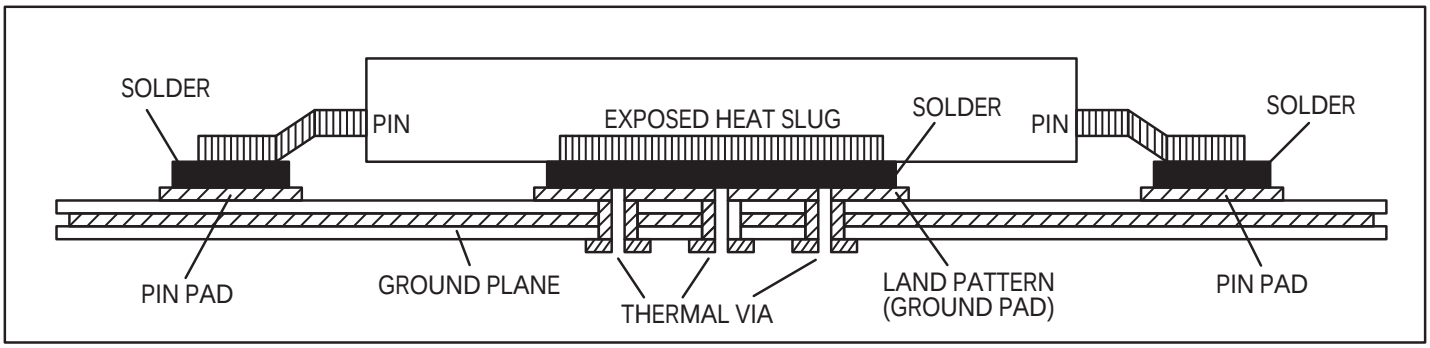


Figure 3. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Layout

Figure 4 shows an example ICS844625I application schematic in which the device is operated at V_{DD} = V_{DDA} = 3.3V.3V and V_{DDO} = 2.5V. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example MR, BYPASS and the output enables, OE[A:C] can be configured from an FPGA instead of pull up and pull down resistors as shown.

There are two LVDS termination options shown as examples of valid terminations.

1) The standard 100Ω resistor termination of R2.
2) An AC termination, used when coupling the ICS844625I LVDS output stage to a different logic family receiver. Always check to make sure LVDS p-p swing is sufficient to drive the receiver to valid logic levels.
    a) If the receiver is HCSL, then the R6-R7 voltage divider is set at the common mode center voltage of 0.35V.
    b) If the receiver is 1.5V CML, then R6 = 0Ω and R7 and C12 are not populated. Typically in this case, the termination resistors, R3 and R4 are integrated into the receiver. In this case only the external coupling caps, C13 and C14 are necessary for the proper termination of the LVDS output.

This device package has an ePAD that is connected to ground internally. The ePAD is to be connected to GND through vias in order to improve heat dissipation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{DD} pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, all the 0.1uf capacitors associated with the V_{DD}, V_{DDA} and V_{DDO} pins as well as the 10Ω resistor of the V_{DDA} filter must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

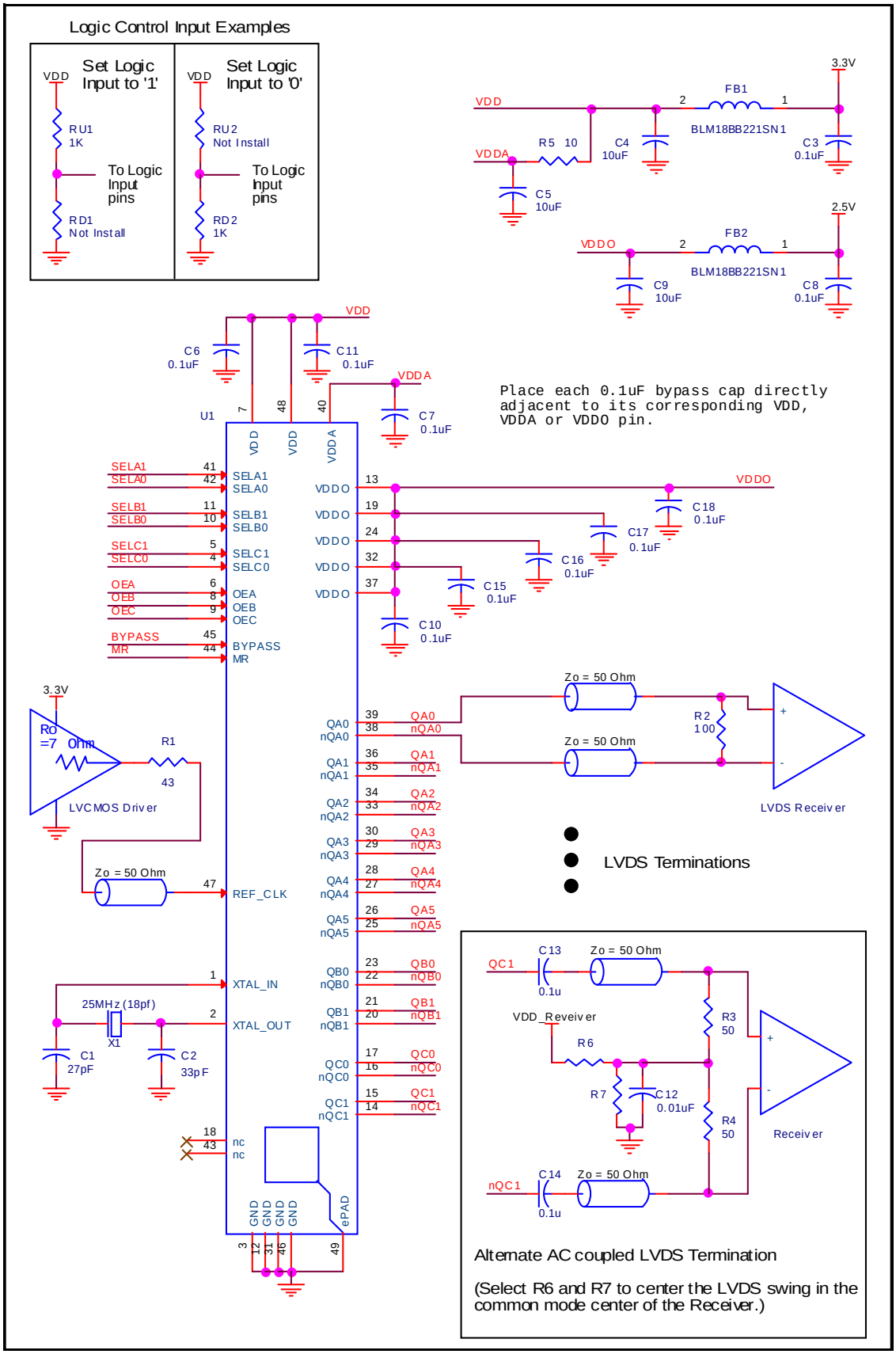


Figure 4. ICS844625I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844625I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844625I is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (125mA + 31mA) = **540.54mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 140mA = **485.1mW**

Total Power$_{\_MAX}$ = 540.54mW + 485.1mW = **1025.64mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 29°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.026W * 29°C/W = 114.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48 Lead TQFP, E-Pad Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.6°C/W	21.1°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 48 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	22.6°C/W	21.1°C/W

Transistor Count

The transistor count for ICS844625I is: 3,716

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead TQFP, E-Pad

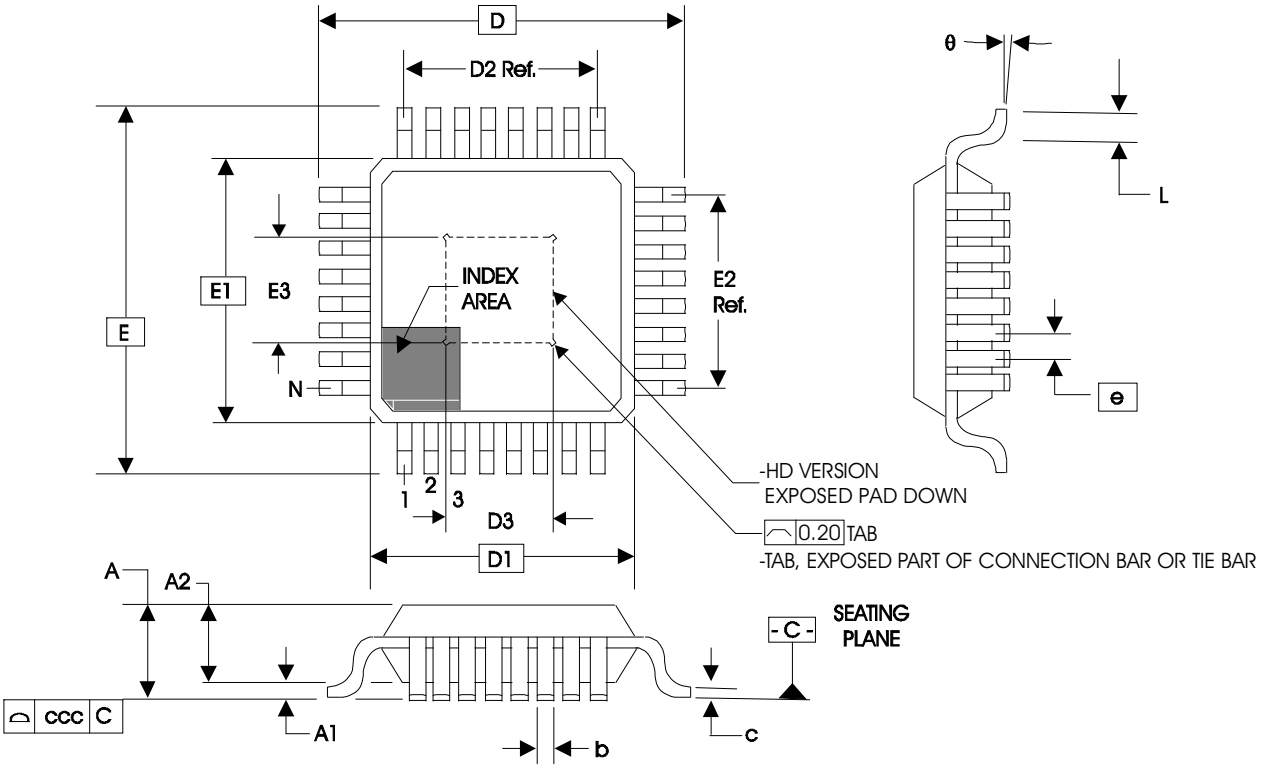


Table 9. Package Dimensions for 48 Lead TQFP, E-Pad

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
D3 & E3		3.5	
e		0.5 Basic	
L	0.45	0.60	0.75
θ	0°		7°

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844625BYILF	ICS844625BIL	“Lead-Free” 48 Lead TQFP, E-Pad	Tray	-40°C to 85°C
844625BYILFT	ICS844625BIL	“Lead-Free” 48 Lead TQFP, E-Pad	Tape & Reel	-40°C to 85°C

We’ve Got Your Timing Solution

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056