



# FEMTOCLOCKS™ SAS/SATA CLOCK GENERATOR

ICS843241

## GENERAL DESCRIPTION

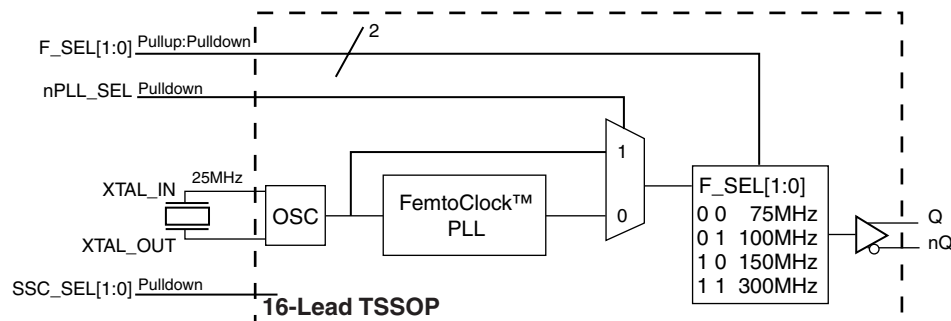
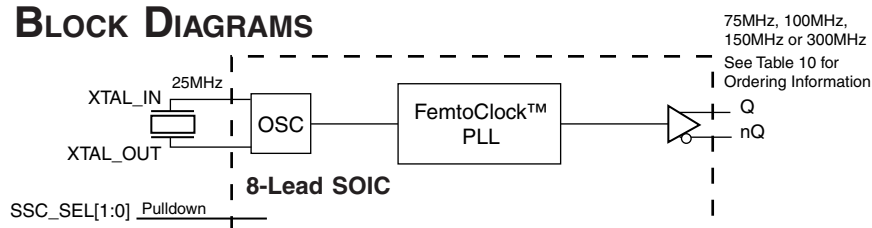


The ICS843241 is a low jitter, high performance clock generator and a member of the FemtoClocks™ family of silicon timing products. The ICS843241 is designed for use in the SAS-2 interconnect and the three transport protocols that use the SAS-2 interconnect: Serial SCSI Protocol (SSP), Serial ATA Tunneled Protocol (STP), and Serial Management Protocol (SMP). The ICS843241 has excellent (<1ps) RMS phase jitter, over the SAS defined integration range. The ICS843241 uses an external, 25MHz, parallel resonant crystal to generate three selectable output frequencies: 75MHz, 100MHz, 150MHz, and 300MHz. This silicon based approach provides excellent frequency stability and reliability. The ICS843241 features up, down, and center spread spectrum (SSC) clocking techniques. The up, down and center SSC will be required in the SAS-2 applications that have three clock trees in the HBA and expander ASICs (see Applications Information section, Figure 3).

## APPLICATIONS:

- SAS/ SATA Host Bus Adapters
- SATA Port Multipliers
- SAS I/O Controllers
- TapeDrive and HDD Array Controllers
- SAS Edge and Fanout Expanders
- HDDs and Tape Drives
- Disk Storage Enterprise

## BLOCK DIAGRAMS



## FEATURES

- Designed for use in SAS-2 systems
- Up, down and center spread spectrum clocking
- One differential 3.3V or 2.5V LVPECL output pair
- Selectable output frequencies: 75MHz, 100MHz, 150MHz, 300MHz
- RMS phase jitter @ 75MHz, (900kHz – 7.5MHz): 0.70ps (typical)
- 3.3V or 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

## ADDITIONAL ORDERING INFORMATION TABLE

| Part Number     | Package  | Output Frequency              |
|-----------------|----------|-------------------------------|
| ICS843241BG     | 16 TSSOP | 75MHz, 100MHz, 150MHz, 300MHz |
| ICS843241BM-75  | 8 SOIC   | 75MHz                         |
| ICS843241BM-100 | 8 SOIC   | 100MHz                        |
| ICS843241BM-150 | 8 SOIC   | 150MHz                        |
| ICS843241BM-300 | 8 SOIC   | 300MHz                        |

## PIN ASSIGNMENT

|          |   |   |                 |
|----------|---|---|-----------------|
| XTAL_OUT | 1 | 8 | V <sub>EE</sub> |
| XTAL_IN  | 2 | 7 | nQ              |
| SSC_SEL0 | 3 | 6 | Q               |
| SSC_SEL1 | 4 | 5 | V <sub>CC</sub> |

### ICS843241-XXX

**8-Lead SOIC, 150 mil**

3.90mm x 4.90mm x 1.37mm package body

**M Package**

Top View

## PIN ASSIGNMENT

|                 |   |    |                 |
|-----------------|---|----|-----------------|
| V <sub>EE</sub> | 1 | 16 | F_SEL1          |
| XTAL_OUT        | 2 | 15 | V <sub>EE</sub> |
| XTAL_IN         | 3 | 14 | nPLL_SEL        |
| SSC_SEL0        | 4 | 13 | nQ              |
| nc              | 5 | 12 | Q               |
| nc              | 6 | 11 | V <sub>CC</sub> |
| nc              | 7 | 10 | F_SEL0          |
| SSC_SEL1        | 8 | 9  | V <sub>CC</sub> |

### ICS843241

**16-Lead TSSOP**

4.4mm x 5.0mm x 0.92mm package body

**G Package**

Top View

TABLE 1. PIN DESCRIPTIONS

| Name               | Type   |          | Description                                                                 |
|--------------------|--------|----------|-----------------------------------------------------------------------------|
| XTAL_OUT, XTAL_IN  | Input  |          | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| SSC_SEL0, SSC_SEL1 | Input  | Pulldown | SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.               |
| F_SEL0             | Input  | Pulldown | Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.   |
| F_SEL1             | Input  | Pullup   | Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.   |
| nPLL_SEL           | Input  | Pulldown | Bypasses the PLL. LVCMOS/LVTTL interface levels.                            |
| nQ, Q              | Output |          | Differential clock outputs. LVPECL interface levels.                        |
| V <sub>EE</sub>    | Power  |          | Negative supply pin.                                                        |
| V <sub>CC</sub>    | Power  |          | Power supply pin.                                                           |
| nc                 | Unused |          | No connect.                                                                 |

TABLE 2. PIN CHARACTERISTICS

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |

TABLE 3A. SSC\_SEL[1:0] FUNCTION TABLE

| Inputs      |             | Mode               |
|-------------|-------------|--------------------|
| SSC_SEL1    | SSC_SEL0    |                    |
| 0 (default) | 0 (default) | SSC Off            |
| 0           | 1           | 0.5% Down-spread   |
| 1           | 0           | 0.5% Up-spread     |
| 1           | 1           | 0.5% Center-spread |

TABLE 3B. F\_SEL[1:0] FUNCTION TABLE

| Inputs      |             | Output Frequency |
|-------------|-------------|------------------|
| F_SEL1      | F_SEL0      |                  |
| 0           | 0           | 75MHz            |
| 0           | 1           | 100MHz           |
| 1 (default) | 0 (default) | 150MHz           |
| 1           | 1           | 300MHz           |

**ABSOLUTE MAXIMUM RATINGS**

|                                          |                          |
|------------------------------------------|--------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ |                          |
| 8 SOIC                                   | 96°C/W (0 lfpm)          |
| 16 TSSOP                                 | 92.4°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Power Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$ | Power Supply Current |                 |         |         | 77      | mA    |

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Power Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{EE}$ | Power Supply Current |                 |         |         | 75      | mA    |

**TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter          |                                | Test Conditions                               | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|--------------------------------|-----------------------------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                                | $V_{CC} = 3.3V$                               | 2       |         | $V_{CC} + 0.3$ | V       |
|          |                    |                                | $V_{CC} = 2.5V$                               | 1.7     |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                                | $V_{CC} = 3.3V$                               | -0.3    |         | 0.8            | V       |
|          |                    |                                | $V_{CC} = 2.5V$                               | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current | F_SEL0, nPLL_SEL, SSC_SEL[0:1] | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 150            | $\mu A$ |
|          |                    | F_SEL1                         | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current  | F_SEL0, nPLL_SEL, SSC_SEL[0:1] | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|          |                    | F_SEL1                         | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -150    |         |                | $\mu A$ |

**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum        | Typical | Maximum        | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CC} - 1.4$ |         | $V_{CC} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CC} - 2.0$ |         | $V_{CC} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6            |         | 1.0            | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .**TABLE 4E. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum        | Typical | Maximum        | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CC} - 1.4$ |         | $V_{CC} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CC} - 2.0$ |         | $V_{CC} - 1.5$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.4            |         | 1.0            | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 25      |         | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

**TABLE 6A. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol               | Parameter                             | Test Conditions                                | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------------------|------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                      | $F\_SEL[1:0] = 00$                             |         | 75      |         | MHz   |
|                      |                                       | $F\_SEL[1:0] = 01$                             |         | 100     |         | MHz   |
|                      |                                       | $F\_SEL[1:0] = 10$                             |         | 150     |         | MHz   |
|                      |                                       | $F\_SEL[1:0] = 11$                             |         | 300     |         | MHz   |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter ( Random);<br>NOTE 1 | 75MHz @ Integration Range:<br>900kHz - 7.5MHz  |         | 0.70    |         | ps    |
|                      |                                       | 100MHz @ Integration Range:<br>900kHz - 7.5MHz |         | 0.69    |         | ps    |
|                      |                                       | 150MHz @ Integration Range:<br>900kHz - 7.5MHz |         | 0.69    |         | ps    |
|                      |                                       | 300MHz @ Integration Range:<br>900kHz - 7.5MHz |         | 0.68    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                 | 20% to 80%                                     | 335     |         | 590     | ps    |
| odc                  | Output Duty Cycle                     |                                                | 48      |         | 52      | %     |

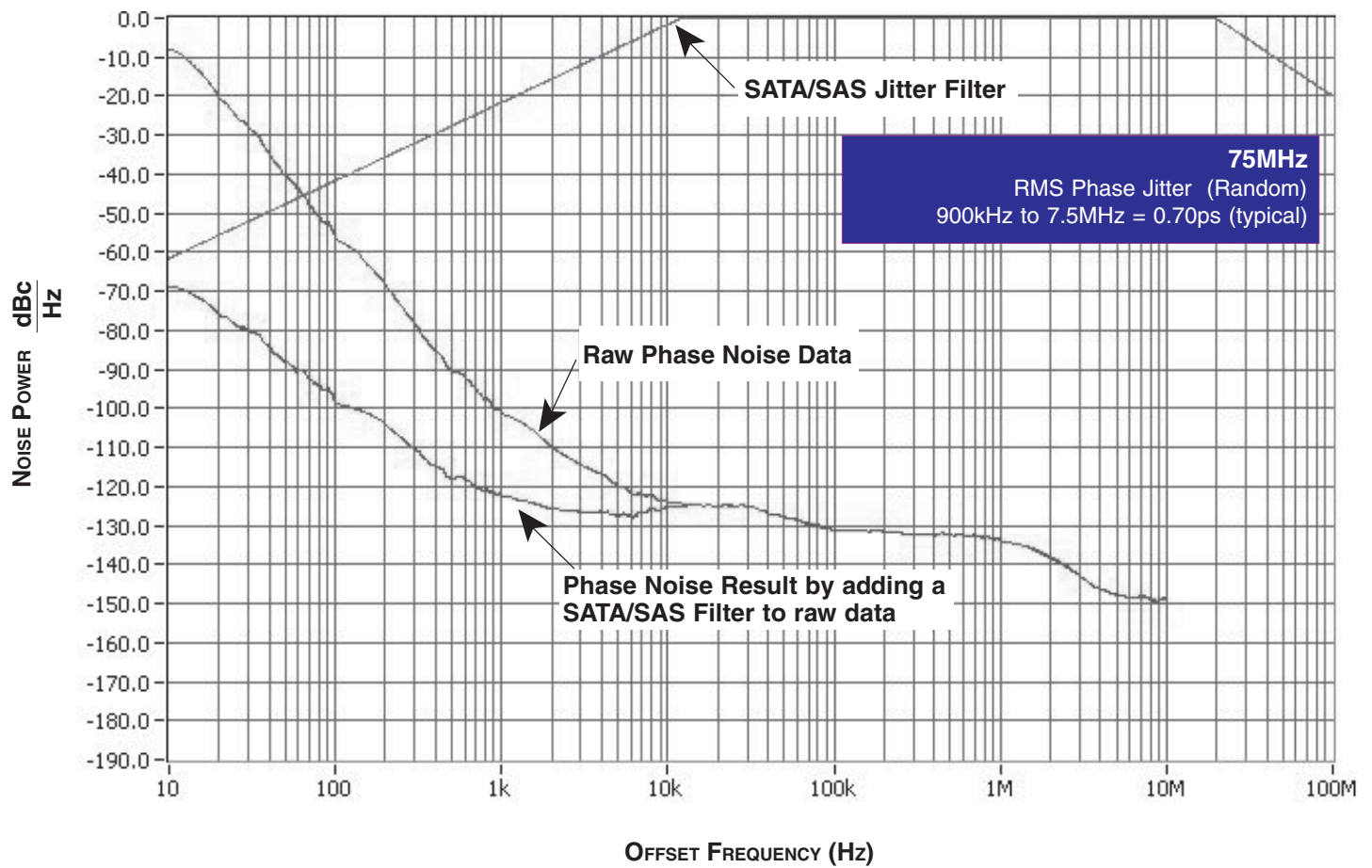
NOTE 1: Refer to the Phase Noise Plots.

**TABLE 6B. AC CHARACTERISTICS**,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

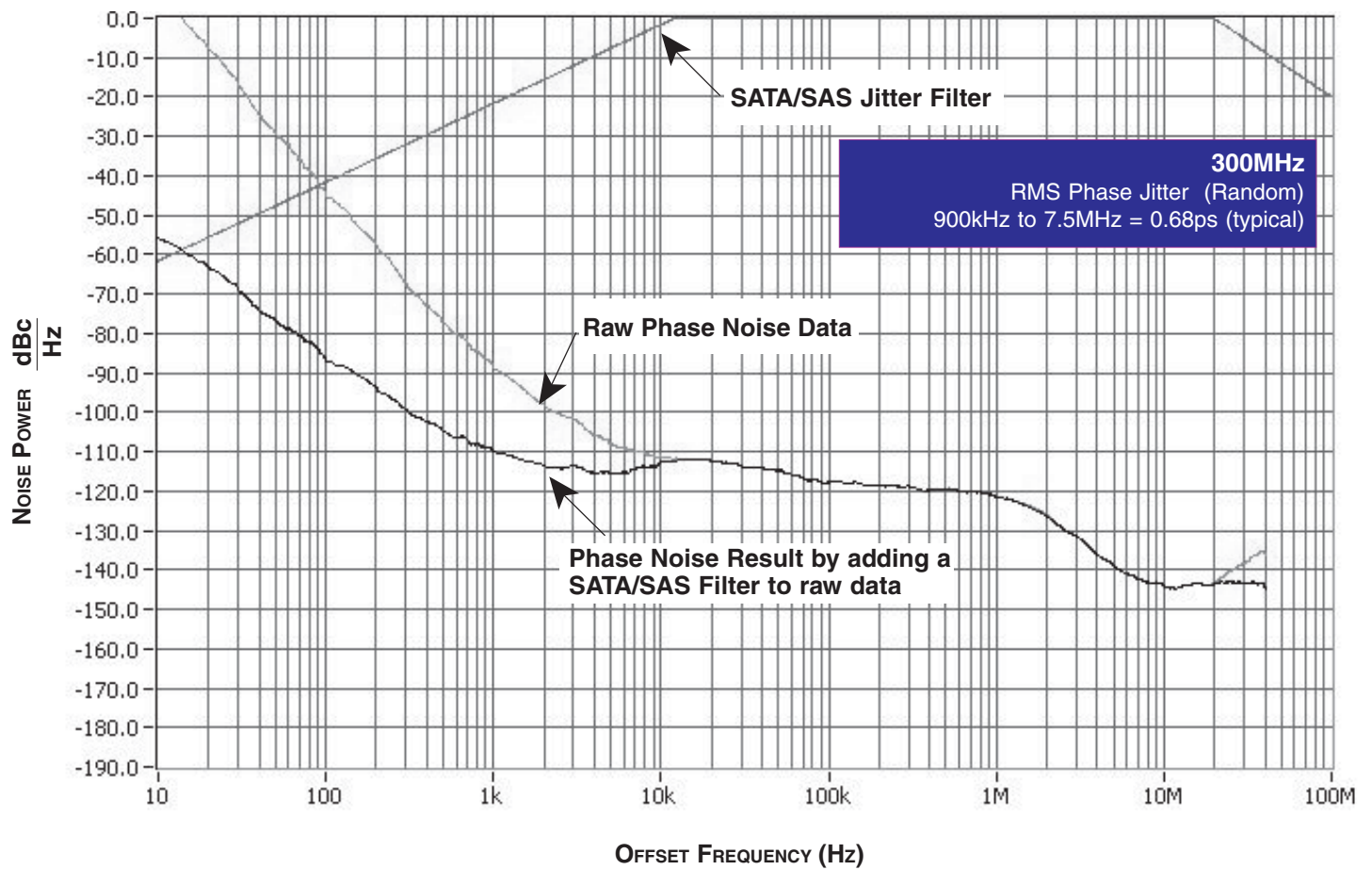
| Symbol               | Parameter                             | Test Conditions                                | Minimum | Typical | Maximum | Units |
|----------------------|---------------------------------------|------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                      | F_SEL[1:0] = 00                                |         | 75      |         | MHz   |
|                      |                                       | F_SEL[1:0] = 01                                |         | 100     |         | MHz   |
|                      |                                       | F_SEL[1:0] = 10                                |         | 150     |         | MHz   |
|                      |                                       | F_SEL[1:0] = 11                                |         | 300     |         | MHz   |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter ( Random);<br>NOTE 1 | 75MHz @ Integration Range:<br>900kHz - 7.5MHz  |         | 0.72    |         | ps    |
|                      |                                       | 100MHz @ Integration Range:<br>900kHz - 7.5MHz |         | 0.61    |         | ps    |
|                      |                                       | 150MHz @ Integration Range:<br>900kHz - 7.5MHz |         | 0.68    |         | ps    |
|                      |                                       | 300MHz @ Integration Range:<br>900kHz - 7.5MHz |         | 0.64    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time                 | 20% to 80%                                     | 360     |         | 500     | ps    |
| odc                  | Output Duty Cycle                     |                                                | 48      |         | 52      | %     |

NOTE 1: Refer to the Phase Noise Plots.

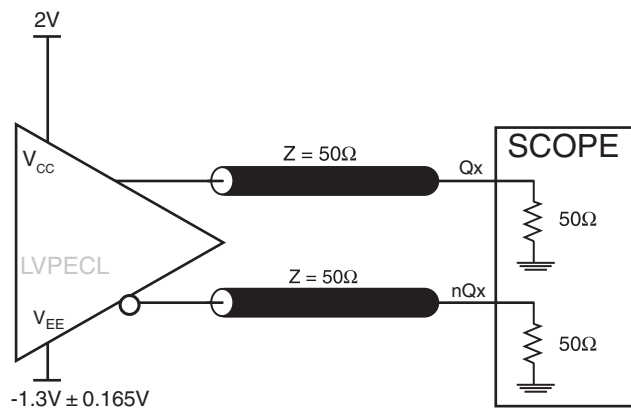
## TYPICAL PHASE NOISE AT 75MHz (3.3V)



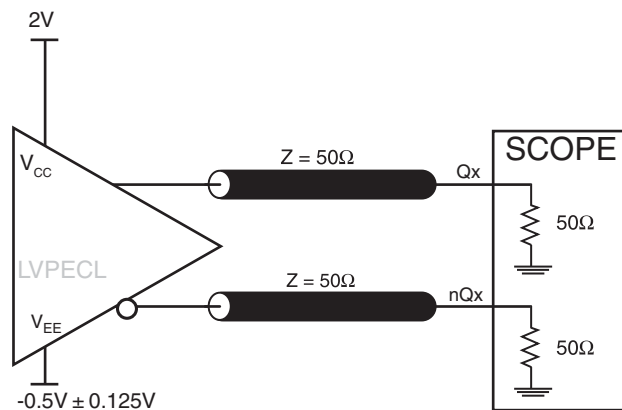
## TYPICAL PHASE NOISE AT 300MHz (3.3V)



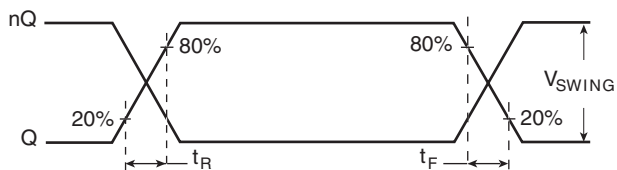
## PARAMETER MEASUREMENT INFORMATION



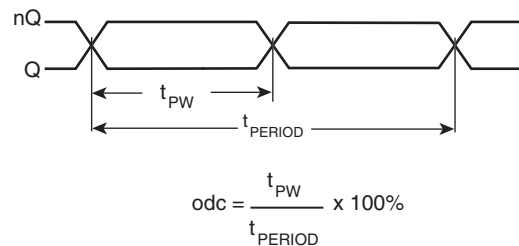
3.3V OUTPUT LOAD AC TEST CIRCUIT



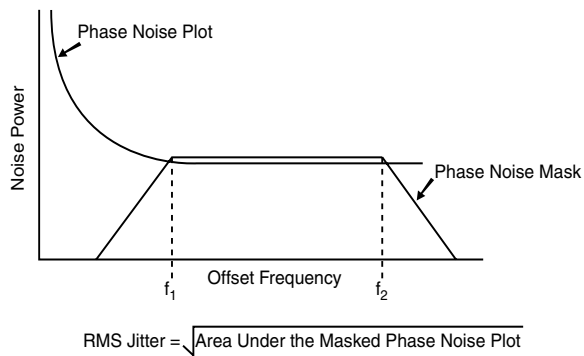
2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



RMS PHASE JITTER

## APPLICATION INFORMATION

### CRYSTAL INPUT INTERFACE

The ICS843241 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

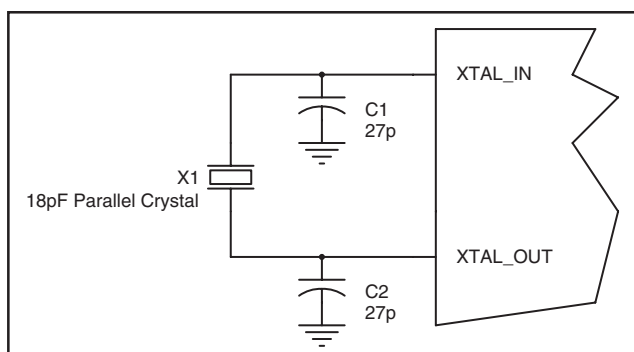


FIGURE 1. CRYSTAL INPUT INTERFACE

### LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R1$  and  $R2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R1$  and  $R2$  can be 100Ω. This can also be accomplished by removing  $R1$  and making  $R2$  50Ω.

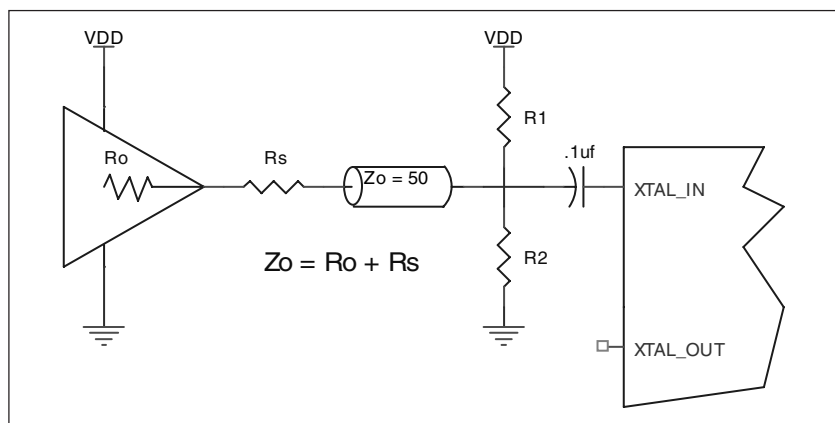


FIGURE 2. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

## RECOMMENDATIONS FOR UNUSED INPUT PINS

### INPUTS:

#### LVC MOS CONTROL PINS

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

## TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

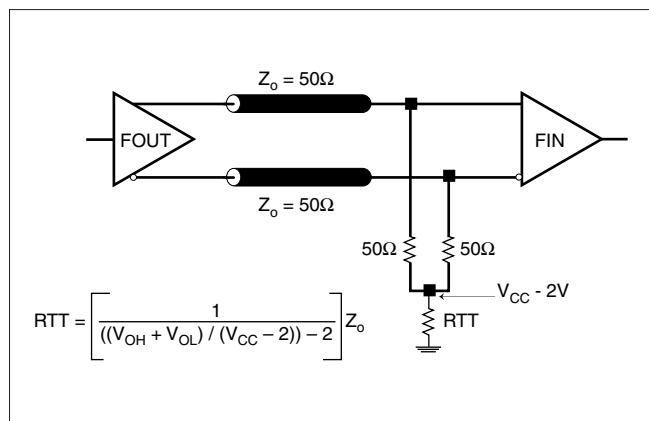


FIGURE 3A. LVPECL OUTPUT TERMINATION

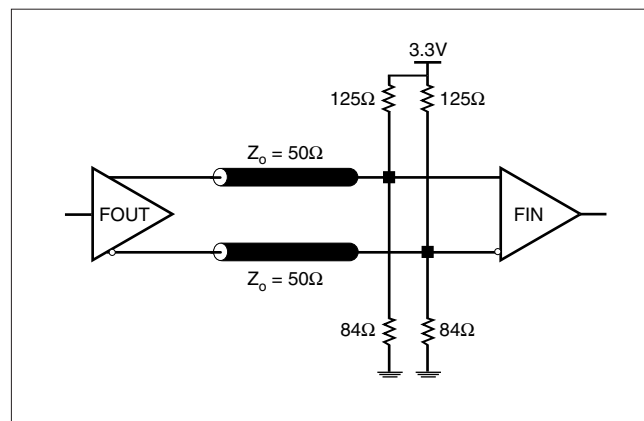


FIGURE 3B. LVPECL OUTPUT TERMINATION

## TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

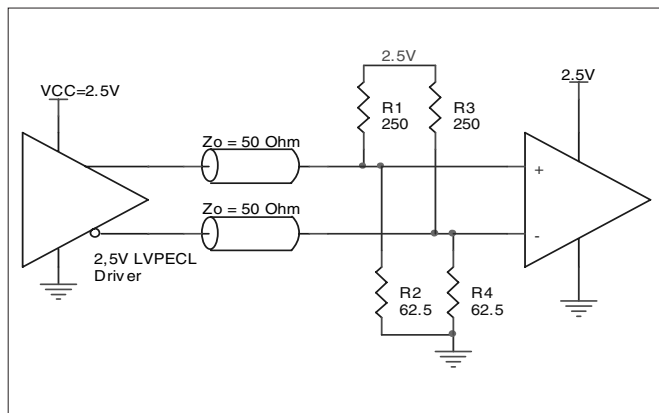


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

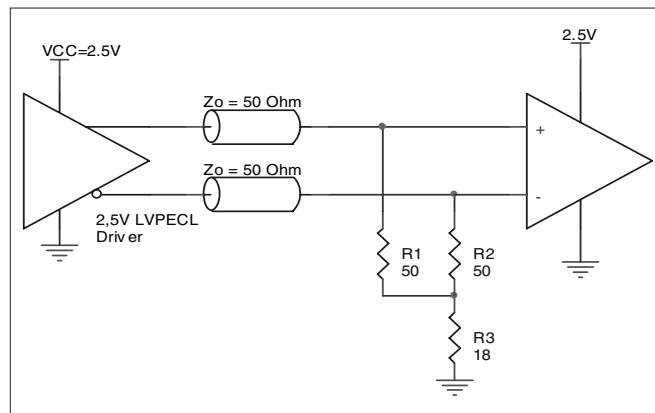


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

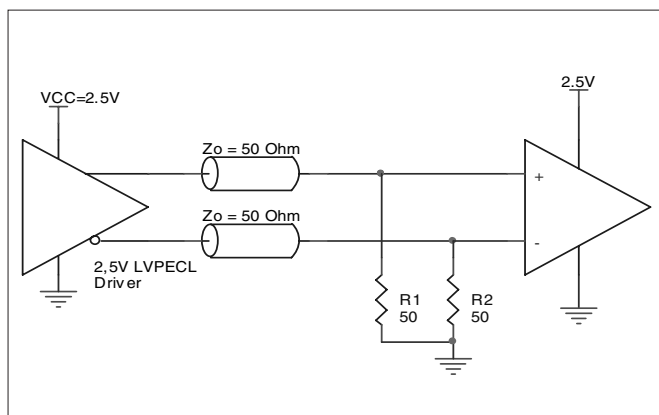


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

## SCHEMATIC EXAMPLE

Figure 5 shows an example of ICS843241 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The  $C1 = 27pF$  and  $C2 = 27pF$  are recommended for frequency accuracy. For different

board layout, the  $C1$  and  $C2$  may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

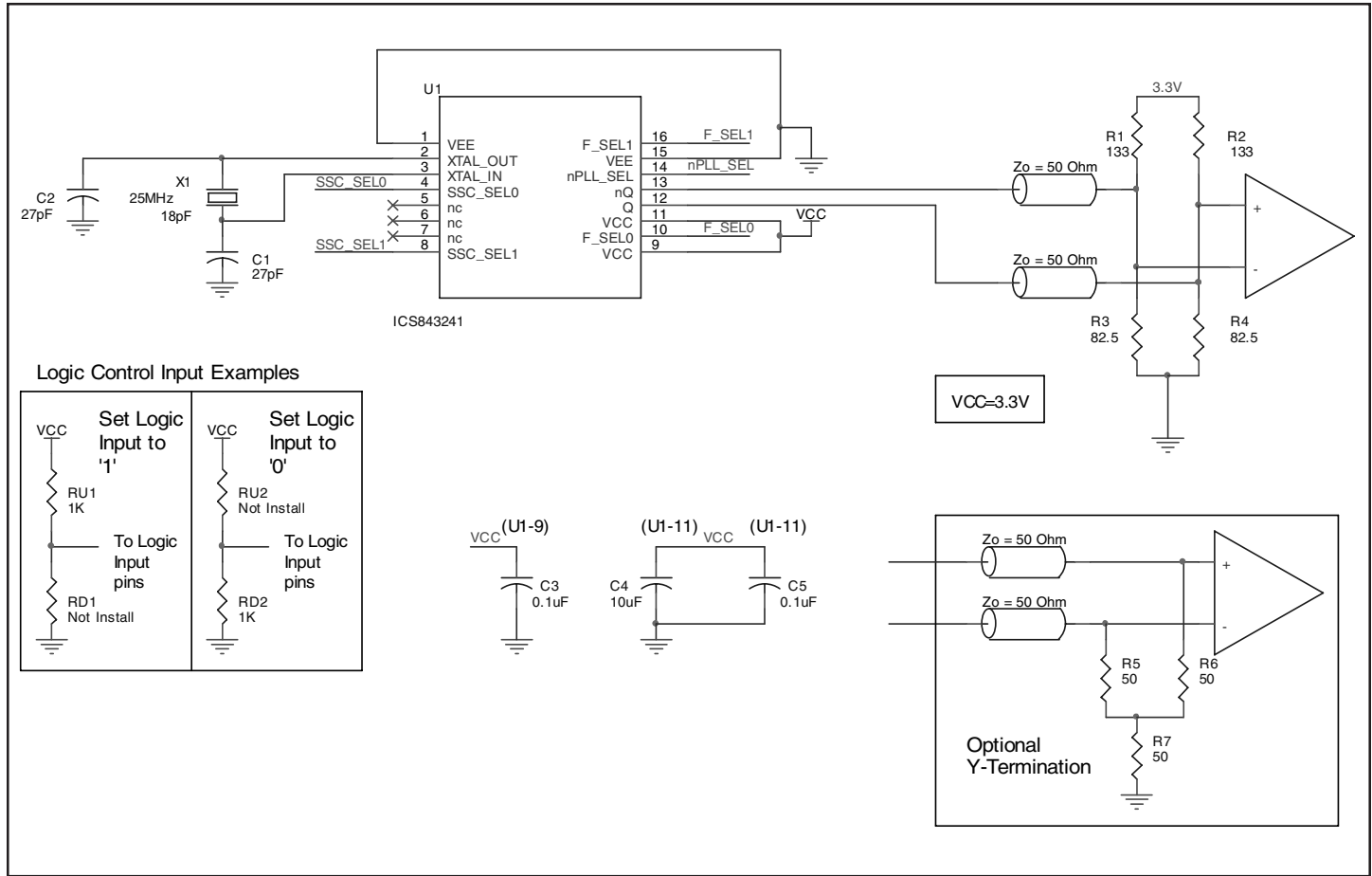


FIGURE 5. ICS843241 SCHEMATIC EXAMPLE

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843241. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS843241 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 77mA = 266.8mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) = 266.8mW + 30mW = **296.8mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 7B below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70^\circ C + 0.297W * 96^\circ C/W = 97.6^\circ C$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board.

**TABLE 7A.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 16 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) |          |          |          |
|-----------------------------------------------|----------|----------|----------|
|                                               | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 92.4°C/W | 88.0°C/W | 85.9°C/W |

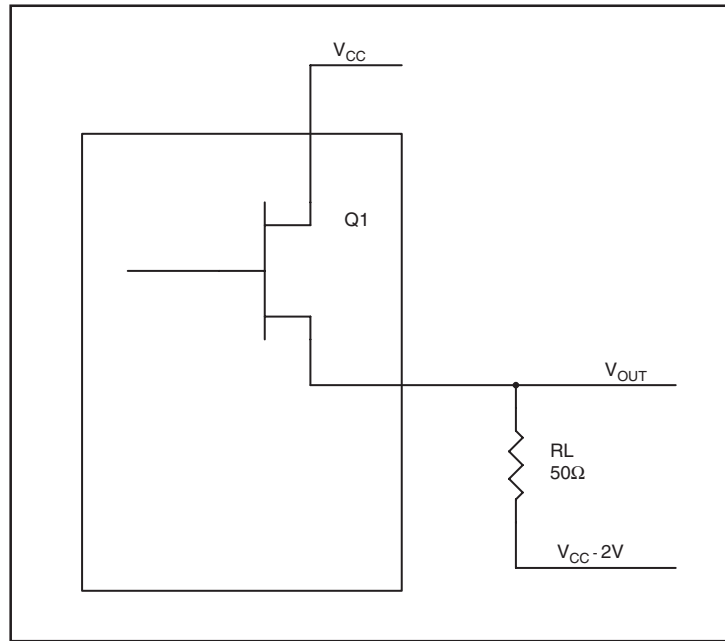
**TABLE 7B.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD SOIC**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |        |        |        |
|----------------------------------------------------|--------|--------|--------|
|                                                    | 0      | 200    | 500    |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 96°C/W | 87°C/W | 82°C/W |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

## RELIABILITY INFORMATION

**TABLE 8A.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD SOIC**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |        |        |        |
|----------------------------------------------------|--------|--------|--------|
|                                                    | 0      | 200    | 500    |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 96°C/W | 87°C/W | 82°C/W |

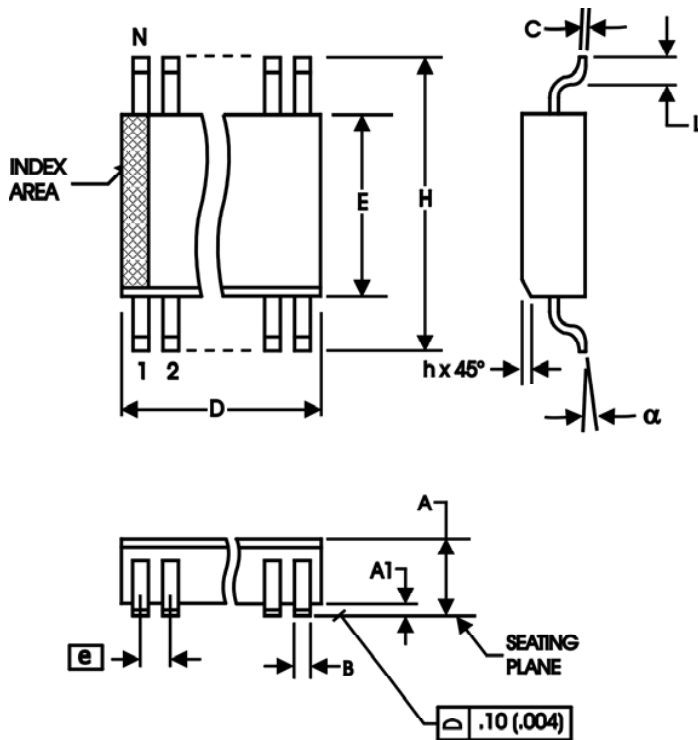
**TABLE 8B.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 16 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) |          |          |          |
|-----------------------------------------------|----------|----------|----------|
|                                               | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 92.4°C/W | 88.0°C/W | 85.9°C/W |

### TRANSISTOR COUNT

The transistor count for ICS843241 is: 2986

## PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC



## PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

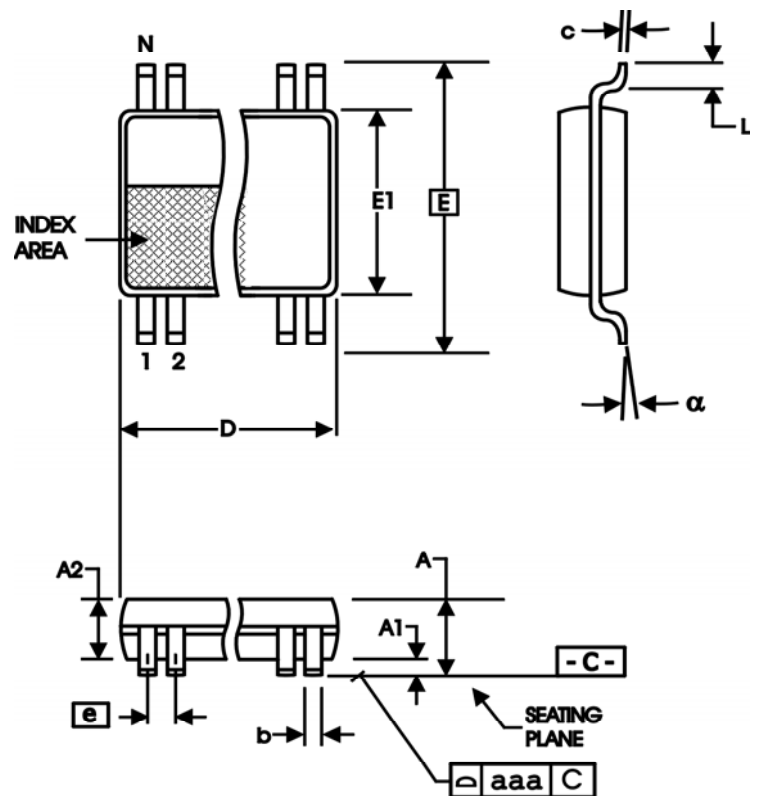


TABLE 9A. 8 LEAD SOIC PACKAGE DIMENSIONS

| SYMBOL   | Millimeters |         |
|----------|-------------|---------|
|          | MINIMUM     | MAXIMUM |
| N        | 8           |         |
| A        | 1.35        | 1.75    |
| A1       | 0.10        | 0.25    |
| B        | 0.33        | 0.51    |
| C        | 0.19        | 0.25    |
| D        | 4.80        | 5.00    |
| E        | 3.80        | 4.00    |
| e        | 1.27 BASIC  |         |
| H        | 5.80        | 6.20    |
| h        | 0.25        | 0.50    |
| L        | 0.40        | 1.27    |
| $\alpha$ | 0°          | 8°      |

Reference Document: JEDEC Publication 95, MS-012

TABLE 9B. 16 LEAD TSSOP PACKAGE DIMENSIONS

| SYMBOL   | Millimeters |         |
|----------|-------------|---------|
|          | Minimum     | Maximum |
| N        | 16          |         |
| A        | --          | 1.20    |
| A1       | 0.05        | 0.15    |
| A2       | 0.80        | 1.05    |
| b        | 0.19        | 0.30    |
| c        | 0.09        | 0.20    |
| D        | 4.90        | 5.10    |
| E        | 6.40 BASIC  |         |
| E1       | 4.30        | 4.50    |
| e        | 0.65 BASIC  |         |
| L        | 0.45        | 0.75    |
| $\alpha$ | 0°          | 8°      |
| aaa      | --          | 0.10    |

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

| Part/Order Number  | Marking  | Package                   | Shipping Packaging | Temperature |
|--------------------|----------|---------------------------|--------------------|-------------|
| ICS843241BGLF      | 843241BL | 16 Lead "Lead-Free" TSSOP | tube               | 0°C to 70°C |
| ICS843241BGLFT     | 843241BL | 16 Lead "Lead-Free" TSSOP | 2500 tape & reel   | 0°C to 70°C |
| ICS843241BM-75LF   | 3241B75L | 8 Lead "Lead-Free" SOIC   | tube               | 0°C to 70°C |
| ICS843241BM-75LFT  | 3241B75L | 8 Lead "Lead-Free" SOIC   | 2500 tape & reel   | 0°C to 70°C |
| ICS843241BM-100LF  | 241B100L | 8 Lead "Lead-Free" SOIC   | tube               | 0°C to 70°C |
| ICS843241BM-100LFT | 241B100L | 8 Lead "Lead-Free" SOIC   | 2500 tape & reel   | 0°C to 70°C |
| ICS843241BM-150LF  | 241B150L | 8 Lead "Lead-Free" SOIC   | tube               | 0°C to 70°C |
| ICS843241BM-150LFT | 241B150L | 8 Lead "Lead-Free" SOIC   | 2500 tape & reel   | 0°C to 70°C |
| ICS843241BM-300LF  | 241B300L | 8 Lead "Lead-Free" SOIC   | tube               | 0°C to 70°C |
| ICS843241BM-300LFT | 241B300L | 8 Lead "Lead-Free" SOIC   | 2500 tape & reel   | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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