FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL CLOCK MULTIPLIER

ICS843081I-33

General Description

The ICS843081I-33 is an Ethernet Clock Multiplier and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS843081I-33 accepts a crystal reference of 20MHz. The ICS843081I-33 has excellent 1ps or lower phase jitter performance, over the 12kHz - 20MHz integration range. The ICS843081I-33 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

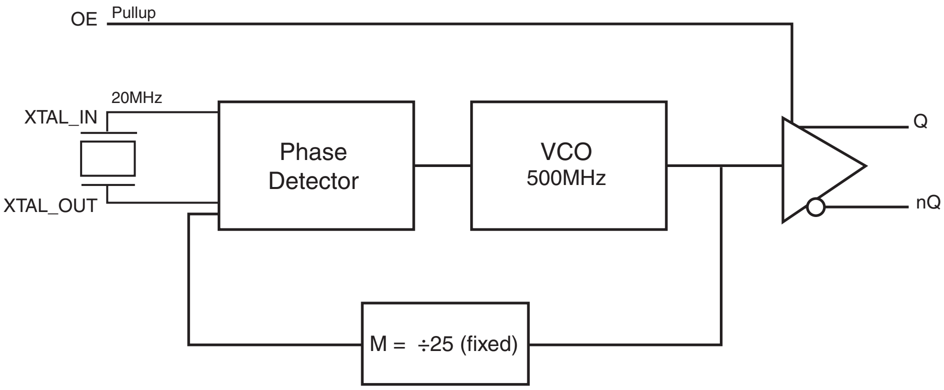
Features

- One differential 3.3V LVPECL output
- One crystal oscillator interface: 20MHz
- Output frequency: 500MHz
- VCO: 500MHz
- RMS phase jitter at 500MHz using a 20MHz crystal, (12kHz – 20MHz): 0.72ps (typical)
- Full 3.3V output supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

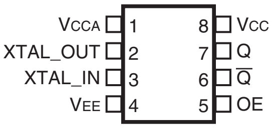
Table 1. Frequency Table

Input	M/N Multiplier	Output Frequency (MHz)
Crystal Frequency (MHz)		
20	25	500

Block Diagram



Pin Assignment



ICS843081I-33
8 Lead TSSOP
4.40mm x 3.0mm x 0.925 package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2, 3	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	V_{EE}	Power		Negative supply pin.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q/$\overline{Q}$ outputs are enabled. When LOW, forces Q/nQ in high-impedance state. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	
I_{CCA}	Analog Supply Current			10		mA
I_{EE}	Power Supply Current			80		mA

Table 3B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

Table 3C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	µA
V_{OL}	Output Low Current; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	µA
V_{SWING}	Peak-to-peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			20		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

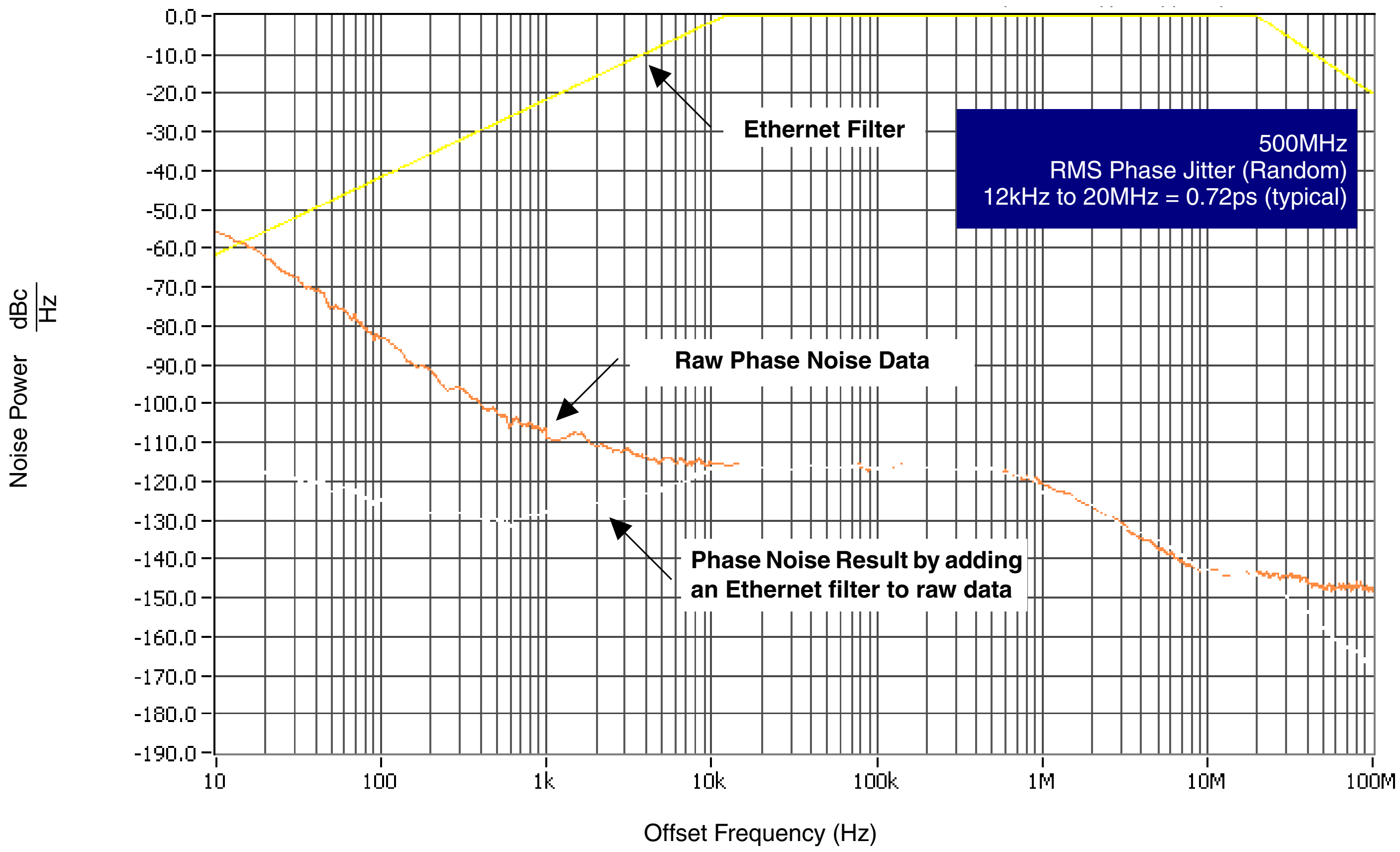
AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 3.3V ± 5%, T_A = -40°C to 85°

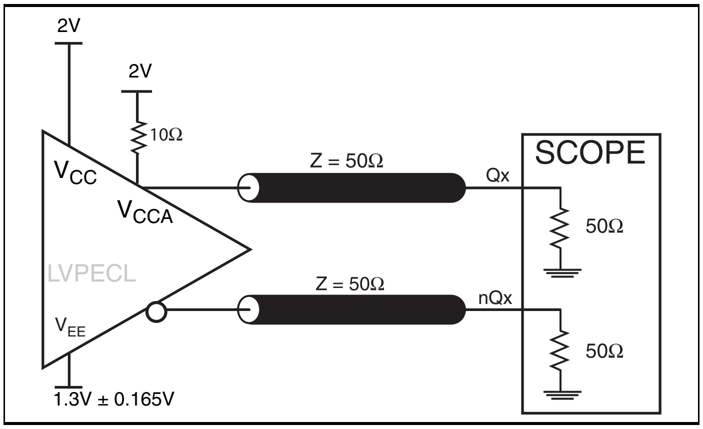
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				500	MHz
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 1	500MHz, Integration Range: 12kHz – 20MHz		0.72		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

NOTE 1: Refer to the Phase Noise Plot.

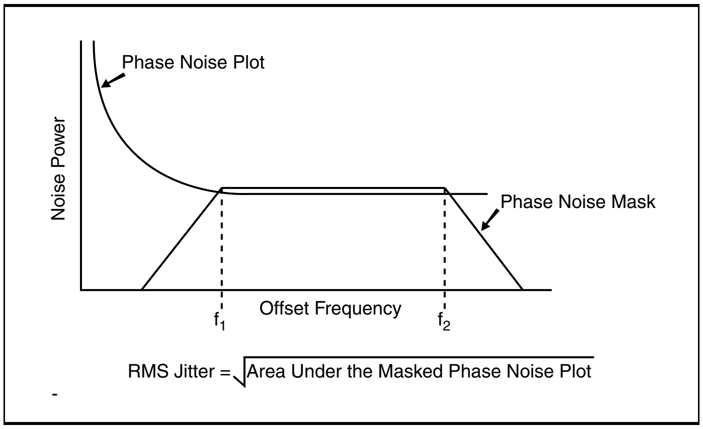
Typical Phase Noise at 500MHz



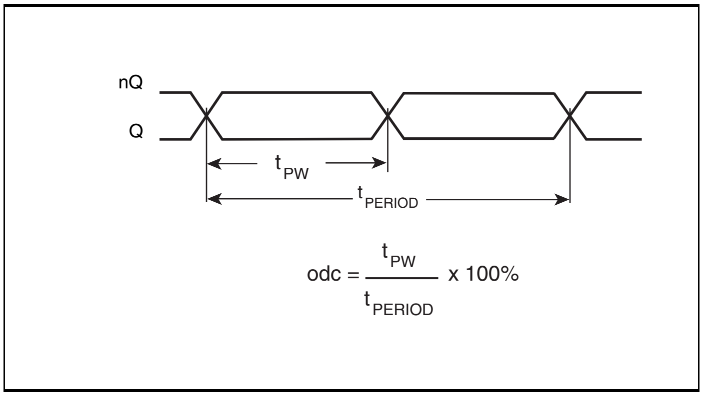
Parameter Measurement Information



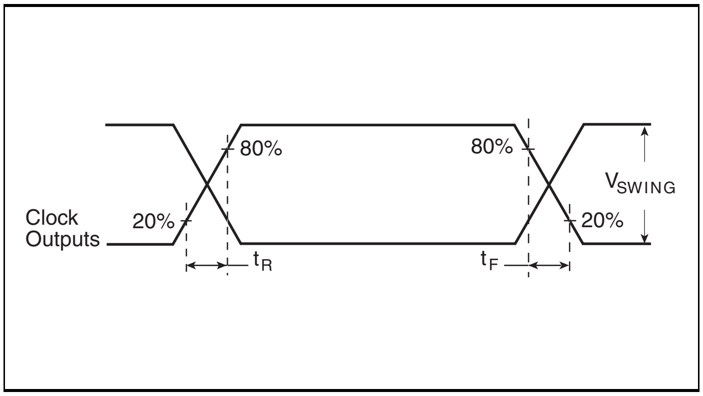
3.3V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843081I-33 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

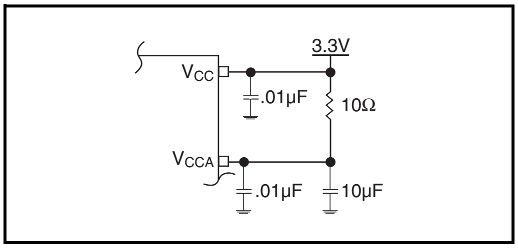


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS843081I-33 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

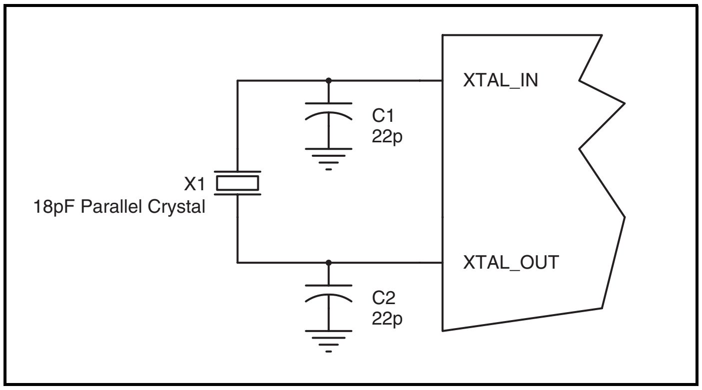


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

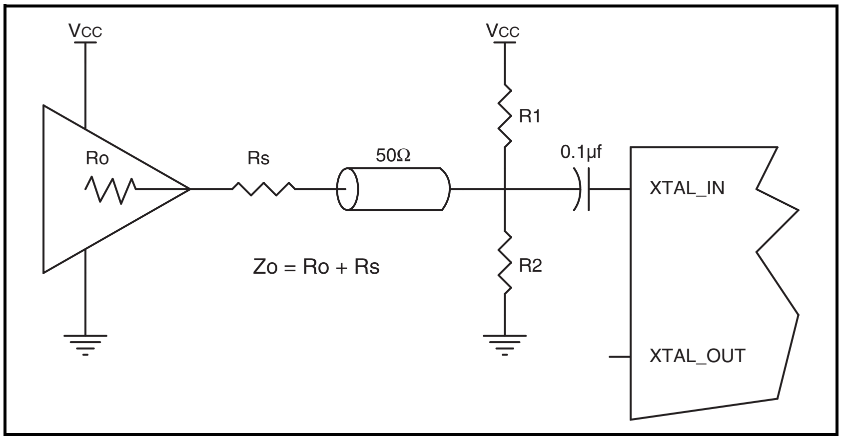


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

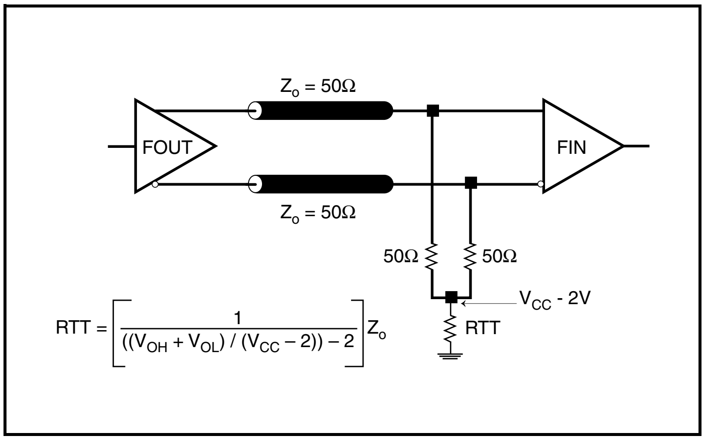


Figure 4A. 3.3V LVPECL Output Termination

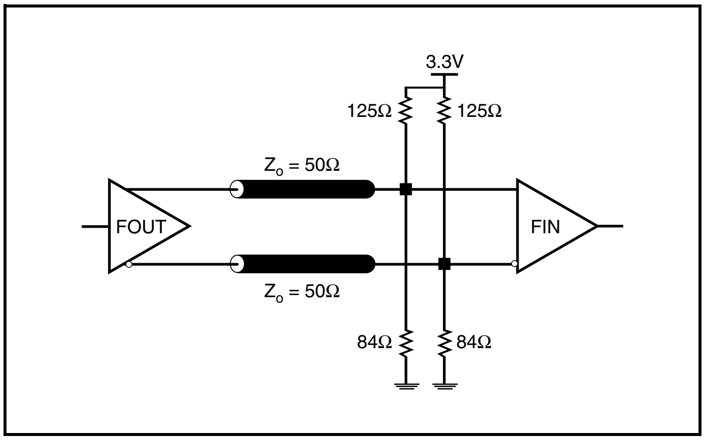


Figure 4B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843081I-33.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843081I-33 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC} = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(\text{core})_{MAX} = V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 80mA =$ **277.2mW**
- Power $(\text{outputs})_{MAX} =$ **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 277.2mW + 30mW = **307.2mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 0 air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.307W * 129.5°C/W = 124.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5	123.5

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

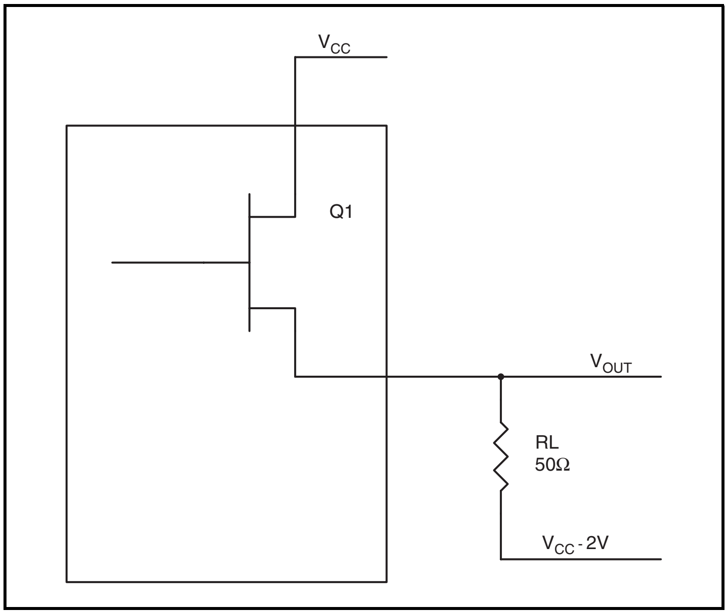


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5	123.5

Transistor Count

The transistor count for ICS843081I-33 is: 1697

Package Outline and Package Dimension

Package Outline - G Suffix for 8 Lead TSSOP

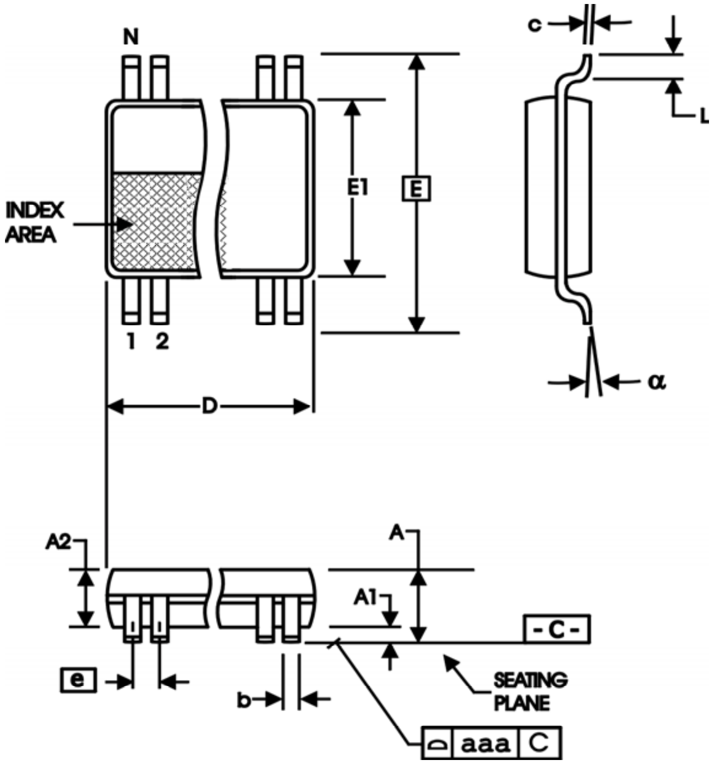


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843081AGI-33	TBD	8 Lead TSSOP	Tube	-40°C to 85°C
843081AGI-33T	TBD	8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
843081AGI-33LF	AI33L	“Lead-Free” 8 Lead TSSOP	Tube	-40°C to 85°C
843081AGI-33LFT	AI33L	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

netcom@idt.com
480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe

IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com