ICS83940-02

LOW SKEW, 1-TO-18
DIFFERENTIAL-TO-LVCMOS/LVTTL FANOUT BUFFER

GENERAL DESCRIPTION

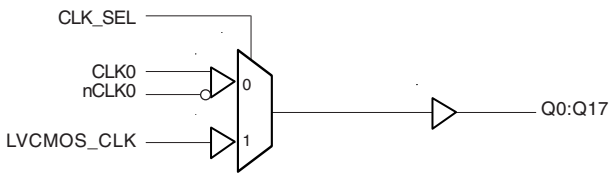
The ICS83940-02 is a low skew, 1-to-18 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The 83940-02 has two selectable clock inputs. The CLK0, nCLK0 pair can accept most standard differential input levels. The single ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 18 to 36 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83940-02 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940 ideal for those clock distribution applications demanding well defined performance and repeatability.

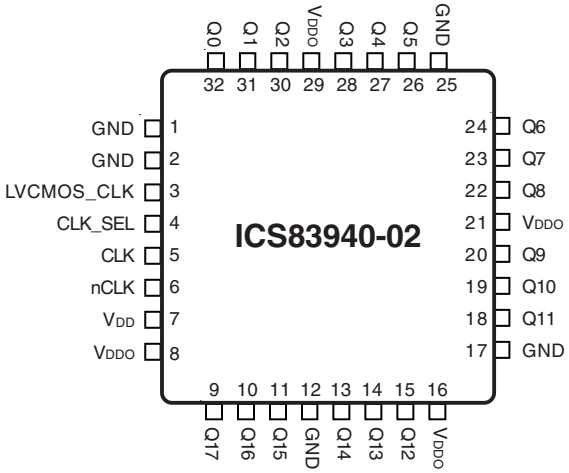
FEATURES

- 18 LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable LVCMOS_Clock or CLK0, nCLK0 input pair
- LVCMOS_CLK supports the following input types: LVCMOS or LVTTL
- CLK0, nCLK0 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 200MHz
- Output skew: 120ps (maximum)
- Part-to-part skew: 850ps (maximum)
- Output supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Pin compatible with the MPC940L in single supply applications

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Pacakge
7mm x 7mm x 1.4mm package body
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Output supply ground.
3	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS/LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK0, nCLK0 inputs when LOW. LVCMOS/LVTTL itnerface levels.
5	CLK0	Input	Pulldown	Non-inverting differential clock input.
6	nCLK0	Input	Pullup	Inverting differential clock input
7	V_{DD}	Power		Core supply pin.
8, 16, 21, 29	V_{DDO}	Power		Output supply pins.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V		12		pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V		18		pF
		V_{DD}, V_{DDO} = 2.625V		18		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK0, nCLK0	LVCMOS_CLK
0	Selected	De-selected
1	De-selected	Selected

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK0	nCLK0	Q0:Q17		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%, V_{DDO} = 3V±5% OR 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				25	mA
I_{DDO}	Output Supply Current				25	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%, V_{DDO} = 3V±5% OR 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		V_{DD} + 0.3	V
		CLK_SEL					
V_{IL}	Input Low Voltage	LVCMOS_CLK		-0.3		1.3	V
		CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	LVCMOS_CLK, CLK_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	LVCMOS_CLK, CLK_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.465V	2.4			V
			V_{DDO} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See 3.3V Output Load Test Circuit Diagram.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%, V_{DDO} = 3V±5% OR 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nCLK0	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLK0	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay; NOTE 1		2		3.5	ns
tp_{HL}	Propagation Delay; NOTE 1		2		3.5	ns
*t*sk(o)	Output Skew; NOTE 2, 4				120	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				850	ps
t_R	Output Rise Time	20% to 80%	350		1050	ns
t_F	Output Fall Time	20% to 80%	350		1050	ns
odc	Output Duty Cycle	f ≤ 133MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%; V_{DDO} = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay; NOTE 1		2		3.5	ns
tp_{HL}	Propagation Delay; NOTE 1		2		3.5	ns
*t*sk(o)	Output Skew; NOTE 2, 4				120	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				850	ps
t_R	Output Rise Time	20% to 80%	350		1050	ns
t_F	Output Fall Time	20% to 80%	350		1050	ns
odc	Output Duty Cycle	f ≤ 133MHz	45		55	%

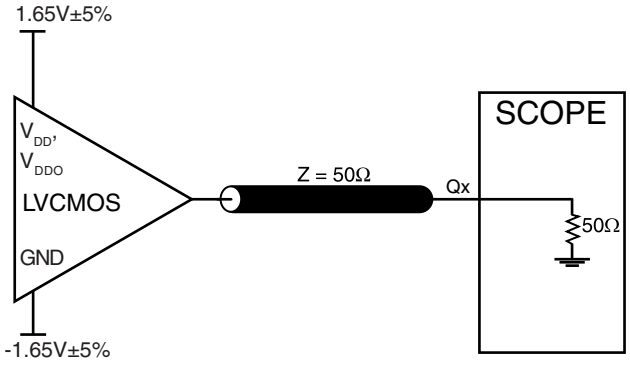
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 2.5V±5%, T_A = 0° TO 70°

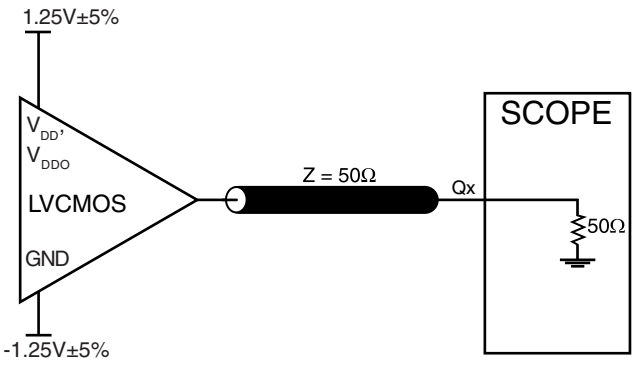
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay; NOTE 1		2		3.5	ns
tp_{HL}	Propagation Delay; NOTE 1		2		3.5	ns
*t*sk(o)	Output Skew; NOTE 2, 4				120	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				850	ps
t_R	Output Rise Time	20% to 80%	350		1050	ns
t_F	Output Fall Time	20% to 80%	350		1050	ns
odc	Output Duty Cycle	f ≤ 133MHz	40		60	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

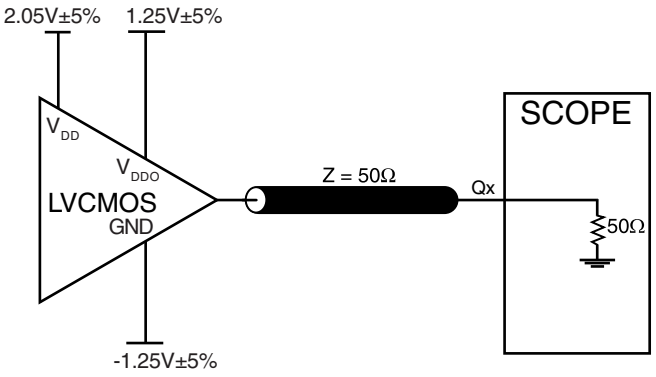
PARAMETER MEASUREMENT INFORMATION



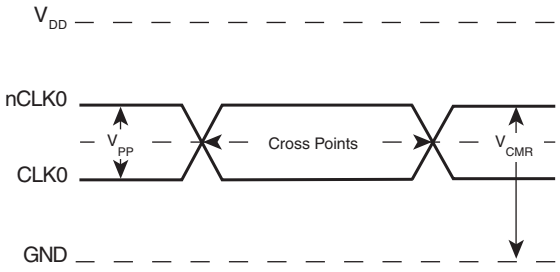
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



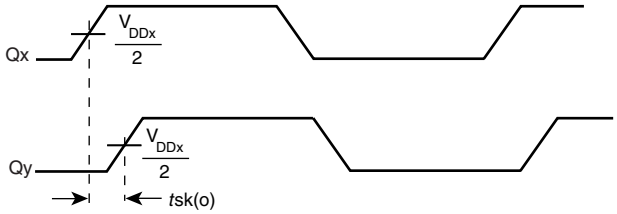
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



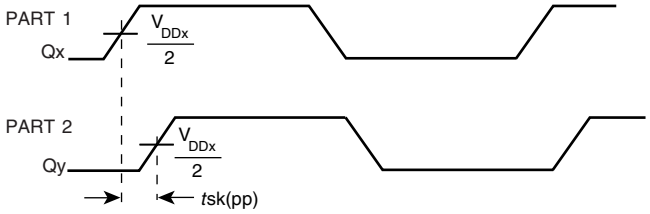
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



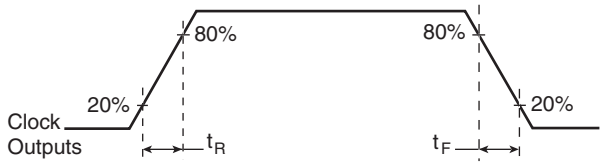
DIFFERENTIAL INPUT LEVEL



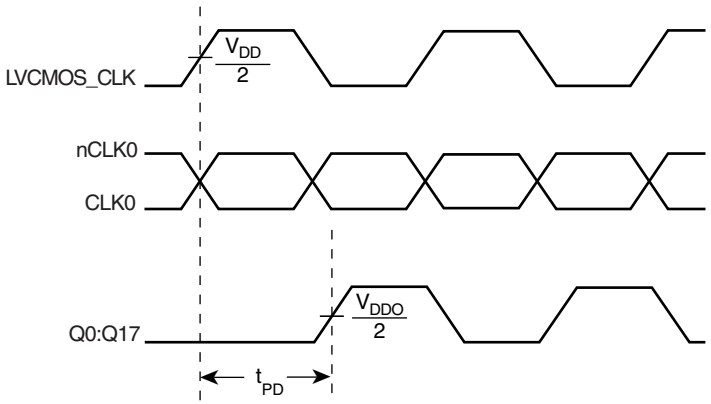
OUTPUT SKEW



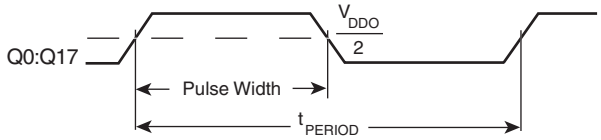
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

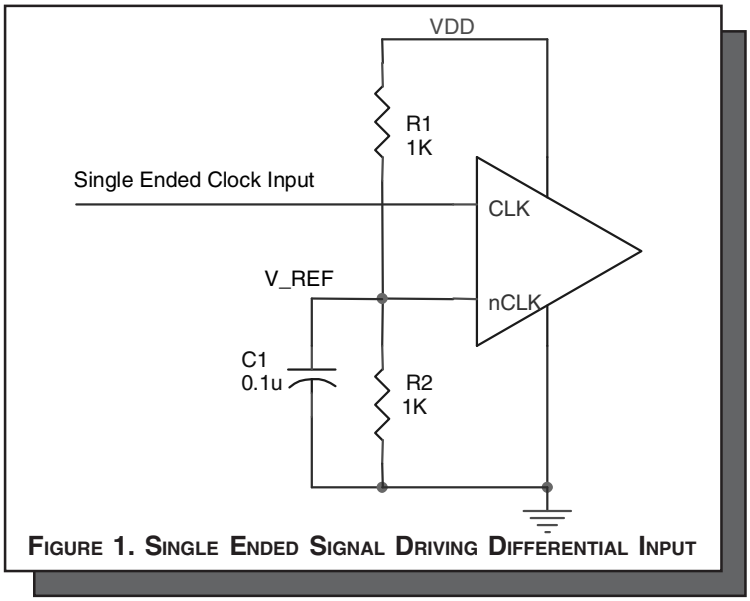


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

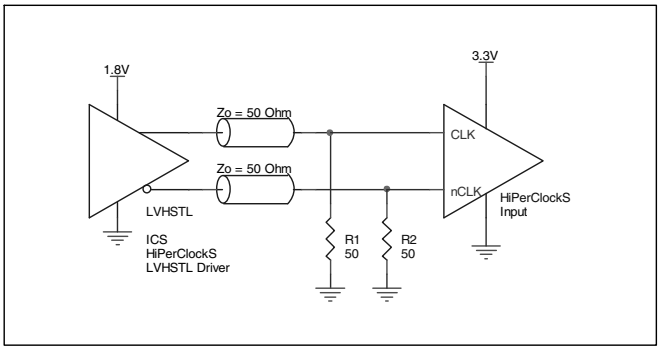


FIGURE 2A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

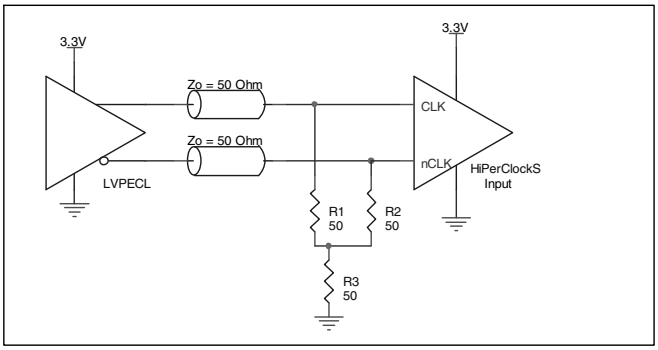


FIGURE 2B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

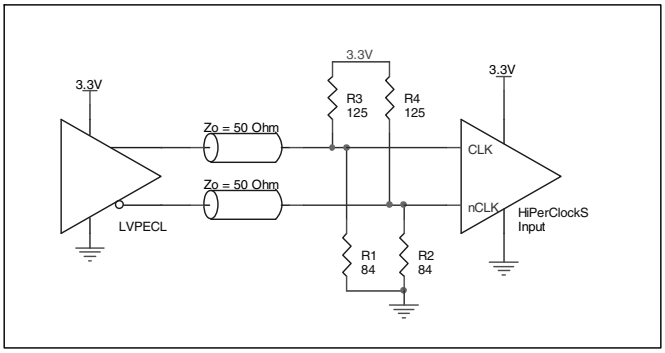


FIGURE 2C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

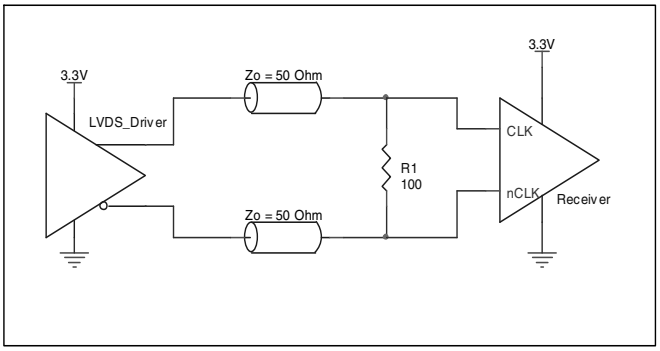


FIGURE 2D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

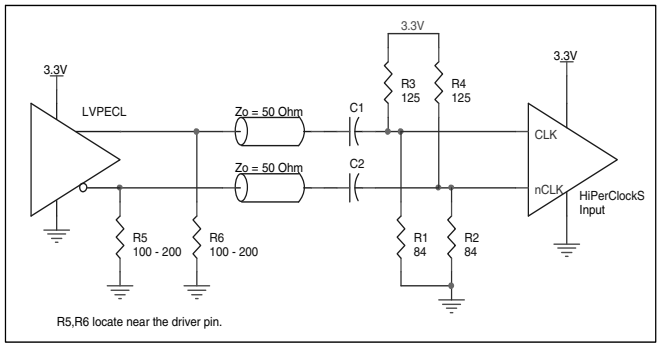


FIGURE 2E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

APPLICATION SCHEMATIC EXAMPLE

Figure 3 shows an example of ICS83940-02 application schematic. In this example, the device is operated at V_{CC}=3.3V. The decoupling capacitor should be located as close as possible to the power pin. The differential input can accept different type of input signals. In this example, this input is driven by a 3.3V LVPECL driver. For the LVCMOS output, a termination example is shown in this schematic. For more termination approaches, please refer to the LVCMOS Termination Application Note.

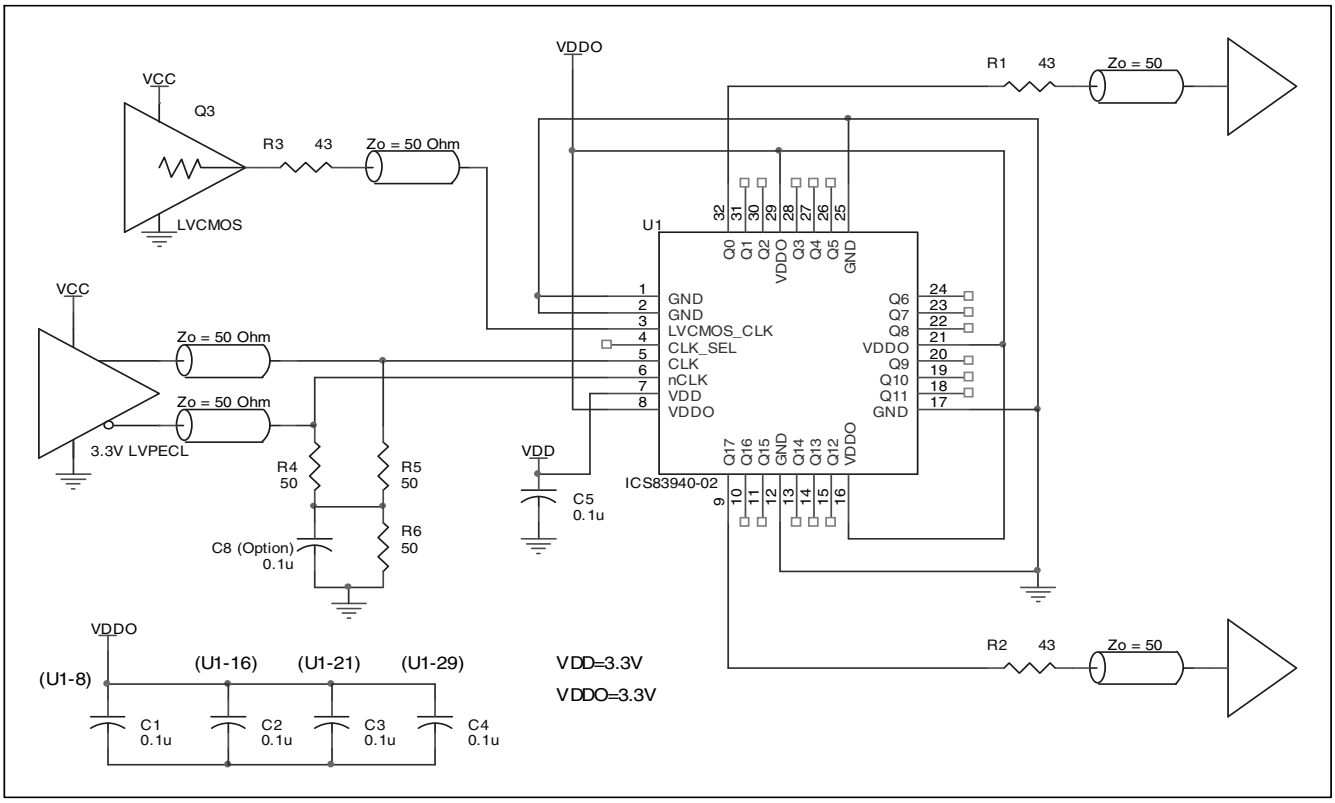


FIGURE 3. APPLICATION SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83940-02 is: 4270

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

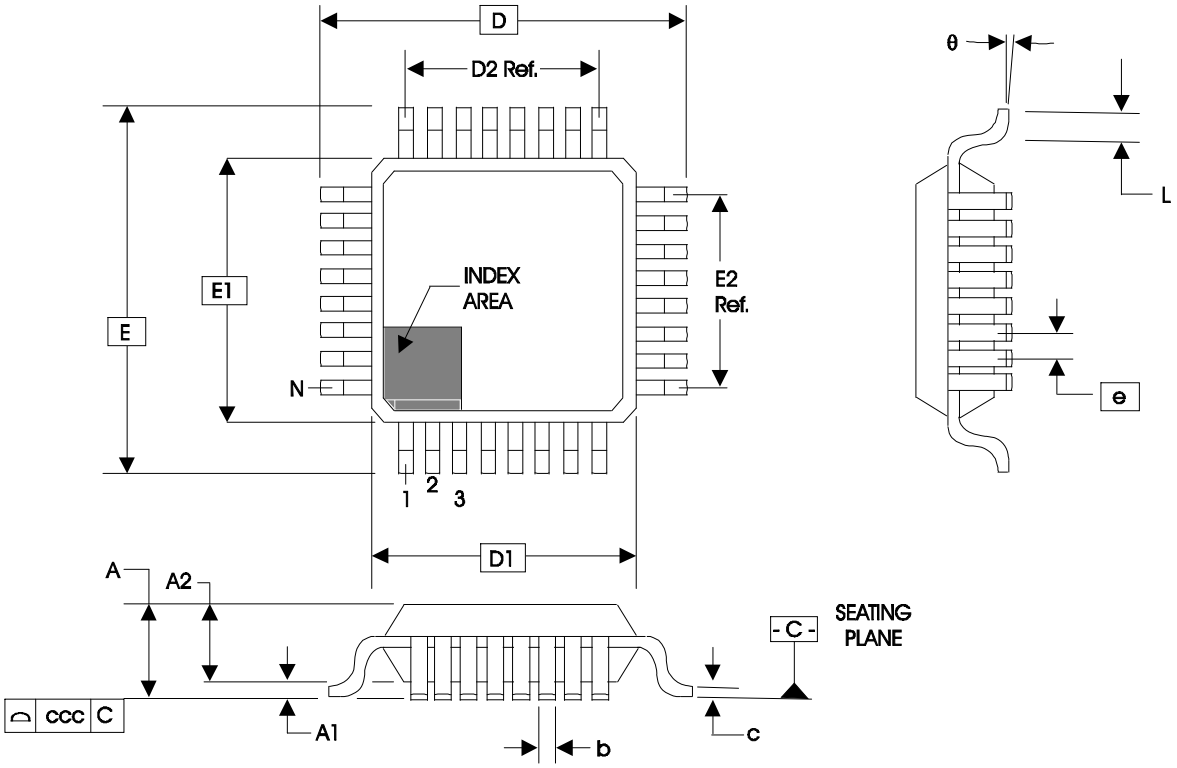


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83940AY-02	ICS83940AY-02	32 Lead LQFP	tray	0°C to 70°C
ICS83940AY-02T	ICS83940AY-02	32 Lead LQFP	1000 Tape and Reel	0°C to 70°C
ICS83940AY-02LF	ICS3940AY02L	32 Lead LQFP Lead Free	tray	0°C to 70°C
ICS83940AY-02LFT	ICS3940AY02L	32 Lead LQFP Lead Free	1000 Tape and Reel	0°C to 70°C

NOTE: Parts that are ordered with an ""LF"" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	13	Ordering Information Table - Added Lead Free Marking and Note	7-30-07