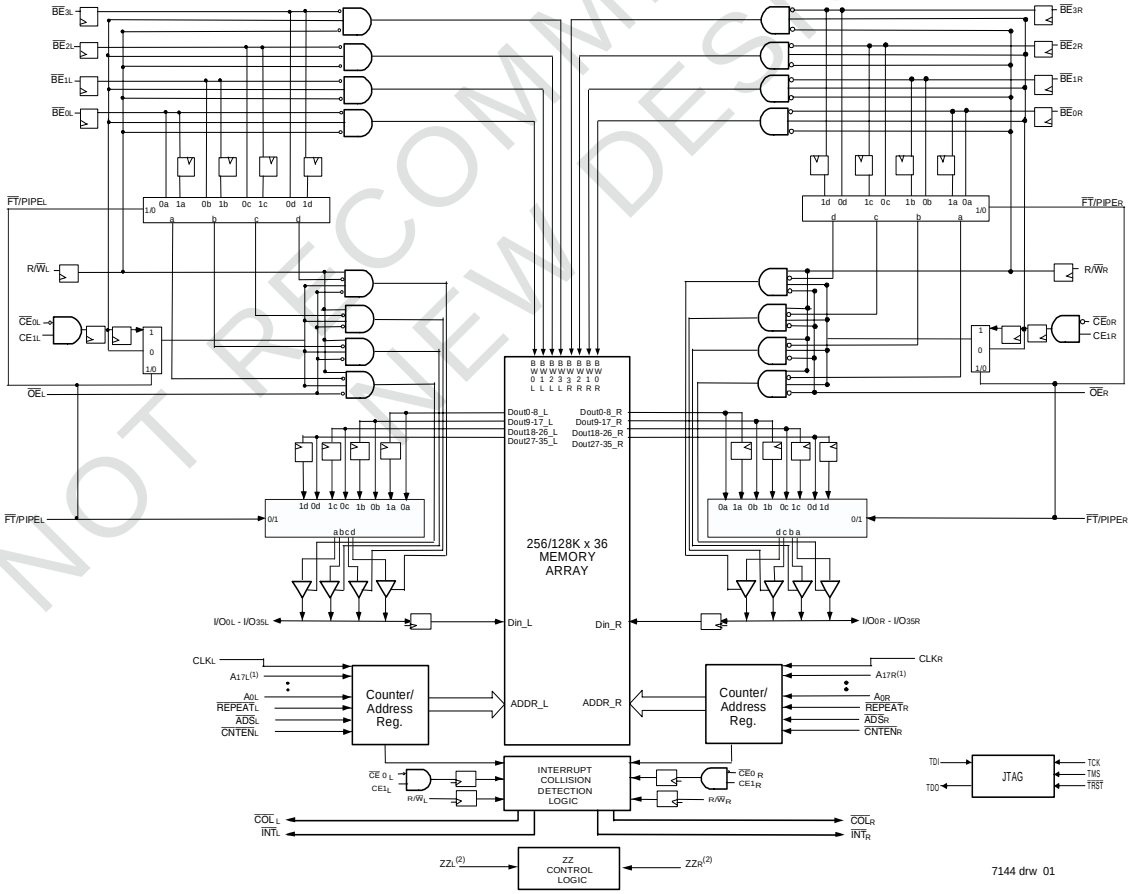
HIGH-SPEED 1.8V 256/128K x 36 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V/2.5V/1.8V INTERFACE

IDT70P3519/99

Features:

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- Low Power
- High-speed data access
  - *Commercial: 3.4 (200MHz)/3.6ns (166MHz)*
  - *Industrial: 3.6ns (166MHz)*
- Selectable Pipelined or Flow-Through output mode
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - *5ns cycle time, 200MHz operation (14Gbps bandwidth)*
  - *Fast 3.4ns clock to data out*
  - *1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz*
  - *Data input, address, byte enable and control registers*
  - *Self-timed write allows fast cycle time*
- Counter enable and repeat features
- Interrupt and Collision Detection Flags
- Separate byte controls for multiplexed bus and bus matching compatibility
- Dual Cycle Deselect (DCD) for Pipelined Output Mode
- 1.8V (±100mV) power supply for core
- LVTTL compatible,1.8V to 3.3V power supply for I/Os and control signals on each port
- Industrial temperature range (-40°C to +85°C) is available at 166MHz
- Available in a 256-pin Ball Grid Array (BGA) and 208-pin fine pitch Ball Grid Array (fpBGA)
- Supports JTAG features compliant with IEEE 1149.1
- Green parts available, see ordering information

Functional Block Diagram



NOTES:

1. Address A_{17} is a NC for the IDT70P3599.

+. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}$x and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

JUNE 2009

Description:

The IDT70P3519/99 is a high-speed 256/128K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70P3519/99 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70P3519/99 can support an operating voltage of 3.3V, 2.5V or 1.8V on one or both ports. The power supply for the core of the device (V_{DD}) is 1.8V.

Pin Configuration (2,3,4)

70P3519/99BC
BC-256(5)

256-Pin BGA
Top View(6)

02/12/08

A1 NC	A2 TDI	A3 NC	A4 A_{17L}(1)	A5 A_{14L}	A6 A_{11L}	A7 A_{8L}	A8 $\overline{BE}_{2L}$	A9 CE_{1L}	A10 $\overline{OE}_L$	A11 $\overline{CNTEN}_L$	A12 A_{5L}	A13 A_{2L}	A14 A_{0L}	A15 NC	A16 NC
B1 I/O_{18L}	B2 NC	B3 TDO	B4 NC	B5 A_{15L}	B6 A_{12L}	B7 A_{9L}	B8 $\overline{BE}_{3L}$	B9 $\overline{CE}_{0L}$	B10 $R/\overline{W}_L$	B11 $\overline{REPEAT}_L$	B12 A_{4L}	B13 A_{1L}	B14 V_{DD}	B15 I/O_{17L}	B16 NC
C1 I/O_{18R}	C2 I/O_{19L}	C3 V_{SS}	C4 A_{16L}	C5 A_{13L}	C6 A_{10L}	C7 A_{7L}	C8 $\overline{BE}_{1L}$	C9 $\overline{BE}_{0L}$	C10 CLK_L	C11 $\overline{ADS}_L$	C12 A_{6L}	C13 A_{3L}	C14 NC	C15 I/O_{17R}	C16 I/O_{16L}
D1 I/O_{20R}	D2 I/O_{19R}	D3 I/O_{20L}	D4 $PIPE/\overline{FT}_L$	D5 V_{DDQL}	D6 V_{DDQL}	D7 V_{DDQR}	D8 V_{DDQR}	D9 V_{DDQL}	D10 V_{DDQL}	D11 V_{DDQR}	D12 V_{DDQR}	D13 V_{DD}	D14 I/O_{15R}	D15 I/O_{15L}	D16 I/O_{16R}
E1 I/O_{21R}	E2 I/O_{21L}	E3 I/O_{22L}	E4 V_{DDQL}	E5 V_{DD}	E6 V_{DD}	E7 $\overline{INT}_L$	E8 V_{SS}	E9 V_{SS}	E10 V_{SS}	E11 V_{DD}	E12 V_{DD}	E13 V_{DDQR}	E14 I/O_{13L}	E15 I/O_{14L}	E16 I/O_{14R}
F1 I/O_{23L}	F2 I/O_{22R}	F3 I/O_{23R}	F4 V_{DDQL}	F5 V_{DD}	F6 NC	F7 $\overline{COL}_L$	F8 V_{SS}	F9 V_{SS}	F10 V_{SS}	F11 V_{SS}	F12 V_{DD}	F13 V_{DDQR}	F14 I/O_{12R}	F15 I/O_{13R}	F16 I/O_{12L}
G1 I/O_{24R}	G2 I/O_{24L}	G3 I/O_{25L}	G4 V_{DDQR}	G5 V_{SS}	G6 V_{SS}	G7 V_{SS}	G8 V_{SS}	G9 V_{SS}	G10 V_{SS}	G11 V_{SS}	G12 V_{SS}	G13 V_{DDQL}	G14 I/O_{10L}	G15 I/O_{11L}	G16 I/O_{11R}
H1 I/O_{26L}	H2 I/O_{25R}	H3 I/O_{26R}	H4 V_{DDQR}	H5 V_{SS}	H6 V_{SS}	H7 V_{SS}	H8 V_{SS}	H9 V_{SS}	H10 V_{SS}	H11 V_{SS}	H12 V_{SS}	H13 V_{DDQL}	H14 I/O_{9R}	H15 IO_{9L}	H16 I/O_{10R}
J1 I/O_{27L}	J2 I/O_{28R}	J3 I/O_{27R}	J4 V_{DDQL}	J5 ZZ_R	J6 V_{SS}	J7 V_{SS}	J8 V_{SS}	J9 V_{SS}	J10 V_{SS}	J11 V_{SS}	J12 ZZ_L	J13 V_{DDQR}	J14 I/O_{8R}	J15 I/O_{7R}	J16 I/O_{8L}
K1 I/O_{29R}	K2 I/O_{29L}	K3 I/O_{28L}	K4 V_{DDQL}	K5 V_{SS}	K6 V_{SS}	K7 V_{SS}	K8 V_{SS}	K9 V_{SS}	K10 V_{SS}	K11 V_{SS}	K12 V_{SS}	K13 V_{DDQR}	K14 I/O_{6R}	K15 I/O_{6L}	K16 I/O_{7L}
L1 I/O_{30L}	L2 I/O_{31R}	L3 I/O_{30R}	L4 V_{DDQR}	L5 V_{DD}	L6 NC	L7 $\overline{COL}_R$	L8 V_{SS}	L9 V_{SS}	L10 V_{SS}	L11 V_{SS}	L12 V_{DD}	L13 V_{DDQL}	L14 I/O_{5L}	L15 I/O_{4R}	L16 I/O_{5R}
M1 I/O_{32R}	M2 I/O_{32L}	M3 I/O_{31L}	M4 V_{DDQR}	M5 V_{DD}	M6 V_{DD}	M7 $\overline{INT}_R$	M8 V_{SS}	M9 V_{SS}	M10 V_{SS}	M11 V_{DD}	M12 V_{DD}	M13 V_{DDQL}	M14 I/O_{3R}	M15 I/O_{3L}	M16 I/O_{4L}
N1 I/O_{33L}	N2 I/O_{34R}	N3 I/O_{33R}	N4 $PIPE/\overline{FT}_R$	N5 V_{DDQR}	N6 V_{DDQR}	N7 V_{DDQL}	N8 V_{DDQL}	N9 V_{DDQR}	N10 V_{DDQR}	N11 V_{DDQL}	N12 V_{DDQL}	N13 V_{DD}	N14 I/O_{2L}	N15 I/O_{1R}	N16 I/O_{2R}
P1 I/O_{35R}	P2 I/O_{34L}	P3 TMS	P4 A_{16R}	P5 A_{13R}	P6 A_{10R}	P7 A_{7R}	P8 $\overline{BE}_{1R}$	P9 $\overline{BE}_{0R}$	P10 CLK_R	P11 $\overline{ADS}_R$	P12 A_{6R}	P13 A_{3R}	P14 I/O_{0L}	P15 I/O_{0R}	P16 I/O_{1L}
R1 I/O_{35L}	R2 NC	R3 $\overline{TRST}$	R4 NC	R5 A_{15R}	R6 A_{12R}	R7 A_{9R}	R8 $\overline{BE}_{3R}$	R9 $\overline{CE}_{0R}$	R10 $R/\overline{W}_R$	R11 $\overline{REPEAT}_R$	R12 A_{4R}	R13 A_{1R}	R14 NC	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 A_{17R}(1)	T5 A_{14R}	T6 A_{11R}	T7 A_{8R}	T8 $\overline{BE}_{2R}$	T9 CE_{1R}	T10 $\overline{OE}_R$	T11 $\overline{CNTEN}_R$	T12 A_{5R}	T13 A_{2R}	T14 A_{0R}	T15 NC	T16 NC

7144 drw 02d

NOTES:
1. Pin is a NC for IDT70P3599.
2. All V_{DD} pins must be connected to 1.8V power supply.
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration [2,3,4] (con't.)

02/12/08

A1 I/O_{19L}	A2 I/O_{18L}	A3 V_{SS}	A4 TDO	A5 $\overline{COL}_L$	A6 A_{16L}	A7 A_{12L}	A8 A_{8L}	A9 $\overline{BE}_{1L}$	A10 V_{DD}	A11 CLK_L	A12 $\overline{CNTEN}_L$	A13 A_{4L}	A14 A_{0L}	A15 NC	A16 I/O_{17L}	A17 V_{SS}
B1 I/O_{20R}	B2 V_{SS}	B3 I/O_{18R}	B4 TDI	B5 A_{17L}(1)	B6 A_{13L}	B7 A_{9L}	B8 $\overline{BE}_{2L}$	B9 $\overline{CE}_{0L}$	B10 V_{SS}	B11 $\overline{ADS}_L$	B12 A_{5L}	B13 A_{1L}	B14 NC	B15 V_{DDQR}	B16 I/O_{16L}	B17 I/O_{15R}
C1 V_{DDQL}	C2 I/O_{19R}	C3 V_{DDQR}	C4 $PL/\overline{FT}_L$	C5 $\overline{INT}_L$	C6 A_{14L}	C7 A_{10L}	C8 $\overline{BE}_{3L}$	C9 CE_{1L}	C10 V_{SS}	C11 $R/\overline{W}_L$	C12 A_{6L}	C13 A_{2L}	C14 V_{DD}	C15 I/O_{16R}	C16 I/O_{15L}	C17 V_{SS}
D1 I/O_{22L}	D2 V_{SS}	D3 I/O_{21L}	D4 I/O_{20L}	D5 A_{15L}	D6 A_{11L}	D7 A_{7L}	D8 $\overline{BE}_{0L}$	D9 V_{DD}	D10 $\overline{OE}_L$	D11 $\overline{REPEAT}_L$	D12 A_{3L}	D13 V_{DD}	D14 I/O_{17R}	D15 V_{DDQL}	D16 I/O_{14L}	D17 I/O_{14R}
E1 I/O_{23L}	E2 I/O_{22R}	E3 V_{DDQR}	E4 I/O_{21R}										E14 I/O_{12L}	E15 I/O_{13R}	E16 V_{SS}	E17 I/O_{13L}
F1 V_{DDQL}	F2 I/O_{23R}	F3 I/O_{24L}	F4 V_{SS}										F14 V_{SS}	F15 I/O_{12R}	F16 I/O_{11L}	F17 V_{DDQR}
G1 I/O_{26L}	G2 V_{SS}	G3 I/O_{25L}	G4 I/O_{24R}										G14 I/O_{9L}	G15 V_{DDQL}	G16 I/O_{10L}	G17 I/O_{11R}
H1 V_{DD}	H2 I/O_{26R}	H3 V_{DDQR}	H4 I/O_{25R}										H14 V_{DD}	H15 I/O_{9R}	H16 V_{SS}	H17 I/O_{10R}
J1 V_{DDQL}	J2 V_{DD}	J3 V_{SS}	J4 ZZ_R										J14 ZZ_L	J15 V_{DD}	J16 V_{SS}	J17 V_{DDQR}
K1 I/O_{28R}	K2 V_{SS}	K3 I/O_{27R}	K4 V_{SS}										K14 I/O_{7R}	K15 V_{DDQL}	K16 I/O_{8R}	K17 V_{SS}
L1 I/O_{29R}	L2 I/O_{28L}	L3 V_{DDQR}	L4 I/O_{27L}										L14 I/O_{6R}	L15 I/O_{7L}	L16 V_{SS}	L17 I/O_{8L}
M1 V_{DDQL}	M2 I/O_{29L}	M3 I/O_{30R}	M4 V_{SS}										M14 V_{SS}	M15 I/O_{6L}	M16 I/O_{5R}	M17 V_{DDQR}
N1 I/O_{31L}	N2 V_{SS}	N3 I/O_{31R}	N4 I/O_{30L}										N14 I/O_{3R}	N15 V_{DDQL}	N16 I/O_{4R}	N17 I/O_{5L}
P1 I/O_{32R}	P2 I/O_{32L}	P3 V_{DDQR}	P4 I/O_{35R}	P5 $\overline{TRST}$	P6 A_{16R}	P7 A_{12R}	P8 A_{8R}	P9 $\overline{BE}_{1R}$	P10 V_{DD}	P11 CLK_R	P12 $\overline{CNTEN}_R$	P13 A_{4R}	P14 I/O_{2L}	P15 I/O_{3L}	P16 V_{SS}	P17 I/O_{4L}
R1 V_{SS}	R2 I/O_{33L}	R3 I/O_{34R}	R4 TCK	R5 A_{17R}(1)	R6 A_{13R}	R7 A_{9R}	R8 $\overline{BE}_{2R}$	R9 $\overline{CE}_{0R}$	R10 V_{SS}	R11 $\overline{ADS}_R$	R12 A_{5R}	R13 A_{1R}	R14 NC	R15 V_{DDQL}	R16 I/O_{1R}	R17 V_{DDQR}
T1 I/O_{33R}	T2 I/O_{34L}	T3 V_{DDQL}	T4 TMS	T5 $\overline{INT}_R$	T6 A_{14R}	T7 A_{10R}	T8 $\overline{BE}_{3R}$	T9 CE_{1R}	T10 V_{SS}	T11 $R/\overline{W}_R$	T12 A_{6R}	T13 A_{2R}	T14 V_{SS}	T15 I/O_{0R}	T16 V_{SS}	T17 I/O_{2R}
U1 V_{SS}	U2 I/O_{35L}	U3 $PL/\overline{FT}_R$	U4 $\overline{COL}_R$	U5 A_{15R}	U6 A_{11R}	U7 A_{7R}	U8 $\overline{BE}_{0R}$	U9 V_{DD}	U10 $\overline{OE}_R$	U11 $\overline{REPEAT}_R$	U12 A_{3R}	U13 A_{0R}	U14 V_{DD}	U15 NC	U16 I/O_{0L}	U17 I/O_{1L}

70P3519/99BF
BF-208(5)

208-Pin fpBGA
Top View(6)

7144 drw 02c

NOTES:
1. Pin is a NC for IDT70P3599.
2. All V_{DD} pins must be connected to 1.8V power supply.
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables (Input)[5]
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A_{0L} - A_{17L}[4]	A_{0R} - A_{17R}[4]	Address (Input)
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
CLK_L	CLK_R	Clock (Input)
PL/$\overline{FT}_L$	PL/$\overline{FT}_R$	Pipeline/Flow-Through (Input)
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable (Input)
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable (Input)
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat[2]
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes) (Input)[5]
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V, 2.5V or 1.8V)[1] (Input)
ZZ_L	ZZ_R	Sleep Mode pin[3] (Input)
V_{DD}		Power (1.8V)[1] (Input)
V_{SS}		Ground (0V) (Input)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz) (Input)
TMS		Test Mode Select (Input)
$\overline{TRST}$		Reset (Initialize TAP Controller) (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
$\overline{COL}_L$	$\overline{COL}_R$	Collision Alert (Output)

7144 tbl 01

NOTES:
1. V_{DD} and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
2. When $\overline{REPEAT}_X$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_X$.
3. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/$\overline{FT}$x and the sleep mode pins themselves (ZZx) are not affected during sleep mode.
4. Address A_{17x} is a NC for the IDT70P3599.
5. Chip Enables and Byte Enables are double buffered when PL/$\overline{FT}$ = V_{IH}, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control(1,2,3,4)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	R/$\overline{W}$	ZZ	Byte 3 I/O_{27-35}	Byte 2 I/O_{18-26}	Byte 1 I/O_{9-17}	Byte 0 I/O_{0-8}	MODE
X	↑	H	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	X	L	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	↑	L	H	H	H	H	H	X	L	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	L	High-Z	High-Z	High-Z	D_{IN}	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	L	High-Z	High-Z	D_{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	L	High-Z	D_{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	L	D_{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	L	High-Z	High-Z	D_{IN}	D_{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	L	D_{IN}	D_{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	L	High-Z	High-Z	High-Z	D_{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	L	High-Z	High-Z	D_{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	L	High-Z	D_{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	L	D_{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	L	High-Z	High-Z	D_{OUT}	D_{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	L	D_{OUT}	D_{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	L	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read All Bytes
H	↑	X	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Outputs Disabled
X	X	X	X	X	X	X	X	X	H	High-Z	High-Z	High-Z	High-Z	Sleep Mode

7144 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X.
3. $\overline{OE}$ and ZZ are asynchronous input signals.
4. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address Counter Control(1,2)

Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$(4)	$\overline{CNTEN}$(5)	$\overline{REPEAT}$(4,6)	I/O(3)	MODE
An	X	An	↑	L	X	H	$D_{I/O}$ (n)	External Address Used
X	An	An + 1	↑	H	L	H	$D_{I/O}$(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	$D_{I/O}$(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	An	↑	X	X	L	$D_{I/O}$(n)	Counter Set to last valid $\overline{ADS}$ load

7144 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. Read and write operations are controlled by the appropriate setting of R/$\overline{W}$, $\overline{CE}_0$, CE_1, $\overline{BE}$n and $\overline{OE}$.
3. Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{BE}$n
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1, $\overline{BE}$n.
6. When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.

Recommended Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	VDD
Commercial	0°C to +70°C	0V	1.8V ± 100mV
Industrial	-40°C to +85°C	0V	1.8V ± 100mV

7144 tbl 04

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions with VDDQ at 1.8V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	1.7	1.8	1.9	V
VDDQ	I/O Supply Voltage	1.7	1.8	1.9	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	0.7 VDDQ	—	VDDQ + 100mV(2)	V
VIH	Input High Voltage – JTAG(3)	0.7 VDDQL	—	VDDQL + 100mV(2)	V
VIH	Input High Voltage - ZZ, PIPE/$\overline{FT}$	VDDQ - 0.2V	—	VDDQ + 100mV(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.3 VDDQ	V
VIL	Input Low Voltage - ZZ, PIPE/$\overline{FT}$	-0.3(1)	—	0.2	V

7144 tbl 05c

NOTES:
1. VIL (min.) = -0.75V for pulse width less than tCYC/2, or 5ns, whichever is less.
2. VIH (max.) = VDDQ + 0.75V for pulse width less than tCYC/2 or 5ns, whichever is less.
3. JTAG is driven by the left port VDDQL.

Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	1.7	1.8	1.9	V
VDDQ	I/O Supply Voltage	2.4	2.5	2.6	V
VSS	Ground	0	0	0	V
VIH	Input High Volltage	1.7	—	VDDQ + 100mV(2)	V
VIH	Input High Voltage – JTAG(3)	1.7	—	VDDQL + 100mV(2)	V
VIH	Input High Voltage - ZZ, PIPE/$\overline{FT}$	VDDQ - 0.2V	—	VDDQ + 100mV(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.7	V
VIL	Input Low Voltage - ZZ, PIPE/$\overline{FT}$	-0.3(1)	—	0.2	V

7144 tbl 05a

NOTES:
1. VIL (min.) = -1.0V for pulse width less than tCYC/2 or 5ns, whichever is less.
2. VIH (max.) = VDDQ + 1.0V for pulse width less than tCYC/2 or 5ns, whichever is less.
3. JTAG is driven by the left port VDDQL.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage	3.15	3.3	3.45	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DDQ} + 150mV[2]	V
V_{IH}	Input High Voltage – JTAG[3]	2.0	—	V_{DDQL} + 150mV[2]	V
V_{IH}	Input High Voltage - ZZ, PIPE/$\overline{FT}$	V_{DDQ} - 0.2V	—	V_{DDQ} + 150mV[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V
V_{IL}	Input Low Voltage - ZZ, PIPE/$\overline{FT}$	-0.3[1]	—	0.2	V

7144 tbl 05b

NOTES:
1. V_{IL} (min.) = -1.0V for pulse width less than t_{CYC}/2, or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than t_{CYC}/2 or 5ns, whichever is less.
3. JTAG is driven by the left port V_{DDQL}.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM} (V_{DD})	V_{DD} Terminal Voltage with Respect to GND	- 0.5 to + 2.5	V
V_{TERM}[2] (V_{DDQ})	V_{DDQ} Terminal Voltage with Respect to GND	- 0.3 to + 4.2	V
V_{TERM}[2] (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	- 0.3 to min. {V_{DDQ} + 0.3, 4.2}[4]	V
T_{BIAS}[3]	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}(For V_{DDQ} = 3.3V)	DC Output Current	50	mA
I_{OUT}(For V_{DDQ} = 2.5V)	DC Output Current	40	mA
I_{OUT}(For V_{DDQ} = 1.8V)	DC Output Current	35	mA

7144 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.
4. V_{TERM} (Inputs and I/O's) -0.3 to min {V_{DDQ} + 0.3, 4.2} means that the range is -0.3V to either V_{DDQ} +0.3V or 4.2V whichever is less.

Capacitance[1]

(T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10.5	pF

7144 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(V_{DD} = 1.8V ± 100mV)

Symbol	Parameter	Test Conditions	70P3519/99S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LI}\|$	JTAG & ZZ Input Leakage Current[1]	V_{DDQL} = Max., V_{IN} = 0V to V_{DDQL}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current[2]	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V
V_{OL} (1.8V)	Output Low Voltage	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (1.8V)	Output High Voltage	I_{OH} = -2mA, V_{DDQ} = Min.	V_{DDQ} -0.40	—	V

7144 tbl 08

NOTES:
1. Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
2. Outputs tested in tri-state mode.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3] (V_{DD} = 1.8V ± 100mV)

Symbol	Parameter	Test Condition	Version		70P3519/99 S200 Com'l Only		70P3519/99 S166 Com'l & Ind		Unit
					Typ.[4]	Max.	Typ.[4]	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	226	325	190	285	mA
			IND	S	—	—	190	325	
I_{SB1}[6]	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	S	120	195	102	170	mA
			IND	S	—	—	102	205	
I_{SB2}[6]	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	S	176	265	148	230	mA
			IND	S	—	—	148	270	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ}$ - 0.2V, $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	S	15	45	15	45	mA
			IND	S	—	—	15	60	
I_{SB4}[6]	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" $\leq$ 0.2V and $\overline{CE}$"B" $\geq V_{DDQ}$ - 0.2V[5] $V_{IN} \geq V_{DDQ}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port, Outputs Disabled, f = f_{MAX}[1]	COM'L	S	176	265	148	230	mA
			IND	S	—	—	148	270	
I_{ZZ}	Sleep Mode Current (Both Ports - TTL Level Inputs)	ZZ_L = ZZ_R = V_{IH} f=f_{MAX}[1]	COM'L	S	15	45	15	45	mA
			IND	S	—	—	15	60	

7144 tbl 09

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS".
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 1.8V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 15mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and $CE_{1X} \geq V_{DDQ}$ - 0.2V
   $\overline{CE}_X \geq V_{DDQ}$ - 0.2V means $\overline{CE}_{0X} \geq V_{DDQ}$ - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.
6. I_{SB1}, I_{SB2} and I_{SB4} will all reach full standby levels (I_{SB3}) on the appropriate port(s) if ZZ_L and/or ZZ_R = V_{IH}.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V/1.8V)

Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V/GND to 1.7V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V/GND to 1.7V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V/0.85V
Output Reference Levels	1.5V/1.25V/0.85V
Output Load	Figure 1

7144 tbl 10

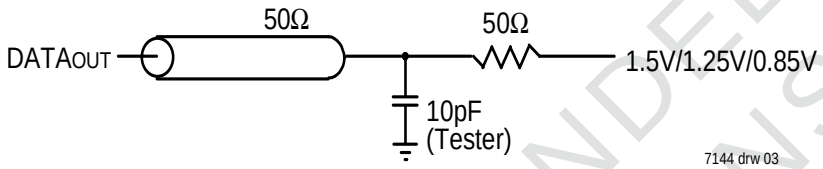
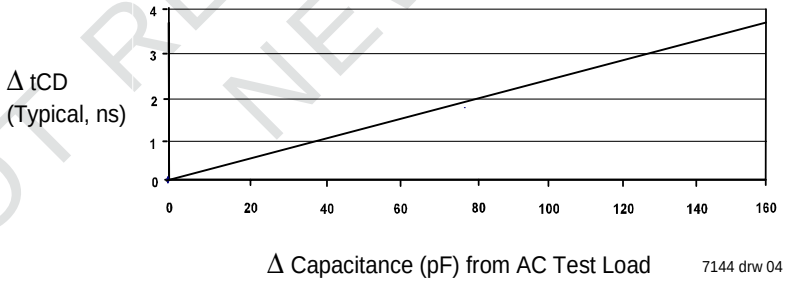


Figure 1. AC Output Test load.



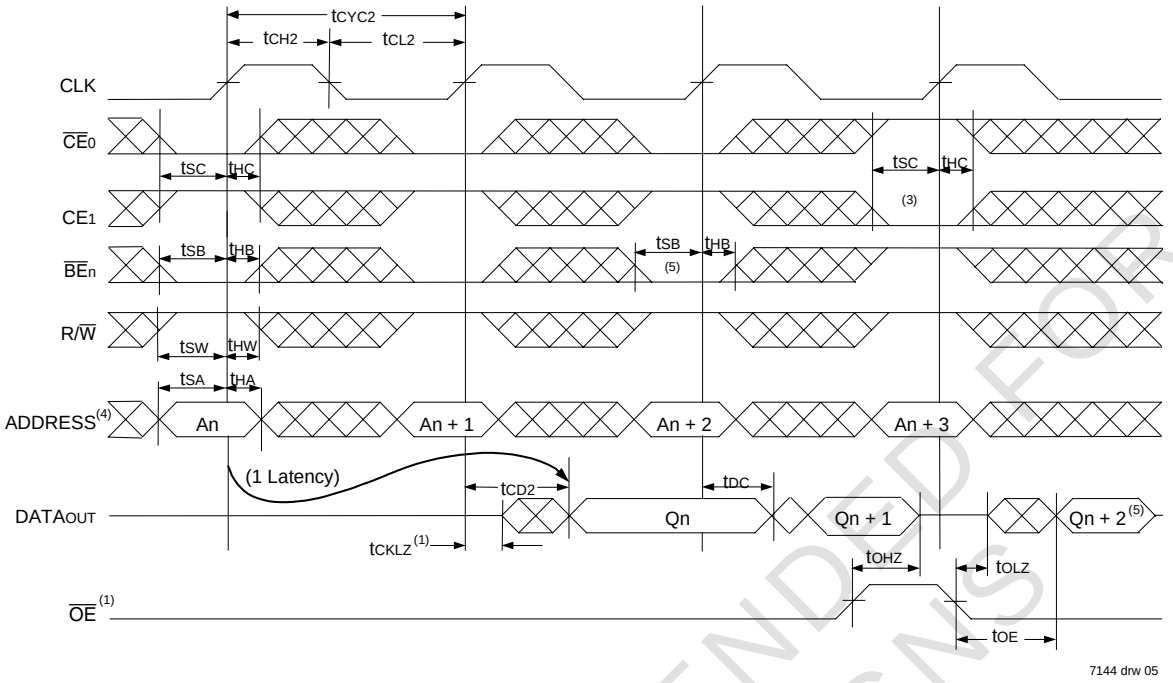
AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[2,3] (V_{DD} = 1.8V ± 100mV, T_A = 0°C to +70°C)

		70P3519/99 S200 Com'l Only		70P3519/99 S166 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{CYC1}	Clock Cycle Time (Flow-Through)[1]	15	—	20	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[1]	5	—	6	—	ns
t_{CH1}	Clock High Time (Flow-Through)[1]	6	—	8	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[1]	6	—	8	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	2	—	2.4	—	ns
t_{CL2}	Clock Low Time (Pipelined)[1]	2	—	2.4	—	ns
t_{SA}	Address Setup Time	1.5	—	1.7	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	ns
t_{SC}	Chip Enable Setup Time	1.5	—	1.7	—	ns
t_{HC}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{SB}	Byte Enable Setup Time	1.5	—	1.7	—	ns
t_{HB}	Byte Enable Hold Time	0.5	—	0.5	—	ns
t_{SW}	R/W Setup Time	1.5	—	1.7	—	ns
t_{HW}	R/W Hold Time	0.5	—	0.5	—	ns
t_{SD}	Input Data Setup Time	1.5	—	1.7	—	ns
t_{HD}	Input Data Hold Time	0.5	—	0.5	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	1.5	—	1.7	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	1.5	—	1.7	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	ns
t_{SRPT}	$\overline{REPEAT}$ Setup Time	1.5	—	1.7	—	ns
t_{HRPT}	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	ns
t_{OE}	Output Enable to Data Valid	—	4.4	—	4.4	ns
t_{OLZ}[4]	Output Enable to Output Low-Z	1	—	1	—	ns
t_{OHZ}[4]	Output Enable to Output High-Z	1	3.4	1	3.6	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[1]	—	10	—	12	ns
t_{CD2}	Clock to Data Valid (Pipelined)[1]	—	3.4	—	3.6	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	ns
t_{CKHZ}[4]	Clock High to Output High-Z	1	3.4	1	3.6	ns
t_{CKLZ}[4]	Clock High to Output Low-Z	1	—	1	—	ns
t_{INS}	Interrupt Flag Set Time	—	7	—	7	ns
t_{INR}	Interrupt Flag Reset Time	—	7	—	7	ns
t_{COLS}	Collision Flag Set Time	—	3.4	—	3.6	ns
t_{COLR}	Collision Flag Reset Time	—	3.4	—	3.6	ns
t_{ZZSC}	Sleep Mode Set Cycles	2	—	2	—	cycles
t_{ZZRC}	Sleep Mode Recovery Cycles	3	—	3	—	cycles
Port-to-Port Delay						
t_{CO}	Clock-to-Clock Offset	4	—	5	—	ns
t_{OFS}	Clock-to-Clock Offset for Collision Detection	Please refer to Collision Detection Timing Table on Page 21				

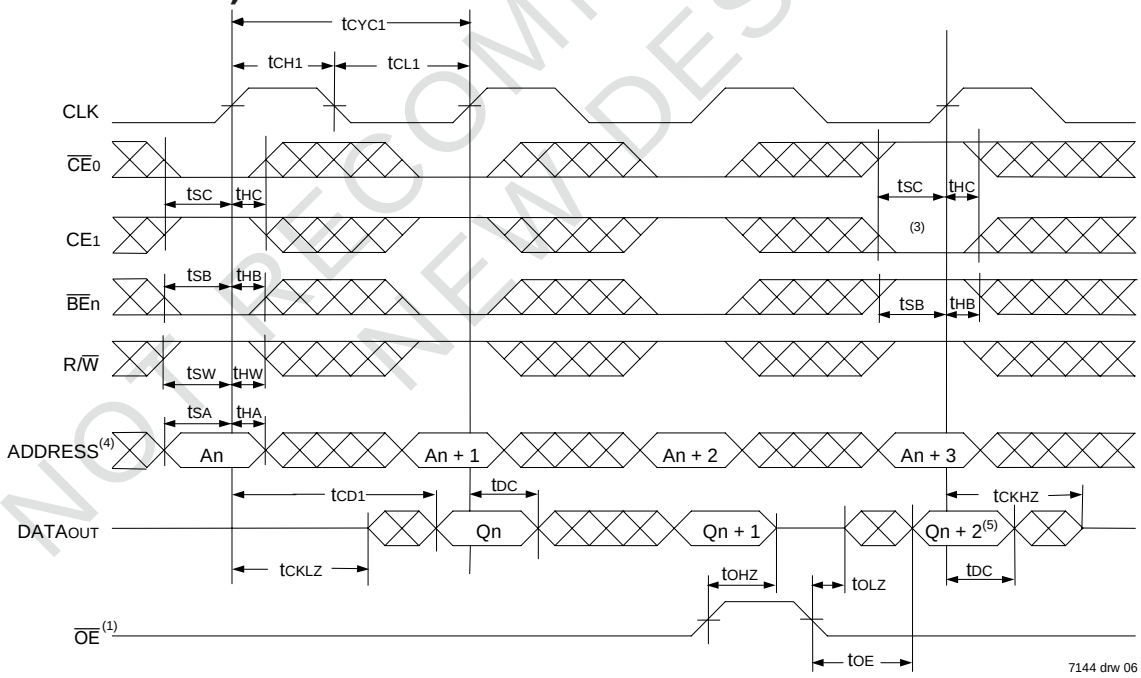
7144 tbl 11

NOTES:
1. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when PL/$\overline{FT}$x = V_{DD} (1.8V). Flow-through parameters (t_{CYC1}, t_{CD1}) apply when PL/$\overline{FT}$ = V_{SS} (0V) for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and PL/$\overline{FT}$. PL/$\overline{FT}$ should be treated as DC signals, i.e. steady state during operation.
3. These values are valid for any level of V_{DDQ} (3.3V/2.5V/1.8V).
4. Guaranteed by design (not production tested).

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE'X' = V_{IH})(1,2)

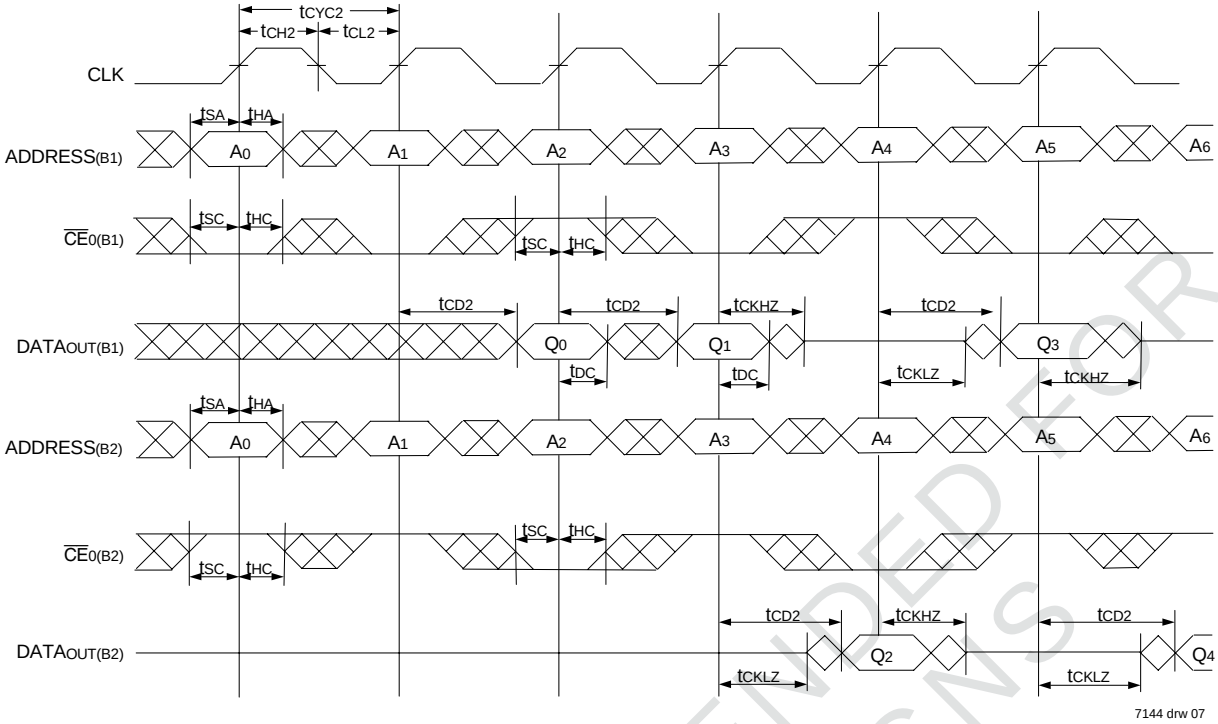


Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}$/PIPE"X" = V_{IL})(1,2,6)

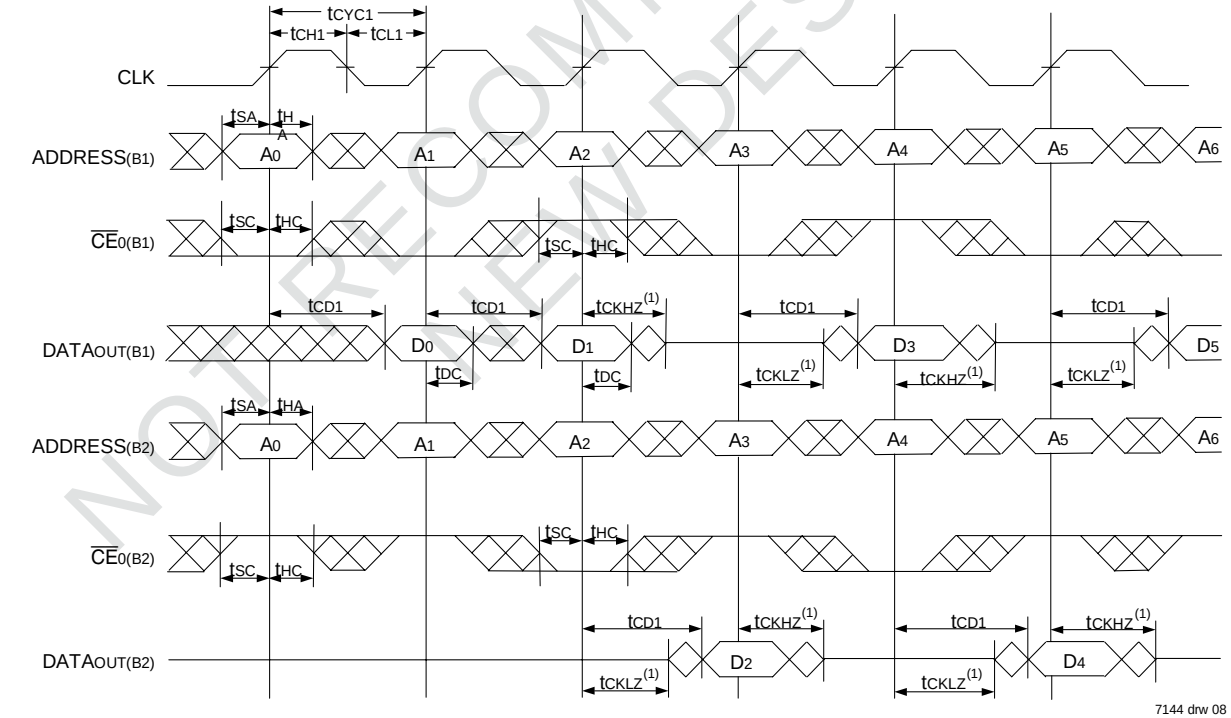


NOTES:
1. $\overline{OE}$ is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{REPEAT}$ = V_{IH}.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH}, CE_1 = V_{IL}, $\overline{BE}_n$ = V_{IH} following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{BE}_n$ was HIGH, then the appropriate Byte of $DATA_{OUT}$ for Qn + 2 would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read(1,2)



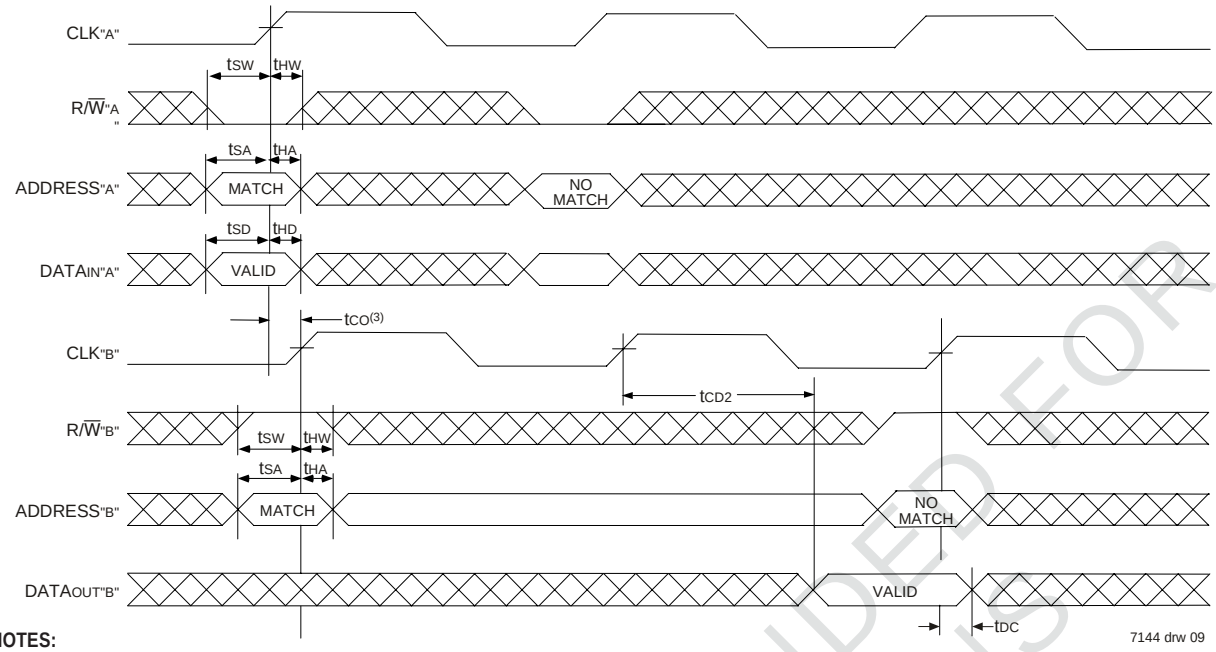
Timing Waveform of a Multi-Device Flow-Through Read(1,2)



NOTES:

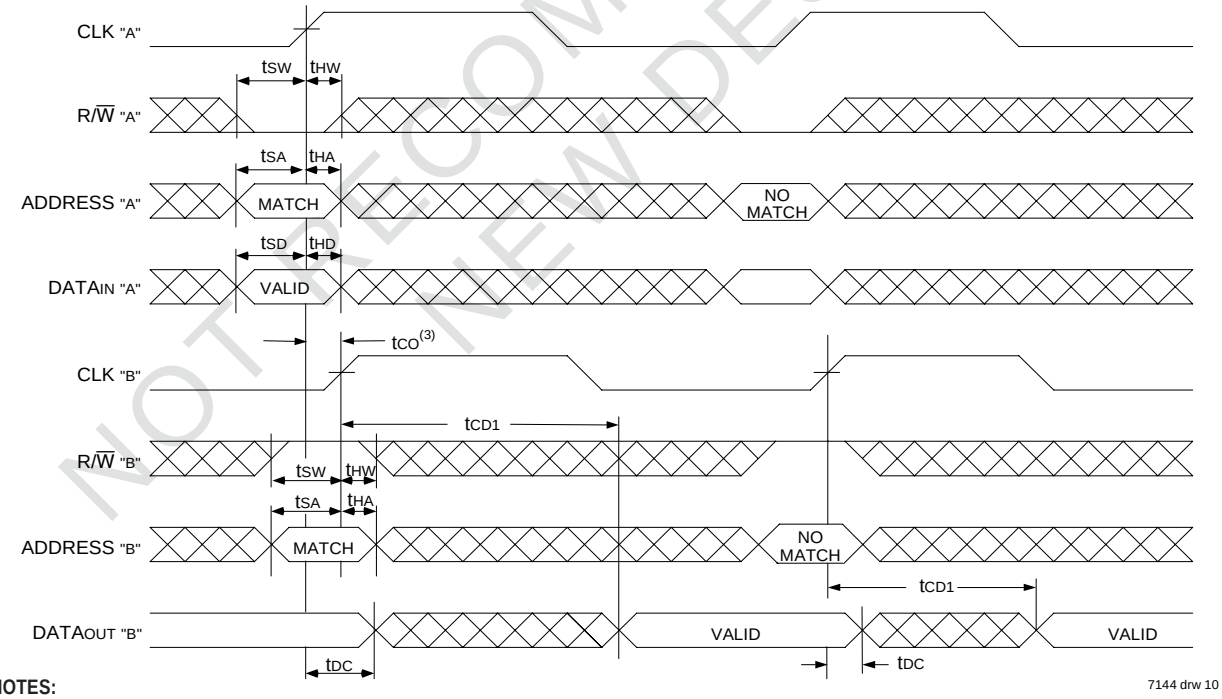
1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70P3519/99 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{BE}_n$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.

Timing Waveform of Left Port Write to Pipelined Right Port Read(1,2,4)



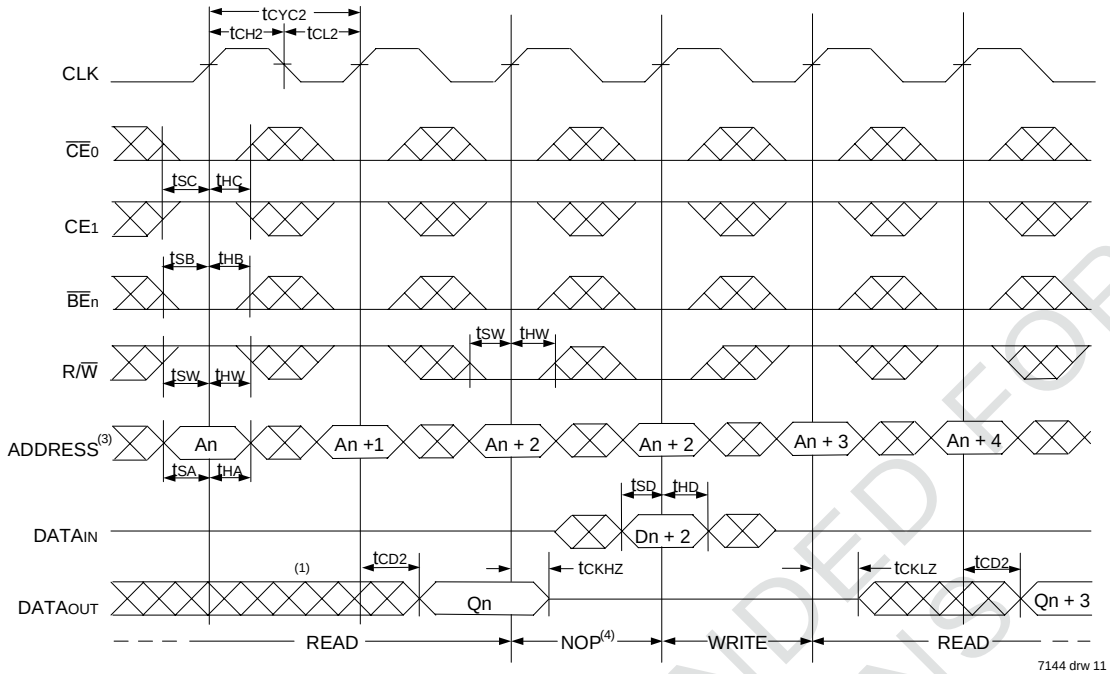
NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port "B", which is being read from. $\overline{OE}$ = V_{IH} for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)



NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD1}$). If t_{CO} > minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

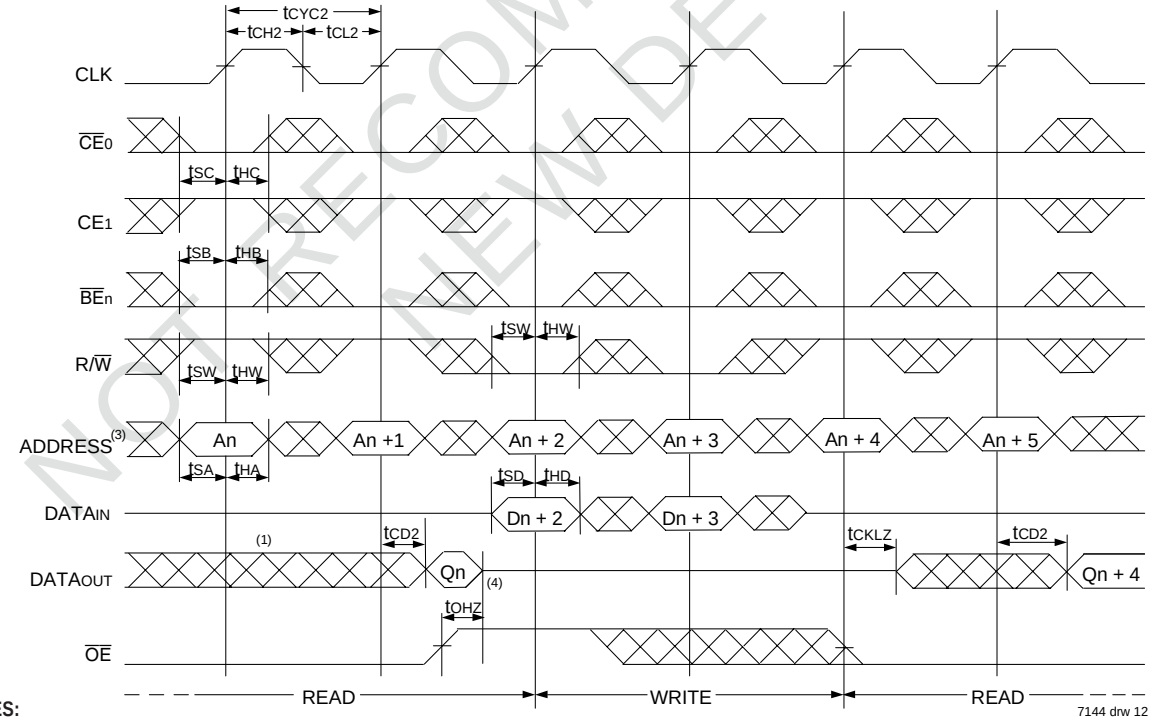
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(2)



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

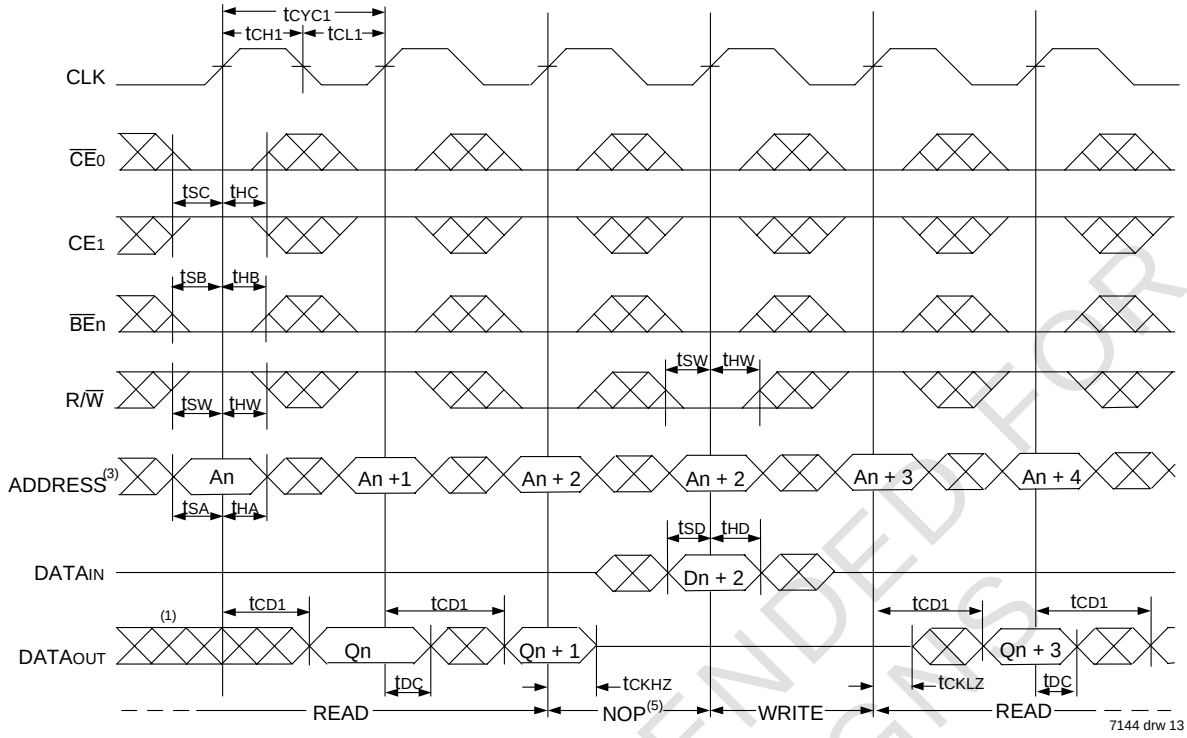
Timing Waveform of Pipelined Read-to-Write-to-Read($\overline{OE}$ Controlled)(2)



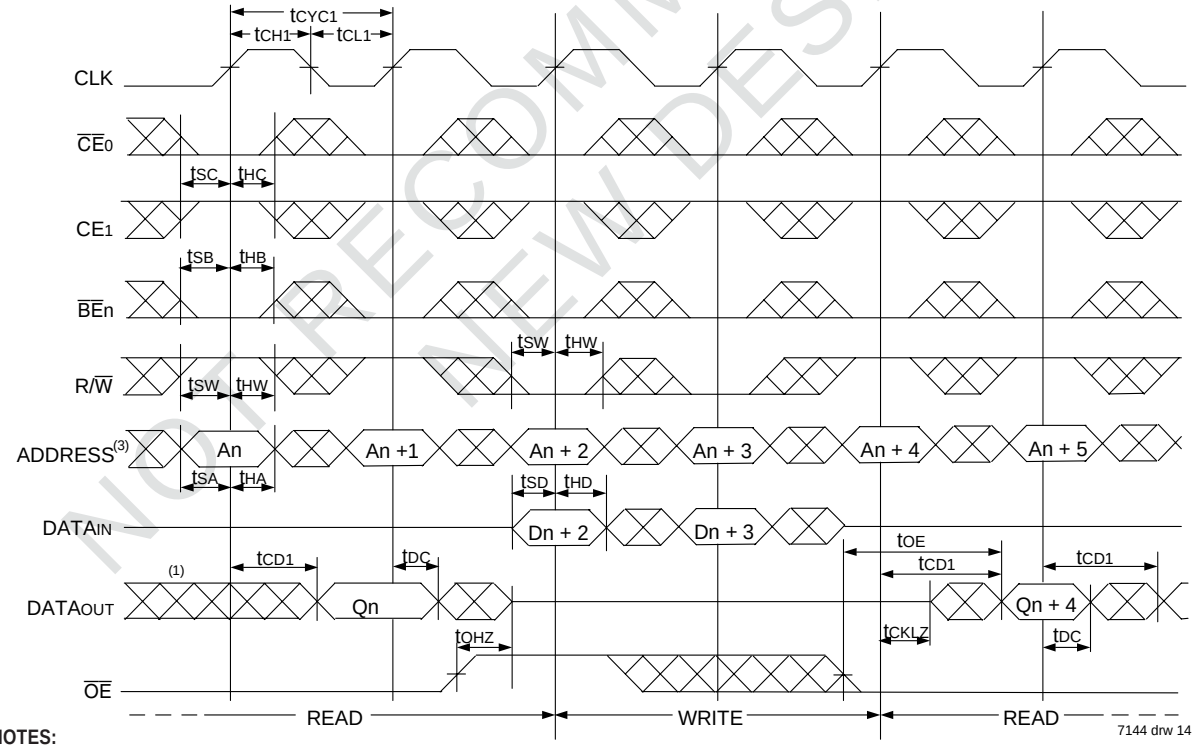
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

Timing Waveform of Flow-Through Read-to-Write-to-Read($\overline{OE}$ = VIL)(2)



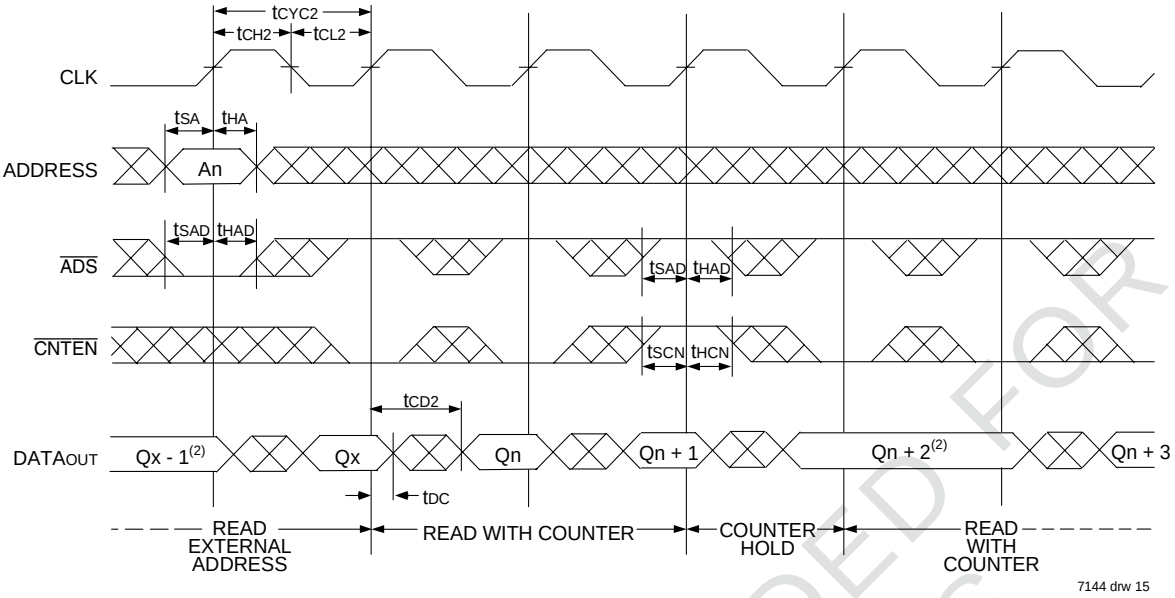
Timing Waveform of Flow-Through Read-to-Write-to-Read($\overline{OE}$ Controlled)(2)



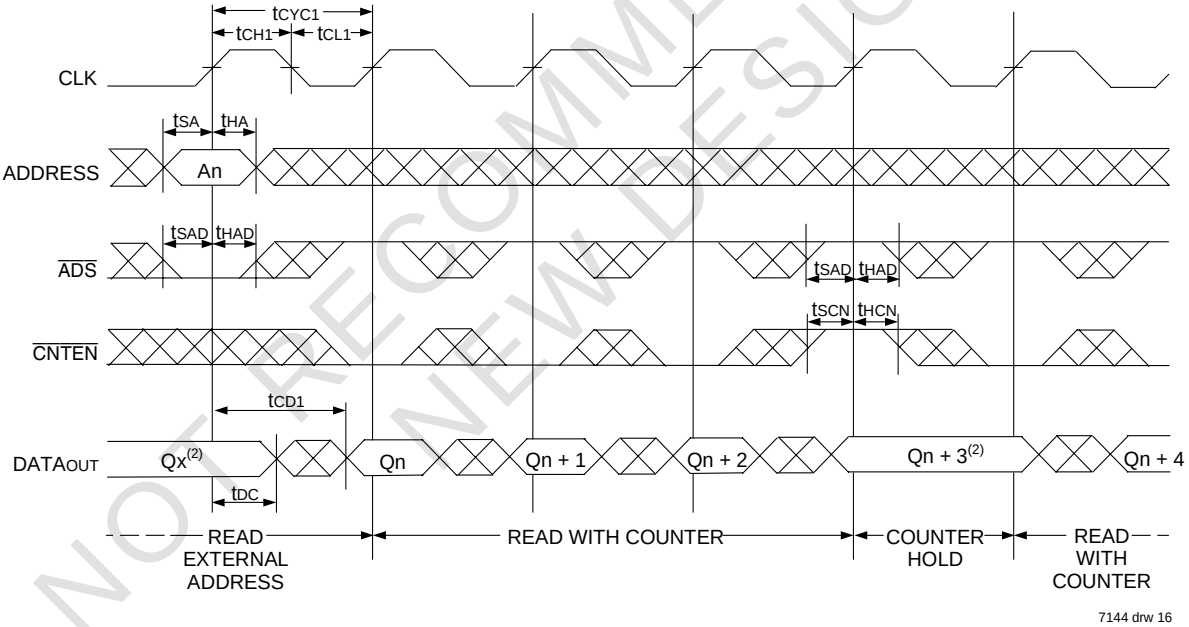
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, $\overline{BE}n$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = VIH.
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance(1)



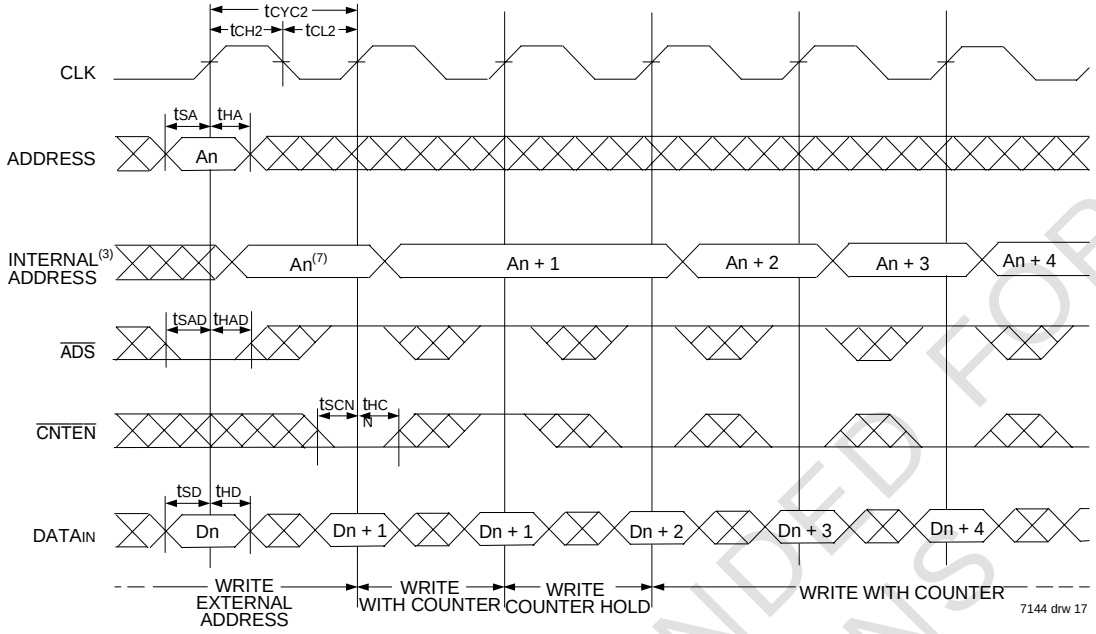
Timing Waveform of Flow-Through Read with Address Counter Advance(1)



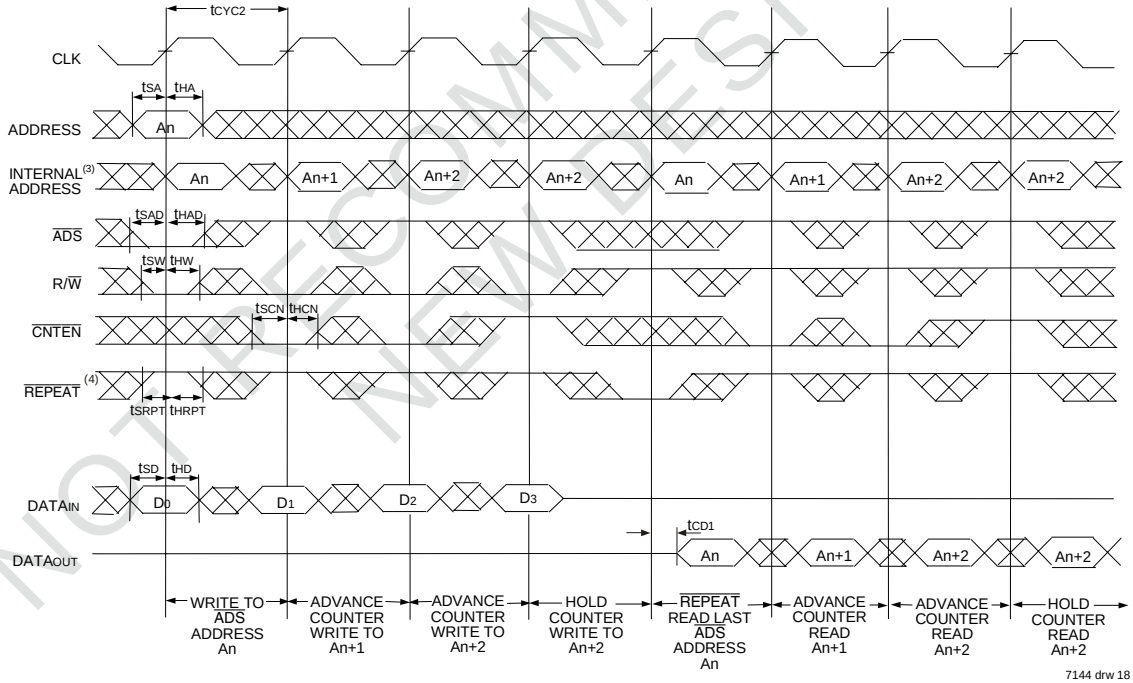
NOTES:

1. $\overline{CE_0}$, $\overline{OE}$, $\overline{BE}n$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{REPEAT}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)(1)

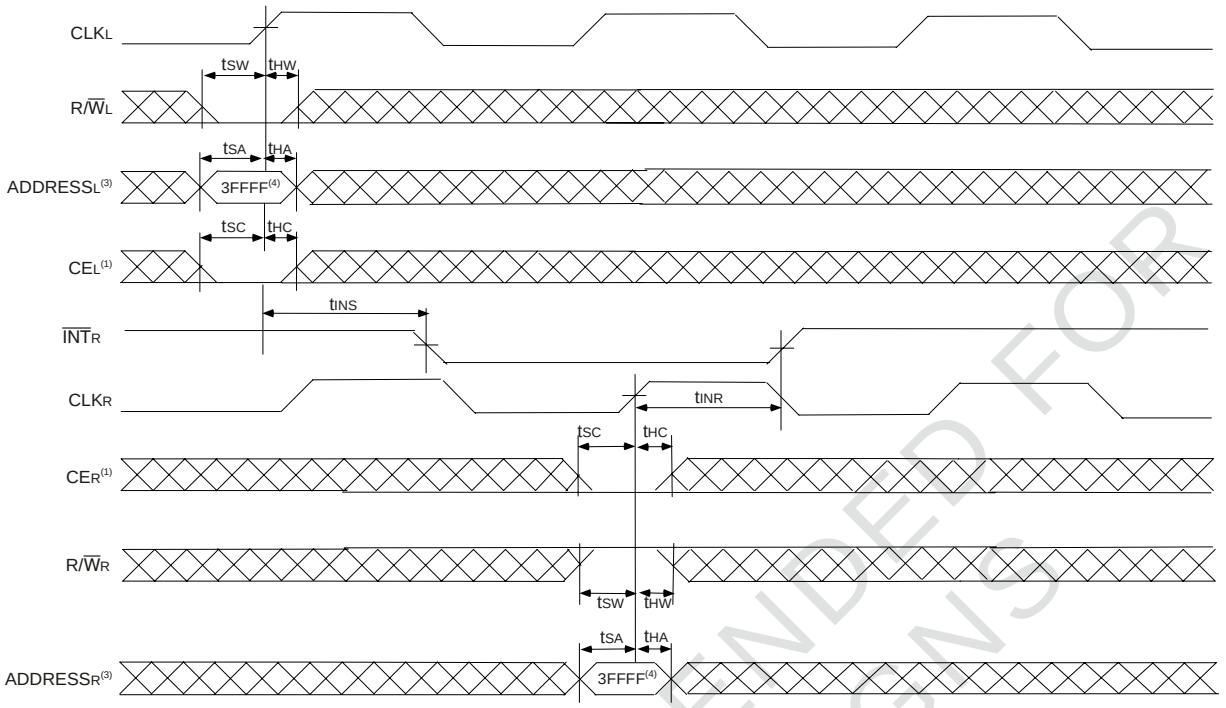


Timing Waveform of Counter Repeat(2,6)



NOTES:
1. $\overline{CE_0}$, $\overline{BE_n}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{CE_0}$, $\overline{BE_n}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
5. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.
6. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

Waveform of Interrupt Timing(2)



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NOTES:
1. $\overline{CE_0}$ = V_{IL} and CE_1 = V_{IH}
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.
4. For IDT70P3599, the Interrupt Address is 1FFFF.

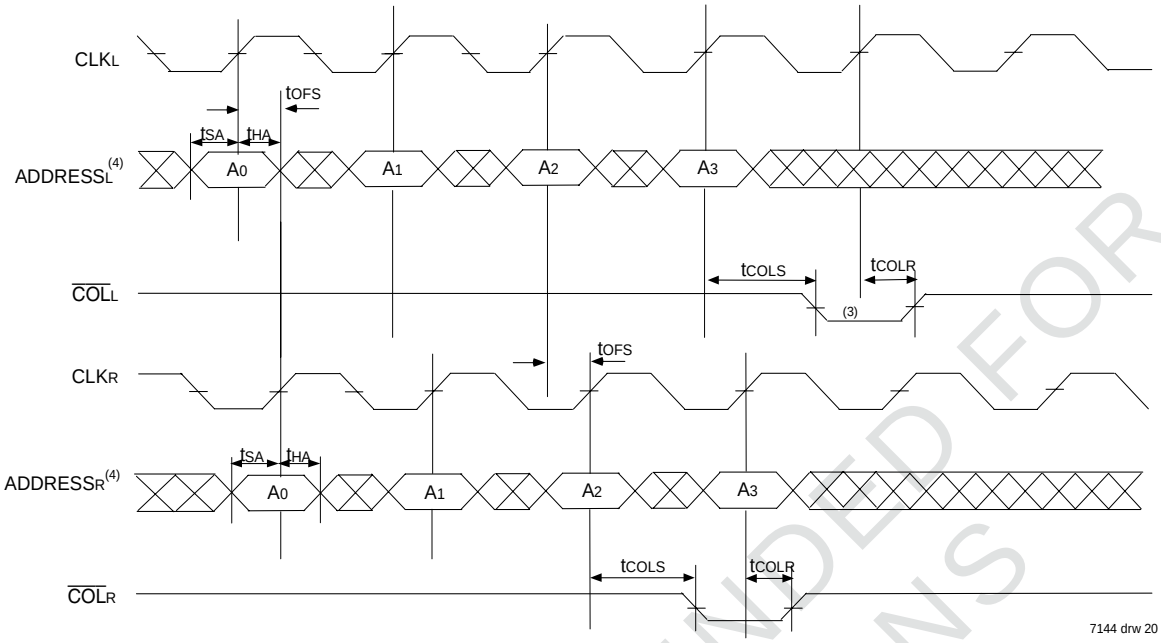
Truth Table III — Interrupt Flag(1)

Left Port					Right Port					
CLKL	R/W̄L(2)	CEL(2)	A17L-A0L(3,4)	INTL	CLKR	R/W̄R(2)	CER(2)	A17R-A0R(3,4)	INTR	Function
↑	L	L	3FFFF	X	↑	X	X	X	L	Set Right INTR Flag
↑	X	X	X	X	↑	H	L	3FFFF	H	Reset Right INTR Flag
↑	X	X	X	L	↑	L	L	3FFFE	X	Set Left INTL Flag
↑	H	L	3FFFE	H	↑	X	X	X	X	Reset Left INTL Flag

7144 tbl 12

NOTES:
1. INTL and INTR must be initialized at power-up by Resetting the flags.
2. $\overline{CE_0}$ = V_{IL} and CE_1 = V_{IH}. R/W̄ and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. A17X is a NC for IDT70P3599, therefore Interrupt Addresses are 1FFFF and 1FFFE.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Waveform of Collision Timing(1,2)
Both Ports Writing with Left Port Clock Leading



NOTES:
1. $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$.
2. For reading port, $\overline{OE}$ is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
3. Leading Port Output flag might output $3t_{CYC2} + t_{COLS}$ after Address match.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Collision Detection Timing(3,4)

Cycle Time	tOFS (ns)	
	Region 1 (ns) (1)	Region 2 (ns) (2)
5ns	0 - 2.8	2.81 - 4.6
6ns	0 - 3.8	3.81 - 5.6
7.5ns	0 - 5.3	5.31 - 7.1

7144 tbl 13

NOTES:
1. Region 1
   Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
2. Region 2
   Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc.
   while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
3. All the production units are tested to midpoint of each region.
4. These ranges are based on characterization of a typical device.

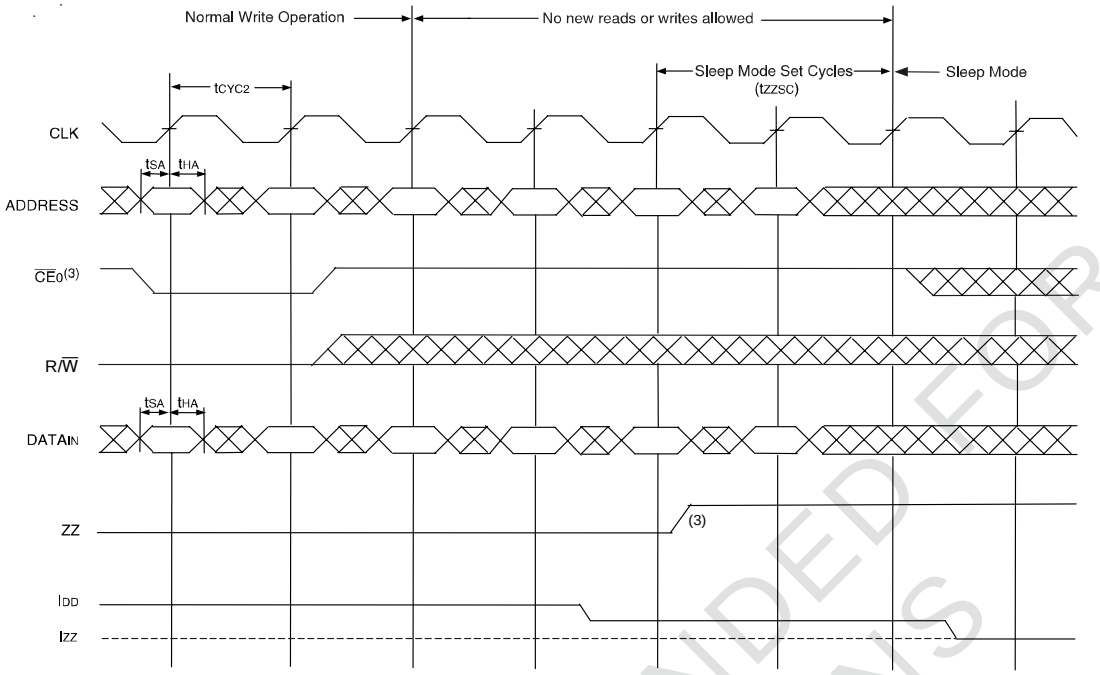
Truth Table IV — Collision Detection Flag

Left Port					Right Port					
CLKL	R/$\overline{W}$L(1)	CEL(1)	A17L-A0L(2)	$\overline{COL}$L	CLKR	R/$\overline{W}$R(1)	CER(1)	A17R-A0R(2)	$\overline{COL}$R	Function
↑	H	L	MATCH	H	↑	H	L	MATCH	H	Both ports reading. Not a valid collision. No flag output on either port.
↑	H	L	MATCH	L	↑	L	L	MATCH	H	Left port reading, Right port writing. Valid collision, flag output on Left port.
↑	L	L	MATCH	H	↑	H	L	MATCH	L	Right port reading, Left port writing. Valid collision, flag output on Right port.
↑	L	L	MATCH	L	↑	L	L	MATCH	L	Both ports writing. Valid collision. Flag output on both ports.

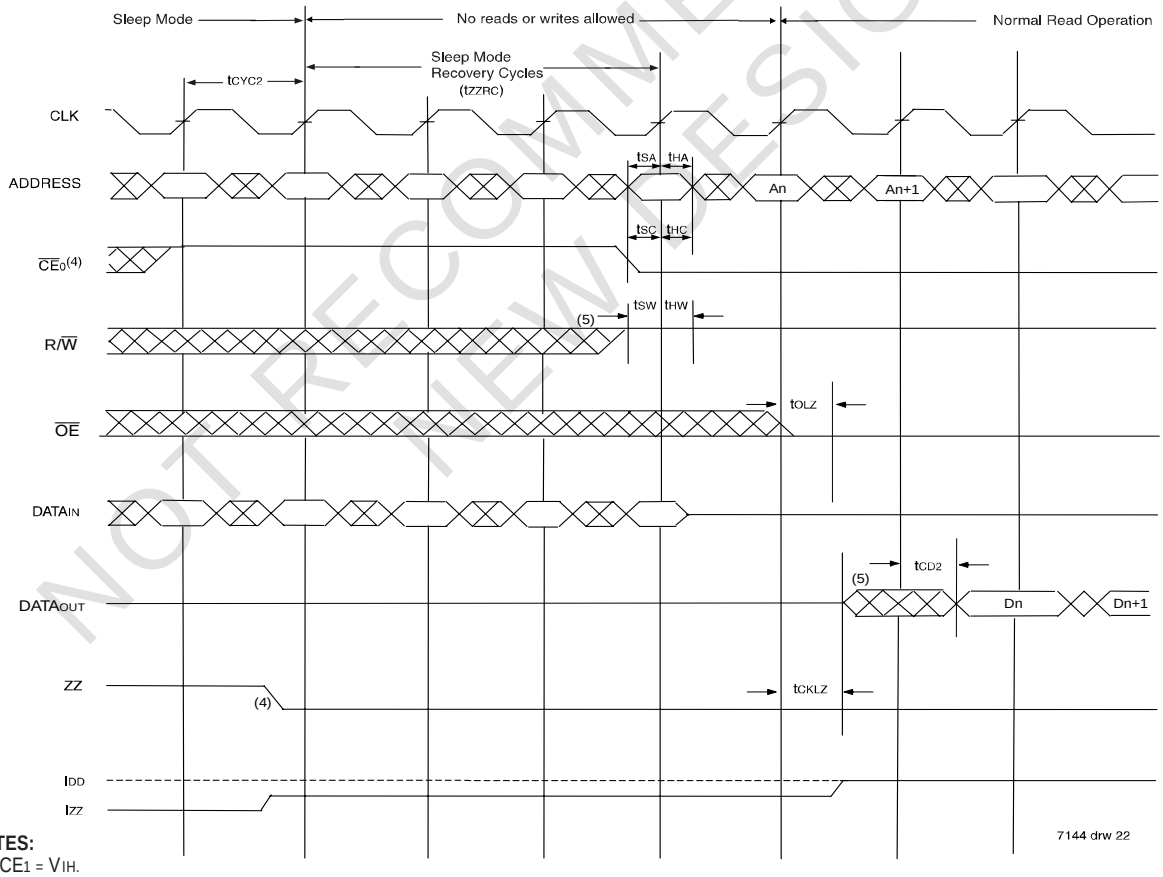
7144 tbl 14

NOTES:
1. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$. R/$\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
2. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

Timing Waveform - Entering Sleep Mode(1,2)



Timing Waveform - Exiting Sleep Mode(1,2)



NOTES:
1. $CE_1 = V_{IH}$.
2. All timing is same for Left and Right ports.
3. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0 = V_{IH}$) three cycles prior to asserting ZZ ($ZZ_X = V_{IH}$) and held for two cycles after asserting ZZ ($ZZ_X = V_{IH}$).
4. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0 = V_{IH}$) one cycle prior to de-asserting ZZ ($ZZ_X = V_{IL}$) and held for three cycles after de-asserting ZZ ($ZZ_X = V_{IL}$).
5. The device must be in Read Mode (R/$\overline{W}$ High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

Functional Description

The IDT70P3519/99 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70P3519/99 for depth expansion configurations. Two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FFFE (1FFFE for IDT70P3599), where a write is defined as $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 3FFFE (1FFFE for IDT70P3599) when $\overline{CE}_L$ = V_{IL} and R/$\overline{W}_L$ = V_{IH}. Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FFFF (1FFF for IDT70P3599) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FFFF (1FFFF for IDT70P3599). The message (36 bits) at 3FFFE or 3FFFF (1FFFF or 1FFFE for IDT70P3599) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFFE and 3FFFF (1FFFF or 1FFFE for IDT70P3599) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Collision Detetion

Collision is defined as accessing the same memory address from both ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag ($\overline{COL}$x) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing table on Page 21. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert flag. A third collision will generate the proper alert flag. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection timing waveform on Page 21.

Collision detection on the IDT70P3519/99 represents an advance in functionality over other sync multi-ports, which have no such capability. The IDT70P3519/99 sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

Sleep Mode

The IDT70P3519/99 is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ (ZZx = V_{IH}) and three cycles after de-asserting ZZ (ZZx = V_{IL}), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode (R/$\overline{W}$x = V_{IH})when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

Depth and Width Expansion

The IDT70P3519/99 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70P3519/99 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

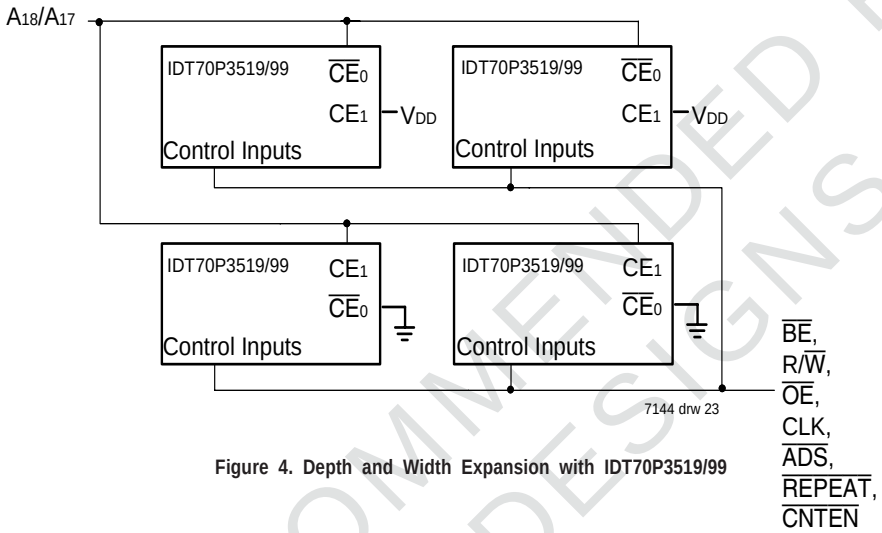


Figure 4. Depth and Width Expansion with IDT70P3519/99

NOTE:
1. A_{18} is for IDT70P3519, A_{17} is for IDT70P3599.

JTAG Timing Specifications

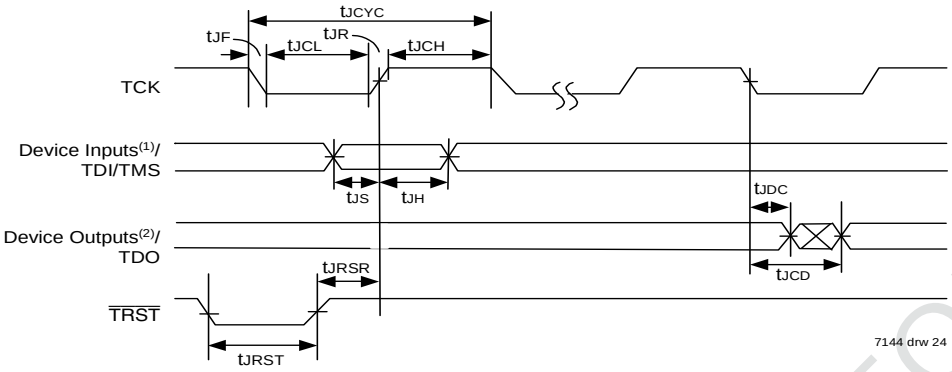


Figure 5. Standard JTAG Timing

NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics (1,2,3,4)

Symbol	Parameter	70P3519/99		
		Min.	Max.	Units
tJCYC	JTAG Clock Input Period	100	—	ns
tJCH	JTAG Clock HIGH	40	—	ns
tJCL	JTAG Clock Low	40	—	ns
tJR	JTAG Clock Rise Time	—	3(1)	ns
tJF	JTAG Clock Fall Time	—	3(1)	ns
tJRST	JTAG Reset	50	—	ns
tJRSR	JTAG Reset Recovery	50	—	ns
tJCD	JTAG Data Output	—	25	ns
tJDC	JTAG Data Output Hold	0	—	ns
tJS	JTAG Setup	15	—	ns
tJH	JTAG Hold	15	—	ns

7144 tbl 15

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x380[1]	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

7144 tbl 16

NOTE:
1. Device ID for IDT70P3599 is 0x383.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

7144 tbl 17

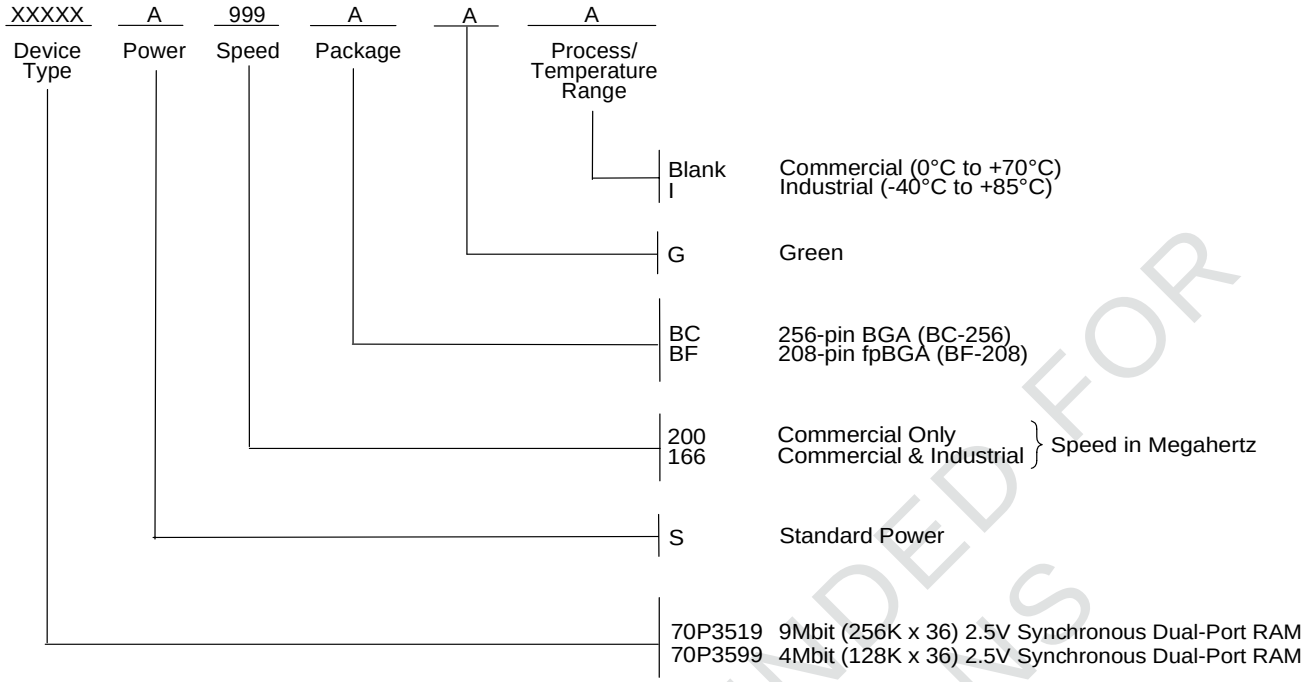
System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state except $\overline{COL}$x & $\overline{INT}$x outputs.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	0101, 0111, 1000, 1001, 1010, 1011, 1100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	0110,1110,1101	For internal use only.

7144 tbl 18

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



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IDT Clock Solution for IDT70P3519/99 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70P3519/99	2.5	LVTTL	3.5-6pF	40%	200	75ps	5T2010 5T9010	5T905, 5T9050 5T907, 5T9070

7144 tbl 19

Datasheet Document History:

07/07/08: Initial Datasheet
01/19/09: Page 28 Removed "IDT" from orderable part number
06/08/09: Removed preliminary status

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