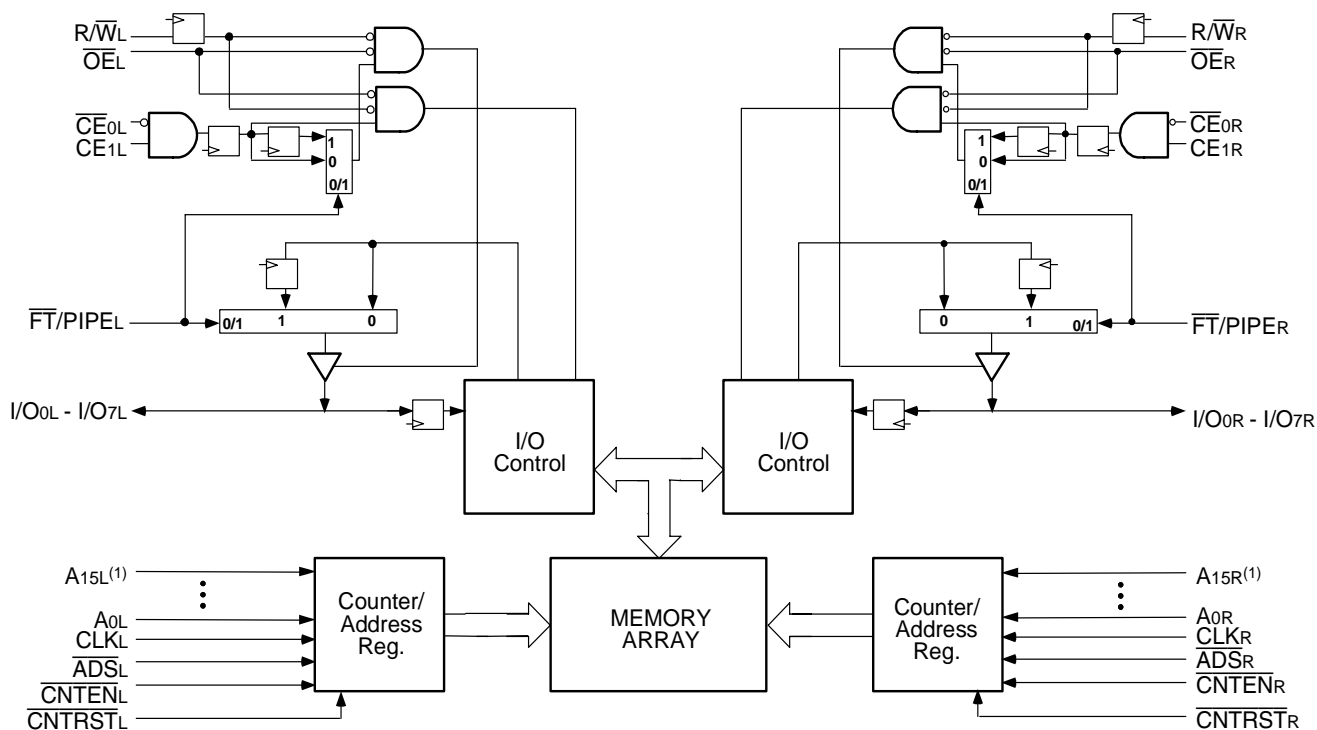# HIGH-SPEED 64/32K x 8 SYNCHRONOUS DUAL-PORT STATIC RAM

IDT709089/79S/L

Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - Commercial: 9/12/15ns (max.)
  - Industrial: 12ns (max.)
- Low-power operation
  - IDT709089/79S
    Active: 950mW (typ.)
    Standby: 5mW (typ.)
  - IDT709089/79L
    Active: 950mW (typ.)
    Standby: 1mW (typ.)
- Flow-Through or Pipelined output mode on either port via the $\overline{FT}$/PIPE pin
- Counter enable and reset features

- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - 4ns setup to clock and 1ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 9ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 15ns cycle time, 66.7MHz operation in the Pipelined output mode
- TTL- compatible, single 5V (±10%) power supply
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Available in 100-pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

Functional Block Diagram

3242 drw 01

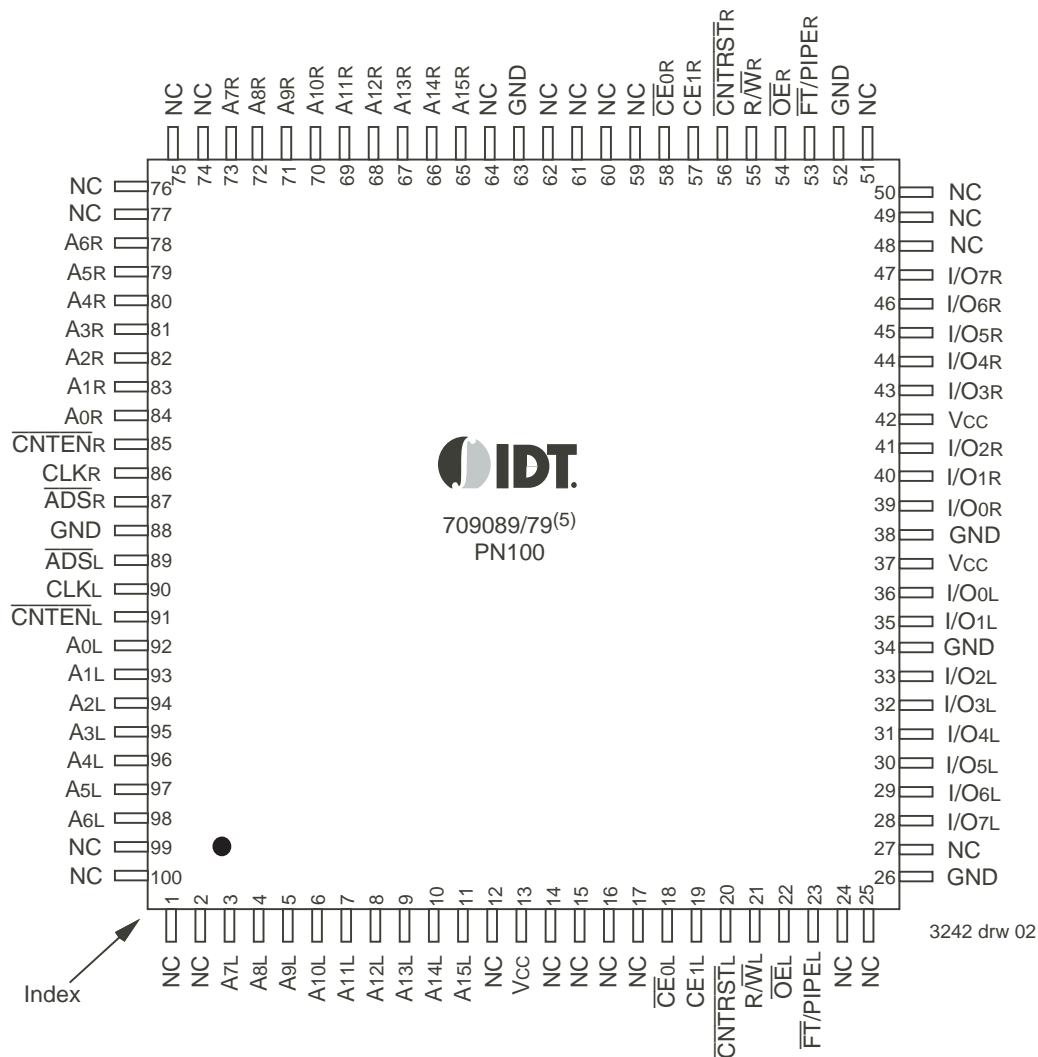NOTE:
1. A_{15X} is a NC for IDT709079.

FEBRUARY 2016

DSC-3242/16

Description:

The IDT709089/79 is a high-speed 64/32K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709089/79 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}0$ and $CE1$, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 950mW of power.

Pin Configuration[1,2,3]

3242 drw 02

NOTES:
1. A15x is a NC for IDT709079.
2. All Vcc pins must be connected to power supply.
3. All GND pins must be connected to ground supply.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{15L}[1]	A_{0R} - A_{15R}[1]	Address
I/O_{0L} - I/O_{7L}	I/O_{0R} - I/O_{7R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipeline
V_{CC}		Power
GND		Ground

NOTE:
1. A_{15X} is a NC for IDT709079.

3242 tbl 01

Truth Table I— Read/Write and Enable Control[1,2,3]

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$R/\overline{W}$	I/O_{0-7}	Mode
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

3242 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control[1,2]

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O[3]	MODE
A_n	X	A_n	↑	L[4]	X	H	$D_{I/O}(n)$	External Address Used
X	A_n	$A_n + 1$	↑	H	L[5]	H	$D_{I/O}(n+1)$	Counter Enabled—Internal Address generation
X	$A_n + 1$	$A_n + 1$	↑	H	H	H	$D_{I/O}(n+1)$	External Address Blocked—Counter disabled ($A_n + 1$ reused)
X	X	A_0	↑	X	X	L[4]	$D_{I/O}(0)$	Counter Reset to Address 0

5640 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{CE}_0$ and $\overline{OE}$ = V_{IL}; CE_1 and $R/\overline{W}$ = V_{IH}.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ is independent of all other signals including $\overline{CE}_0$ and CE_1.
5. The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE}_0$ and CE_1.

Recommended Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3242 tbl 04

NOTES:
1. This is the parameter T$_A$. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{CC}$	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V$_{IH}$	Input High Voltage	2.2	—	6.0[1]	V
V$_{IL}$	Input Low Voltage	-0.5[2]	—	0.8	V

3242 tbl 05

NOTES:
1. V$_{TERM}$ must not exceed V$_{CC}$ + 10%.
2. V$_{IL}$ ≥ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T$_{BIAS}$	Temperature Under Bias	-55 to +125	°C
T$_{STG}$	Storage Temperature	-65 to +150	°C
T$_{JN}$	Junction Temperature	+150	°C
I$_{OUT}$	DC Output Current	50	mA

3242 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V$_{TERM}$ must not exceed V$_{CC}$+ 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V$_{TERM}$ ≥ V$_{CC}$ + 10%.
3. Ambient Temperature Under DC Bias. No AC Conditions. Chip Deselected.

Capacitance[1]
(T$_A$ = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 3dV	9	pF
C$_{OUT}$[3]	Output Capacitance	V$_{OUT}$ = 3dV	10	pF

3242 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C$_{OUT}$ also references C$_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V$_{CC}$ = 5.0V ± 10%)

			709089/79S/L		
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|I$_{LI}$|	Input Leakage Current[1]	V$_{CC}$ = 5.5V, V$_{IN}$ = 0V to V$_{CC}$	—	10	µA
|I$_{LO}$|	Output Leakage Current	$\overline{CE}_0$ = V$_{IH}$ or CE$_1$ = V$_{IL}$, V$_{OUT}$ = 0V to V$_{CC}$	—	10	µA
V$_{OL}$	Output Low Voltage	I$_{OL}$ = +4mA	—	0.4	V
V$_{OH}$	Output High Voltage	I$_{OH}$ = -4mA	2.4	—	V

3242 tbl 08

NOTE:
1. At V$_{CC}$ ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		709089/79X9 Com'l Only Typ.[4]	Max.	709089/79X12 Com'l & Ind Typ.[4]	Max.	709089/79X15 Com'l Only Typ.[4]	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL} Outputs Disabled f = f_{MAX}[1]	COM'L	S L	210 210	390 350	200 200	345 305	190 190	325 285	mA
			IND	S L	— —	— —	200 200	380 340	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	S L	50 50	135 115	50 50	110 90	50 50	110 90	mA
			IND	S L	— —	— —	50 50	125 105	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[3] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	S L	140 140	270 240	130 130	230 200	120 120	220 190	mA
			IND	S L	— —	— —	130 130	245 215	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	mA
			IND	S L	— —	— —	1.0 0.2	15 5	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" $\leq$ 0.2V and $\overline{CE}$"B" $\geq V_{CC}$ - 0.2V[5] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Disabled, f = f_{MAX}[1]	COM'L	S L	130 130	245 225	120 120	205 185	110 110	195 175	mA
			IND	S L	— —	— —	120 120	220 200	— —	— —	

3242 tbl 09

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 5V, T_A = 25°C for Typ, and are not production tested. I_{CC} DC(f=0) = 150mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE$_{1X}$ = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE$_{1X}$ = V_{IL}
   $\overline{CE}_X \leq$ 0.2V means $\overline{CE}_{0X} \leq$ 0.2V and CE$_{1X} \geq V_{CC}$ - 0.2V
   $\overline{CE}_X \geq V_{CC}$ - 0.2V means $\overline{CE}_{0X} \geq V_{CC}$ - 0.2V or CE$_{1X} \leq$ 0.2V
   "X" represents "L" for left port or "R" for right port.
6. 'X' in part numbers indicate power (S or L).

AC Test Conditions

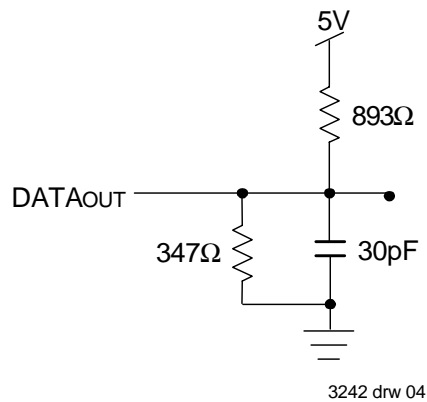|	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3242 tbl 10

5V

893Ω

DATAOUT

347Ω   30pF

3242 drw 04

Figure 1. AC Output Test load.

5V

893Ω

DATAOUT

347Ω   5pF*

3242 drw 05
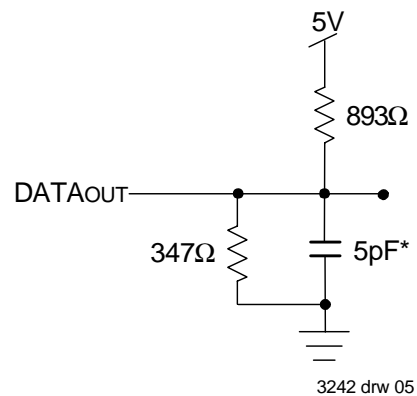
Figure 2. Output Test Load
(**For** tCKLZ, tCKHZ, tOLZ, **and** tOHZ).
*Including scope and jig.

△ tCD1,
△ tCD2
(Typical, ns)

**10 pF is the I/O capacitance
of this device, and 30pF is the
AC Test Load Capacitance**

Capacitance (pF)

3242 drw
06
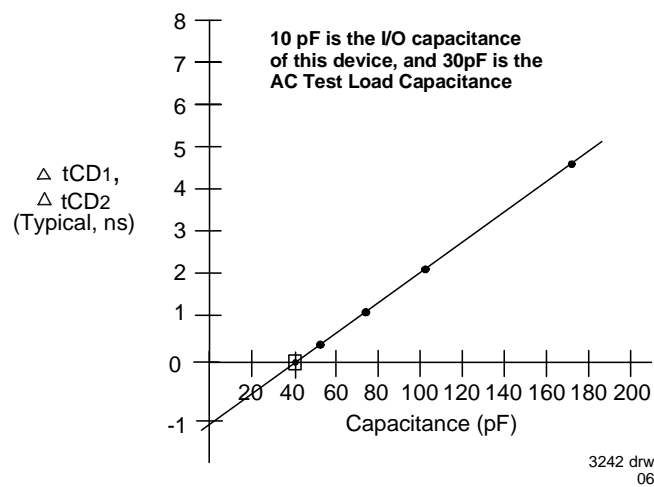
Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3,4] (V_{CC} = 5V ± 10%)

| Symbol	Parameter	709089/79X9 Com'l Only		709089/79X12 Com'l & Ind		709089/79X15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	25	—	30	—	35	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[2]	15	—	20	—	25	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	6	—	8	—	10	—	ns
t_{CL2}	Clock Low Time (Pipelined)[2]	6	—	8	—	10	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	4	—	4	—	4	—	ns
t_{HA}	Address Hold Time	1	—	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	4	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	1	—	1	—	1	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	4	—	4	—	4	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	1	—	1	—	1	—	ns
t_{SD}	Input Data Setup Time	4	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	1	—	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	4	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	1	—	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	4	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	1	—	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	4	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	9	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z[1]	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	20	—	25	—	30	ns
t_{CD2}	Clock to Data Valid (Pipelined)[2]	—	9	—	12	—	15	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	2	—	ns
Port-to-Port Delay								
t_{CWDD}	Write Port Clock High to Read Data Delay	—	35	—	40	—	50	ns
t_{CCS}	Clock-to-Clock Setup Time	—	15	—	15	—	20	ns

3242 tbl 11

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE"x" = V_{IL})[3,6]
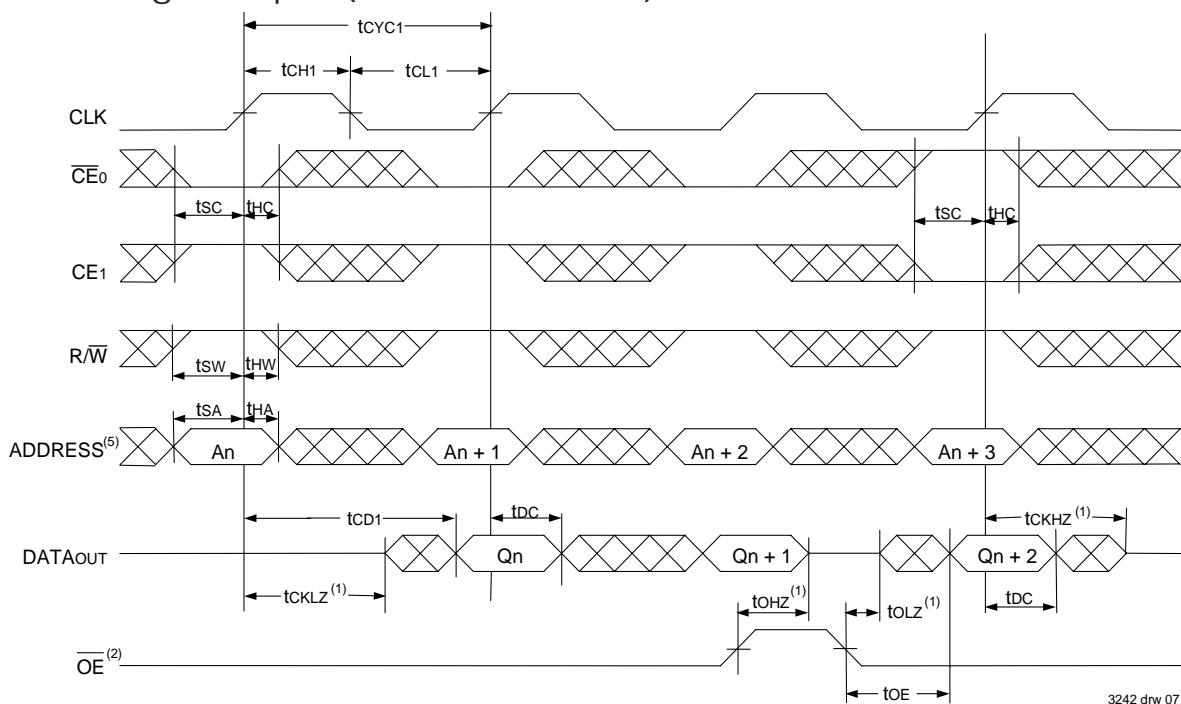
3242 drw 07

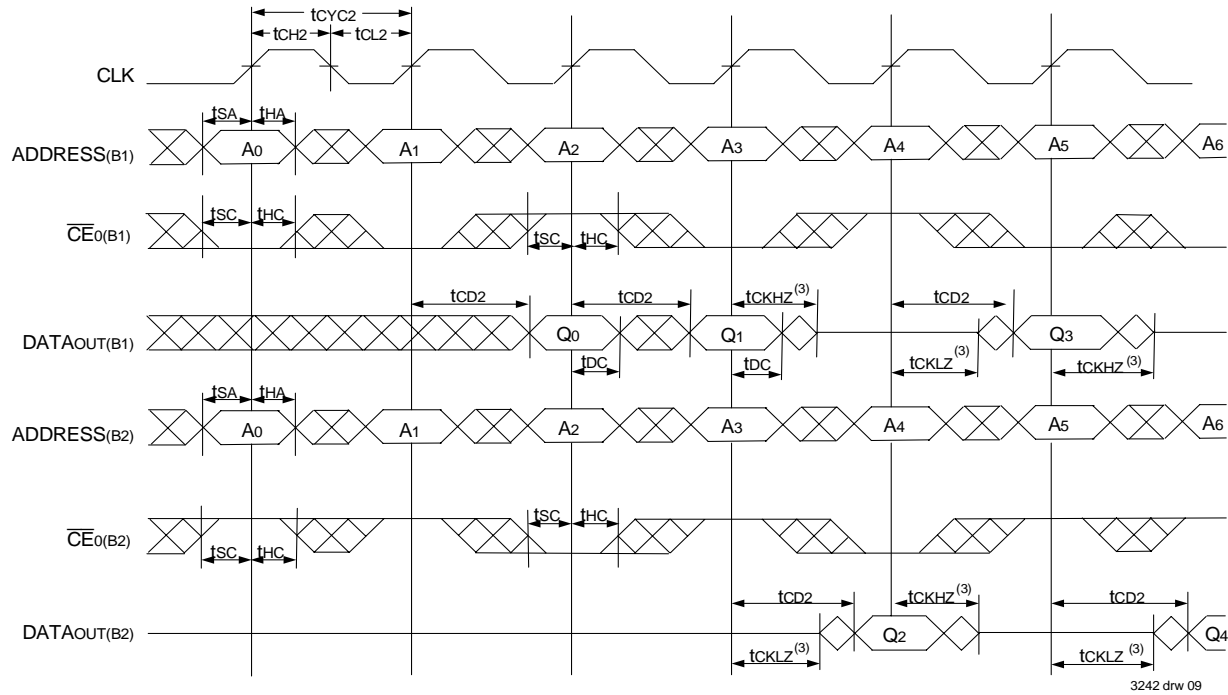## Timing Waveform of Read Cycle for Pipelined Output ($\overline{FT}$/PIPE"x" = V_{IH})[3,6]
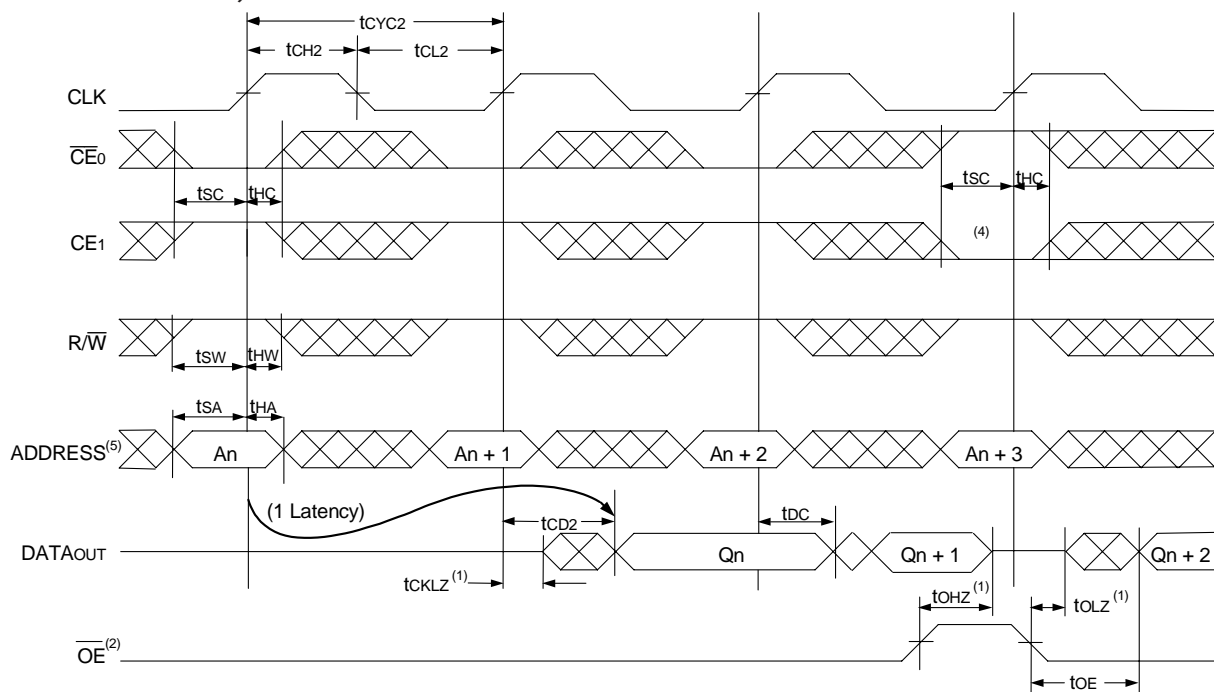
3242 drw 08

NOTES:
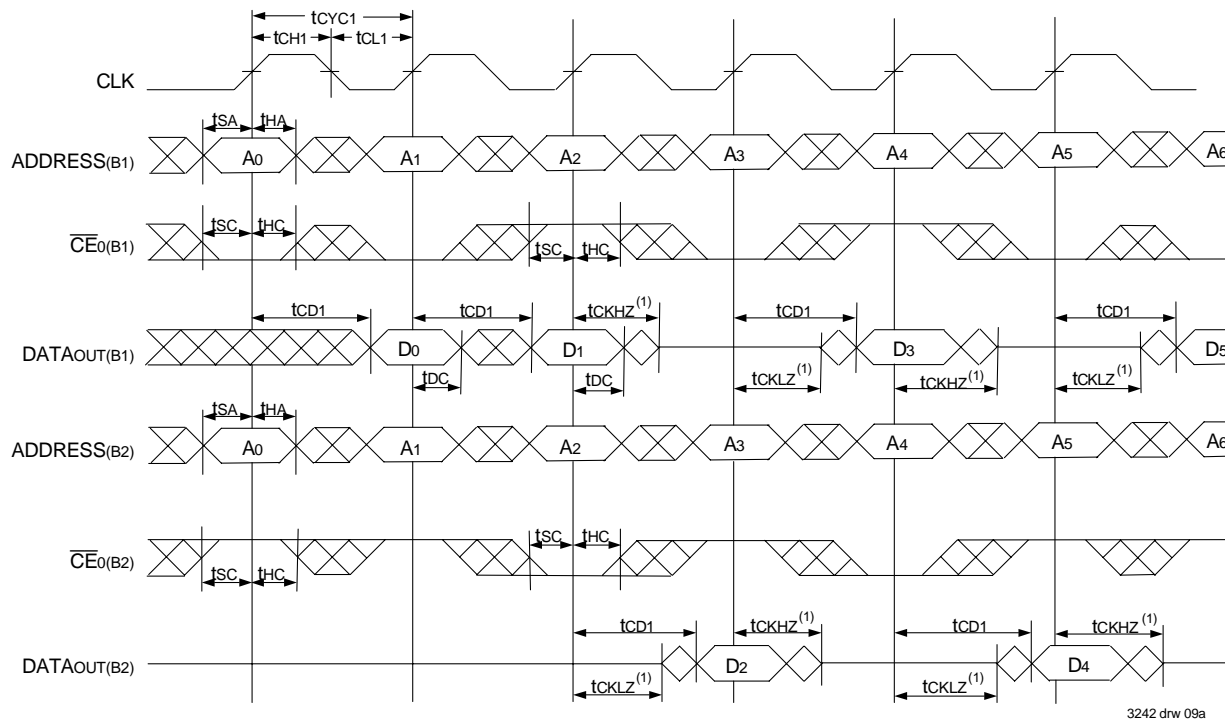1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = V_{IL} and $\overline{CNTRST}$ = V_{IH}.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL} following the next rising edge of clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read[1,2]

3242 drw 09

Timing Waveform of a Bank Select Flow-Through Read[6,7]

3242 drw 09a

NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709089/79 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{OE}$ and $\overline{ADS}$ = VIL; CE1(B1), CE1(B2), R/$\overline{W}$ and $\overline{CNTRST}$ = VIH.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE}$0 and $\overline{ADS}$ = VIL; CE1 and $\overline{CNTRST}$ = VIH.
5. $\overline{OE}$ = VIL for the Right Port, which is being read from. $\overline{OE}$ = VIH for the Left Port, which is being written to.
6. If tCCS $\leq$ maximum specified, then data from right port READ is not valid until the maximum specified for tCWDD.
   If tCCS > maximum specified, then data from right port READ is not valid until tCCS + tCD1. tCWDD does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".
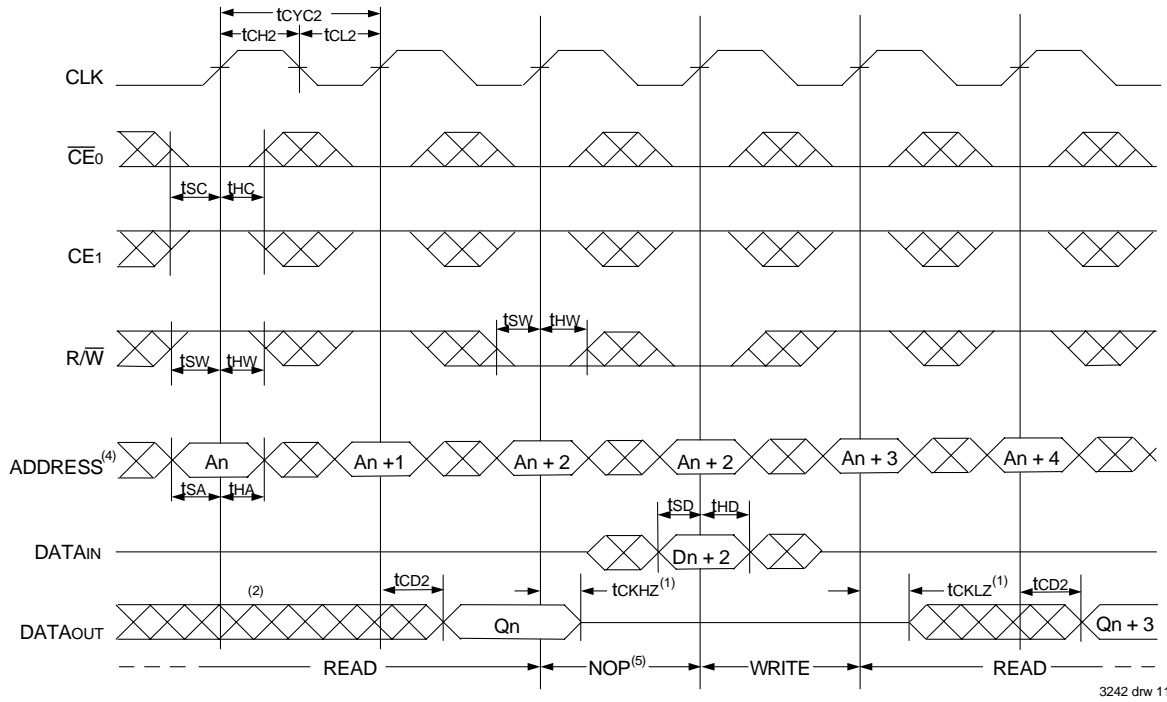
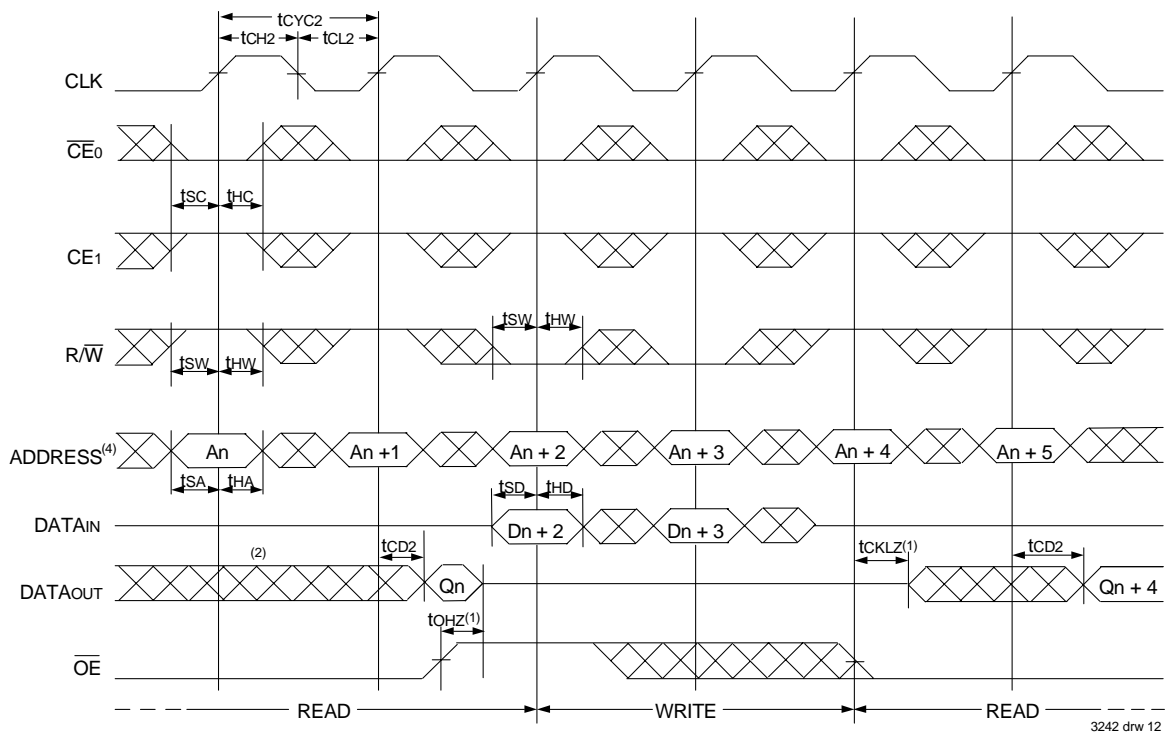# Timing Waveform with Port-to-Port Flow-Through Read[1,2,3,5]
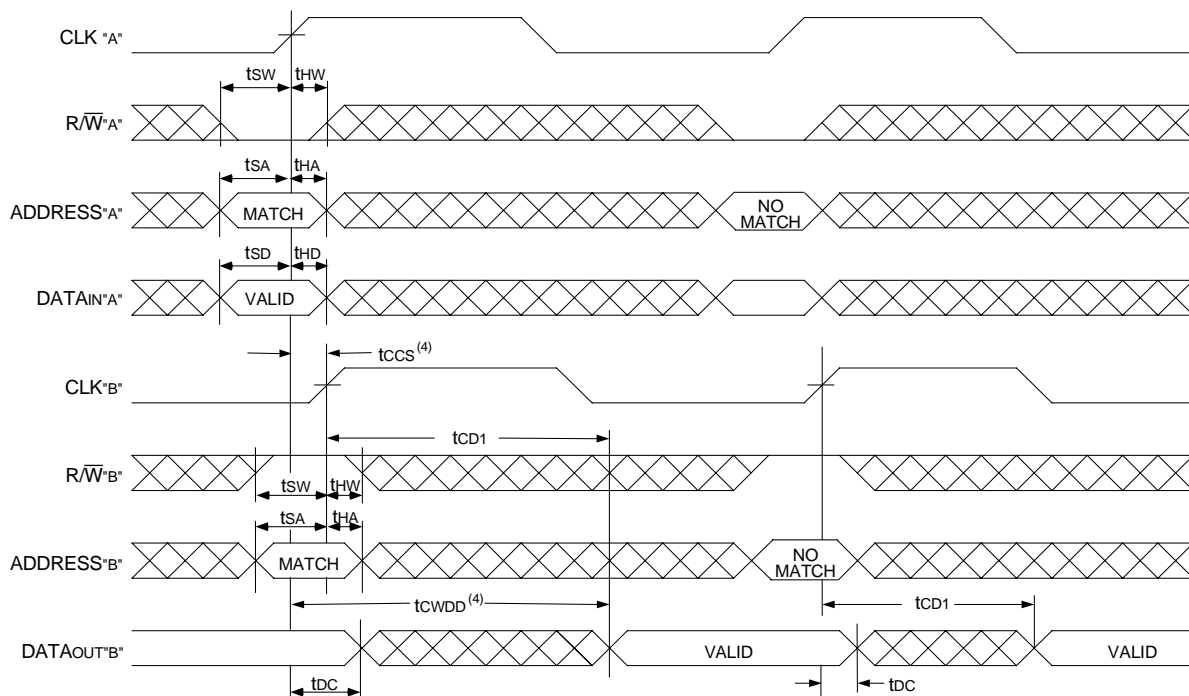
3242 drw 10

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_0$ and $\overline{ADS}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
3. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
4. If t_{CCS} ≤ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until t_{CCS} + t_{CD1}. t_{CWDD} does not apply in this case.
5. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}}$ = V_{IL})[3]
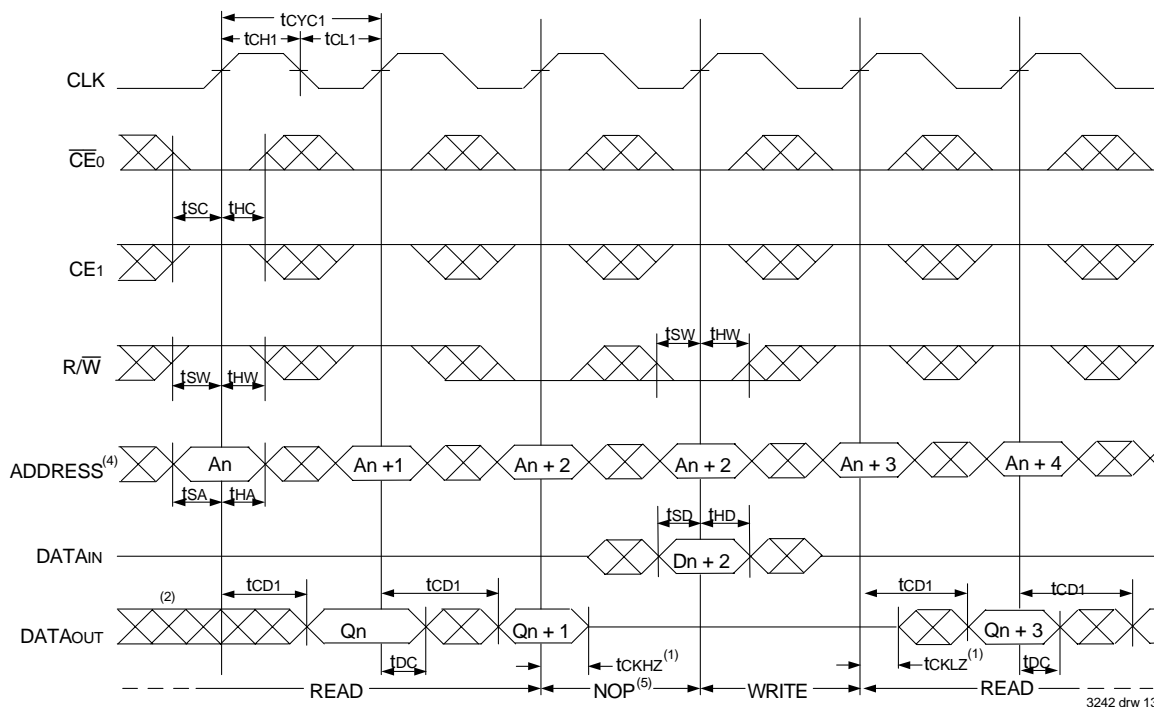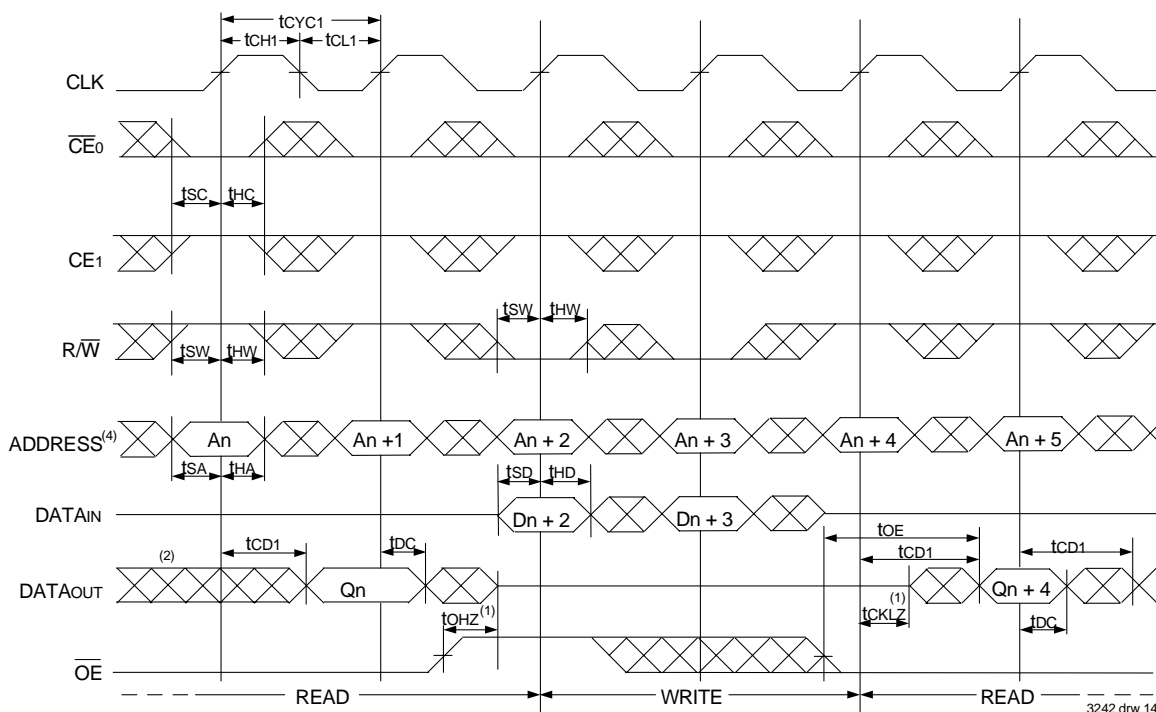

3242 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)[3]


3242 drw 12

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{\text{CE}}_0$ and $\overline{\text{ADS}}$ = V_{IL}; CE_1 and $\overline{\text{CNTRST}}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform Flow-Through Read-to-Write-to-Read ($\overline{\text{OE}}$ = V_{IL})[3]

3242 drw 13

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{\text{OE}}$ Controlled)[3]


3242 drw 14

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance is determined by the previous cycle control signals.
3. $\overline{\text{CE}}_0$ and $\overline{\text{ADS}}$ = V_{IL}; CE_1 and $\overline{\text{CNTRST}}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

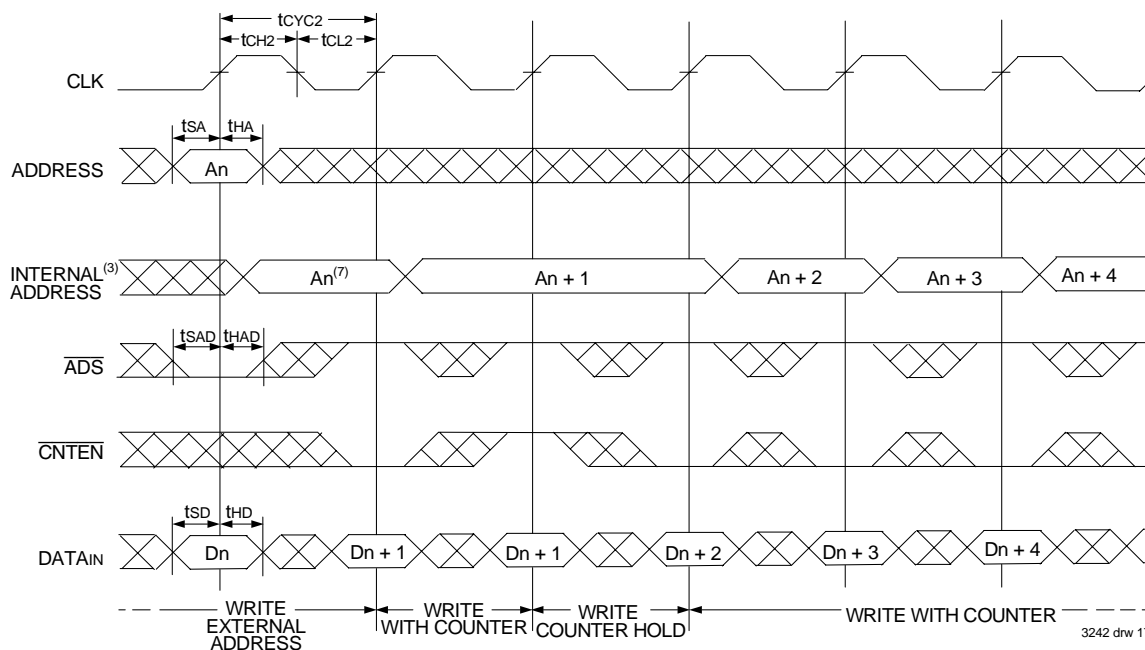## Timing Waveform of Pipelined Read with Address Counter Advance[1]

3242 drw 15
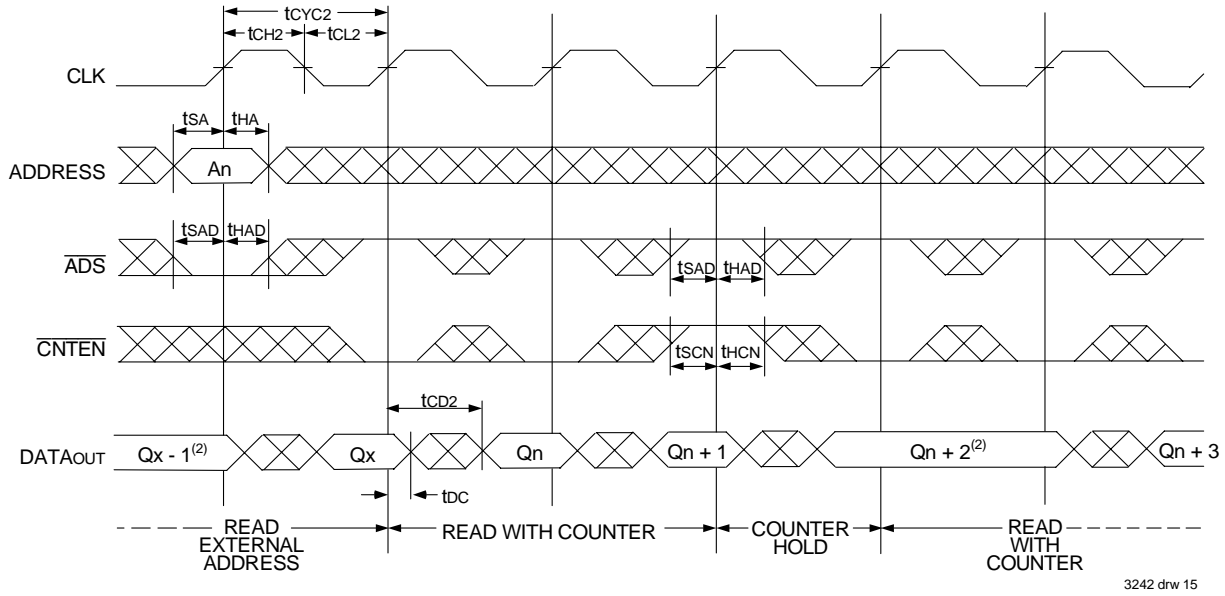
Timing Waveform of Flow-Through Read with Address Counter Advance[1]

3242 drw 16
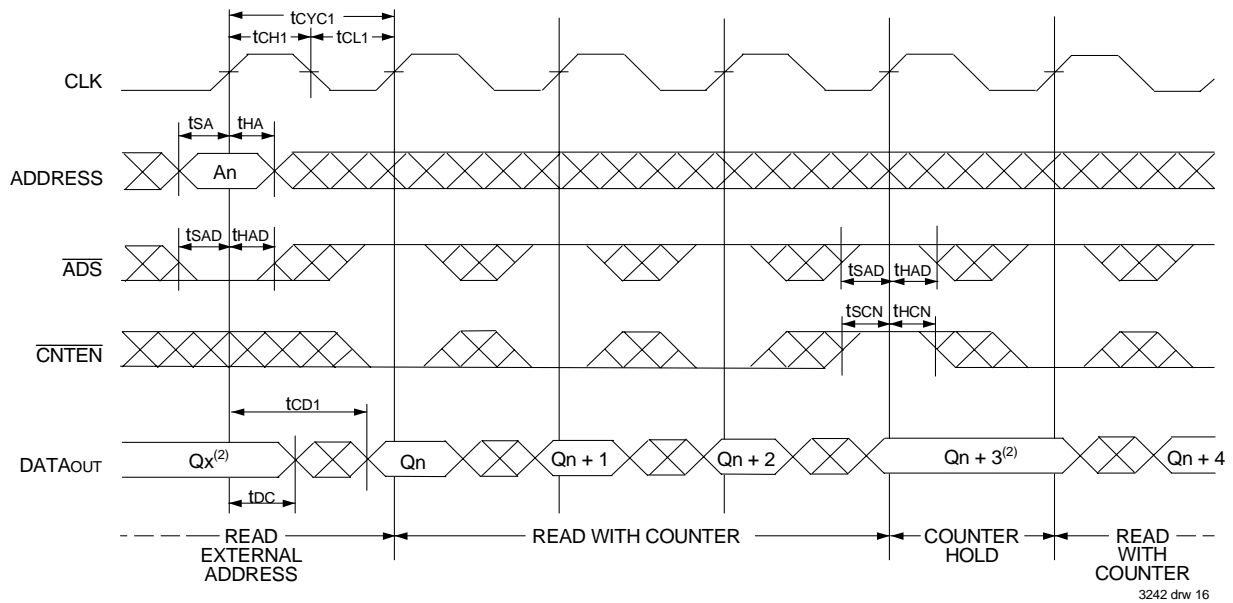
NOTES:
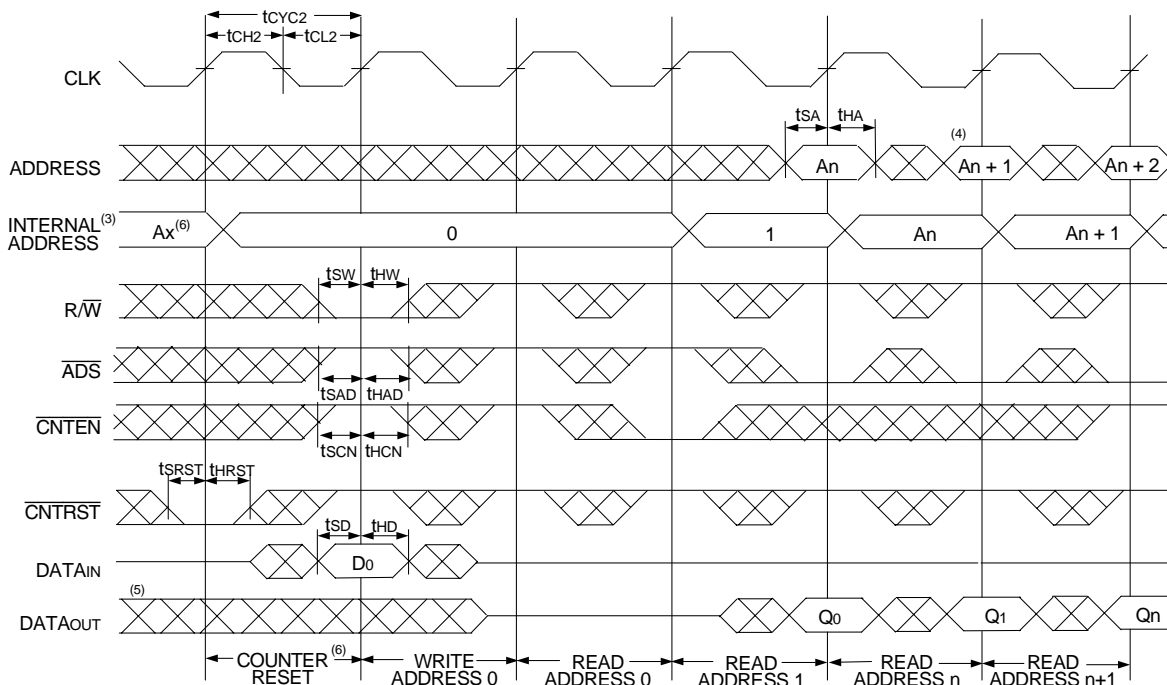1. $\overline{CE}_0$ and $\overline{OE}$ = V_{IL}; CE_1, $R/\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)[1]

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Timing Waveform of Counter Reset (Pipelined Outputs)[2]

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NOTES:
1. $\overline{CE}_0$ and R/$\overline{W}$ = V_{IL}; CE$_1$ and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE}_0$ = V_{IL}; CE$_1$ = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. ADDR$_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

Functional Description

The IDT709089/79 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709089/79's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT709089/79 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT709089/79 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.
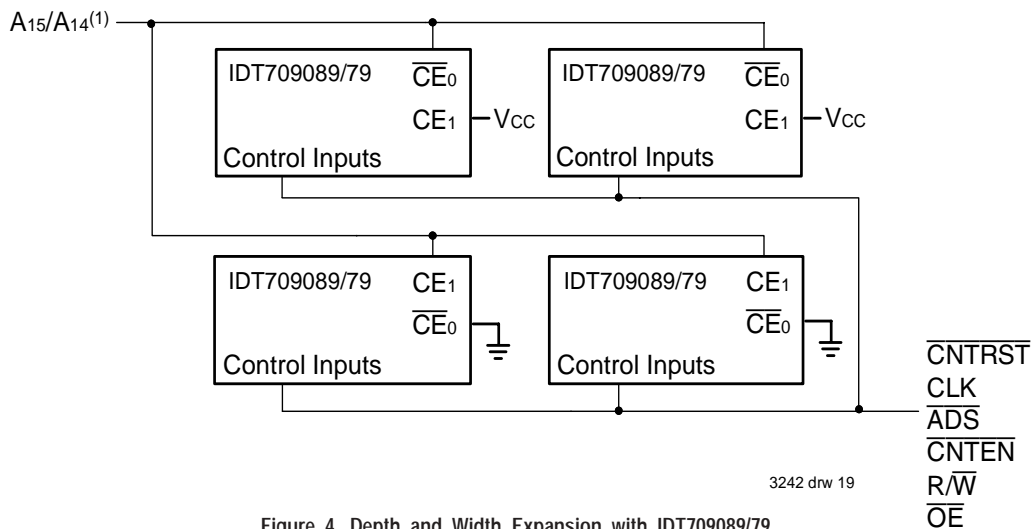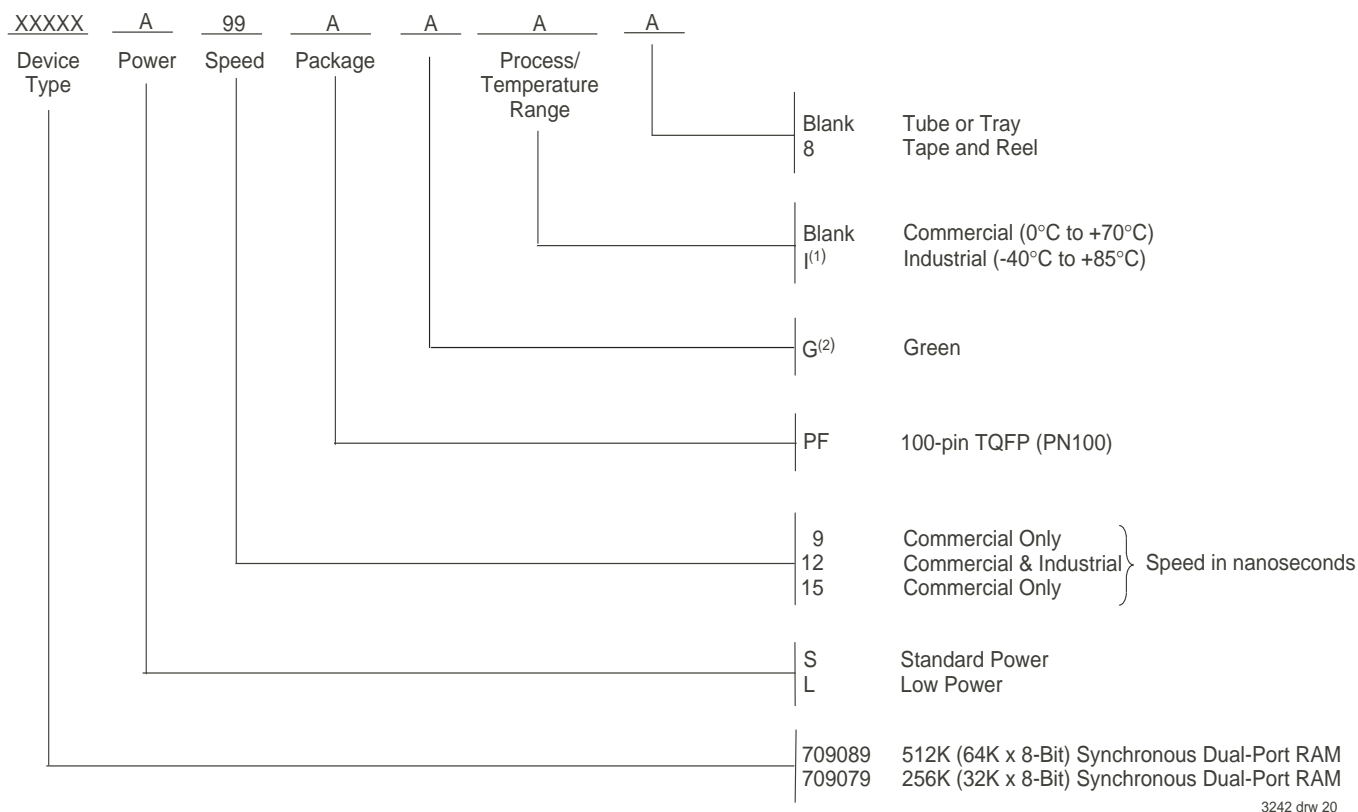

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Figure 4. Depth and Width Expansion with IDT709089/79

NOTE:
1. A_{15} is for IDT709089, A_{14} is for IDT709079.

Ordering Information

XXXXX   A   99   A   A   A   A

Device Type   Power   Speed   Package   Process/Temperature Range

Blank	Tube or Tray
8	Tape and Reel
Blank	Commercial (0°C to +70°C)
I[1]	Industrial (-40°C to +85°C)
G[2]	Green
PF	100-pin TQFP (PN100)
9	Commercial Only
12	Commercial & Industrial } Speed in nanoseconds
15	Commercial Only
S	Standard Power
L	Low Power
709089	512K (64K x 8-Bit) Synchronous Dual-Port RAM
709079	256K (32K x 8-Bit) Synchronous Dual-Port RAM

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NOTE:
1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your sales office.

Ordering Information for Flow-through Devices

Old Flow-through Part	New Combined Part
70908S/L20	709089S/L9
70908S/L25	709089S/L12
70908S/L30	709089S/L15

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Datasheet Document History

1/12/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
		Added additional notes to pin configurations
	Page 15	Added Depth and Width Expansion note
6/7/99:		Changed drawing format
	Page 4	Deleted note 6 for Table II
11/10/99:		Replaced IDT logo

Datasheet Document History (con't)

12/22/99:	Page 1	Removed "Separate upper-byte..." line
1/12/00:		Combined Pipelined 709089 family and Flow-through 70908 family offerings into one data sheet
		Changed ±200mV in waveform notes to 0mV
		Added corresponding part chart with ordering information
2/18/00:	Pages 8 & 9	Changed ±220mV waveform notes to 0mV
	Page 9	Changed "Operation" in heading to "Pipelined Output", fixed drawing 08
		Removed PGA package
5/24/00:	Page 3	Changed information in Truth Table II
	Page 4	Increased storage temperature parameters
		Clarified T_A parameter
	Page 5	DC Electrical parameters--changed wording from "open" to "disabled"
		Added Industrial Temperature Ranges and removed related notes
01/10/02:	Page 2	Added date revision for pin configuration
	Page 5 & 7	Removed industrial temp from column headings and values for 15ns from AC & DC Electrical Characteristics
	Page 16	Removed industrial offering from 15ns ordering info and added industrial temp footnote
	Page 1 & 17	Replaced IDT ™ logo with ® logo
06/21/04:		Consolidated multiple devices into one datasheet
		Removed Preliminary status from datasheet
	Page 4	Added Junction Temperature to Absolute Maximum Ratings Table
		Added Ambient Temperature footnote
	Page 5	Added 6ns & 7ns speed DC timing numbers to the DC Electrical Characteristics Table
	Page 8	Added 6ns & 7ns speed AC timing numbers to the AC Electrical Characteristics Table
	Page 17	Added 6ns & 7ns speed grades to ordering information
		Added IDT Clock Solution Table
	Page 1 & 18	Replaced old ® logo with new ™ logo
01/29/09:	Page 17	Removed "IDT" from orderable part number
07/26/10:	Page 1	Added green parts availability to features
	Page 17	Added green indicator to ordering information
	Page 8	In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial T_A header note has been removed
	Pages 9-13	In order to correct the footnotes of timing diagrams, $\overline{CNTEN}$ has been removed to reconcile the footnotes with the $\overline{CNTEN}$ logic definition found in Truth Table II - Address Counter Control
05/28/15:	Page 1	Updated speed offerings and cycle time in Features
	Page 2	Removed IDT in reference to fabrication
	Page 2	Removed date for the 100-PIN TQFP configuration
	Page 2 & 16	The package code PN100-1 changed to PN100 to match standard package codes
	Page 5	Removed X6 and X7 speed grades from the DC Elec Chars table and combined X9, X12 & X15 speed grades into one DC Elec Chars table
	Page 6	Corrected typo in the Typical Output Derating drawing
	Page 7	Removed X6 and X7 speed grades from the AC Elec Chars table
	Page 16	Added Tape and Reel indicator to, removed X6 & X7 speed grades and updated the commercial and industrial offerings in Ordering Information
	Page 16	Removed the IDT Clock Solution table
02/22/16:	Page 2	Changed diagram for the PN100 pin configuration by rotating the pin1 orientation counter clockwise by 90 degrees for accurate representation of the part and added the black dot as the pin 1 indicator
		Added the IDT logo to the pin configuration and changed the text to be in alignment with new diagram marking specs and rotated the pin names on the vertical sides to an upright position
		Updated footnote references for the PN100 pin configuration