Quad Freq LVDS+CMOS Oscillator

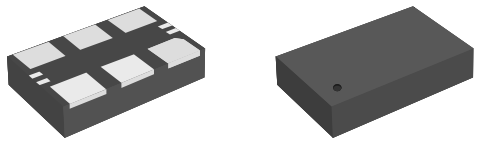
4EA1485A0Z4

148.5 / 74.25 / 148.35 / 74.175MHz with 27MHz CMOS

ADVANCE DATASHEET

Features

- 4 LVDS Frequencies: 148.5, 74.25, 148.35 & 74.175MHz
- 1 CMOS output: 27MHz
- Frequency Stability: ± 50ppm
- Supply Voltage: 2.5V and 3.3V
- Standard Packages: 7.0 x 5.0 mm
- RMS phase jitter: <1 ps typical (12k to 20MHz)
- Operating Temperature: - 40 to 85 °C

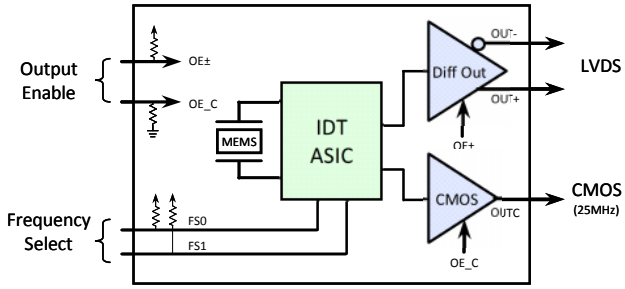


7.0 x 5.0 mm package

General Description

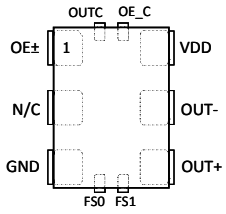
The 4EA1485A0Z4 is a quad frequency oscillator incorporating IDT's pMEMS technology to generate up to four LVDS clock frequencies. An additional synchronous CMOS output is also provided for general purpose clocking. One 4EA1485A0Z4 can replace up to 5 separate crystal oscillators, reducing inventory and bill-of-material cost. The pinout and footprint is backward compatible to industry standard 7050 size oscillators, ensuring second source compatibility to traditional 6 pin SMD oscillators.

Functional Block Diagram



Pin Description

Pin	Name	Description
1	OE±	LVDS Output Enable
6, 7	OUT+, OUT-	LVDS Output
2	N/C	No connect
3, 8	GND, VDD	Supply Voltage
4, 5	FS0, FS1	Frequency Select
9	OE_C	CMOS Output Enable
10	OUTC	CMOS Output



Frequency Table

Input*	Output (MHz)	
FS[1,0]	LVDS	CMOS
1,1	148.50	27.0
1,0	74.25	
0,1	148.35	26.973
0,0	74.175	

** FS0, FS1 includes weak pull-up resistor*

Enable/Disable

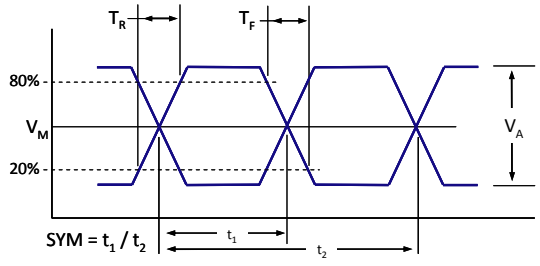
OE±*	LVDS
HI	ON
LOW	OFF

**Includes weak pull-up resistor*

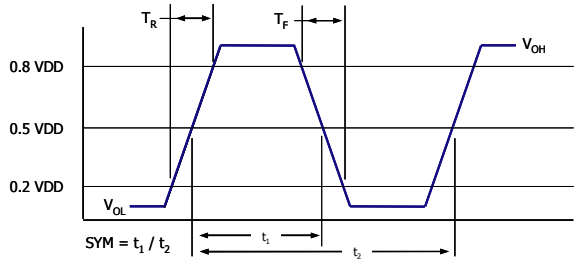
OE_C*	CMOS
HI	ON
LOW	OFF

**Includes weak pull-down resistor*

Output Waveform (LVDS)



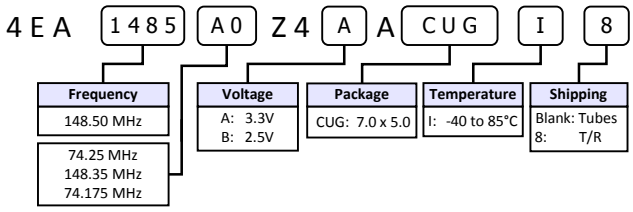
Output Waveform (CMOS)



Part Ordering Information

Package Size	Voltage	Ordering Code
7.0 x 5.0 mm	3.3V	4EA1485A0Z4AACUGI
	2.5V	4EA1485A0Z4BACUGI

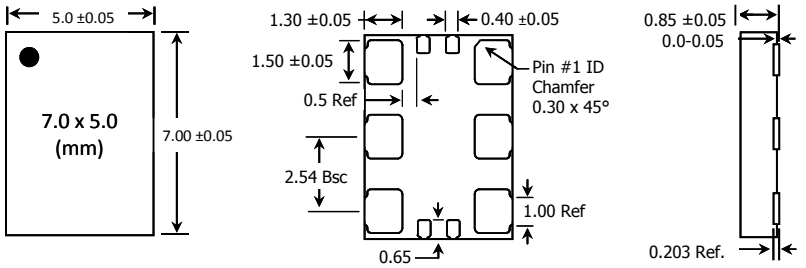
* Factory minimum order quantity: 500pcs (T/R)



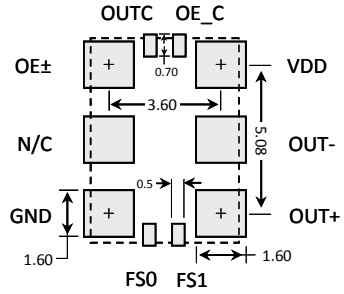
Specification

Parameter	2.5 V Specifications			3.3 V Specifications			Units	Conditions
	Min	Typ	Max	Min	Typ	Max		
Supply Voltage (V_{DD})	2.375	2.50	2.625	2.97	3.30	3.63	V	
Frequency Stability	- 50		+ 50	- 50		+ 50	ppm	Includes supply voltage and temperature variation (-40 to 85°C), reflow drift, and aging.
Supply Current		130			140		mA	No load
Enable/Disable Time			1			1	us	Guaranteed by design
Input HIGH/LOW level	0. $7V_{DD}$		$0.3V_{DD}$	0. $7V_{DD}$		$0.3V_{DD}$	V	At OE± & OE_C pins
Start-up Time		10			10		ms	Output valid time after power up, 25°C
Aging		± 5			± 5		ppm	25°C, 10 years
LVDS Output								
Output LOW level		1.05			1.05		V	
Output HIGH level		1.40			1.40		V	
Amplitude (V_A)		0.35			0.35		V	Single Ended output swing (Pk-Pk)
Mid Level (V_M)		1.22			1.22		V	
Rise Time (T_R)		370	420		410	520	ps	Maximum; 20/80% of V_A; Output load (CL) = 2pF; Guaranteed by Char.
Fall Time (T_F)		370	420		410	520	ps	Maximum; 20/80% of V_A; Output load (CL) = 2pF; Guaranteed by Char.
Symmetry (SYM)	48	50	52	48	50	52	%	Worst case; measured at 50% of waveform
Phase Jitter		1.0			0.9		ps	12k to 20MHz, RMS; Measured Differentially
Period Jitter		4.1			4.2		ps	RMS
Cycle-to-Cycle Jitter		32			32		ps	1,000 cycles, Peak
CMOS Output (27 MHz / 26.973 MHz)								
Rise/Fall Time (T_R/ T_F)		500			500		ps	Maximum; 20/80% of V_A; Output load (CL) = 15pF
Symmetry (SYM)	48		52	48		52	%	Worst case; measured at 50% of waveform
Output HIGH/LOW level	V_{DD} -0.3		0.3	V_{DD} -0.3		0.3	V	I_{OL}=8mA; I_{OH}=-8mA
Period Jitter (rms)		25			20		ps	Measured over 10k cycles
Cycle to Cycle Jitter		120			100		ps	1,000 cycles, Peak

Package Outline and Dimensions



Typical PCB Land Pattern



Unit: (mm)

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