

# TLE8458

LIN Transceiver with integrated Voltage Regulator

TLE8458G  
TLE8458GV33

## Data Sheet

Rev. 1.1, 2014-04-01

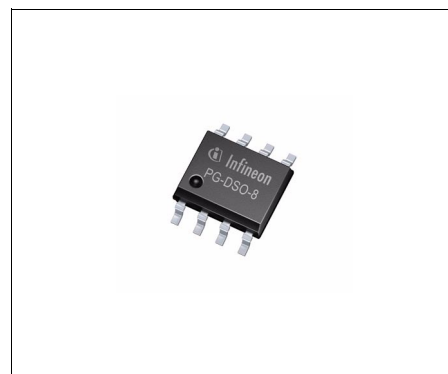
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## 1 Overview

### Features

- LIN Transceiver compliant to LIN 2.1
- 5 V or 3.3 V Low Drop Voltage Regulator
- 50 mA output current capability
- Normal, Stop, and Sleep modes
- Wake-up via bus from Sleep Mode
- Wake-up from Local WK pin
- Very low quiescent current in Stop Mode
- Very low quiescent current in Sleep Mode
- Very high ESD Robustness  $\pm 10$  kV according IEC61000-4-2
- Bus short to ground and  $V_{\text{Bat}}$  protection
- Software Flash mode
- Over-Temperature protection
- Pin- and function compatible to single LIN Transceivers, like TLE7259-3GE
- Green (RoHS compliant) product
- AEC Qualified



**PG-DSO-8-16**

### Description

The TLE8458G and TLE8458GV33 integrate a low drop voltage regulator and a LIN transceiver on one monolithic circuit. The device is suitable to supply microcontrollers and driving a LIN bus at the same time. The TLE8458 is pin compatible to stand-alone LIN transceivers like the TLE7259-3GE. The combination of a voltage regulator and a LIN transceiver on one circuit decreases the quiescent current for a typical application to a value of 8  $\mu\text{A}$ , while the TLE8458 is still able to wake-up off a LIN bus signal or a signal change on the local wake-up input WK. Compliant to all LIN standards and with a wide operational supply range, the TLE8458 can be used in all automotive applications.

Based on the Infineon Smart Power Technology SPT<sup>®</sup>, the TLE8458 provides excellent ESD robustness together with a very high electro-magnetic immunity (EMI). The TLE8458 reaches a very low level of electro-magnetic emission (EME) within a broad frequency range. The TLE8458 family and the Infineon SPT<sup>®</sup> technology are AEC qualified and tailored to withstand the harsh conditions in the automotive environment.

| Type        | Package     | Marking | Note                            |
|-------------|-------------|---------|---------------------------------|
| TLE8458G    | PG-DSO-8-16 | 8458G   | $V_{\text{CC}} = 5 \text{ V}$   |
| TLE8458GV33 | PG-DSO-8-16 | 8458GV3 | $V_{\text{CC}} = 3.3 \text{ V}$ |

## 2 Block Diagram

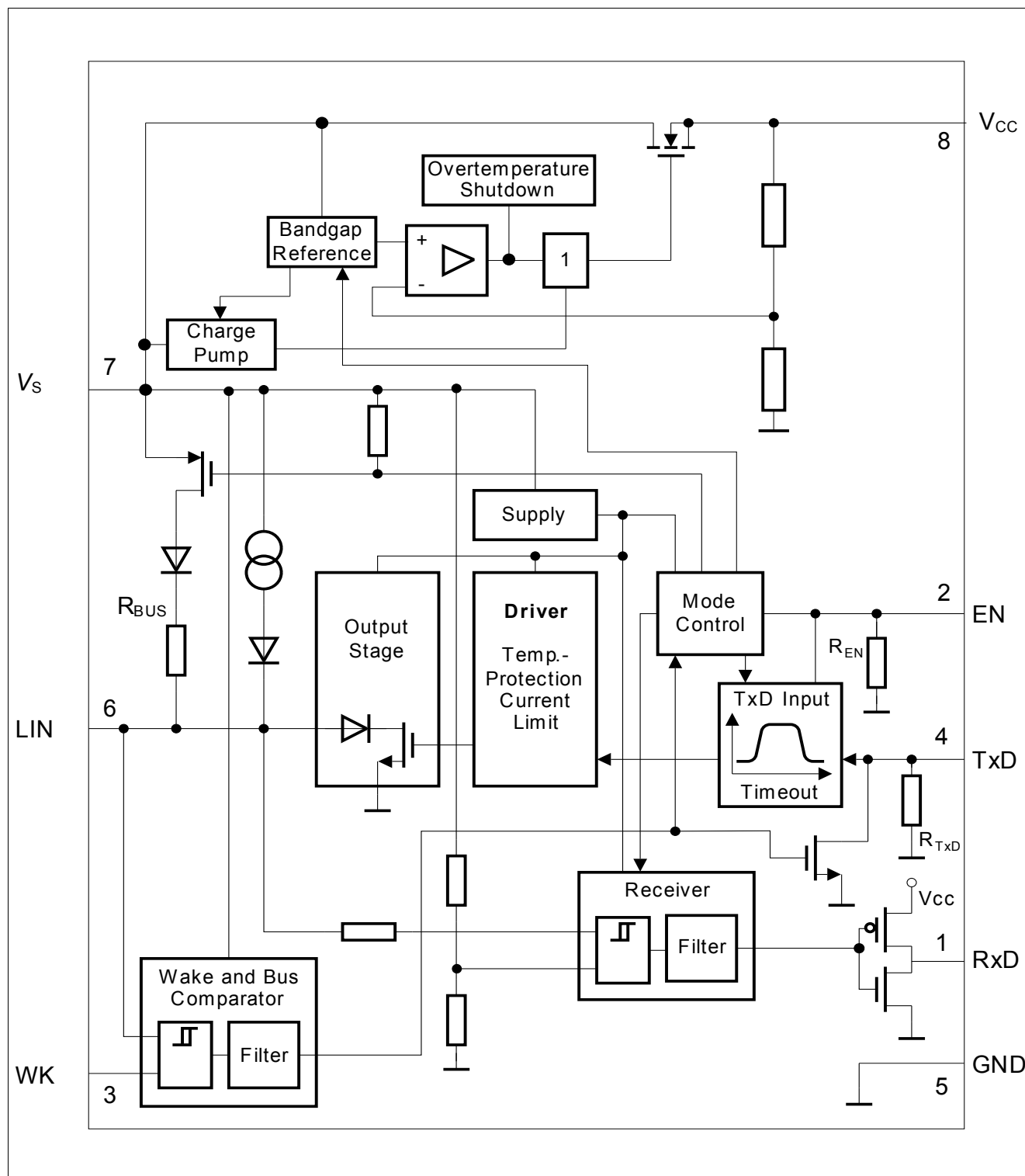


Figure 1 Block Diagram

## 3 Pin Configuration

### 3.1 Pin Assignments

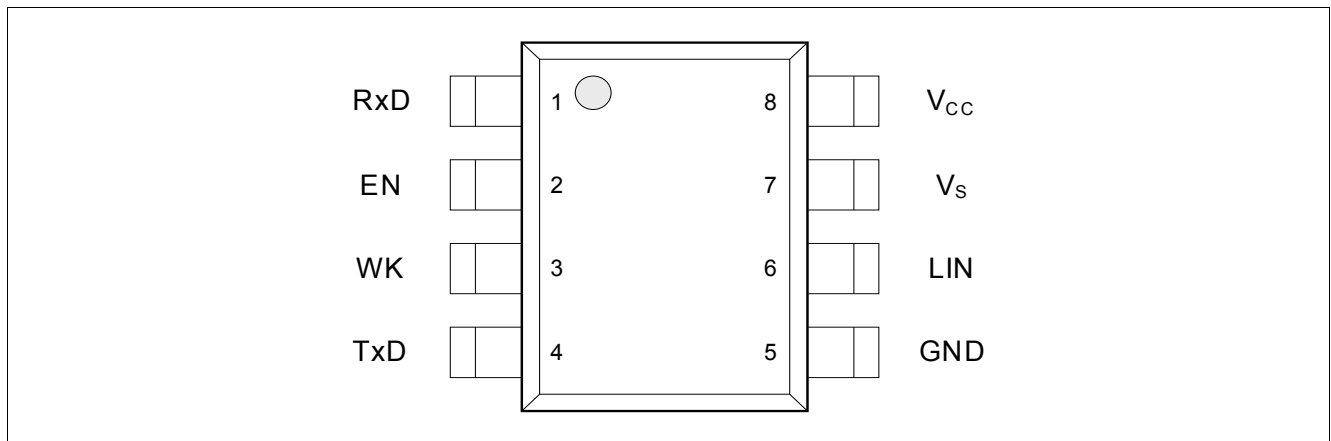


Figure 2 Pin Configuration

### 3.2 Pin Definitions and Functions

Table 1 Pin Definition

| Pin | Symbol   | Function                                                                                                                                                                     |
|-----|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | RxD      | <b>Receive Data Output;</b><br>Low in dominant state, active low after a Wake-up event on BUS or WK pin.                                                                     |
| 2   | EN       | <b>Enable Input;</b><br>Integrated pull-down resistor, device set to normal operation mode when HIGH.                                                                        |
| 3   | WK       | <b>Wake-up Input;</b><br>Active LOW, negative edge triggered, internal pull-up.                                                                                              |
| 4   | TxD      | <b>Transmit Data Input;</b><br>Integrated pull-down resistor, LOW in dominant state. Active LOW after Wake-up via WK pin.                                                    |
| 5   | GND      | <b>Ground</b>                                                                                                                                                                |
| 6   | LIN      | <b>Bus Output / Input;</b><br>LIN bus input / Output,<br>LOW in dominant state,<br>Internal termination and pull-up current source.                                          |
| 7   | $V_S$    | <b>Battery Supply Input</b>                                                                                                                                                  |
| 8   | $V_{CC}$ | <b>Output Voltage;</b><br>Decouple to GND with a capacitor $C_{VCC} \geq 470 \text{ nF}$ , $ESR < 6 \Omega$ at 10 kHz,<br>Active during Normal Mode, disabled in Sleep Mode. |

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings** <sup>1)</sup>

All voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

| Parameter                               | Symbol        | Values |      |      | Unit | Note /<br>Test Condition | Number  |
|-----------------------------------------|---------------|--------|------|------|------|--------------------------|---------|
|                                         |               | Min.   | Typ. | Max. |      |                          |         |
| Voltages                                |               |        |      |      |      |                          |         |
| Supply Voltage on $V_S$ pin             | $V_S$         | -0.3   | –    | 40   | V    | LIN2.1 Param 11          | P_4.1.1 |
| Input Voltage on LIN, WK pin versus GND | $V_{LIN,G}$   | -40    | –    | 40   | V    | –                        | P_4.1.2 |
| Logic Voltages at EN, TxD, RxD pin      | $V_{L,max}$   | -0.3   | –    | 5.5  | V    | –                        | P_4.1.3 |
| Output Voltage at $V_{CC}$ pin          | $V_{CC}$      | -0.3   | –    | 5.5  | V    | Static                   | P_4.1.4 |
| Temperatures                            |               |        |      |      |      |                          |         |
| Junction Temperature                    | $T_j$         | -40    | –    | 150  | °C   | –                        | P_4.1.5 |
| Storage Temperature                     | $T_{stg}$     | -55    | –    | 150  | °C   | –                        | P_4.1.6 |
| ESD Resistivity                         |               |        |      |      |      |                          |         |
| ESD all pins                            | $V_{ESD,HBM}$ | -2     | –    | 2    | kV   | HBM <sup>2)</sup>        | P_4.1.7 |
| ESD $V_S$ , WK, LIN versus GND          | $V_{ESD,HBM}$ | -8     | –    | 8    | kV   | HBM <sup>2)</sup>        | P_4.1.8 |
| ESD Resistivity all pins versus GND     | $V_{ESD,CDM}$ | -750   | –    | 750  | V    | CDM <sup>3)</sup>        | P_4.1.9 |

1) Not subject to production test; specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100pF)

3) ESD susceptibility, Charged Device Model "CDM" EIA / JESD 22-C101 or ESDA STM5.3.1

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

## 4.2 Functional Range

**Table 3 Functional Range**

| Parameter                           | Symbol       | Values |      |      | Unit | Note / Test Condition         | Number  |
|-------------------------------------|--------------|--------|------|------|------|-------------------------------|---------|
|                                     |              | Min.   | Typ. | Max. |      |                               |         |
| Extended Supply Range               | $V_{S(EXT)}$ | 5.5    | –    | 40   | V    | Parameter deviations possible | P_4.2.1 |
| Supply Voltage for Normal Operation | $V_{S(Nor)}$ | 7      | –    | 27   | V    | LIN 2.1 Param. 11             | P_4.2.3 |
| Junction Temperature                | $T_j$        | -40    | –    | 150  | °C   | –                             | P_4.2.2 |

*Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Characteristics

**Table 4 Thermal Resistance**

| Parameter                             | Symbol              | Values |      |      | Unit | Note /<br>Test Condition | Number  |
|---------------------------------------|---------------------|--------|------|------|------|--------------------------|---------|
|                                       |                     | Min.   | Typ. | Max. |      |                          |         |
| Thermal Resistance                    |                     |        |      |      |      |                          |         |
| Junction to Case<br>PG-DSO-8-16       | $R_{thJC,G}$        | –      | 55   | –    | K/W  | 1)                       | P_4.3.1 |
| Junction to Ambient<br>PG-DSO-8-16    | $R_{thJA,G}$        | –      | 120  | –    | K/W  | 1), 2)                   | P_4.3.2 |
| Thermal Shutdown Junction Temperature |                     |        |      |      |      |                          |         |
| $V_{CC}$ Shutdown Temperature         | $T_{SD,Vcc}$        | 150    | –    | 200  | °C   | 3)                       | P_4.3.5 |
| $V_{CC}$ Thermal Shutdown Hysteresis  | $\Delta T_{SD,Vcc}$ | –      | 35   | –    | K    | 3)                       | P_4.3.6 |
| LIN Shutdown Temperature              | $T_{SD,LIN}$        | 150    | –    | 200  | °C   | 3)                       | P_4.3.7 |
| LIN Thermal Shutdown Hysteresis       | $\Delta T_{SD,LIN}$ | –      | 10   | –    | K    | 3)                       | P_4.3.8 |

1) Not subject to production test. Simulated thermal resistance

2) The  $R_{thJA}$  values are according to Jedec JESD51-2,-7 at natural convection on 2s2p board for 1 W. Package was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (70 µm thick).

3) Not subject to production test, specified by design.

## 5 Mode Control

### 5.1 Operation Mode State Diagram

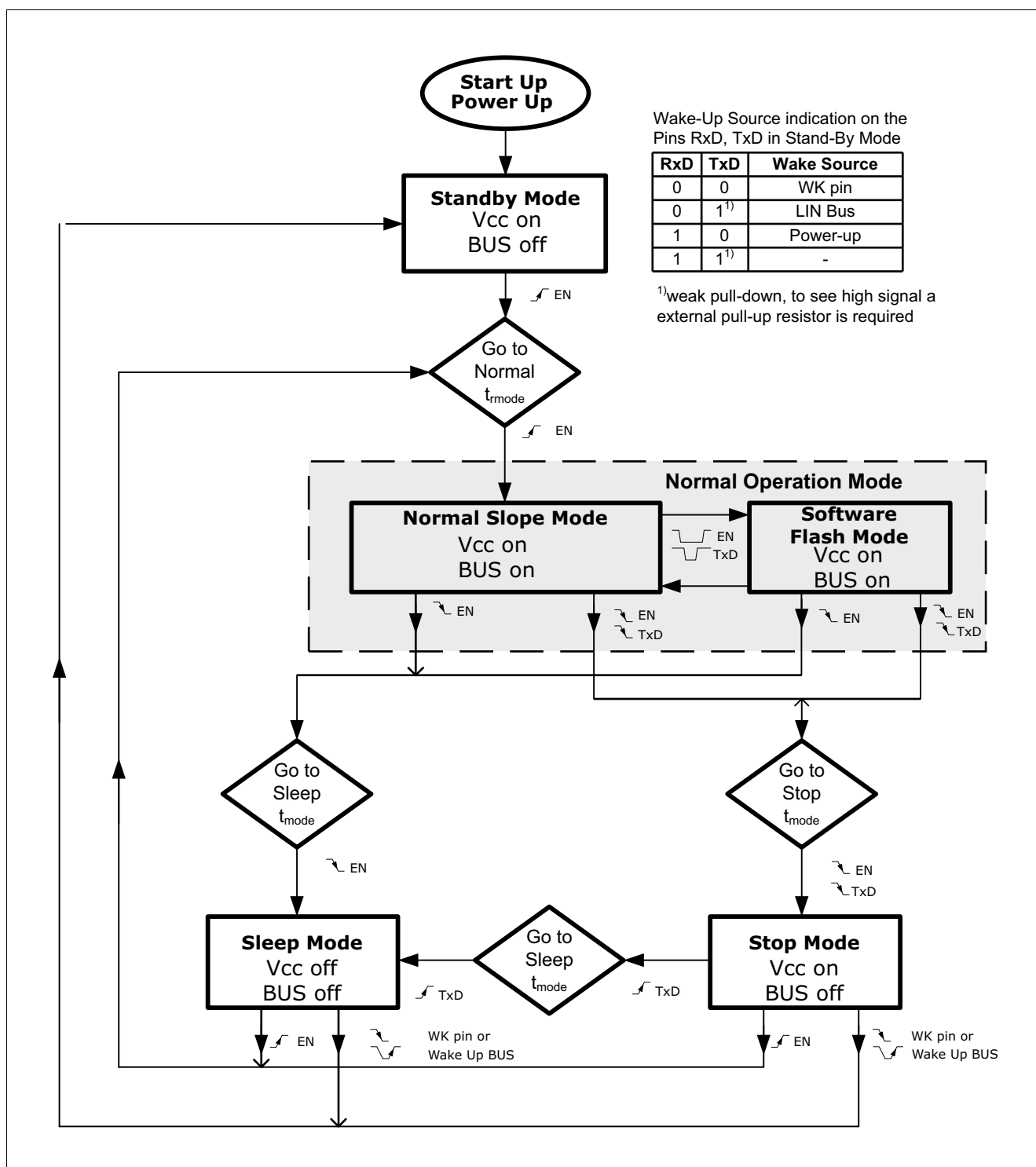


Figure 3 Operation Mode State Diagram



## 5.2 Description of Mode Control

The TLE8458 has 4 major operation modes:

- Normal Operation Mode
- Stand-By Mode
- Sleep Mode
- Stop Mode

The Normal Operation mode contains 2 sub-operation modes, which differentiate by the slew rate control of the LIN Bus signal (see [Figure 3](#)).

Sub-operation modes with different slew rates on the BUS pin:

- Normal Slope Mode, for data transmission rates up to 20 kBaud
- Software Flash mode, for programming of the external microcontroller

The operation mode of the TLE8458 is selected by the EN pin and the TxD pin. (see [Table 5](#), see [Figure 4](#)).

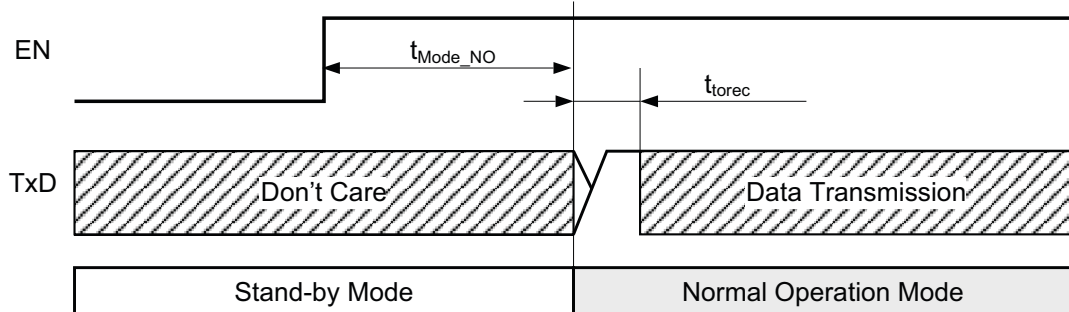
**Table 5 Operation Modes**

| Mode                  | EN   | TxD                       | RxD         | $V_{CC}$ | LIN Bus Termination        | Comments                                                           |
|-----------------------|------|---------------------------|-------------|----------|----------------------------|--------------------------------------------------------------------|
| Normal Operation Mode | HIGH | LOW<br>HIGH <sup>1)</sup> | LOW<br>HIGH | ON       | 30 k $\Omega$<br>(typical) | TxD drives the data to the bus, RxD indicates the data on the bus. |
| Stand-By Mode         | LOW  | LOW<br>HIGH <sup>2)</sup> | LOW<br>HIGH | ON       | 30 k $\Omega$<br>(typical) | In Stand-By Mode the RxD and TxD pins indicate the Wake-up source  |
| Sleep Mode            | LOW  | HIGH                      | Float       | OFF      | High Impedance             | For Sleep Mode TxD needs to be HIGH for the time $t_{mode1}$       |
| Stop Mode             | LOW  | LOW                       | Float       | ON       | High Impedance             | For Stop Mode TxD needs to be LOW for the time $t_{mode1}$         |

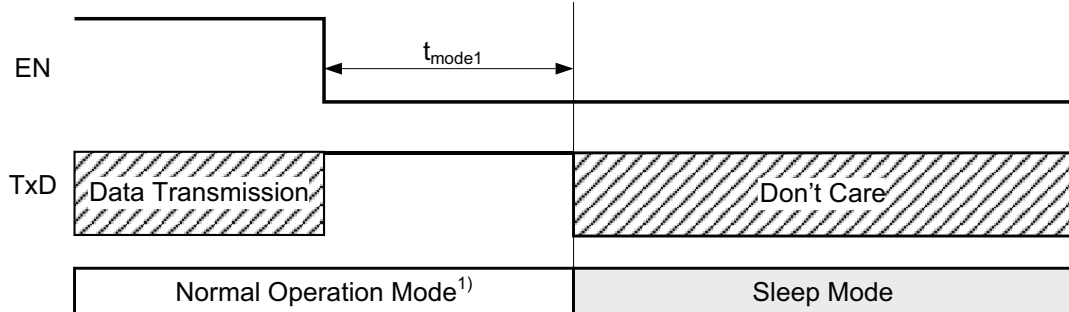
1) The TxD pin acts as an input

2) The TxD pin acts as an output and indicates the Wake-up source. The TxD input needs an external termination to indicate a HIGH or a LOW signal. The external termination could be a pull-up resistor or an active microcontroller output.

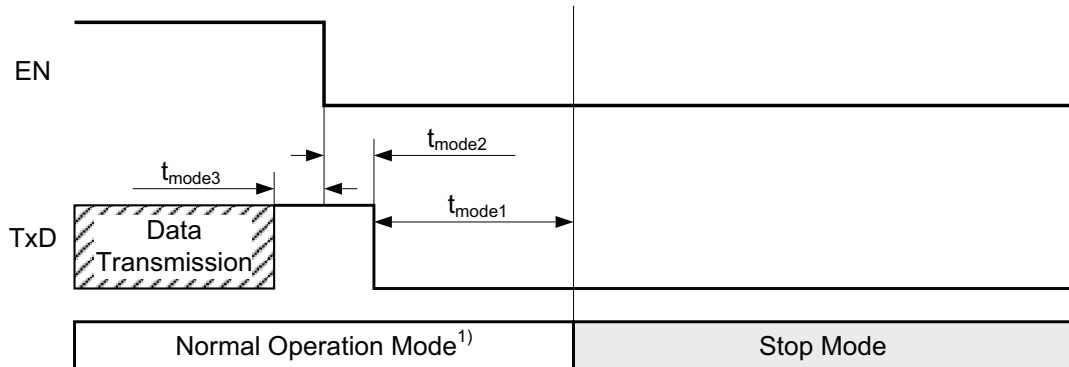
### Stand-By Mode to Normal Operation Mode



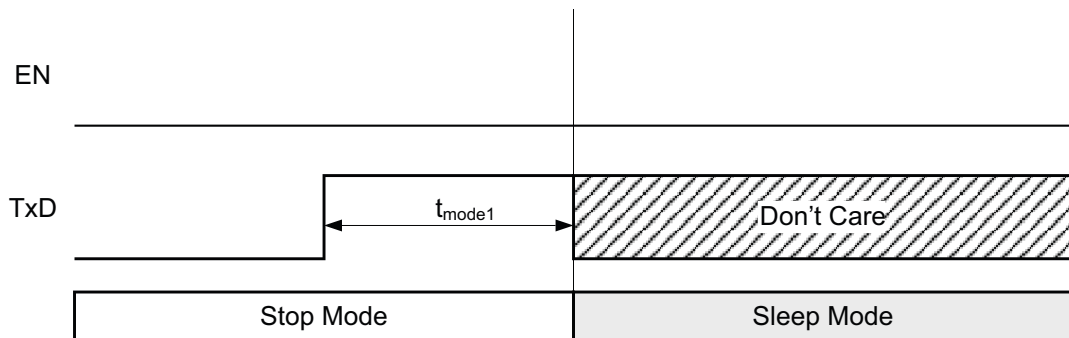
### Normal Operation Mode<sup>1)</sup> to Sleep Mode



### Normal Operation Mode<sup>1)</sup> to Stop Mode



### Stop Mode to Sleep Mode



<sup>1)</sup> Normal Operation Mode can be either Normal Slope Mode or Software Flash Mode

**Figure 4 Mode Transition**

### 5.2.1 Stand-By Mode

The Stand-By Mode is an idle operation mode, which disables the communication to the LIN bus. The TLE8458 enters automatically the Stand-By Mode after a Power-up. By setting the EN pin to HIGH, the operation mode changes to Normal Operation Mode, regardless of the signal applied to the TxD pin.

The TLE8458 can be transferred to Stand-By mode by the following options:

- After Power-up on the supply  $V_S$ , the TLE8458 starts in Stand-By Mode.
- From Sleep Mode or from Stop Mode the TLE8458 changes to Stand-By Mode if a Wake-up event occurs on the LIN bus.
- From Sleep Mode or from Stop Mode the TLE8458 changes to Stand-By Mode if a Wake-up event occurs on the local Wake input WK.
- In case of an undervoltage event on  $V_S$ , the TLE8458 changes to Stand-By Mode regardless of selected operation mode.

In Stand-By mode the external power supply  $V_{CC}$  is active and LIN bus output stage is disabled. The TLE8458 provides the following functionality in Stand-By Mode:

- The power supply  $V_{CC}$  is active and functional.
- The LIN transceiver output stage is disabled, no communication to the LIN bus is possible.
- The LIN transceiver bus input receiver is disabled.
- The LIN bus is terminated by the 30 k $\Omega$ .
- Both digital pins, the TxD pin and the RxD pin act as output pins and indicate a Wake-up or a Power-up event<sup>2)</sup>.
- The EN input pin is active. By setting the EN pin to HIGH the TLE8458 changes the operation mode to Normal Operation Mode (see [Figure 3](#)).
- The Wake-up logic is disabled. Wake-up events don't trigger an operation mode change.

**Table 6** Logic table for Wake-up monitoring<sup>1)</sup>

| Power-up | Wake-up event | RxD  | TxD <sup>2)</sup> | Comments                      |
|----------|---------------|------|-------------------|-------------------------------|
| Yes      | No            | HIGH | LOW               | Power Up event                |
| No       | Via LIN Bus   | LOW  | HIGH              | Wake-up via LIN Bus           |
| No       | Via WK Pin    | LOW  | LOW               | Wake-up via local Wake pin WK |

1) The Wake-up monitor is only active in Stand-By Mode

2) The TxD input needs an external termination to indicate a "High" or a "Low" signal. The external termination could be a pull-up resistor or an active microcontroller output.

### 5.2.2 Normal Operation Mode

The TLE8458 enters the Normal Operation Mode after the microcontroller sets EN to "High" (see [Figure 4](#)). In Normal Operation mode the LIN bus receiver and the LIN bus transmitter are active. The TLE8458 converts the logical HIGH and LOW signals on the TxD input pin to DOMINANT and RECESSIVE signals to the LIN bus. Simultaneously the input receiver of the TLE8458 converts the DOMINANT and RECESSIVE signals on the LIN bus to HIGH and LOW signals to the RxD output. In Normal Operation mode the output voltage  $V_{CC}$  is active and the bus termination is set to 30 k $\Omega$ .

Normal Slope Mode and the Software Flash Mode are Normal Operation Modes. In these two sub-modes the behavior of the power supply  $V_{CC}$  and the bus termination are the same. Per default the TLE8458 always enters into Normal Slope Mode, either from Sleep Mode, Stop Mode or from Stand-By Mode. The Software Flash Mode can only be entered from Normal Slope mode.

In order to avoid any bus disturbance during a mode change, the output stage of the TLE8458 is disabled and set to recessive state during the mode change procedure. To release the TLE8458 for data communication on the LIN bus, the TxD pin needs to be set to HIGH for the time  $t_{\text{to rec}}$  after the operation mode change.

### 5.2.2.1 Normal Slope Mode

In Normal Slope Mode the maximum data transmission rate of the LIN transceiver is limited by the slope control mechanism of LIN output signal. The limitation of the slew rate of the LIN output signal results in an optimized radiated emission fulfilling automotive EMC requirements.

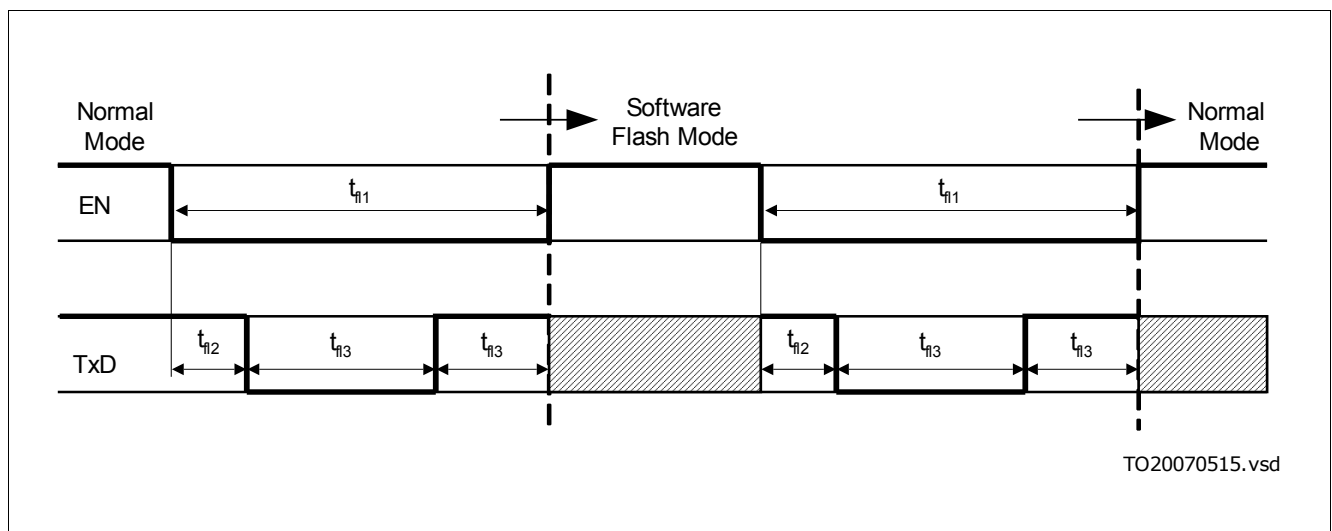
The data transmission rate of the TLE8458G and the TLE8458GV33 is limited to 20 kBaud in Normal Operation Mode and the devices are compliant to the specification LIN2.1.

### 5.2.2.2 Software Flash Mode

Software Flash Mode is a Normal Operation Mode and it is possible to transmit data to the LIN bus and receive data from the LIN bus. The slope control mechanism of the LIN transmitter output stage is disabled and therefore it is possible to reach higher data transmission rates, disregarding the EMC limitation of the LIN network. The Software Flash Mode can be used for programming the external microcontroller via the LIN bus, got example during the production flow of the ECU.

The Software Flash Mode can only be entered from Normal Slope Mode (see [Figure 3](#)). By setting the EN pin to low for the time  $t_{\text{fl1}}$  and by generating a falling and a rising edge at the TxD pin with the time  $t_{\text{fl2}}$  and  $t_{\text{fl3}}$  during the low phase of the EN pin, the TLE8458 changes to the Software Flash Mode (see [Figure 5](#)). Vice versa, the TLE8458 changes from Software Flash Mode to Normal Slope Mode by applying the same sequence to the EN pin and the TxD pin.

In any case, regardless if the device is in Normal Slope Mode or in Software Flash Mode, a LOW signal on the EN pin changes the operation mode to Sleep Mode or Stop Mode. The slope control mechanism will be activated, when the device changes to the Normal Operation Mode again.



**Figure 5** Software Flash Mode

### 5.2.3 Stop Mode

The Stop Mode is a Low Power Mode, meaning the quiescent current of the TLE8458 is reduced to a minimum, while the device is still able to recognize Wake-up events. The following functions are available in Stop Mode:

- The power supply  $V_{CC}$  is active and functional.
- The LIN transceiver output stage is disabled, no communication to the LIN bus is possible.
- The LIN transceiver input receiver is disabled.
- The internal LIN bus termination is switched off.
- The TxD input and the RxD output is inactive.
- The EN input is active. A HIGH signal on the EN pin changes the operation mode to Normal Operation Mode.
- The LIN bus Wake-up receiver is active, a Wake-up event on the LIN bus changes the operation mode to Stand-By Mode.
- The wake input WK is active, a Wake-up event on the WK pin changes the operation mode to Stand-By Mode.

Entering Stop Mode is only possible from the Normal Operation Mode, regardless if the device is in Normal Slope Mode or Software Flash Mode. Setting the signal on the EN pin to LOW, followed by a LOW signal on the TxD pin for the time  $t_{Mode1}$  changes the operation mode to Stop Mode (see [Figure 4](#)).

### 5.2.4 Sleep Mode

The Sleep Mode is a Low Power Mode as well, in comparison to the Stop Mode, the quiescent current of the TLE8458 is even further reduced. In Sleep Mode the TLE8458 is able as well to recognize Wake-up events.

The Wake-up behavior in Sleep Mode is the same as in Stop Mode. The only difference between Sleep Mode and Stop Mode is, that in Stop Mode the output voltage  $V_{CC}$  is active, in Sleep Mode the output voltage  $V_{CC}$  is disabled.

Sleep Mode can be entered from Normal Operation Mode by setting the EN pin to LOW and simultaneously setting the TxD pin to HIGH for the time  $t_{Mode1}$  (see [Figure 4](#)). The Sleep Mode can be also entered from Stop Mode, by setting the signal on the TxD pin to HIGH for the time  $t_{Mode1}$ .

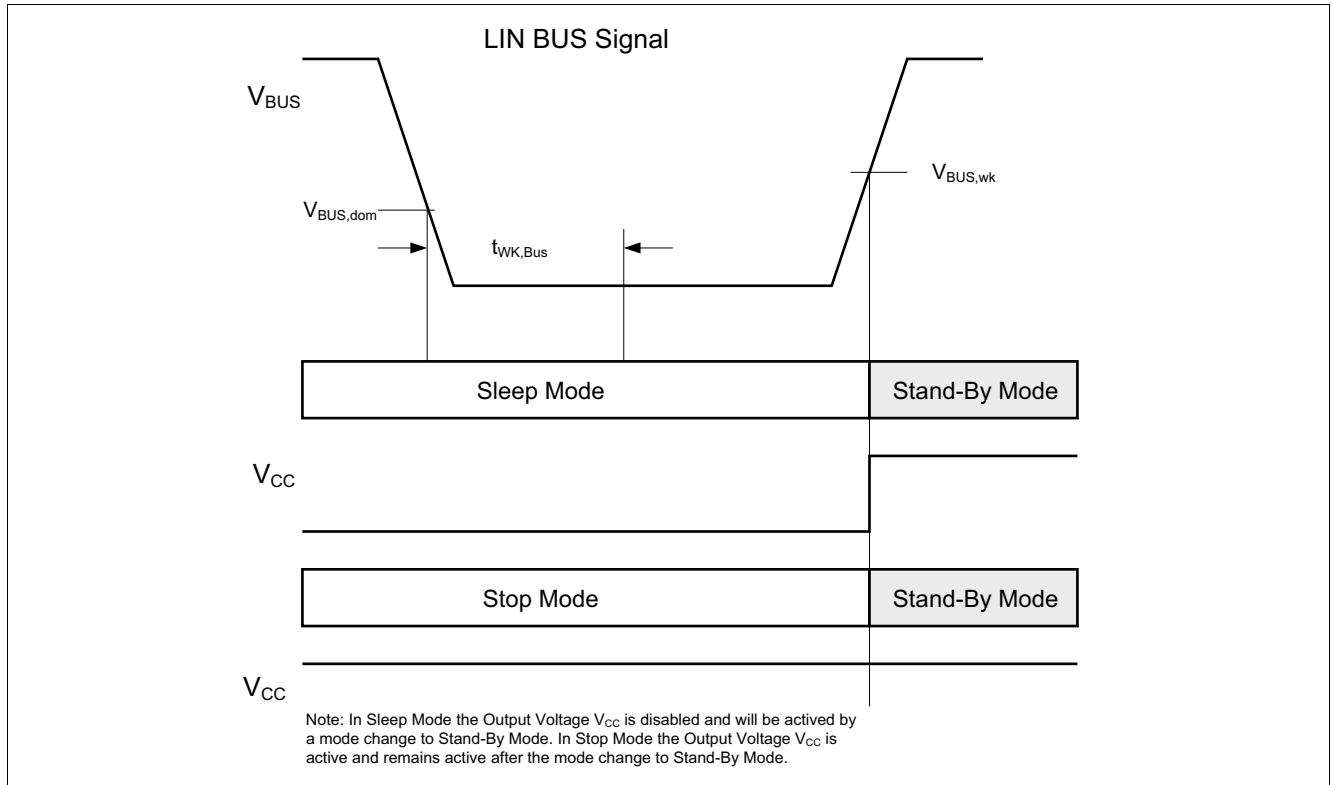
### 5.2.5 Wake-up Events in Sleep and Stop Mode

A Wake-up event in Sleep Mode or Stop Mode changes the operation mode of the TLE8458 to Stand-By Mode. There are 3 different options to Wake-up the TLE8458 from Sleep Mode or Stop Mode:

- A bus Wake-up event, caused by a message on the LIN bus.
- A local Wake-up event, caused by a logical LOW signal on the WK pin.
- A signal change to logical HIGH on the EN pin.

### 5.2.5.1 Bus Wake-up Event

A falling edge on the LIN bus, followed by a dominant bus signal for the time  $t > t_{wk,Bus}$  causes a bus Wake-up or also called remote Wake-up. The mode change becomes active with the following rising edge on the LIN bus (see [Figure 6](#)). In Stand-By Mode the Wake-up source is indicated by the TxD and RxD pins (see [Table 6](#)).



**Figure 6** Bus Wake-up

### 5.2.5.2 Local Wake-up Event

A Wake-up via LOW signal on the pin WK is called local Wake-up. A falling edge of the signal on the pin WK followed by a LOW signal for the time  $t > t_{WK}$  change the operation mode from Sleep Mode or Stop Mode to Stand-By Mode. In the case the LOW signal is shorter then the time  $t < t_{WK}$ , the Wake-up is ignored and the TLE8458 remains in Sleep Mode or Stop Mode. In Stand-By Mode the Wake-up source is indicated by the TxD and RxD pins (see [Table 6](#)). In order to avoid unintended Wake-up's via the local wake pin Wk, the Wk pin should get connected by a serial resistor to the power supply Vs (see [Figure 15](#)). Before the TLE8458 enters into Sleep Mode it is required to set the Voltage on the WK pin to the Vs power supply.

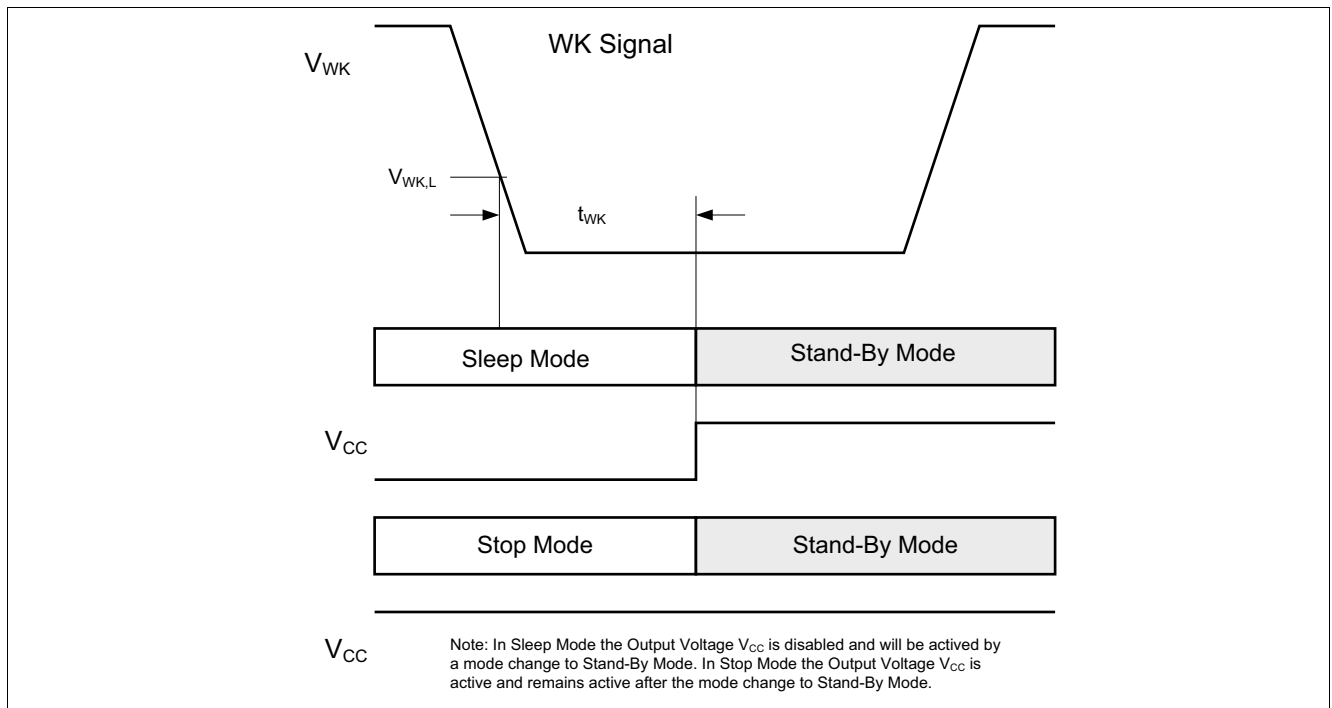


Figure 7 Local Bus Wake-up

### 5.2.5.3 Mode Transition via EN pin

The EN pin is used for the mode selection. In case the power supply  $V_{CC}$  is present, like in Stop Mode or Sleep Mode, the TLE8458 can be directly transferred into Normal Operation Mode by setting the EN pin to HIGH. An integrated pull-down resistor at the EN pin avoids mode changes due to floating signals on the EN input. The TLE8458 changes the operation mode to Normal Operation Mode, from Stop Mode or from Sleep Mode if the EN pin is HIGH for the time  $t > t_{Mode1}$  (see Figure 8). An integrated hysteresis on the EN pin avoids bit toggling. The mode transition via the EN pin will not be indicated in Stand-By Mode.

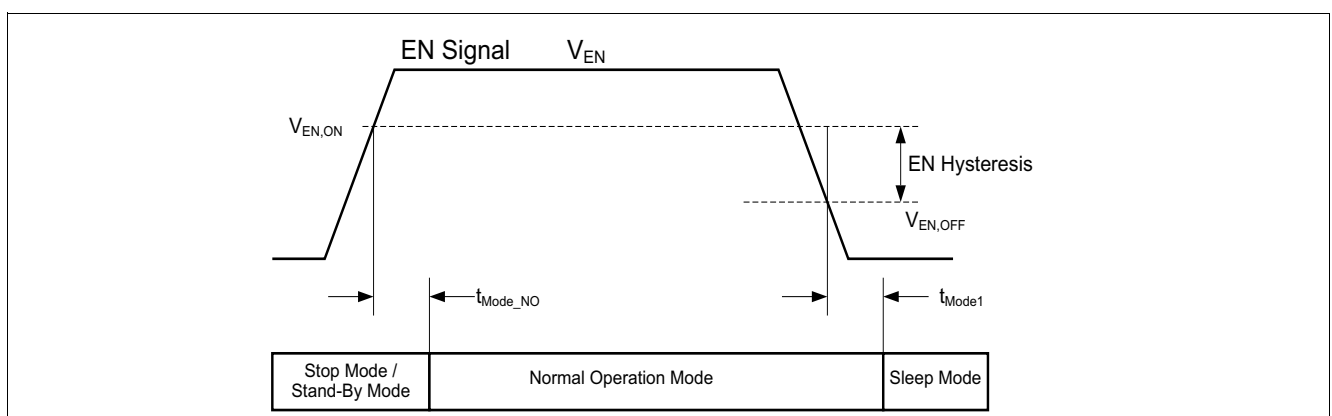


Figure 8 Mode Transition via EN pin

### 5.2.6 Power Up

After a Power-up the device enters per default into Stand-By Mode. Above  $V_{S,PU}$  the  $V_{CC}$  output voltage follows the supply  $V_S$  closely. In Stand-By Mode, the Power-up is indicated by a HIGH signal on the RxD pin and a LOW signal on the TxD pin.

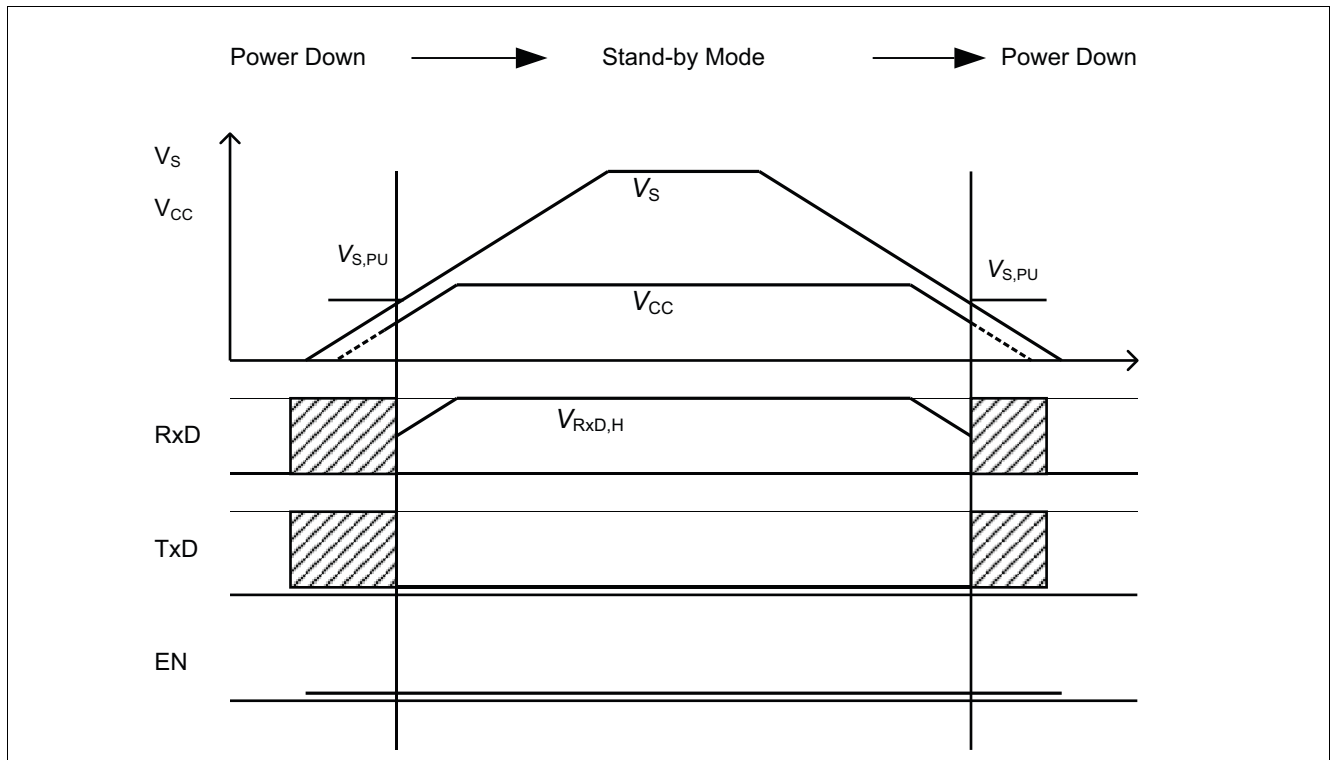


Figure 9 Power-up Level

### 5.2.7 Over-Temperature Protection

The TLE8458 is protected against thermal over-heating. Over-heating could be caused by a short circuit on the  $V_{CC}$  power supply or by a permanent short on the LIN bus combined with a high ambient temperature. In case of an over-temperature event, the TLE8458 eliminates the root cause of the over-temperature event. Two different temperature sensors are implemented inside the TLE8458. One temperature sensor protects the voltage regulator and controls the output voltage  $V_{CC}$ , the second temperature sensor protects the LIN transmitter output stage.

In case the junction temperature on the LIN output stage raises above the threshold  $T > T_{SD,LIN}$ , the temperature sensor disables the LIN output stage. The TLE8458 is still able to receive data from the LIN bus. If the temperature falls below the threshold,  $T < T_{SD,LIN}$ , the output stage will be enabled and the communication can start again. An integrated hysteresis on the temperature sensor avoids toggling during over-temperature events. An over-temperature event on the LIN bus will not cause any operation mode change.

In case the junction temperature on the  $V_{CC}$  power output stage raises above the threshold  $T > T_{SD,VCC}$ , the temperature sensor shuts down the output voltage  $V_{CC}$ . If the junction temperature falls below the threshold,  $T < T_{SD,VCC}$ , the power supply  $V_{CC}$  will be enabled again. An integrated hysteresis on the temperature sensor avoids toggling during over-temperature events.



### 5.3 Current Consumption

**Table 7 Electrical Characteristics: Current Consumption**

$V_S = 13.5 \text{ V}$ ,  $T_j = -40 \text{ }^\circ\text{C} \text{ } +150 \text{ }^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                                                | Symbol                | Values |      |      | Unit          | Note /<br>Test Condition                                                                                                        | Number  |
|--------------------------------------------------------------------------|-----------------------|--------|------|------|---------------|---------------------------------------------------------------------------------------------------------------------------------|---------|
|                                                                          |                       | Min.   | Typ. | Max. |               |                                                                                                                                 |         |
| Current Consumption                                                      |                       |        |      |      |               |                                                                                                                                 |         |
| Current Consumption<br>in Normal Mode<br>at $V_S$ in LIN Recessive State | $I_{S\_rec}$          | —      | 1.3  | 2.2  | mA            | Recessive state,<br>without $R_L$ ;<br>$V_{TXD} = V_{CC}$ ;<br>$I_{CC} = 100\text{ }\mu\text{A}$                                | P_5.3.1 |
| Current Consumption<br>in Normal Mode<br>at $V_S$ in LIN Dominant State  | $I_{S\_dom}$          | —      | 1.8  | 3.2  | mA            | Dominant state,<br>without $R_L$ ;<br>$V_{TXD} = 0\text{ V}$ ;<br>$I_{CC} = 100\text{ }\mu\text{A}$                             | P_5.3.2 |
| Current Consumption at $V_S$<br>in Sleep Mode                            | $I_{S\_sleep}$        | —      | 8    | 12   | $\mu\text{A}$ | Sleep Mode,<br>$-40\text{ }^{\circ}\text{C} < T_j < 85\text{ }^{\circ}\text{C}$ ;<br>$V_{LIN} = V_S$ ;<br>$V_{CC} = 0\text{ V}$ | P_5.3.3 |
| Current Consumption at $V_S$<br>in Stop Mode                             | $I_{S\_stop}$         | —      | —    | 40   | $\mu\text{A}$ | Stop Mode;<br>$-40\text{ }^{\circ}\text{C} < T_j < 85\text{ }^{\circ}\text{C}$ ;<br>$V_{LIN} = V_S$ ;<br>no load on $V_{CC}$    | P_5.3.4 |
| Current Consumption<br>in Sleep Mode, Bus Shorted to<br>Ground           | $I_{S\_sleep\_short}$ | 6      | 40   | 72   | $\mu\text{A}$ | Sleep Mode,<br>$V_{LIN} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$                                                                  | P_5.3.5 |

## 5.4 Electrical Characteristics EN and WK Pins

**Table 8 Electrical Characteristics: Mode Pins**

$7\text{ V} < V_S < 27\text{ V}$ ,  $T_j = -40\text{ }^{\circ}\text{C} \text{ } +150\text{ }^{\circ}\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                                             | Symbol                | Values |      |      | Unit | Note /<br>Test Condition                        | Number   |
|-----------------------------------------------------------------------|-----------------------|--------|------|------|------|-------------------------------------------------|----------|
|                                                                       |                       | Min.   | Typ. | Max. |      |                                                 |          |
| EN Pin                                                                |                       |        |      |      |      |                                                 |          |
| HIGH Level Input Voltage                                              | $V_{\text{EN,H}}$     | 2      | –    | –    | V    | –                                               | P_5.4.6  |
| LOW Level Input Voltage                                               | $V_{\text{EN,L}}$     | –      | –    | 0.8  | V    | –                                               | P_5.4.7  |
| EN Input Hysteresis                                                   | $V_{\text{EN,hys}}$   | –      | 0.3  | –    | V    | –                                               | P_5.4.8  |
| EN pull-down Resistance                                               | $R_{\text{EN}}$       | 20     | 40   | 80   | kΩ   | –                                               | P_5.4.9  |
| Filter Time for Mode Change                                           | $t_{\text{mode1}}$    | 50     | –    | 150  | μs   | –                                               | P_5.4.10 |
| TxD low delay time                                                    | $t_{\text{mode2}}$    | 0      | –    | 50   | μs   | Stop Mode transfer                              | P_5.4.11 |
| TxD high time                                                         | $t_{\text{mode3}}$    | 10     | –    | –    | μs   | Stop Mode transfer                              | P_5.4.12 |
| Time for Mode Change from Stop or Sleep Mode to Normal Operation Mode | $t_{\text{Mode\_NO}}$ | –      | 10   | –    | μs   | <sup>1)</sup> Transfer to Normal Operation Mode | P_5.4.1  |
| Time for Flash Mode activation                                        | $t_{\text{fl1}}$      | 25     | –    | 50   | μs   | <sup>1)</sup> EN pin low                        | P_5.4.13 |
| TxD Time for Flash Mode activation                                    | $t_{\text{fl2}}$      | 5      | –    | –    | μs   | <sup>1)</sup>                                   | P_5.4.14 |
| TxD Time for Flash Mode activation                                    | $t_{\text{fl3}}$      | 10     | –    | –    | μs   | <sup>1)</sup>                                   | P_5.4.15 |

### WK Pin

|                            |                    |           |     |           |               |                                                       |          |
|----------------------------|--------------------|-----------|-----|-----------|---------------|-------------------------------------------------------|----------|
| High Level Input Voltage   | $V_{\text{WK,H}}$  | $V_S - 1$ | –   | $V_S + 3$ | V             | $V_S = 13.5\text{ V}$                                 | P_5.4.16 |
| Low Level Input Voltage    | $V_{\text{WK,L}}$  | -0.3      | –   | $V_S - 4$ | V             | $V_S = 13.5\text{ V}$                                 | P_5.4.17 |
| Pull-up Current            | $I_{\text{WK,PU}}$ | -60       | -30 | -3        | $\mu\text{A}$ | $V_{\text{WK}} = 0\text{ V}$<br>$V_S = 13.5\text{ V}$ | P_5.4.18 |
| High Level Leakage Current | $I_{\text{WK,L}}$  | -5        | –   | 5         | $\mu\text{A}$ | $V_S = 0\text{ V}$ ;<br>$V_{\text{WK}} = 40\text{ V}$ | P_5.4.19 |
| Dominant Time for Wake-up  | $t_{\text{WK}}$    | 30        | –   | 150       | $\mu\text{s}$ | –                                                     | P_5.4.20 |

<sup>1)</sup> Not subject to production test, specified by design

## 5.5 Power Up, Power Down

**Table 9 Electrical Characteristics: Power-up**

$T_j = -40\text{ }^{\circ}\text{C} \text{ } +150\text{ }^{\circ}\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                        | Symbol     | Values |      |      | Unit | Note /<br>Test Condition                             | Number   |
|----------------------------------|------------|--------|------|------|------|------------------------------------------------------|----------|
|                                  |            | Min.   | Typ. | Max. |      |                                                      |          |
| <b><math>V_s</math> Pin</b>      |            |        |      |      |      |                                                      |          |
| $V_S$ Power-up Voltage Threshold | $V_{S,PU}$ | –      | –    | 3.5  | V    | $I_{CC} = 40\text{ mA}$ ,<br>$V_{CC} > 3.0\text{ V}$ | P_5.5.21 |

## 6 Voltage Regulator

### 6.1 Description of Voltage Regulator

The TLE8458G has a monolithic integrated voltage regulator dedicated for microcontroller supplies under harsh automotive environment conditions. Due to its ultra low current consumption, the TLE8458 is perfectly suited for applications permanently connected to a battery. Additionally, the regulator is switched off in Sleep Mode to achieve a very low quiescent current. The TLE8458 is equipped with protection functions against overloading, short circuits, and over temperature.

### 6.2 Electrical Characteristics of the Voltage Regulator

**Table 10 Electrical Characteristics: Voltage Regulator**

$V_S = 5.5 \text{ V}$  to  $13.5 \text{ V}$ ,  $T_j = -40 \text{ }^\circ\text{C}$  to  $+150 \text{ }^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                | Symbol             | Values |      |       | Unit | Note / Test Condition                                                             | Number   |
|------------------------------------------|--------------------|--------|------|-------|------|-----------------------------------------------------------------------------------|----------|
|                                          |                    | Min.   | Typ. | Max.  |      |                                                                                   |          |
| Output Voltage for TLE8458G              | $V_{CC,5}$         | 4.9    | 5    | 5.1   | V    | $1 \text{ mA} < I_{CC} < 50 \text{ mA}$ ;<br>$5.5 \text{ V} < V_S < 18 \text{ V}$ | P_6.2.1  |
| Output Voltage for TLE8458G              | $V_{CC,5}$         | 4.9    | 5    | 5.1   | V    | $I_{CC} = 10 \text{ mA}$ ;<br>$5.5 \text{ V} < V_S < 40 \text{ V}$                | P_6.2.8  |
| Output Voltage for TLE8458GV33           | $V_{CC,3,3}$       | 3.234  | 3.3  | 3.366 | V    | $1 \text{ mA} < I_{CC} < 50 \text{ mA}$ ;<br>$5.5 \text{ V} < V_S < 18 \text{ V}$ | P_6.2.2  |
| Output Voltage for TLE8458GV33           | $V_{CC,3,3}$       | 3.234  | 3.3  | 3.366 | V    | $I_{CC} = 10 \text{ mA}$ ;<br>$5.5 \text{ V} < V_S < 40 \text{ V}$                | P_6.2.9  |
| Output Current Limitation<br>TLE8458G    | $I_{CC,lim}$       | 60     | –    | –     | mA   | $V_{CC,5} > 4.5 \text{ V}$<br>$V_S = 13.5 \text{ V}$                              | P_6.2.3  |
| Output Current Limitation<br>TLE8458GV33 | $I_{CC,lim}$       | 50     | –    | –     | mA   | $V_{CC,3,3} > 2.8 \text{ V}$<br>$V_S = 13.5 \text{ V}$                            | P_6.2.10 |
| Output Voltage Drop                      | $V_{DR}$           | –      | 250  | 500   | mV   | $I_{CC} = 40 \text{ mA}^{1)}$                                                     | P_6.2.4  |
| Load Regulation                          | $\Delta V_{CC,LO}$ | –      | 25   | 50    | mV   | $1 \text{ mA} < I_{CC} < 50 \text{ mA}$<br>$V_S = 13.5 \text{ V}$                 | P_6.2.5  |
| Line Regulation                          | $\Delta V_{CC,LI}$ | –      | 25   | 50    | mV   | $I_{CC} = 1 \text{ mA}$ ;<br>$6 \text{ V} < V_S < 28 \text{ V}$                   | P_6.2.6  |
| Power Supply Ripple Rejection            | $PSRR$             | –      | 60   | –     | dB   | $f = 100 \text{ Hz}$ ;<br>$V_r = 0.5 \text{ Vpp}^{2)3)}$                          | P_6.2.7  |

1) Measured when the output voltage has dropped 100 mV from the nominal value obtained at  $V_S = 13.5 \text{ V}$

2) Voltage of ripple  $V_r$  is 0.5 V peak-to-peak

3) Not subject to production test; specified by design.

## 7 LIN Transceiver

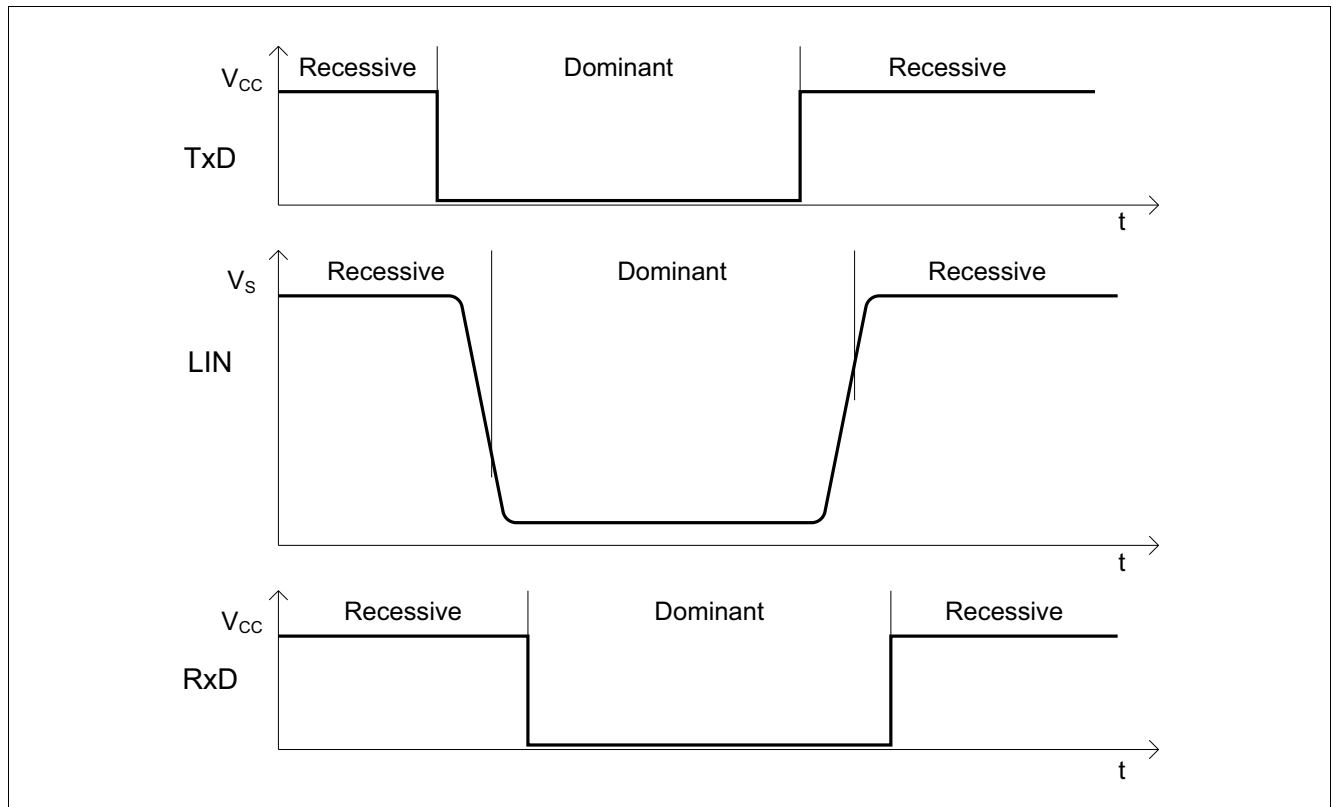
### 7.1 Functional Description

The LIN Bus is a single wire, bi-directional bus, used for in-vehicle networks. The LIN Transceiver implemented inside the TLE8458 is the interface between the microcontroller and the physical LIN Bus. (see [Figure 1](#) and [Figure 15](#)). The digital output data from the microcontroller are driven to the LIN bus via the TxD input pin on the TLE8458. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rate to minimize the EME level of the LIN network. The RxD output sends back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise on the LIN Bus and to increase the EMI (Electro Magnetic Immunity) level of the transceiver.

Two logical states are possible on the LIN bus according to the LIN Specification 2.1 (see [Figure 10](#)):

In dominant state, the voltage on the LIN bus is set close to the GND level. In recessive state, the voltage on the LIN bus is set close to the supply voltage  $V_S$ . By setting the TxD input of the TLE8458 to LOW the transceiver generates a dominant level on the LIN interface pin. The RxD output reads back the signal on the LIN bus and indicates a dominant LIN bus signal with a logical LOW to the microcontroller. Setting the TxD pin to HIGH the transceiver TLE8458 sets the LIN interface pin LIN to the recessive level, at the same time the recessive level on the LIN bus is indicated by a logical "High" on the RxD output.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE8458 for master node applications, a resistor in the range of 1 k $\Omega$  and a reverse diode must be connected between the LIN bus and the power supply  $V_S$ . (see [Figure 15](#)).



**Figure 10** LIN Bus Signals

### 7.1.1 Undervoltage Detection

A dropping power supply  $V_S$  on a local ECU can effect the communication of the whole LIN network. To avoid any blocking of the LIN network by a local ECU the TLE8458 has an integrated Power-On reset at the supply  $V_S$  and an undervoltage detection at the supply  $V_S$ . In case the supply voltage  $V_S$  is dropping below the Power-On reset level  $V_S < V_{S,UV,PON}$ , the TLE8458 changes the operation mode to Stand-By mode. In Stand-By mode the output stage of the TLE8458 is disabled and no communication to the LIN bus is possible. The internal bus termination remains active as well as the  $V_{CC}$  output voltage. (see [Figure 1](#) and [Figure 11](#)).

In Stand-By mode the RxD pin indicates the low power supply condition with a logical HIGH signal. Setting the EN pin to logical HIGH changes the operation mode back to Normal Operation mode.

In case the supply voltage  $V_S$  is dropping below the undervoltage reset level  $V_S < V_{SUV}$  (see [Figure 11](#)), the TLE8458 disables the output and receiver stages. This feature secures the communication on the LIN bus. If the power supply  $V_S$  reaches a higher level as the undervoltage reset level  $V_S > V_{SUV}$  the TLE8458 continues with normal operation. A mode change only applies if the power supply  $V_S$  drops below the power on reset level ( $V_S < V_{S,UV,PON}$ ).

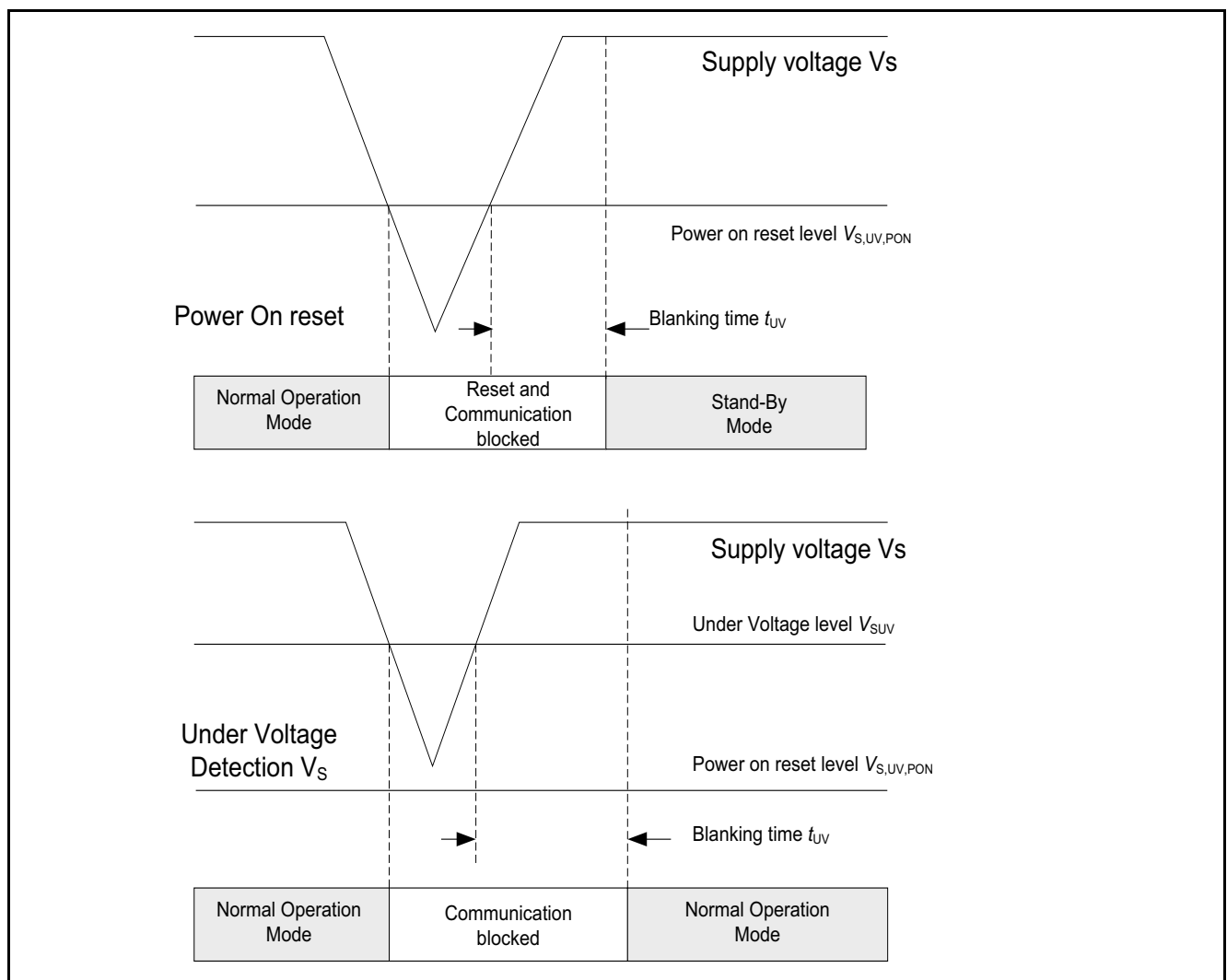


Figure 11 Under-Voltage Detection

### 7.1.2 TxD Time-Out

If the TxD signal is dominant for the time  $t > t_{\text{timeout}}$ , the TxD time-out function deactivates the LIN transmitter output stage. The device remains in recessive state. The TxD time-out function prevents the LIN bus from being blocked by a permanent LOW signal on the TxD pin, caused by a failure. The transmitter output stage is released again, after a rising edge on the TxD pin has been detected (see [Figure 12](#)).

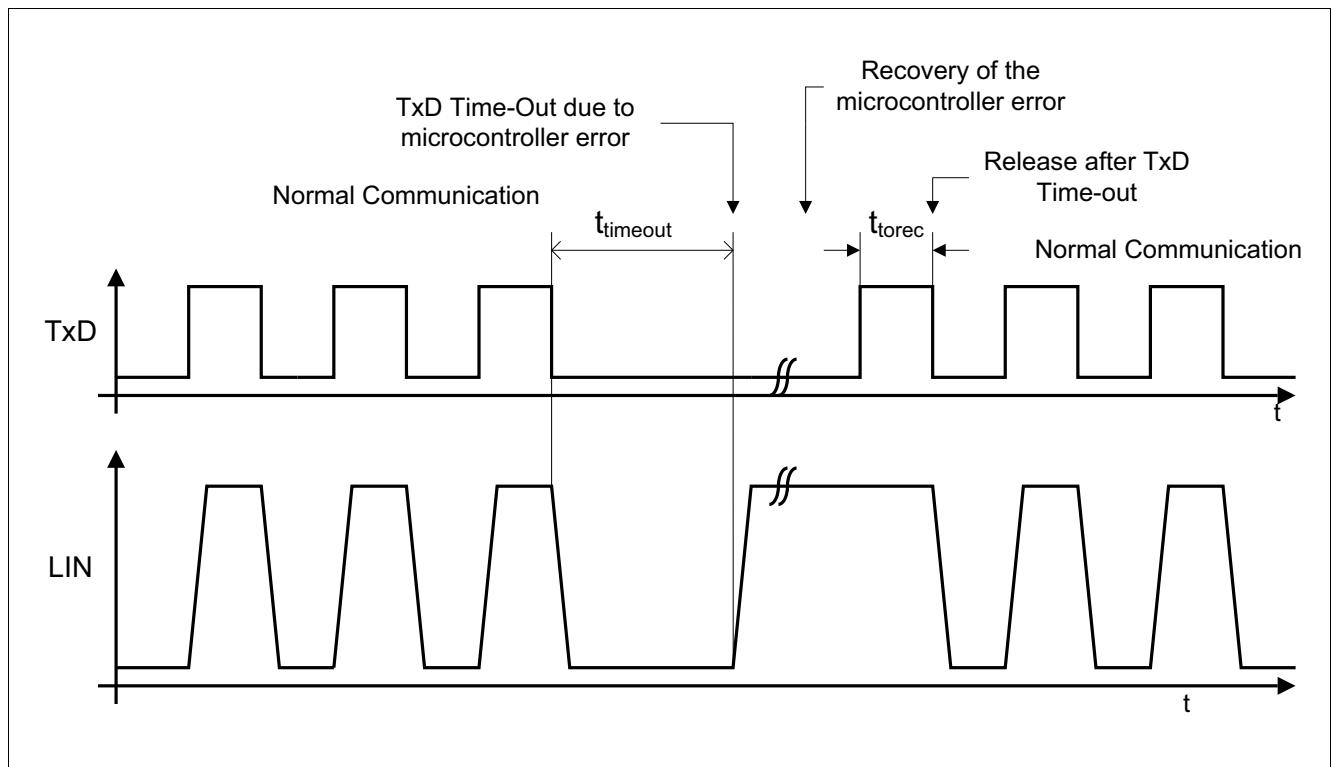


Figure 12 TxD Time-Out function

### 7.1.3 LIN Specifications

The LIN network is standardized by international regulations. The devices TLE8458G and the TLE8458GV33 are compliant to the specification LIN 2.1. The physical layer specification LIN 2.1 is a super set of the previous LIN specifications, like LIN 2.0 or LIN 1.3. The TLE8458G and the TLE8458GV33 have been qualified according to the LIN 2.1 standard, conformance test results are available on request.

## 7.2 Electrical Characteristics of the LIN Transceiver

**Table 11 Electrical Characteristics: LIN Transceiver Supply**

$V_S = 7\text{ V to }27\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                  | Symbol                | Values |      |      | Unit | Note / Test Condition | Number   |
|--------------------------------------------|-----------------------|--------|------|------|------|-----------------------|----------|
|                                            |                       | Min.   | Typ. | Max. |      |                       |          |
| Voltage Supply                             |                       |        |      |      |      |                       |          |
| Undervoltage switch-off                    | $V_{\text{SUV}}$      | 4      | —    | 5    | V    | —                     | P_7.2.1  |
| Power-On Reset Level                       | $V_{\text{S,UV,PON}}$ | 2      | —    | 4    | V    | 1)                    | P_7.2.52 |
| Blanking Time for Under-Voltage switch-off | $t_{\text{uv}}$       | —      | 10   | —    | μs   | 1)                    | P_7.2.2  |

1) Not subject to production test; specified by design.

**Table 12 Electrical Characteristics: LIN Transceiver**

$V_S = 7\text{ V to }27\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ ,  $R_L = 500\text{ }\Omega$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                                        | Symbol               | Values                     |                             |                            | Unit | Note / Test Condition                                                  | Number  |
|------------------------------------------------------------------|----------------------|----------------------------|-----------------------------|----------------------------|------|------------------------------------------------------------------------|---------|
|                                                                  |                      | Min.                       | Typ.                        | Max.                       |      |                                                                        |         |
| Receiver Output (RxD pin)                                        |                      |                            |                             |                            |      |                                                                        |         |
| HIGH Level Output Voltage                                        | $V_{\text{RxD,H}}$   | $0.8 \times V_{\text{CC}}$ | —                           | —                          | V    | $I_{\text{RxD}} = -1.6 \text{ mA};$<br>$V_{\text{bus}} = V_{\text{S}}$ | P_7.2.3 |
| LOW Level Output Voltage                                         | $V_{\text{RxD,L}}$   | —                          | —                           | $0.2 \times V_{\text{CC}}$ | V    | $I_{\text{RxD}} = 1.6 \text{ mA}$<br>$V_{\text{bus}} = 0 \text{ V}$    | P_7.2.4 |
| Transmission Input (TxD pin)                                     |                      |                            |                             |                            |      |                                                                        |         |
| HIGH Level Input Voltage                                         | $V_{\text{TxD,H}}$   | $0.7 \times V_{\text{CC}}$ | —                           | —                          | V    | Recessive State                                                        | P_7.2.5 |
| TxD Input Hysteresis                                             | $V_{\text{TxD,hys}}$ | —                          | $0.12 \times V_{\text{CC}}$ | —                          | mV   | —                                                                      | P_7.2.6 |
| LOW Level Input Voltage                                          | $V_{\text{TxD,L}}$   | —                          | —                           | $0.3 \times V_{\text{CC}}$ | V    | Dominant State                                                         | P_7.2.7 |
| TxD Pull-down Resistance                                         | $R_{\text{TxD}}$     | —                          | 300                         | —                          | kΩ   | $V_{\text{TxD}} = 0 \text{ V}$                                         | P_7.2.8 |
| TxD Low Level Current<br>(Standby Mode, after<br>Wake-up via WK) | $I_{\text{TxD,L}}$   | 1.5                        | 3                           | 10                         | mA   | $V_{\text{TxD}} = 0.9 \text{ V}$                                       | P_7.2.9 |

**Table 12 Electrical Characteristics: LIN Transceiver (cont'd)**

$V_S = 7\text{ V to } 27\text{ V}$ ,  $T_j = -40\text{ °C to } +150\text{ °C}$ ,  $R_L = 500\text{ }\Omega$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                              | Symbol               | Values                      |                            |                             | Unit | Note / Test Condition                                                                      | Number   |
|--------------------------------------------------------|----------------------|-----------------------------|----------------------------|-----------------------------|------|--------------------------------------------------------------------------------------------|----------|
|                                                        |                      | Min.                        | Typ.                       | Max.                        |      |                                                                                            |          |
| LIN Bus Receiver (LIN Pin)                             |                      |                             |                            |                             |      |                                                                                            |          |
| Receiver Threshold Voltage, Recessive to Dominant Edge | $V_{\text{Bus,rd}}$  | $0.4 \times V_{\text{S}}$   | $0.45 \times V_{\text{S}}$ | —                           | V    | $V_{\text{Bus,rec}} < V_{\text{Bus}} < 27 \text{ V}$                                       | P_7.2.10 |
| Receiver Dominant State                                | $V_{\text{Bus,dom}}$ | —                           | —                          | $0.4 \times V_{\text{S}}$   | V    | LIN2.1 Param. 17                                                                           | P_7.2.11 |
| Receiver Threshold Voltage, Dominant to Recessive Edge | $V_{\text{Bus,dr}}$  | —                           | $0.55 \times V_{\text{S}}$ | $0.60 \times V_{\text{S}}$  | V    | $V_{\text{Bus,rec}} < V_{\text{Bus}} < 27 \text{ V}$                                       | P_7.2.12 |
| Receiver Recessive State                               | $V_{\text{Bus,rec}}$ | $0.6 \times V_{\text{S}}$   | —                          | —                           | V    | LIN2.1 Param 18                                                                            | P_7.2.13 |
| Receiver Center Voltage                                | $V_{\text{Bus,c}}$   | $0.475 \times V_{\text{S}}$ | $0.5 \times V_{\text{S}}$  | $0.525 \times V_{\text{S}}$ | V    | LIN2.1 Param 19                                                                            | P_7.2.14 |
| Receiver Hysteresis                                    | $V_{\text{Bus,hys}}$ | $0.07 \times V_{\text{S}}$  | $0.1 \times V_{\text{S}}$  | $0.175 \times V_{\text{S}}$ | V    | $V_{\text{bus,hys}} = V_{\text{bus,rec}} - V_{\text{bus,dom}}$<br>LIN2.1 Param 20          | P_7.2.15 |
| Wake-up Threshold Voltage                              | $V_{\text{Bus,wk}}$  | $0.40 \times V_{\text{S}}$  | $0.5 \times V_{\text{S}}$  | $0.6 \times V_{\text{S}}$   | V    | —                                                                                          | P_7.2.16 |
| Dominant Time for Bus Wake-up                          | $t_{\text{WK,Bus}}$  | 30                          | —                          | 150                         | μs   | —                                                                                          | P_7.2.17 |
| LIN Bus Transmitter (LIN Pin)                          |                      |                             |                            |                             |      |                                                                                            |          |
| Bus Recessive Output Voltage                           | $V_{\text{BUS,ro}}$  | $0.8 \times V_{\text{S}}$   | —                          | $V_{\text{S}}$              | V    | $V_{\text{TXD}} = \text{high Level}$                                                       | P_7.2.18 |
| Bus Dominant Output Voltage                            | $V_{\text{BUS,do}}$  | —                           | —                          | 1.2                         | V    | $V_{\text{TXD}} = 0 \text{ V};$<br>$6.0 \text{ V} \leq V_{\text{S}} \leq 7.3 \text{ V};$   | P_7.2.53 |
| Bus Dominant Output Voltage                            | $V_{\text{BUS,do}}$  | —                           | —                          | $0.2 \times V_{\text{S}}$   | V    | $V_{\text{TXD}} = 0 \text{ V};$<br>$7.3 \text{ V} \leq V_{\text{S}} \leq 10.0 \text{ V};$  | P_7.2.19 |
| Bus Dominant Output Voltage                            | $V_{\text{BUS,do}}$  | —                           | —                          | 2.0                         | V    | $V_{\text{TXD}} = 0 \text{ V};$<br>$10.0 \text{ V} \leq V_{\text{S}} \leq 18.0 \text{ V};$ | P_7.2.20 |
| Bus Short Circuit Current                              | $I_{\text{BUS,sc}}$  | 40                          | 100                        | 150                         | mA   | $V_{\text{BUS}} = 13.5 \text{ V};$<br>LIN2.1 Param 12                                      | P_7.2.23 |
| Leakage Current Loss of Ground                         | $I_{\text{BUS,lg}}$  | -1000                       | -450                       | 0                           | μA   | $V_{\text{S}} = 0 \text{ V}; V_{\text{BUS}} = -12 \text{ V};$<br>LIN2.1 Param 15           | P_7.2.24 |
| Leakage Current Loss of Battery                        | $I_{\text{BUS,lg}}$  | —                           | —                          | 5                           | μA   | $V_{\text{S}} = 0 \text{ V}; V_{\text{BUS}} = 18 \text{ V};$<br>LIN2.1 Param 16            | P_7.2.25 |
| Leakage Current                                        | $I_{\text{BUS,lg}}$  | -1                          | —                          | —                           | mA   | $V_{\text{S}} = 18 \text{ V}; V_{\text{BUS}} = 0 \text{ V};$<br>LIN2.1 Param 13            | P_7.2.26 |
| Leakage Current Driver Off                             | $I_{\text{BUS,lg}}$  | —                           | —                          | 5                           | μA   | $V_{\text{S}} = 8 \text{ V}; V_{\text{BUS}} = 18 \text{ V};$<br>LIN2.1 Param 14            | P_7.2.27 |
| Bus Pull-up Resistance                                 | $R_{\text{BUS}}$     | 20                          | 30                         | 47                          | kΩ   | Normal Mode<br>LIN2.1 Param 26                                                             | P_7.2.28 |



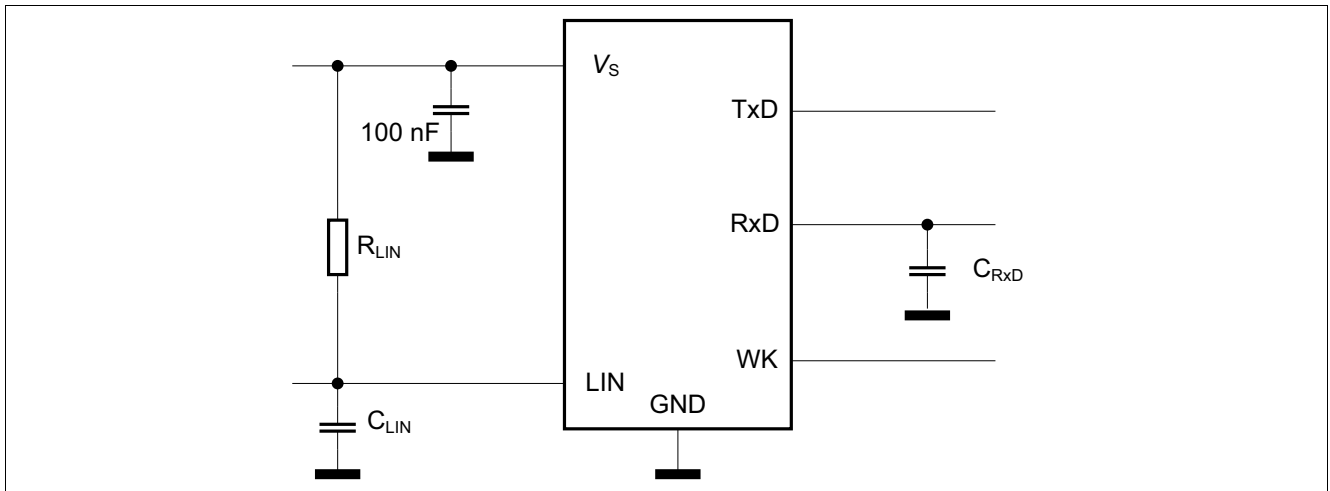
**Table 12 Electrical Characteristics: LIN Transceiver (cont'd)**

$V_S = 7\text{ V to } 27\text{ V}$ ,  $T_j = -40\text{ °C to } +150\text{ °C}$ ,  $R_L = 500\text{ }\Omega$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

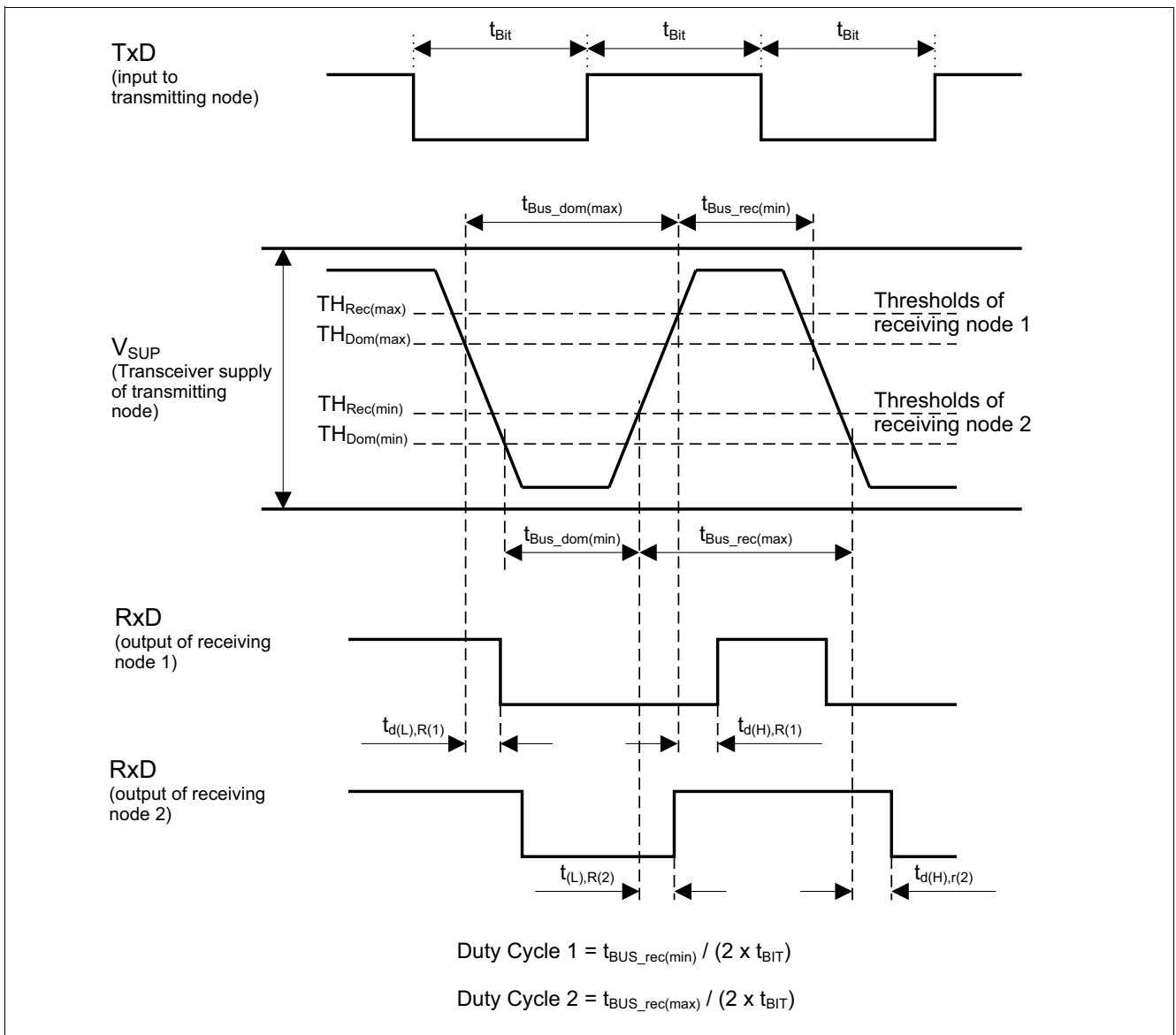
| Parameter                                                             | Symbol               | Values |      |       | Unit          | Note / Test Condition                                                                                                                                                                                                                                                                                                | Number   |
|-----------------------------------------------------------------------|----------------------|--------|------|-------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
|                                                                       |                      | Min.   | Typ. | Max.  |               |                                                                                                                                                                                                                                                                                                                      |          |
| LIN Output Current                                                    | $I_{\text{BUS}}$     | -60    | -30  | -5    | $\mu\text{A}$ | Sleep Mode<br>$V_S = 12\text{ V}$ ;<br>$\text{EN} = 0\text{ V}$ ; $V_{\text{LIN}} = 0\text{ V}$                                                                                                                                                                                                                      | P_7.2.29 |
| LIN Input Capacitance                                                 | $C_{\text{BUS}}$     |        | 15   |       | $\text{pF}$   | <sup>1)</sup>                                                                                                                                                                                                                                                                                                        | P_7.2.55 |
| Receiver propagation delay bus dominant to RxD LOW                    | $t_{\text{d(L),R}}$  | –      | 1    | 6     | $\mu\text{s}$ | $C_{\text{RxD}} = 20\text{ pF}$ ;<br>LIN2.1 Param 31                                                                                                                                                                                                                                                                 | P_7.2.38 |
| Receiver propagation delay bus recessive to RxD HIGH                  | $t_{\text{d(H),R}}$  | –      | 1    | 6     | $\mu\text{s}$ | $C_{\text{RxD}} = 20\text{ pF}$ ;<br>LIN2.1 Param 31                                                                                                                                                                                                                                                                 | P_7.2.39 |
| Receiver delay symmetry                                               | $t_{\text{sym,R}}$   | -2     | –    | 2     | $\mu\text{s}$ | $t_{\text{sym,R}} = t_{\text{d(L),R}} - t_{\text{d(H),R}}$ ;<br>LIN2.1 Param 32                                                                                                                                                                                                                                      | P_7.2.40 |
| TxD Dominant Time Out                                                 | $t_{\text{timeout}}$ | 6      | 12   | 20    | $\text{ms}$   | $V_{\text{TxD}} = 0\text{ V}$                                                                                                                                                                                                                                                                                        | P_7.2.44 |
| TxD Dominant Time Out Recovery Time                                   | $t_{\text{torec}}$   | –      | 10   | –     | $\mu\text{s}$ | <sup>1)</sup>                                                                                                                                                                                                                                                                                                        | P_7.2.45 |
| Duty Cycle D1<br>(For worst case at 20 kbit/s)<br>LIN2.1 Normal Slope | D1                   | 0.396  | –    | –     |               | <sup>2)</sup> $\text{TH}_{\text{Rec}}(\text{max}) = 0.744 \times V_S$ ;<br>$\text{TH}_{\text{Dom}}(\text{max}) = 0.581 \times V_S$ ;<br>$V_S = 7.0 \dots 18\text{ V}$ ;<br>$t_{\text{bit}} = 50\text{ }\mu\text{s}$ ;<br>$\text{D1} = t_{\text{bus\_rec}(\text{min})}/2 \cdot t_{\text{bit}}$ ;<br>LIN2.1 Param 27   | P_7.2.46 |
| Duty Cycle D2<br>(for worst case at 20 kbit/s)<br>LIN2.1 Normal Slope | D2                   | –      | –    | 0.581 |               | <sup>2)</sup> $\text{TH}_{\text{Rec}}(\text{min.}) = 0.422 \times V_S$ ;<br>$\text{TH}_{\text{Dom}}(\text{min.}) = 0.284 \times V_S$ ;<br>$V_S = 7.6 \dots 18\text{ V}$ ;<br>$t_{\text{bit}} = 50\text{ }\mu\text{s}$ ;<br>$\text{D2} = t_{\text{bus\_rec}(\text{max})}/2 \cdot t_{\text{bit}}$ ;<br>LIN2.1 Param 28 | P_7.2.47 |

1) Not subject to production test, specified by design.

2) Bus load conditions concerning LIN spec 2.1  $C_{\text{LIN}}$ ,  $R_{\text{LIN}} = 1\text{ nF}$ ,  $1\text{ k}\Omega$  /  $6.8\text{ nF}$ ,  $660\text{ }\Omega$  /  $10\text{ nF}$ ,  $500\text{ }\Omega$



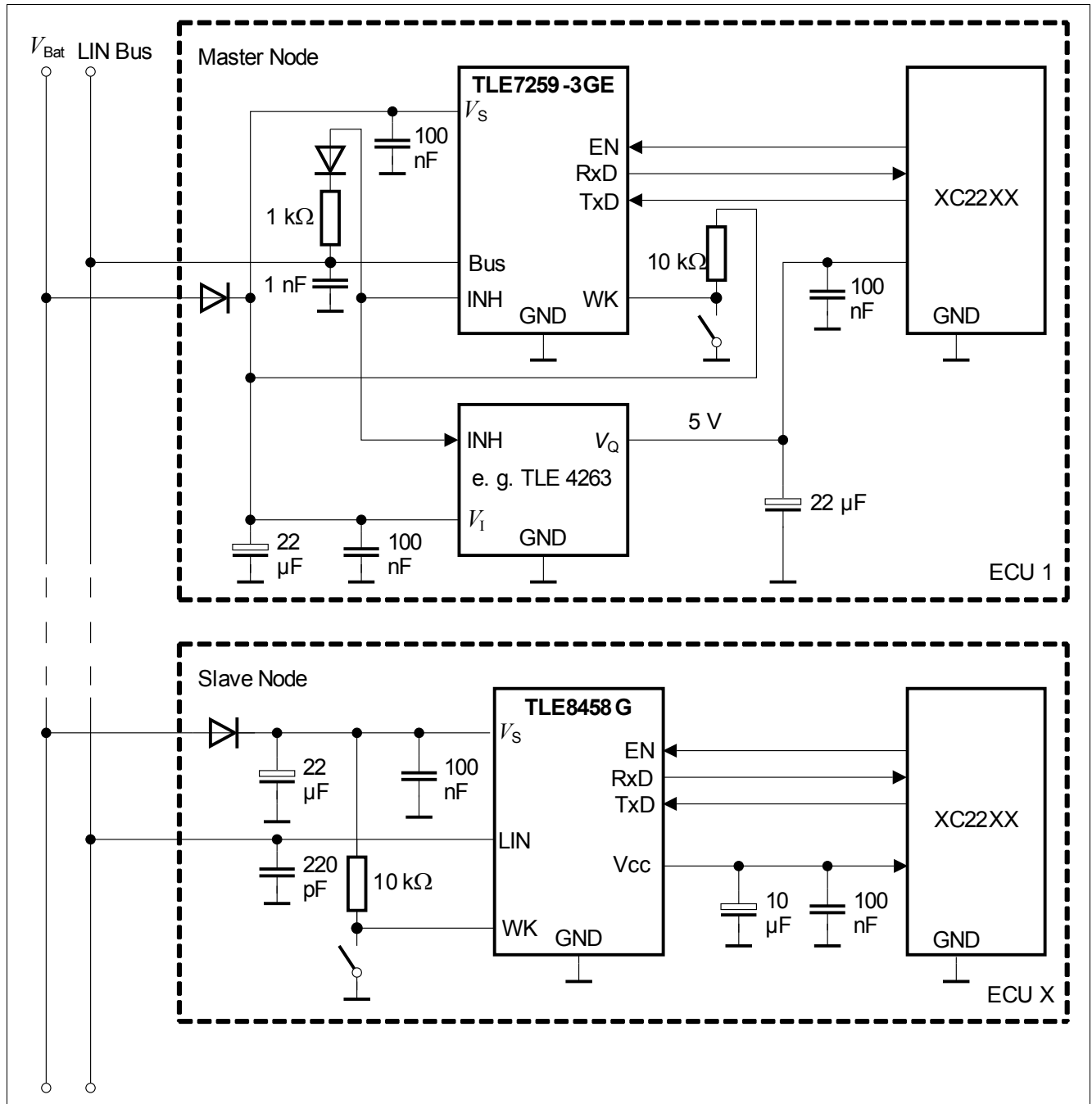
**Figure 13** Simplified Test Circuit for Dynamic Characteristics



**Figure 14** Timing Diagram for Dynamic Characteristics

## 8 Application Information

*Note: The following information is given as a hint for the implementation of the device only and should not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 15 Application Example**

*Note: This is a simplified example of an application circuit. The function must be verified in the actual application.*

## 8.1 ESD Tests

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330  $\Omega$ ) have been performed. The results and test conditions are available in a separate test report (see [Table 13](#)).

**Table 13 ESD “Gun test”**

| Parameter                     | Symbol        | Values |      |      | Unit | Note / Test Condition | Number  |
|-------------------------------|---------------|--------|------|------|------|-----------------------|---------|
|                               |               | Min.   | Typ. | Max. |      |                       |         |
| Performed Test                |               |        |      |      |      |                       |         |
| ESD at $V_S$ , LIN versus GND | $V_{ESD,GUN}$ | -10    | —    | 10   | kV   | GUN <sup>1)</sup>     | P_8.1.1 |
| ESD at WK PIN                 | $V_{ESD,GUN}$ | -6     | —    | 6    | kV   | GUN <sup>1)</sup>     | P_8.1.1 |

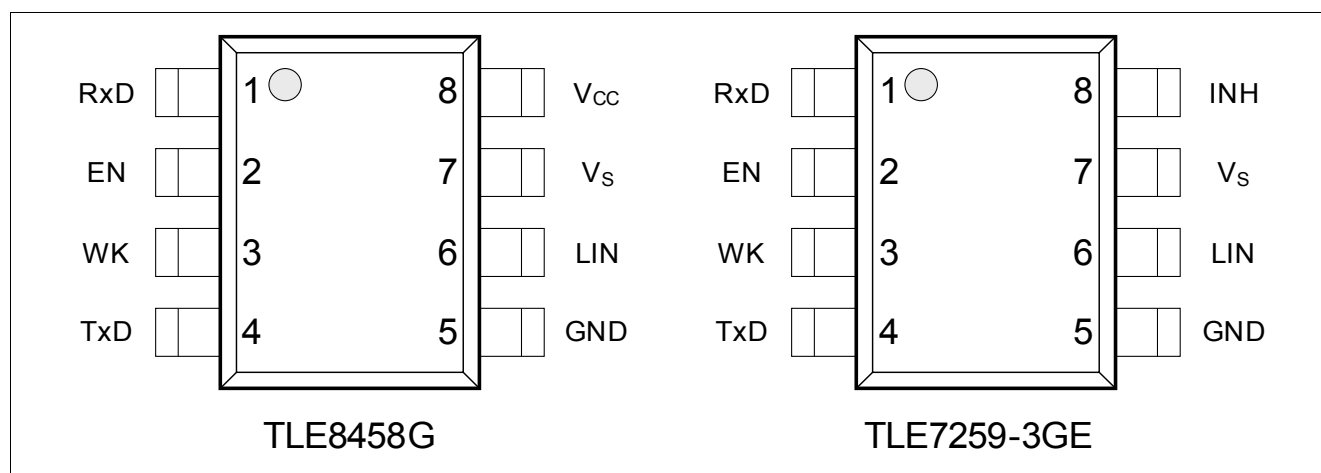
1) ESD susceptibility “ESD GUN” according LIN EMC Test Specification, Section 3.4.3 (IEC 61000-4-2:2001-12), tested by external test house (IBEE Zwickau, EMC Test report Nr. 05-12-13a)

### 8.1.1 EMC Measurement

The EMC performance has been qualified by an external test house according to the LIN EMC Test specification Version 1.0 (August 1, 2004). For the DPI measurements according to the LIN EMC Test Specification, Section 4.2 (ISO62132 part 1: 2006, ISO62132 part 4: 2006) the verification limit for the output voltage  $V_{CC}$ , was set to a limit of +/- 100 mV. External test reports are available on request.

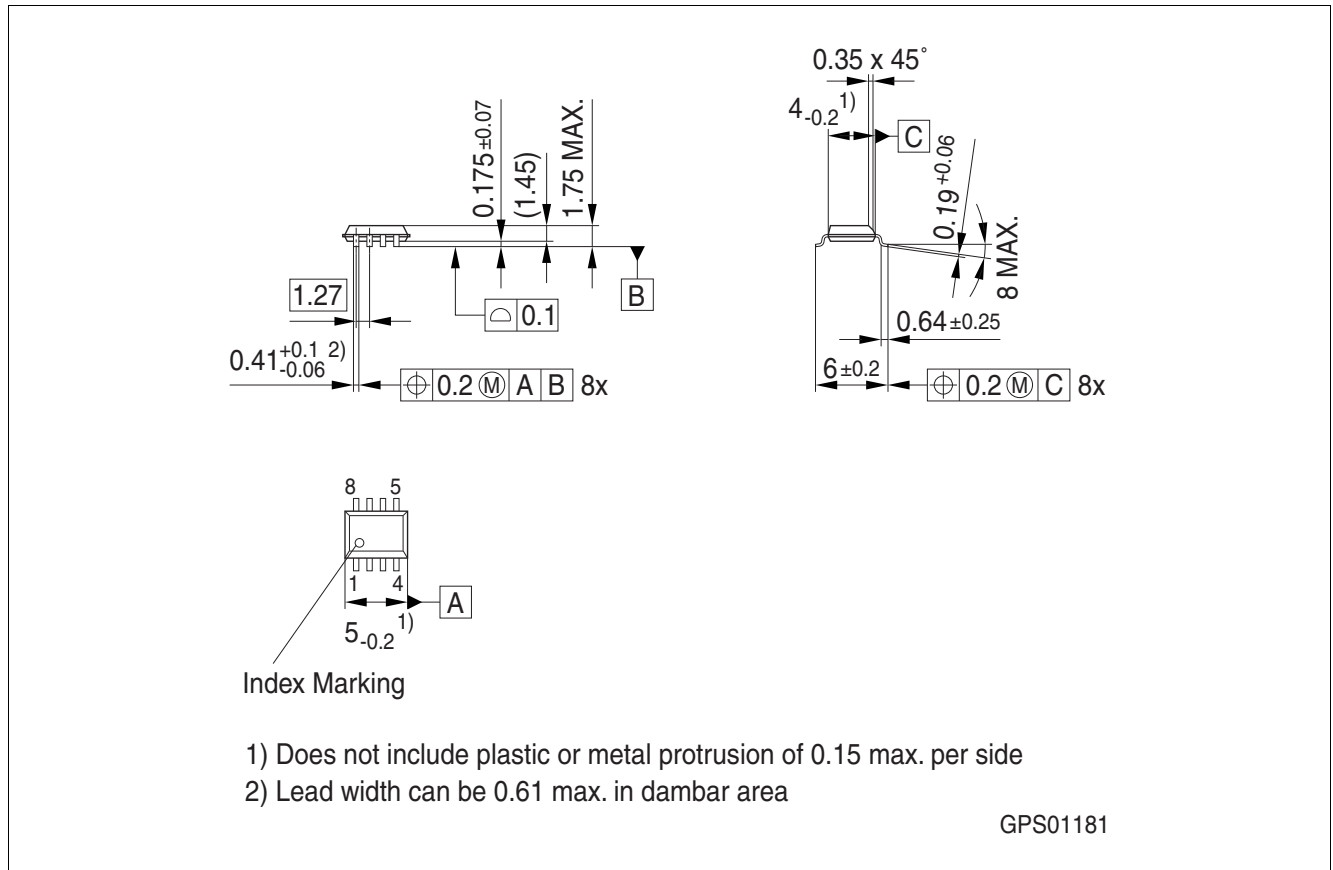
## 8.2 Pin Compatibility to Stand-Alone LIN transceivers

The TLE8458G is pin - and function compatible to the single LIN transceivers like the TLE7259-3GE (see [Figure 16](#)). Instead of the INH output pin on the single LIN transceiver TLE7259-3GE the  $V_{CC}$  power supply output can be connected to the external microcontroller. The TLE8458G provides the same operation modes and features as single LIN transceiver TLE7259-3GE.



**Figure 16 Pinning of TLE8458G versus the TLE7259-3GE**

## 9 Package Outlines



**Figure 17 PG-DSO-8-16 (SO-8 Standard, Green (RoHS compliant))**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 10 Revision History

| Revision | Date       | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.1      | 2014-04-01 | All pages: - Editorial changes, updated with latest Infineon style guide<br>Updated compatibility with stand alone transceiver with TLE7259-3G<br>Updated condition for Parameter P_5.3.4: no load on $V_{CC}$<br>Removed device versions TLE8458GU and -GUV33, references and description<br>Removed LIN Duty Cycle parameters D3 and D4 (only applicable to -GU and -GUV33)<br>Chapter 8.1: Updated ESD and EMC references to the latest IBEE test report |
| 1.02     | 2010-03-08 | all pages: Editorial changes<br>table 10: changed Output current limitation min. to 60 mA<br>table 11: changed power on reset values<br>figure 15: deleted 2 resistors                                                                                                                                                                                                                                                                                      |
| 1.01     | 2009-04-28 | Editorial Change to the data sheet<br>Update table 13 on page 30.<br>P_8.1.1 performed test changed from:<br>"ESD at LIN Pin"<br>to:<br>"ESD at $V_S$ , LIN versus GND"                                                                                                                                                                                                                                                                                     |
| 1.0      | 2009-03-23 | Initial data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                          |

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