SPIDER - TLE7230GS

SPI Driver for Enhanced Relay Control

Automotive Power

Never stop thinking

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SPI Driver for Enhanced Relay Control
Eight Channel Low-Side Switch

SPIDER - TLE7230GS

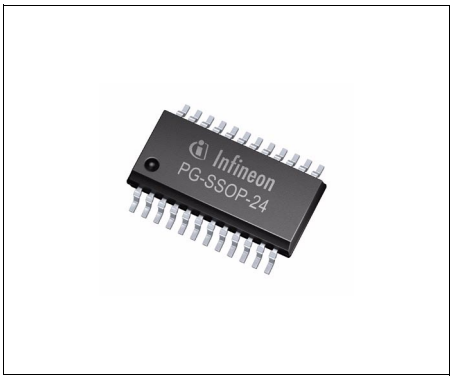
AEC Qualified

RoHS

1 Product Summary

Features

- 16 bit SPI for diagnostics and control
- SPI providing daisy chain capability
- 3.3 V and 5 V compatible SPI
- 3 input pins offers complete flexibility for PWM operation
- Stable behavior at undervoltage
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-24-6

Table 1 Product Summary

Supply voltage	V_{DD}	4.5 … 5.5 V
Supply voltage for SO buffer	V_{VSO}	3.0 … 5.5 V
On-State Resistance at 150 °C	$R_{DS(ON, max)}$	1.7 Ω
Nominal load current	$I_{L(nom, min)}$	300 mA
Overload current limitation	$I_{DS(LIM, min)}$	1 A
Power supply reset current (quiscent current)	$I_{DD(RST, max)}$	5 µA
Output leakage current per channel at 25 °C	$I_{DS(OFF, max)}$	1 µA
Drain to source clamping voltage	$V_{DS(CL, min)}$	48 V
SPI clock frequency	$f_{SCLK(max)}$	5 MHz

Type	Package	Marking
SPIDER - TLE7230GS	PG-SSOP-24-6	TLE7230GS

Protective Functions

- Short circuit protection
- Overload protection, configurable behavior (limitation or shutdown)
- Thermal shutdown, configurable behavior (latch or restart)
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Diagnostic information via SPI
- Open load detection in OFF-state
- Shorted to GND detection in OFF-state
- Overtemperature in ON-state
- Overload in ON-state

Applications

- Especially designed for driving relays in automotive applications
- All types of capacitive, resistive and inductive loads

Description

The SPIDER - TLE7230GS is an eight channel low-side relay switch (typ. 0.8 Ω per channel) in PG-SSOP-24-6 package providing embedded protective functions. The 16 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy-chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins.

The SPIDER - TLE7230GS is equipped with three input pins that can be individually routed to the output control of some channels (please refer to **Section 5.1.2** for details) thus offering complete flexibility in design and PCB-layout. The input mapping as well as the boolean operation between input signal an output control signal is configured via SPI.

The device provides full diagnosis of the load, which is open load, short to GND as well as short circuit to V_{bat} detection and overload / overtemperature indication. The SPI diagnosis flags indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of overload, the current of the affected channel is limited. There is a temperature sensor available for each channel to protect the device in case of overtemperature. The shut down behavior in case of overload or overtemperature can be configured via SPI for each channel individually.

2 Block Diagram

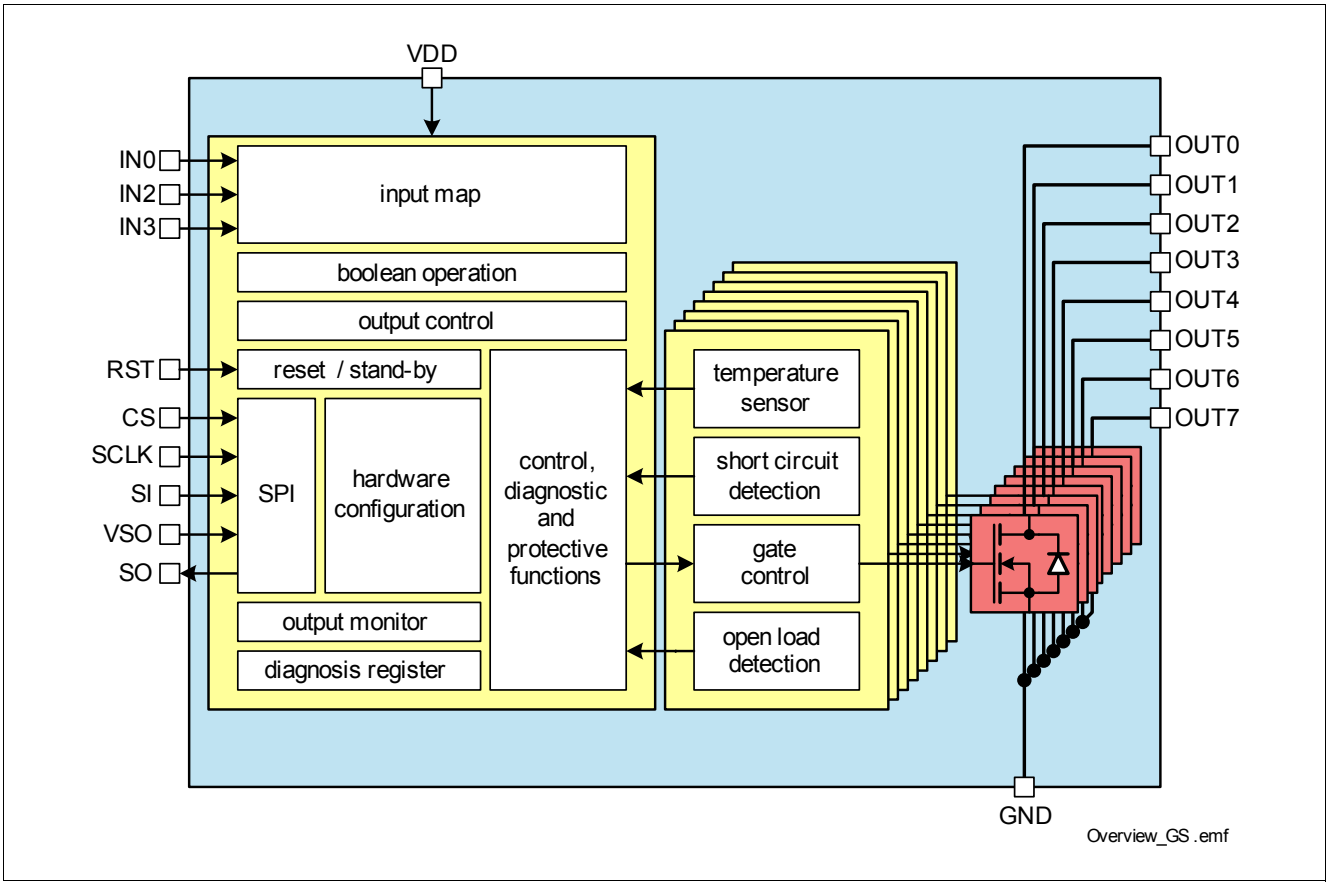


Figure 1 Block Diagram

2.1 Terms

Following figure shows all terms used in this data sheet.

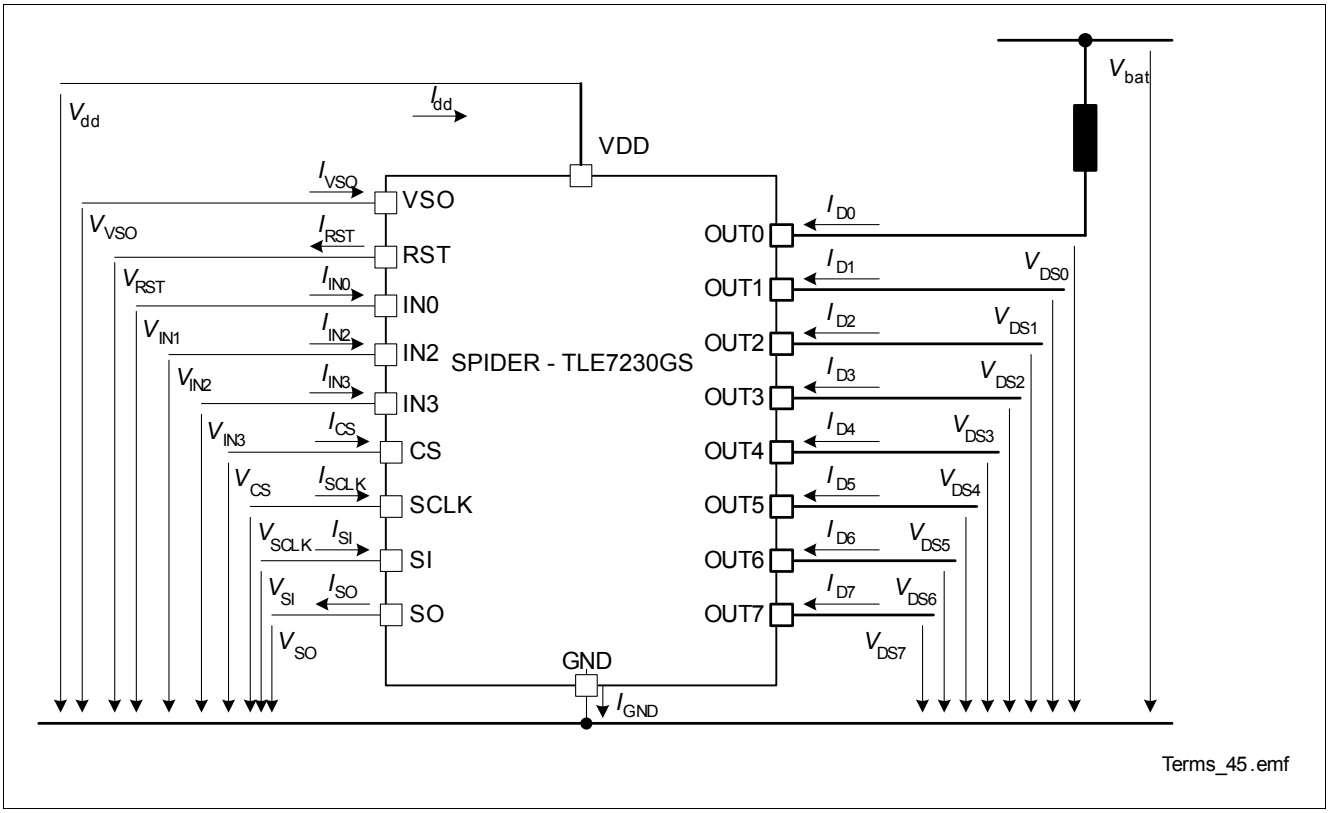


Figure 2 Terms

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} ... V_{DS7}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `CTL.OUT0`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment

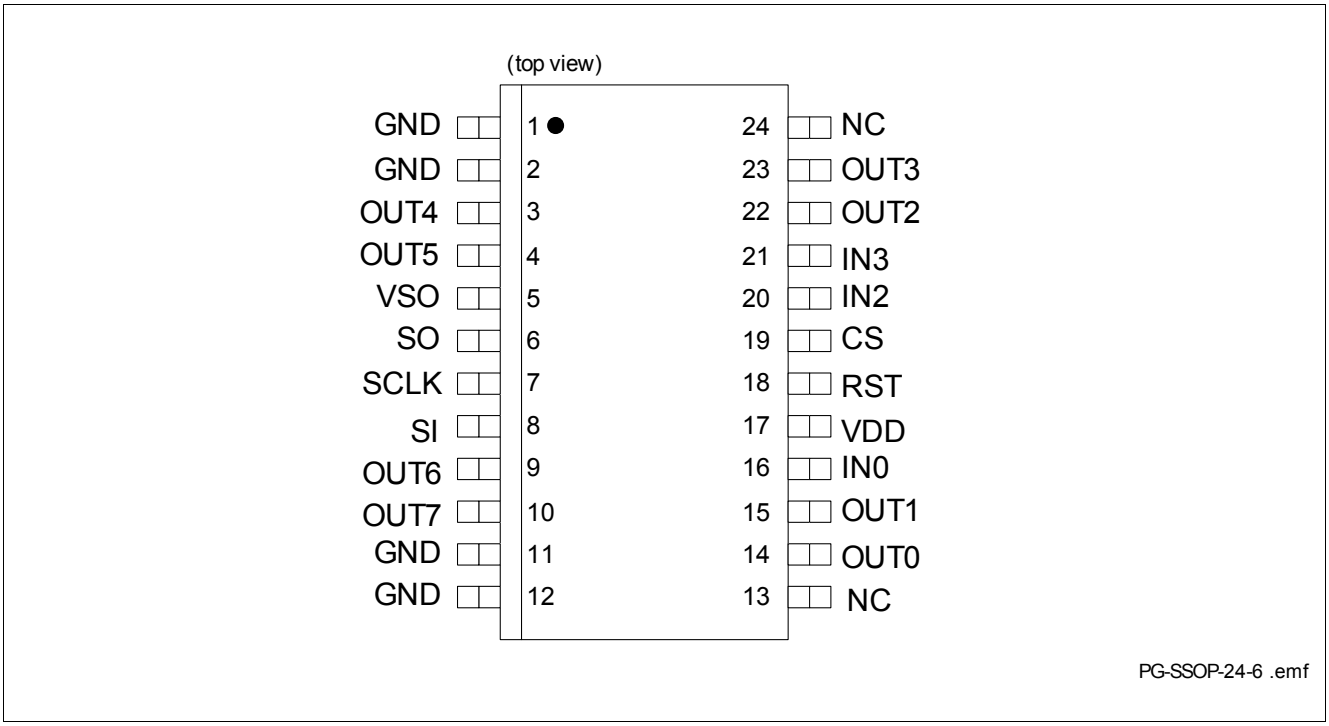


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply			
17	V_{DD}	–	**Power Supply**
5	V_{SO}	–	**Power Supply** for SO buffer
1, 2, 11, 12	GND	–	**Ground**
Power Stages			
14	OUT0	O	**Drain** of power transistor channel 0
15	OUT1	O	**Drain** of power transistor channel 1
22	OUT2	O	**Drain** of power transistor channel 2
23	OUT3	O	**Drain** of power transistor channel 3
3	OUT4	O	**Drain** of power transistor channel 4
4	OUT5	O	**Drain** of power transistor channel 5
9	OUT6	O	**Drain** of power transistor channel 6
10	OUT7	O	**Drain** of power transistor channel 7

Pin	Symbol	I/O	Function
Inputs			
18	RST	I	**Reset Input Pin** (active low)
16	IN0	I	**Input Multiplexer Input Pin** for output Out0
20	IN2	I	**Input Multiplexer Input Pin** for output Out2
21	IN3	I	**Mappable Input Pin** for all outputs, default Out3
SPI			
19	CS	I	**SPI Chip Select** (active low)
7	SCLK	I	**Serial Clock**
8	SI	I	**Serial Data In**
6	SO	O	**Serial Data Out**
Not Used			
13, 24	NC	–	Not connected

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to 150 °C; V_{DD} = 4.5 V to 5.5 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Power Supply						
4.1.1	Power supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.2	V_{SO} supply voltage	V_{VSO}	-0.3	V_{DD} + 0.3	V	[2)]
4.1.3	Power supply voltage for full short circuit protection (single pulse)	$V_{bat(SC)}$	0 –	20 28	V	OVL = 0 [3)] OVL = 1
Power Stages						
4.1.4	Load current	I_D	-1	1	A	–
4.1.5	Voltage at power transistor	V_{DS}	–	48	V	–
4.1.6	Maximum energy dissipation one channel single pulse	E_{AS}	 – –	 65 50	mJ	[4)] $T_{j(0)}$ = 85 °C $I_{D(0)}$ = 0.4 A $T_{j(0)}$ = 150 °C $I_{D(0)}$ = 0.3 A
	Maximum energy dissipation one channel repetitive pulses $1 \cdot 10^4$ cycles $1 \cdot 10^6$ cycles	E_{AR}	 – –	 20 16	mJ	[4)] $T_{j(0)}$ = 150 °C $I_{D(0)}$ = 0.25 A $I_{D(0)}$ =0.2 A
Logic Pins						
4.1.7	Voltage at input pins	V_{IN}	-0.3	5.5	V	–
4.1.8	Voltage at reset pin	V_{RST}	-0.3	5.5	V	–
4.1.9	Voltage at chip select pin	V_{CS}	-0.3	5.5	V	–
4.1.10	Voltage at serial clock pin	V_{SCLK}	-0.3	5.5	V	–
4.1.11	Voltage at serial input pin	V_{SI}	-0.3	5.5	V	–
4.1.12	Voltage at serial output pin	V_{SO}	-0.3	5.5	V	–
Temperatures						
4.1.13	Junction Temperature	T_j	-40	150	°C	–
4.1.14	Dynamic temperature increase while switching	ΔT_j	–	60	°C	–
4.1.15	Storage Temperature	T_{stg}	-55	150	°C	–

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 °C to 150 °C; V_{DD} = 4.5 V to 5.5 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
ESD Susceptibility						
4.1.16	ESD capability of all pins versus GND	V_{ESD}	-2	2	kV	HBM[5)]

1) Not subject to production test, specified by design.
2) V_{DD} + 0.3 V < 5.5 V
3) Details on configuration of protective function OLCR.OVL can be found in **Section 5.2.5**
4) Pulse shape represents inductive switch off: $I_D(t) = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$
5) ESD susceptibility, HBM according to EIA/JESD 22-A114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.17	Junction to Solder Point	R_{thJSP}	–	–	25	K/W	pin 1, 2, 11, 12[1)]
4.2.18	Junction to Ambient (1s0p+600mm^2 Cu)	R_{thJA}	–	64	–	K/W	[1)2)]
4.2.19	Junction to Ambient (2s2p)	R_{thJA}	–	55	–	K/W	[1)3)]

1) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_a = 25 °C. LS0 to LS7 are dissipating 1 W power (0.125 W each).
2) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 µm thickness. T_a = 25 °C, LS0 to LS7 are dissipating 1 W power (0.125 W each).
3) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). T_a = 25 °C, LS0 to LS7 are dissipating 1 W power (0.125 W each).

5 Block Description and Electrical Characteristics

5.1 Power Stages

The SPIDER - TLE7230GS is an eight channel low-side relay switch. The power stages are built by N-channel vertical power MOSFET transistors.

5.1.1 Power Supply

The SPIDER - TLE7230GS is supplied by power supply line V_{DD} which is used for the digital as well as the analog functions of the device including the gate control of the power stages. There is a power-on reset function implemented for the supply line. After start-up of the power supply, all SPI registers are reset to their default values. A capacitor at pins V_{DD} to GND is recommended.

The pin V_{SO} is the supply pin of the digital output buffer at pin SO.

V_{SO} can therefore be used to vary the high state output voltage of the SO pin, in order to be compatible to 3.3 V and 5 V microcontrollers. If V_{SO} supply voltage is missing the device is fully functional, only the SO pin has no output.

There is a reset pin available. At low level at this pin, all registers are set to their default values and the quiescent supply current is minimized.

5.1.2 Input Circuit

There are three input pins available at SPIDER - TLE7230GS to control the output stages.

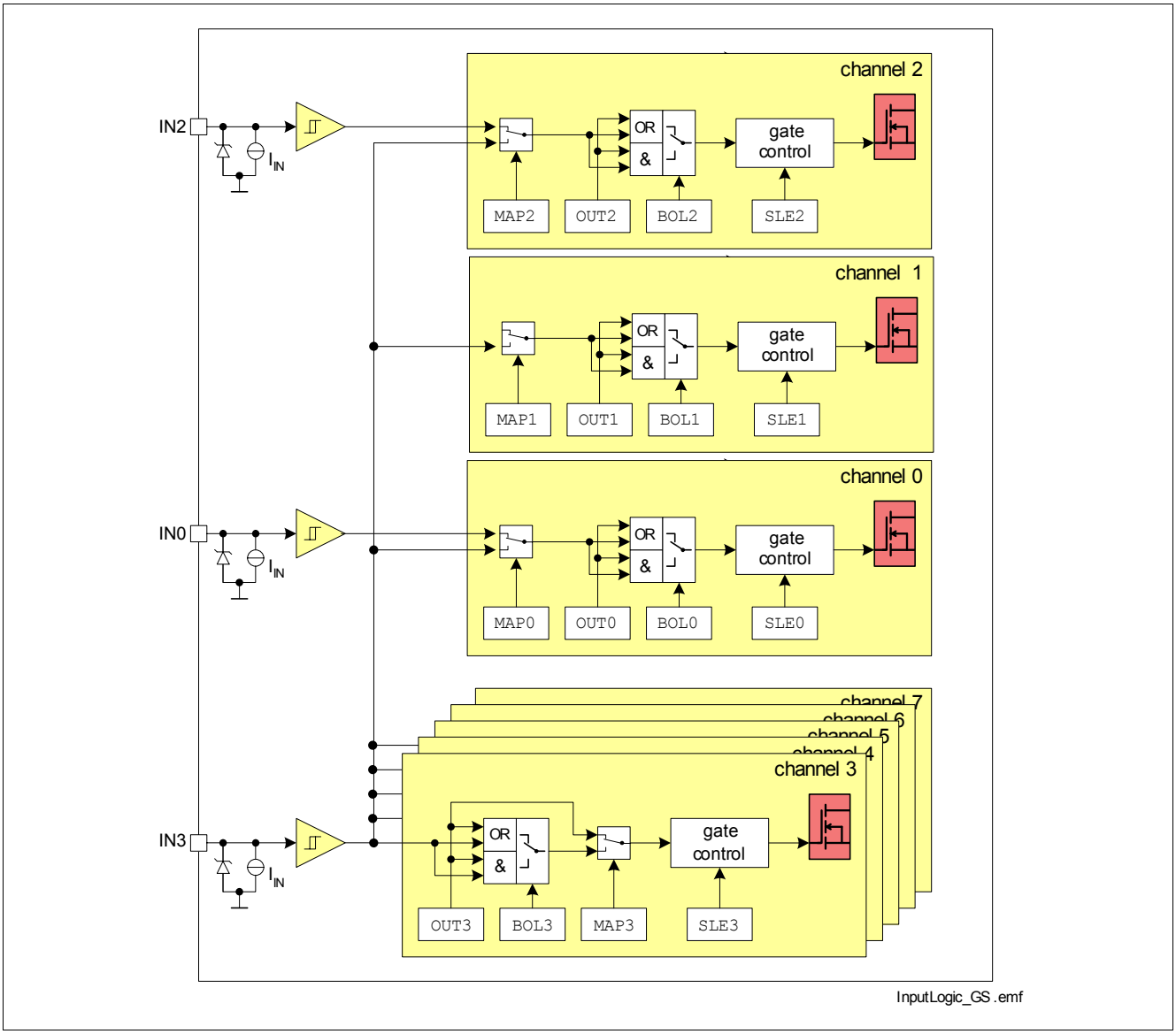


Figure 4 Input Mapping and Boolean Operator

The input signal of IN3 can be configured to be used as control signal of the output stages for each channel separately. The channels 0 to 2 differ from the channels 3 to 7 in the mapping behavior.

IN0 is a direct input to channel Out0, while IN2 is a direct input to Out2.

OUT0 can be switched with the SPI Flag MAP0 to the mappable input IN3, default is IN0.

OUT2 can be switched with the SPI Flag MAP2 to the mappable input IN3, default is IN2.

OUT3 is controlled by default with IN3, but IN3 can be programmed to each channel.

Therefore after power up the inputs are always mapped to their corresponding outputs.

Please refer to **Figure 4** for details.

The current sink to ground at the input pins ensures that the channels switch off in case of open pin. The zener diode protects the input circuit against ESD pulses.

5.1.3 Inductive Output Clamp

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited.

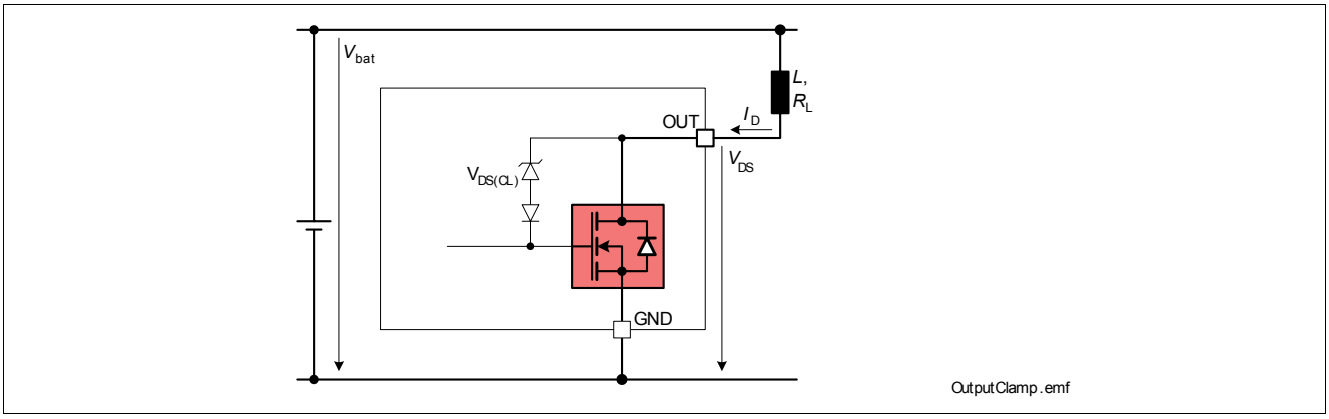


Figure 5 Output Clamp Implementation

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the SPIDER - TLE7230GS. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{bat} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_D}{V_{bat} - V_{DS(CL)}}\right) + I_D \right] \cdot \frac{L}{R_L} \quad (1)$$

The equation simplifies under the assumption of R_L = 0:

$$E = \frac{1}{2} L I_D^2 \cdot \left(1 - \frac{V_{bat}}{V_{bat} - V_{DS(CL)}}\right) \quad (2)$$

The energy, which is converted into heat, is limited by the thermal design of the component.

5.1.4 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the `OUT` bits of the serial peripheral interface SPI. The switching times t_{ON} and t_{OFF} are designed equally.

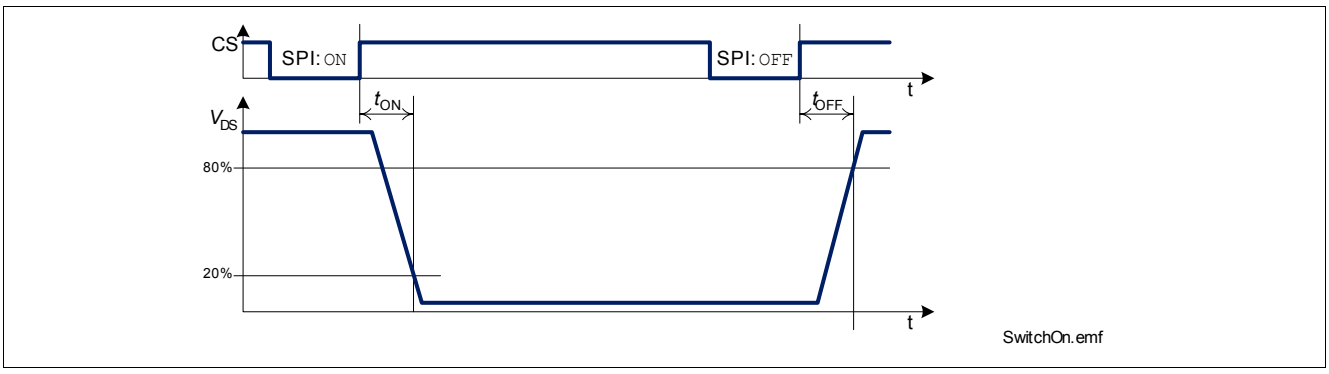


Figure 6 Switching a Resistive Load

When the input mapping is configured accordingly, a high signal at the input pin is equivalent to a SPI ON command.

5.1.5 Electrical Characteristics

Electrical Characteristics: Power Stages

T_j = -40 °C to 150 °C; V_{DD} = 4.5 V to 5.5 V (unless otherwise specified); all voltages with respect to ground, positive current flowing into pin; typical values: V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power Supply							
5.1.1	Power supply voltage	V_{DD}	4.5	–	5.5	V	–
5.1.2	Power supply current	$I_{DD(ON)}$	–	3	5	mA	all channels ON
5.1.3	Power supply reset current	$I_{DD(RST)}$	–	–	5	µA	V_{RST} = 0 V V_{IN} = 0 V V_{SCLK} = 0 V V_{SI} = 0 V V_{CS} = V_{DD}
5.1.4	Power-on reset threshold voltage	$V_{DD(PO)}$	–	–	4.5	V	–
Output Characteristics							
5.1.5	On-State resistance per channel	$R_{DS(ON)}$	–	0.8 1.7	1.0	Ω	T_j = 25 °C[1)] T_j = 150 °C I_L = 500 mA V_{DD} = 5 V
5.1.6	Nominal load current	$I_{L(nom)}$	300	–	–	mA	[1)] all channels ON based on R_{thJA} = 55 K/W $R_{DS(ON)}$ = 1.7 Ω T_A = 85 °C $T_{j,max}$ = 150 °C
5.1.7	Output leakage current in stand-by mode (per channel)	$I_{D(RST)}$	– – –	– – –	1 2 5	µA	V_{DS} = 13.5 V T_j = 25 °C[1)] T_j = 125 °C T_j = 150 °C[1)]
5.1.8	Output clamping voltage	$V_{DS(CL)}$	48	–	60	V	–
Input Characteristics							
5.1.9	L level of pin IN	$V_{IN(L)}$	0	–	1.0	V	–
5.1.10	H level of pin IN	$V_{IN(H)}$	2.0	–	V_{DD}	V	–
5.1.11	Input voltage hysteresis at pin IN	ΔV_{IN}	–	0.1	–	V	[1)]
5.1.12	L-input pull-down current through pin IN	$I_{IN(L)}$	10	–	100	µA	[1)] V_{IN} = 1 V
5.1.13	H-input pull-down current through pin IN	$I_{IN(H)}$	20	50	100	µA	V_{IN} = 5 V

Electrical Characteristics: Power Stages (cont'd)

T_j = -40 °C to 150 °C; V_{DD} = 4.5 V to 5.5 V (unless otherwise specified); all voltages with respect to ground, positive current flowing into pin; typical values: V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reset							
5.1.14	L level of pin RST	$V_{RST(L)}$	0	–	1	V	–
5.1.15	H level of pin RST	$V_{RST(H)}$	2	–	V_{DD}	V	–
5.1.16	L-input pull-up current through pin RST	$I_{RST(L)}$	0	–	10	µA	V_{RST} = 1 V
5.1.17	H-input pull-up current through pin RST	$I_{RST(H)}$	20	50	100	µA	V_{RST} = 2 V
Timings							
5.1.18	Power-on wake-up time	$t_{wu(PO)}$	–	–	200	µs	–
5.1.19	Reset duration	$t_{RST(L)}$	10	–	–	µs	–
5.1.20	Turn-on time V_{DS} = 20% V_{bat}	t_{ON}	 – –	 – –	 15 60	µs	V_{bat} = 14 V I_{DS} = 500 mA, resistive load SLE = 0 SLE = 1
5.1.21	Turn-off time V_{DS} = 80% V_{bat}	t_{OFF}	 – –	 – –	 15 60	µs	V_{bat} = 14 V I_{DS} = 500 mA, resistive load SLE = 0 SLE = 1

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

5.1.6 Command Description

IMCR
Input Mapping Configuration Register **Reset Value: 08_H**

7	6	5	4	3	2	1	0
MAP7	**MAP6**	**MAP5**	**MAP4**	**MAP3**	**MAP2**	**MAP1**	**MAP0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MAPn (n = 7-0)	n	rw	**Input Mapping Configuration Channel n** 0 Channel n can not be controlled with mappable input pin IN3. OUT0 is controlled by IN0. OUT2 is controlled by IN2. OUT3 is controlled by the mappable IN3 (default value). 1 Channel n can be controlled with mapable input pin IN3, depending on additional set-up.

BOCR
Boolean Operator Configuration Register **Reset Value: 00_H**

7	6	5	4	3	2	1	0
BOL7	**BOL6**	**BOL5**	**BOL4**	**BOL3**	**BOL2**	**BOL1**	**BOL0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
BOLn (n = 7-0)	n	rw	**Boolean Operator Configuration Channel n** 0 Logic “OR” for channel n (default value). 1 Logic “AND” for channel n.

SRCR
Slew Rate Configuration Register **Reset Value: 00_H**

7	6	5	4	3	2	1	0
SLE7	**SLE6**	**SLE5**	**SLE4**	**SLE3**	**SLE2**	**SLE1**	**SLE0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SLEn (n = 7-0)	n	rw	**Slew Rate Configuration Channel n** 0 Channel n is switched fast (default value). 1 Channel n is switched slowly.

CTL
Output Control Register **Reset Value: 00_H**

7	6	5	4	3	2	1	0
OUT7	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
OUTn (n = 7-0)	n	rw	**Output Control Channel n** 0 Channel n is switched off (default value). 1 Channel n is switched on, depending on additional set-up.

5.2 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this Data Sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

There is an overload and overtemperature protection implemented in the SPIDER - TLE7230GS. The behavior of the protective functions can be set-up via SPI. Following figure gives an overview about the protective functions.

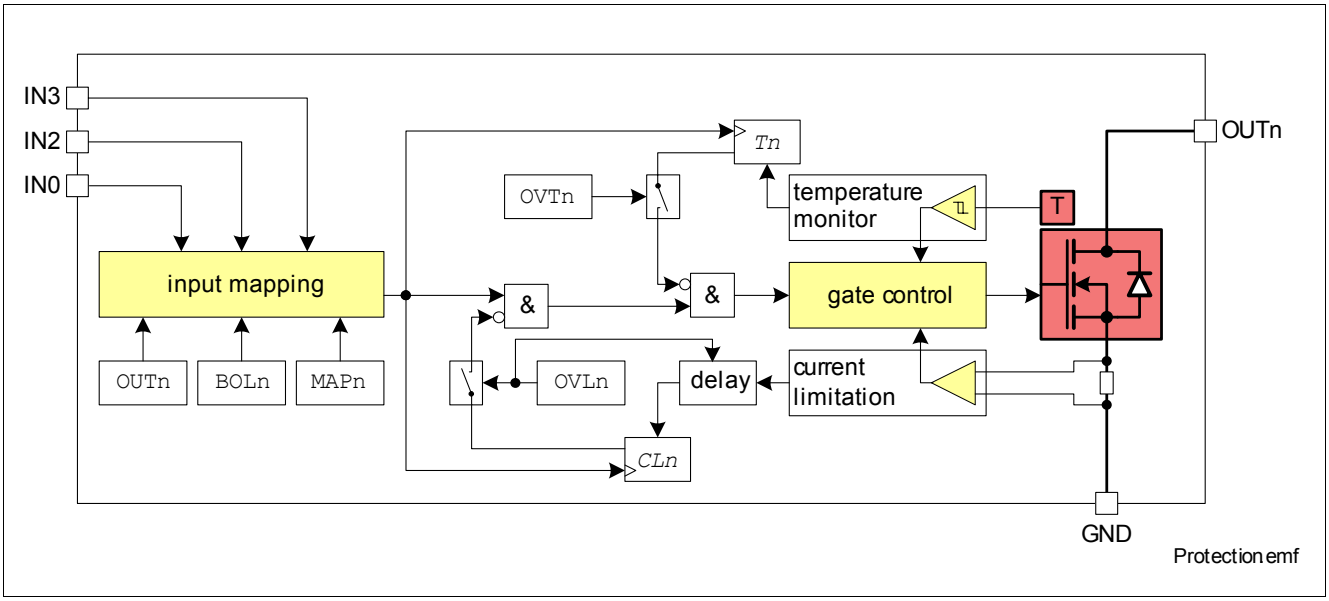


Figure 7 Protective Functions

5.2.1 Overload Protection

The SPIDER - TLE7230GS is protected in case of overload or short circuit of the load. The behavior in case of overload can be configured as follows:

1. The current is limited to $I_{DS(LIM)}$. After time $t_{d(fault)}$, the according overload flag CLn is set. The channel may shut down due to overtemperature.
2. The current is limited to $I_{DS(LIM)}$. After time $t_{d(off)}$, the overloaded channel n switches off and the according overload flag CLn is set.

The overload flag (CLn) of the affected channel is cleared by a low-high transition of the input signal. For timing information, please refer to **Figure 8** for details.

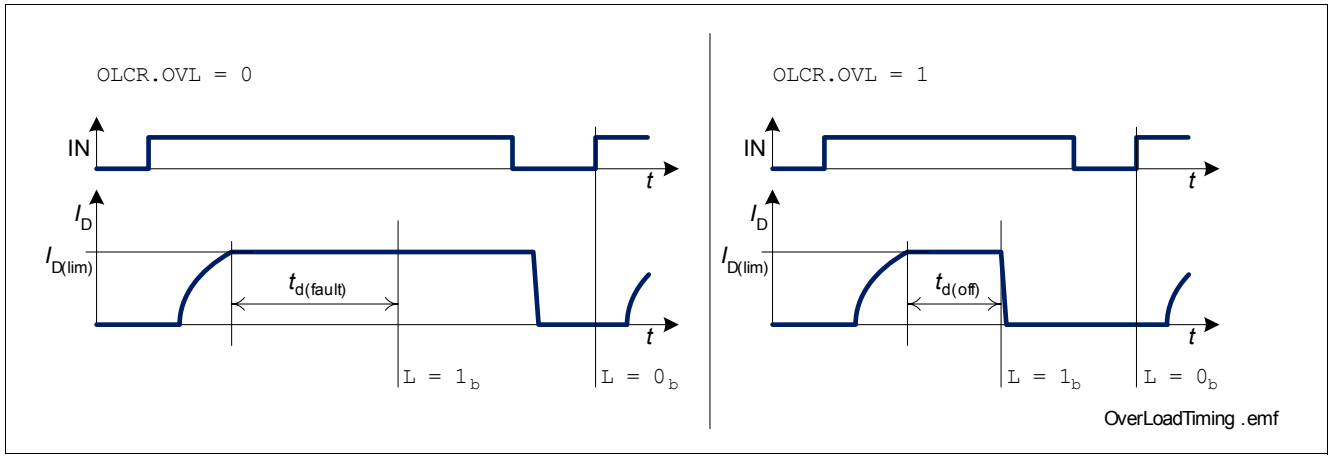


Figure 8 Overload Behavior

5.2.2 Overtemperature Protection

A temperature sensor for each channel causes an overheated channel n to switch off immediately to prevent destruction. The behavior in case of overtemperature can be configured as follows:

1. After cooling down, the channel is switched on again with thermal hysteresis ΔT_j.
2. The affected channel stays switched off until the overtemperature flag is cleared.

The overtemperature flag of the affected channel is cleared by a low-high transition of the input signal.

5.2.3 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power transistor causes power dissipation. The reverse current through the intrinsic body diode has to be limited by the connected load. The V_{DD} supply pin must be protected against reverse polarity externally. The overtemperature protection as well as other protective functions are not active during reverse polarity.

5.2.4 Electrical Characteristics

Electrical Characteristics: Protection Functions

V_{DD} = 4.5 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified); typical values: V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Overload Protection							
5.2.1	Overload current limitation	$I_{D(lim)}$	1	–	2	A	OVL = 0
5.2.2	Overload shut-down delay time	$t_{d(off)}$	10	–	50	µs	OVL = 1
Overtemperature Protection							
5.2.3	Overtemperature shut-down threshold	$T_{j(OT)}$	170	–	200	°C	1)
5.2.4	Thermal hysteresis	$\Delta T_{j(OT)}$	–	10	–	K	1)

1) Not subject to production test, specified by design.

5.2.5 Command Description

OLCR
Overload Configuration Register **Reset Value: 00_H**

7	6	5	4	3	2	1	0
OVL7	**OVL6**	**OVL5**	**OVL4**	**OVL3**	**OVL2**	**OVL1**	**OVL0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
OVLn (n = 7-0)	n	rw	**Overload Configuration Channel n** 0 Channel n limits the current in case of overload (default value). 1 Channel n shuts down in case of overload.

OTCR
Overtemperature Configuration Register **Reset Value: 00_H**

7	6	5	4	3	2	1	0
OVT7	**OVT6**	**OVT5**	**OVT4**	**OVT3**	**OVT2**	**OVT1**	**OVT0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
OVTn (n = 7-0)	n	rw	**Overtemperature Configuration Channel n** 0 Autorestart (default value) 1 Latched shut down

5.3 Diagnostic Features

The SPI of SPIDER - TLE7230GS provides diagnosis information about the device and about the load. There are following diagnosis flags implemented:

- The diagnosis information of the protective functions (flags CLn and Tn) of channel n is latched in the diagnosis flag Pn.
- The open load diagnosis of channel n is latched in the diagnosis flag OLn.
- The short to GND monitor information of channel n is latched in the diagnosis flag SGn.

All flags are cleared after a successful SPI transmission.

There is an output state monitor implemented in the device that indicates the switch state of the device in register STA. Depending on the voltage level at input pin and protective functions the bits are high or low.

Please see **Figure 9** for details:

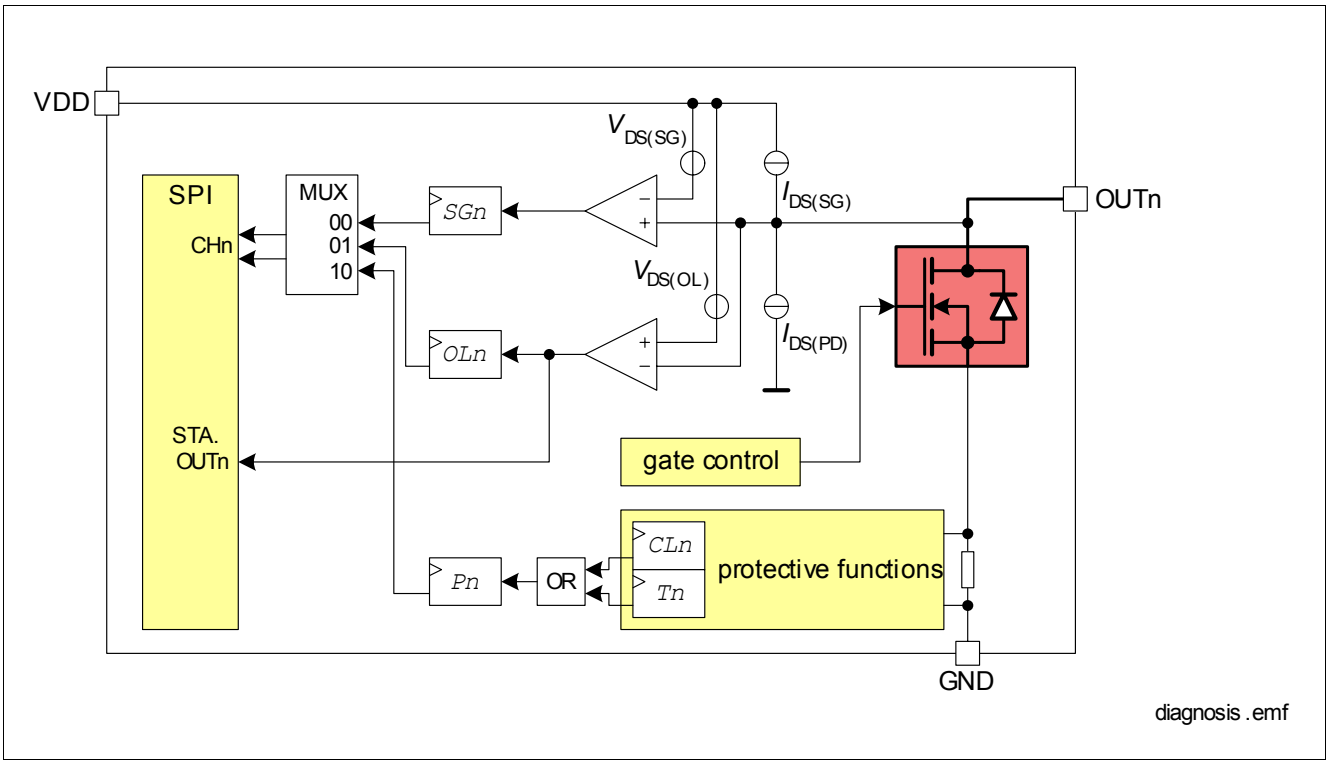


Figure 9 Block Diagram Diagnosis

5.3.1 Diagnosis Timing

The SPIDER - TLE7230GS offers 2 different diagnosis for each channel in OFF mode.

5.3.1.1 Open Load Behavior

The device offers a open load diagnosis for each channel in OFF mode.

The time $t_{d(fault)}$ is applied to filter short time events.

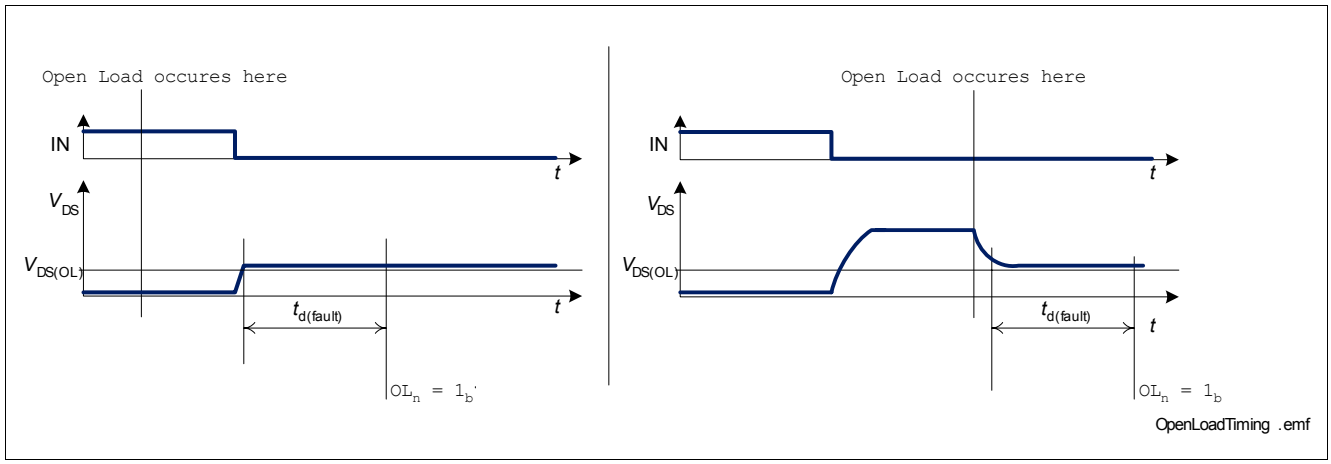


Figure 10 Open Load Timing

5.3.1.2 Short to Ground Behavior

The device offers a short to ground detection for each channel in OFF mode.

The time $t_{d(fault)}$ is applied to filter short time events.

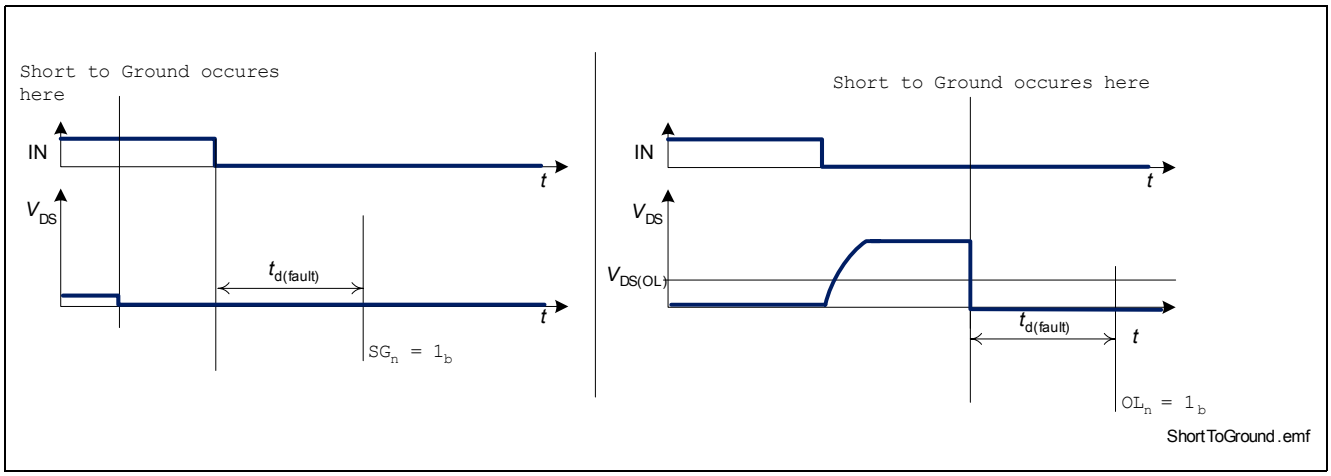


Figure 11 Short to Ground Timing

5.3.2 Electrical Characteristics

Electrical Characteristics: Diagnostic

V_{DD} = 4.5 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified); typical values: V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
OFF State Diagnosis							
5.3.1	Open load detection threshold voltage	$V_{DS(OL)}$	V_{DD} - 2.5	V_{DD} - 2	V_{DD} - 1.3	V	–
5.3.2	Output pull-down diagnosis current per channel	$I_{D(PD)}$	50	90	150	µA	–
5.3.3	Short to GND detection threshold voltage	$V_{DS(SG)}$	V_{DD} - 3.4	V_{DD} - 3.0	V_{DD} - 2.6	V	–
5.3.4	Output diagnosis current for short to GND per channel	$I_{D(SG)}$	-150	-100	-50	µA	V_{DS} = 0 V
5.3.5	Fault delay time	$t_{d(fault)}$	50	100	200	µs	–

5.3.3 Command Description

STA

Output Status Monitor **Reset Value: 00_H**

7	6	5	4	3	2	1	0
OUT7	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
OUTn (n = 7-0)	n	r	**Output Status** 0 Voltage level at channel n: $V_{DS} > V_{DS(OL)}$. 1 Voltage level at channel n: $V_{DS} < V_{DS(OL)}$.

5.4 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

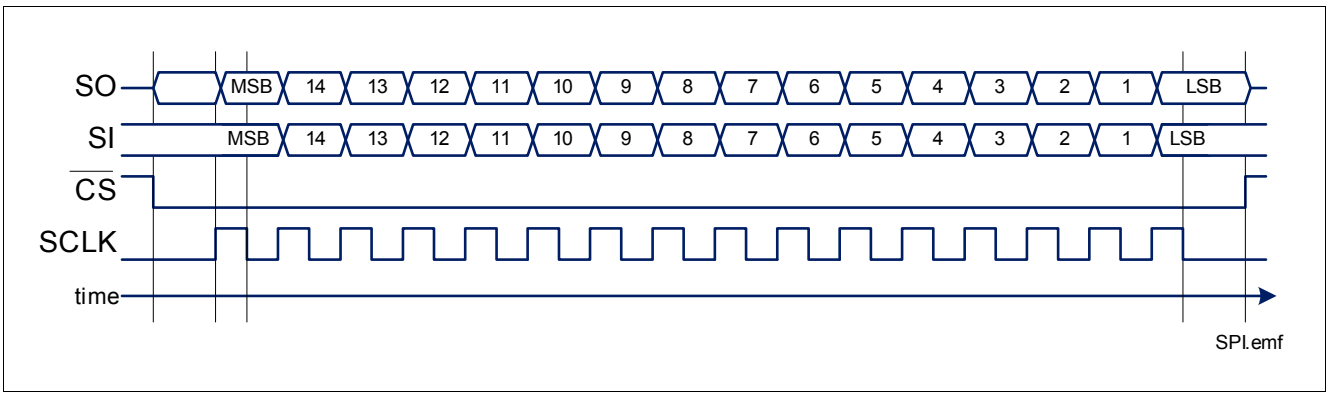


Figure 12 Serial Peripheral Interface

The SPI protocol is described in **Section 5.4.5**. It is reset to the default values after power-on reset or a low signal at pin RST.

5.4.1 SPI Signal Description

$\overline{CS}$ - Chip Select: The system microcontroller selects the SPIDER - TLE7230GS by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low Transition: ⎺_

- The diagnosis information is transferred into the shift register.

$\overline{CS}$ Low to High Transition: _/⎺

- Command decoding is only done, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected.
- Data from shift register is transferred into the input matrix register.
- The diagnosis flags are cleared.

SCLK - Serial Clock: This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input: Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The 16 bit input data consist of two parts (control and data). Please refer to **Section 5.4.5** for further information.

SO Serial Output: Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 5.4.5** for further information. The high state output voltage depends on the voltage at pin V_{SO}.

5.4.2 Daisy Chain Capability

The SPI of SPIDER - TLE7230GS provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 13**), which builds a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.

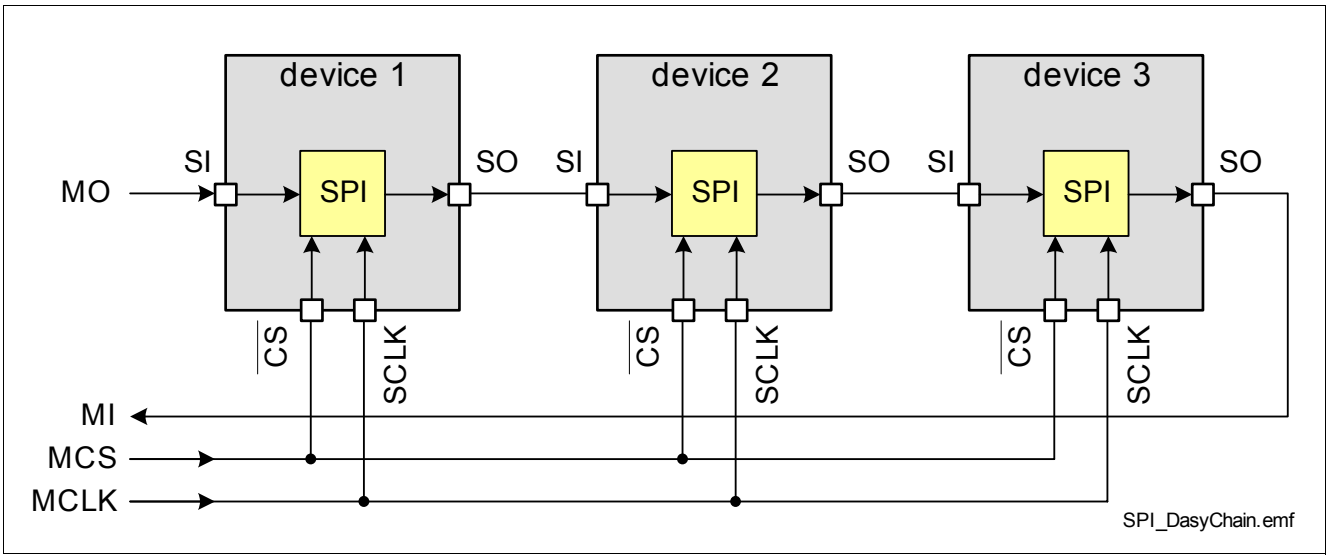


Figure 13 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 16 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device #1 has been shifted in to device #2. When using three devices in daisy chain, three times 16 bits have to be shifted through the devices. After that, the $\overline{MCS}$ line must go high (see **Figure 14**).

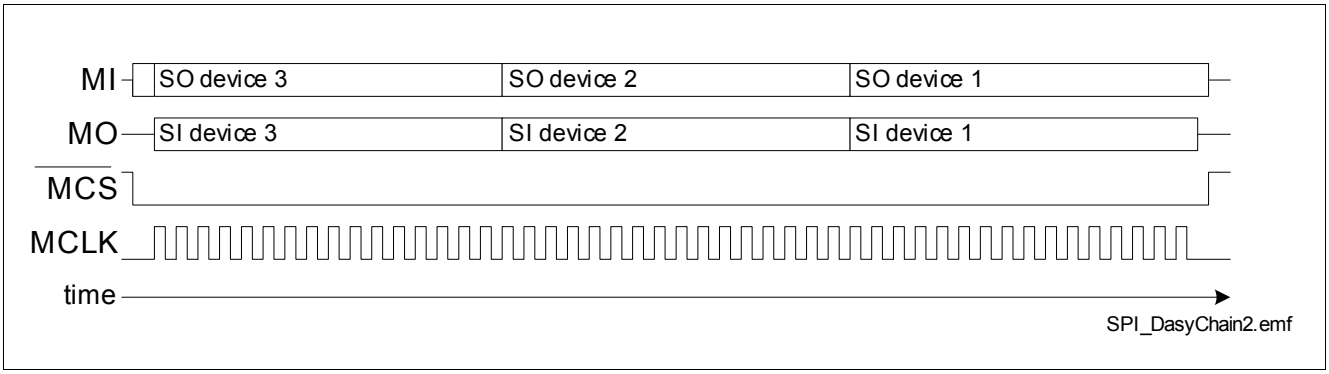


Figure 14 Data Transfer in Daisy Chain Configuration

5.4.3 Timing Diagrams

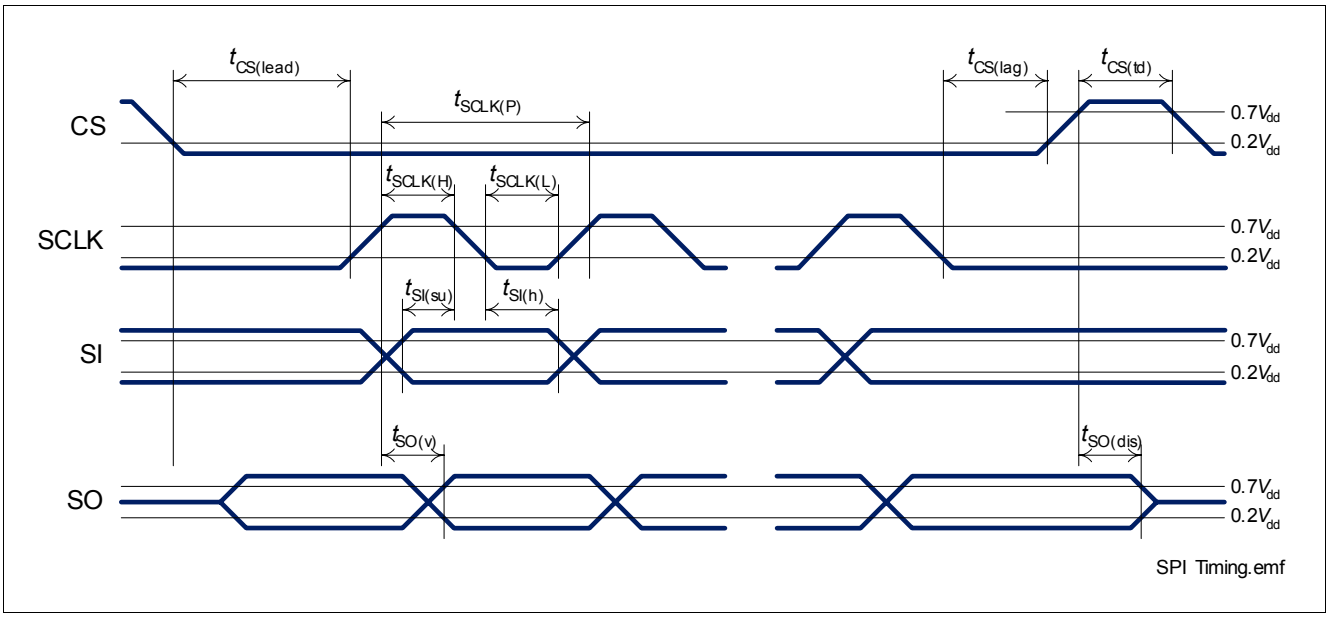


Figure 15 Timing Diagram

5.4.4 Electrical Characteristics

Electrical Characteristics: SPI

V_{DD} = 4.5 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified); typical values: V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power Supply							
5.4.1	Power supply voltage for SO buffer	V_{VSO}	3.0	–	5.5	V	–
Input Characteristics ($\overline{CS}$, SCLK, SI)							
5.4.2	L level of pin $\overline{CS}$ SCLK SI	 $V_{CS(L)}$ $V_{SCLK(L)}$ $V_{SI(L)}$	0	–	1	V	–
5.4.3	H level of pin $\overline{CS}$ SCLK SI	 $V_{CS(H)}$ $V_{SCLK(H)}$ $V_{SI(H)}$	2	–	V_{DD}	V	–
5.4.4	L-input pull-up current through $\overline{CS}$	$I_{CS(L)}$	10	20	50	µA	V_{CS} = 0 V
5.4.5	H-input pull-up current through $\overline{CS}$	$I_{CS(H)}$	5	–	50	µA	[1] V_{CS} = 2 V
5.4.6	L-input pull-down current through pin SCLK SI	 $I_{SCLK(L)}$ $I_{SI(L)}$	 5 5	 – –	 50 50	µA	[1] V_{SCLK} = 1 V V_{SI} = 1 V

Electrical Characteristics: SPI (cont'd)

V_{DD} = 4.5 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified); typical values: V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.7	H-input pull-down current through pin SCLK SI	 $I_{SCLK(H)}$ $I_{SI(H)}$	 10 10	 20 20	 50 50	µA	 V_{SCLK} = 5 V V_{SI} = 5 V
Output Characteristics (SO)							
5.4.8	L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = -2.5 mA
5.4.9	H level output voltage	$V_{SO(H)}$	– 4.6 2.4	– – –	– 5 3	–	I_{SO} = 2 mA V_{VSO} = 5 V V_{VSO} = 3 V
5.4.10	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} = V_{DD}
Timings							
5.4.11	Serial clock frequency	f_{SCLK}	0	–	5	MHz	–
5.4.12	Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	–
5.4.13	Serial clock high time	$t_{SCLK(H)}$	50	–	–	ns	–
5.4.14	Serial clock low time	$t_{SCLK(L)}$	50	–	–	ns	–
5.4.15	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{SCLK(lead)}$	250	–	–	ns	–
5.4.16	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{SCLK(lag)}$	250	–	–	ns	–
5.4.17	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(del)}$	250	–	–	ns	–
5.4.18	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	–
5.4.19	Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	–

1) Not subject to production test, specified by design.

5.4.5 SPI Protocol

The SPI protocol of the SPIDER - TLE7230GS provides two types of registers. The control registers and the diagnosis registers. After power-on reset, all register bits set to default values.

SI

Reset Value: $xxxx_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD		0	0	0	ADDR			DATA							

Field	Bits	Type	Description
CMD	15:14		**Command** 00 Diagnosis only: The requested data is shifted out at SO. This command does not change any register setting. 01 Read register: The register content of the addressed register will be sent in the next frame. 10 Reset registers: All registers are reset to their default values. 11 Write register: The data of the SI word will be written to the addressed register.
ADDR	10:8		**Address** Pointer to register for read and write command
DATA	7:0		**Data** Data written to or read from register selected by address ADDR

SO

Standard Diagnosis

Reset Value: $xxxx_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH7		CH6		CH5		CH4		CH3		CH2		CH1		CH0	

Field	Bits	Type	Description
CHn (n = 7-0)	(2n+1):2n		**Standard Diagnosis for Channel n** 00 Short circuit to GND 01 Open load 10 Overload, overtemperature 11 Normal operation

SO

Second Frame of Read Command

Reset Value: $xxxx_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	ADDR			DATA							

Field	Bits	Type	Description
ADDR	10:8		**Address** Pointer to register for read and write command
DATA	7:0		**Data** Data written to or read from register selected by address ADDR

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame.

5.4.6 Register Overview

Name	W/$\overline{R}$	Addr	7	6	5	4	3	2	1	0	Default[1)]
IMCR	W/R	001_B	MAP7	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0	08_H
BOCR	W/R	010_B	BOL7	BOL6	BOL5	BOL4	BOL3	BOL2	BOL1	BOL0	00_H
OLCR	W/R	011_B	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0	00_H
OTCR	W/R	100_B	OVT7	OVT6	OVT5	OVT4	OVT3	OVT2	OVT1	OVT0	00_H
SRCR	W/R	101_B	SLE7	SLE6	SLE5	SLE4	SLE3	SLE2	SLE1	SLE0	00_H
STA	R	110_B	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0	00_H
CTL	W/R	111_B	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0	00_H

1) The default values are set after reset.

Due to the default value of the mapping register the IN3 is mapped to OUT3 after power up.

6 Application Circuit

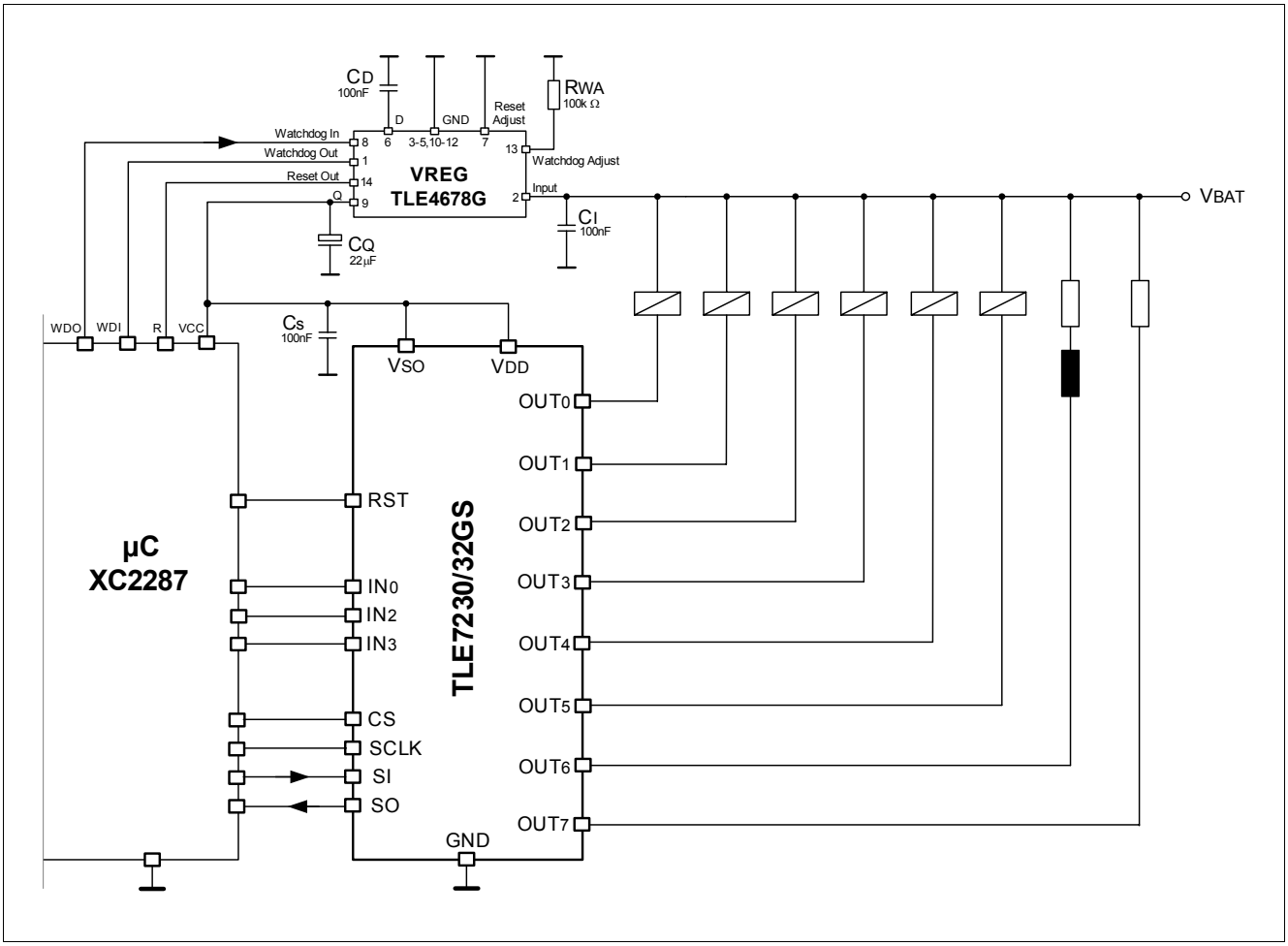


Figure 16 Application Circuit

7 Package Outlines

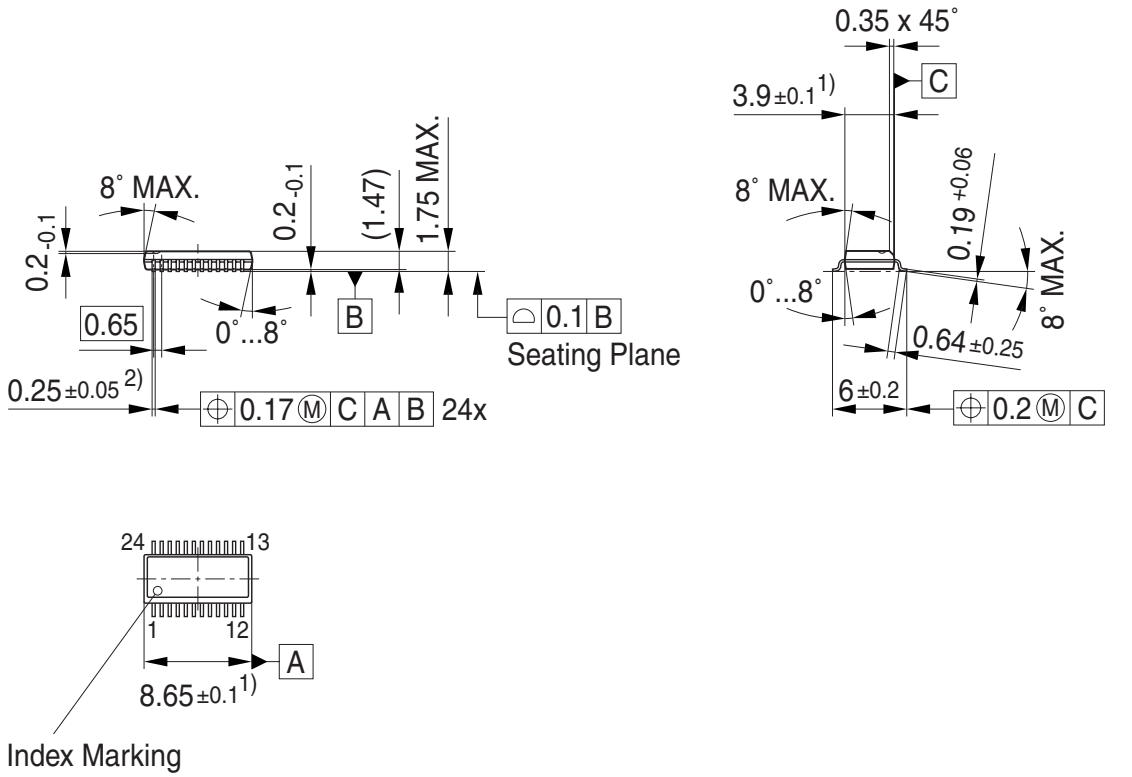


Figure 17 PG-SSOP-24-6 (Plastic Green Shrink Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
Rev. 1.0	2007-12-18	layout completely updated (A4 page size)
		Application circuit added
		Nominal load current inserted (page 14)
		Thermal Resistance section (page 15) updated

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