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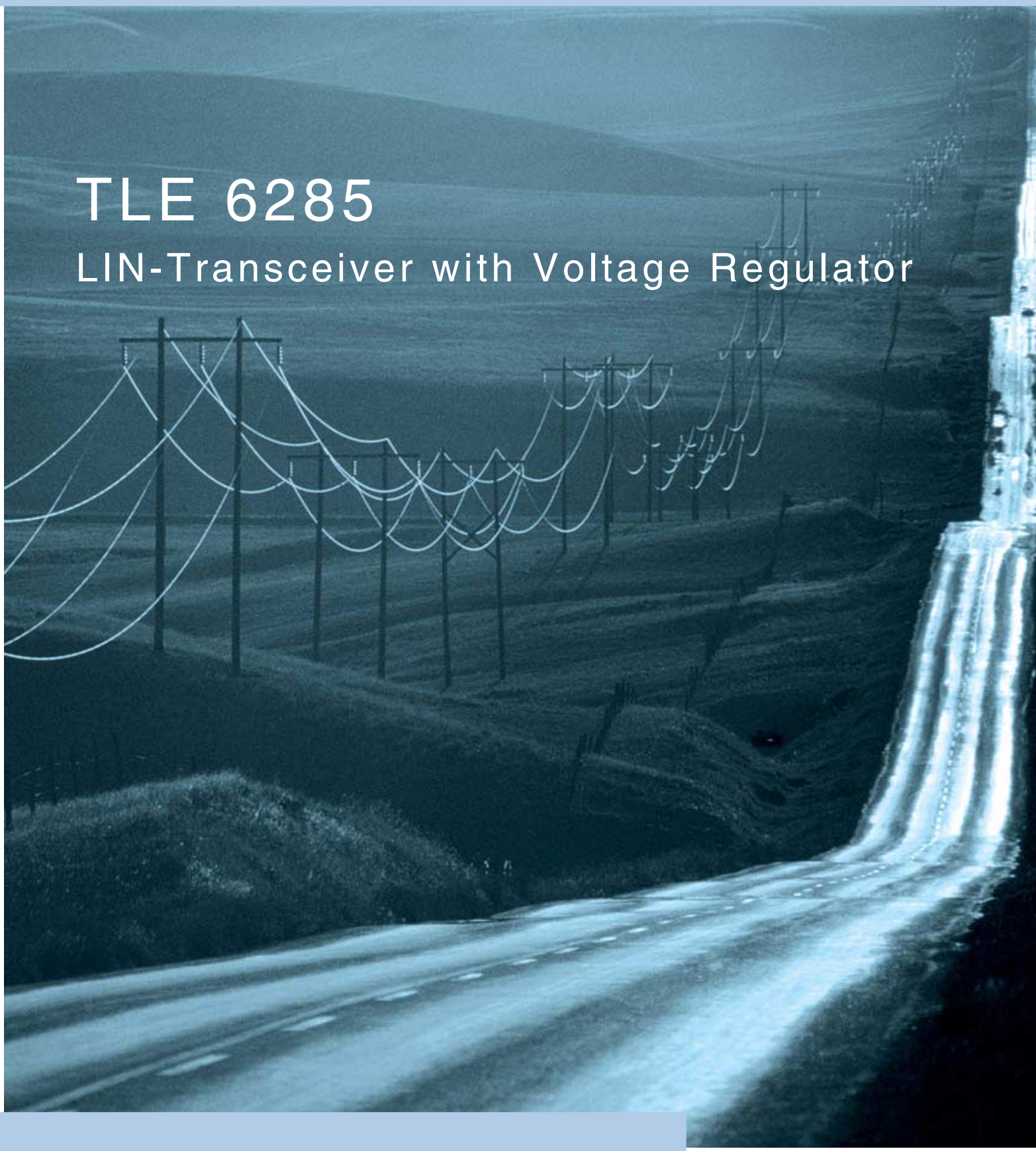
TLE 6285

LIN-Transceiver with Voltage Regulator



Automotive Power

Infineon technologies

Never stop thinking.

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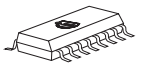
Features

- Single-wire transceiver, suitable for **LIN** protocol
- Transmission rate up to 20 kBaud
- Compatible to LIN specification 1.3, 2.0
- Compatible to ISO 9141 functions
- Low current consumption in sleep mode
- Control output for voltage regulator
- LIN bus, short circuit proof to ground and battery
- Integrated 5V ±2%, low drop voltage regulator
- 150 mA output current capability
- Adjustable reset threshold
- Overtemperature protection
- Wide temperature range
- Suitable for use in automotive electronics



P-DSO-16-9, -11

Description

The TLE 6285 is a single-wire transceiver with a LDO. It is a chip by chip integrated circuit in a P-DSO-16-11 package. It works as an interface between the protocol controller and the physical bus. The TLE 6285 is especially suitable to drive the bus line in LIN systems in automotive and industrial applications. Further it can be used in standard ISO9141 systems.

In order to reduce the current consumption the TLE 6285 offers a sleep operation mode. In this mode a voltage regulator can be controlled in order to minimize the current consumption of the whole application. The on-chip voltage regulator (VR) is designed for this application but it is also possible to use an external voltage regulator. A wake-up caused by a message on the bus enables the voltage regulator and sets the RxD output low until the device is switched to normal operation mode. To achieve proper operation of the µC, the device supplies a reset signal. The reset delay time is selected application specific by an external capacitor. The reset threshold is adjustable.

The TLE 6285 is designed to withstand the severe conditions of automotive applications.

Type	Ordering Code	Package
TLE 6285 G	Q67065-A7059	P-DSO-16-11

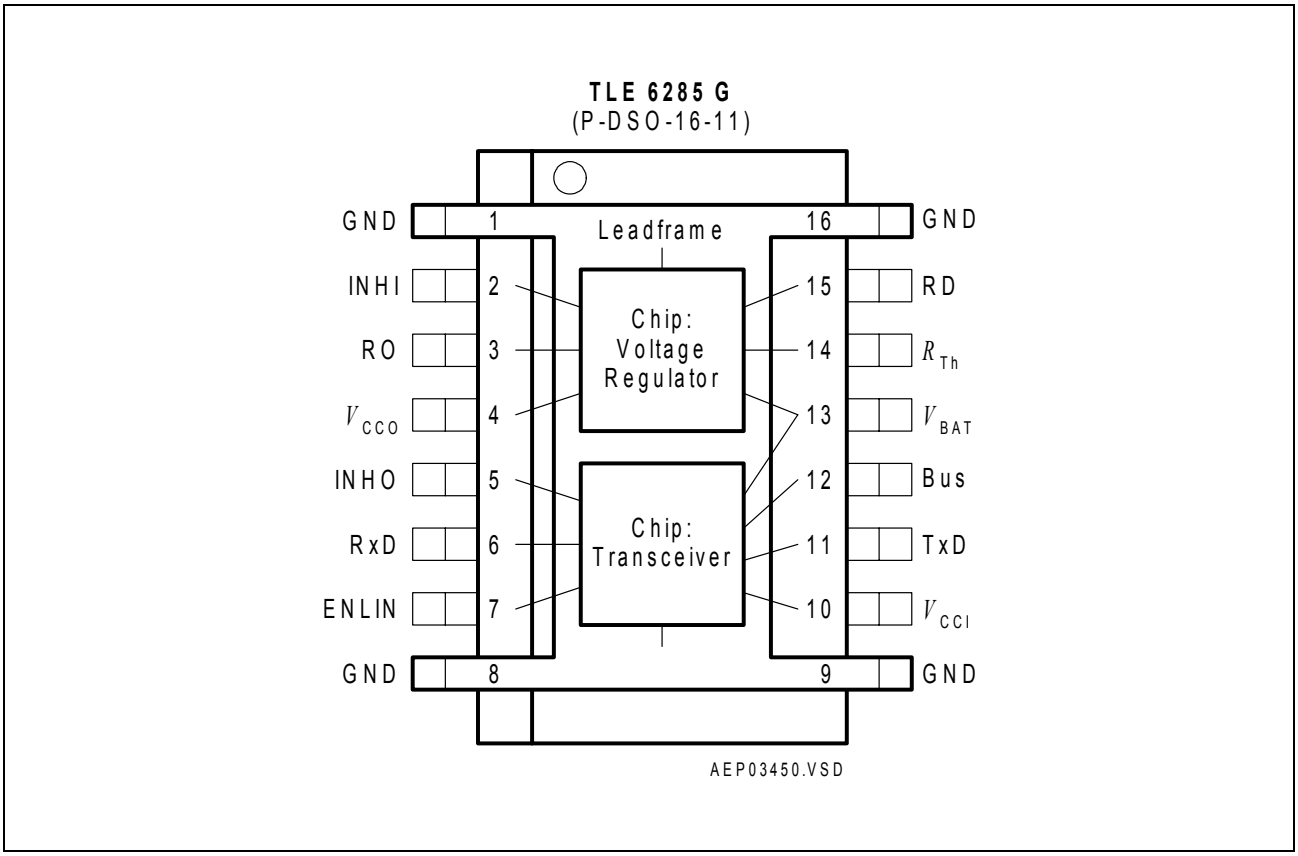


Figure 1 **Pin Configuration** (top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1, 8, 9, 16	GND	**Ground;** place to cooling tabs to improve thermal behavior
2	INHI	**Inhibit Voltage Regulator Input;** TTL compatible, HIGH active (HIGH switches the VR on); connect to V_{BAT} if not needed
3	RO	**Reset Output;** open collector output connected to the output via a resistor of 20 kΩ
4	V_{CCO}	**5-V Output;** connected to GND with 22 µF capacitor, ESR < 5Ω
5	INHO	**Inhibit LIN Output;** to control a voltage regulator
6	RxD	**Receive Data Output;** Integrated pull-up, LOW in dominate state
7	ENLIN	**Enable LIN Input;** integrated 30 kΩ pull-down, transceiver in normal operation mode when HIGH
10	V_{CCI}	**5-V Supply Input;** V_{CC} input to supply the LIN transceiver
11	TxD	**Transmit Data Input;** internal pull-up, LOW in dominant state
12	BUS	**LIN BUS Output/Input;** internal 30 kΩ pull-up to V_S, LOW in dominant state
13	V_{BAT}	**Battery Supply Input;** a reverse current protection diode is required, block GND with 100 nF ceramic capacitor and 22 µF capacitor
14	RTh	**Reset Threshold;** internal defined typical 4.6 V, adjustable down to 3.5 V according to the voltage level on this pin; connect to GND if not needed
15	RD	**Reset Delay;** connected to ground via external delay capacitor

Functional Block Diagram

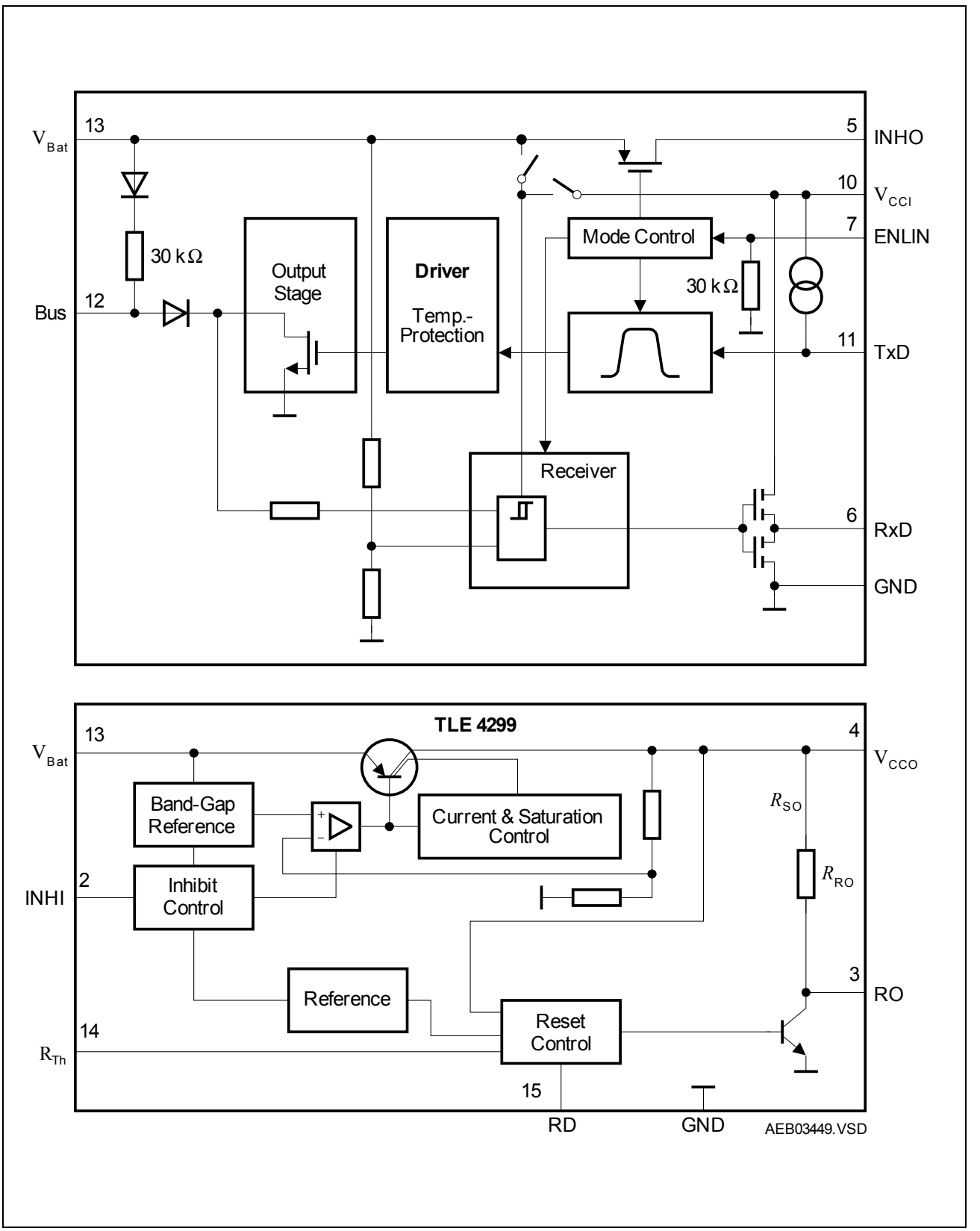


Figure 2 Block Diagram

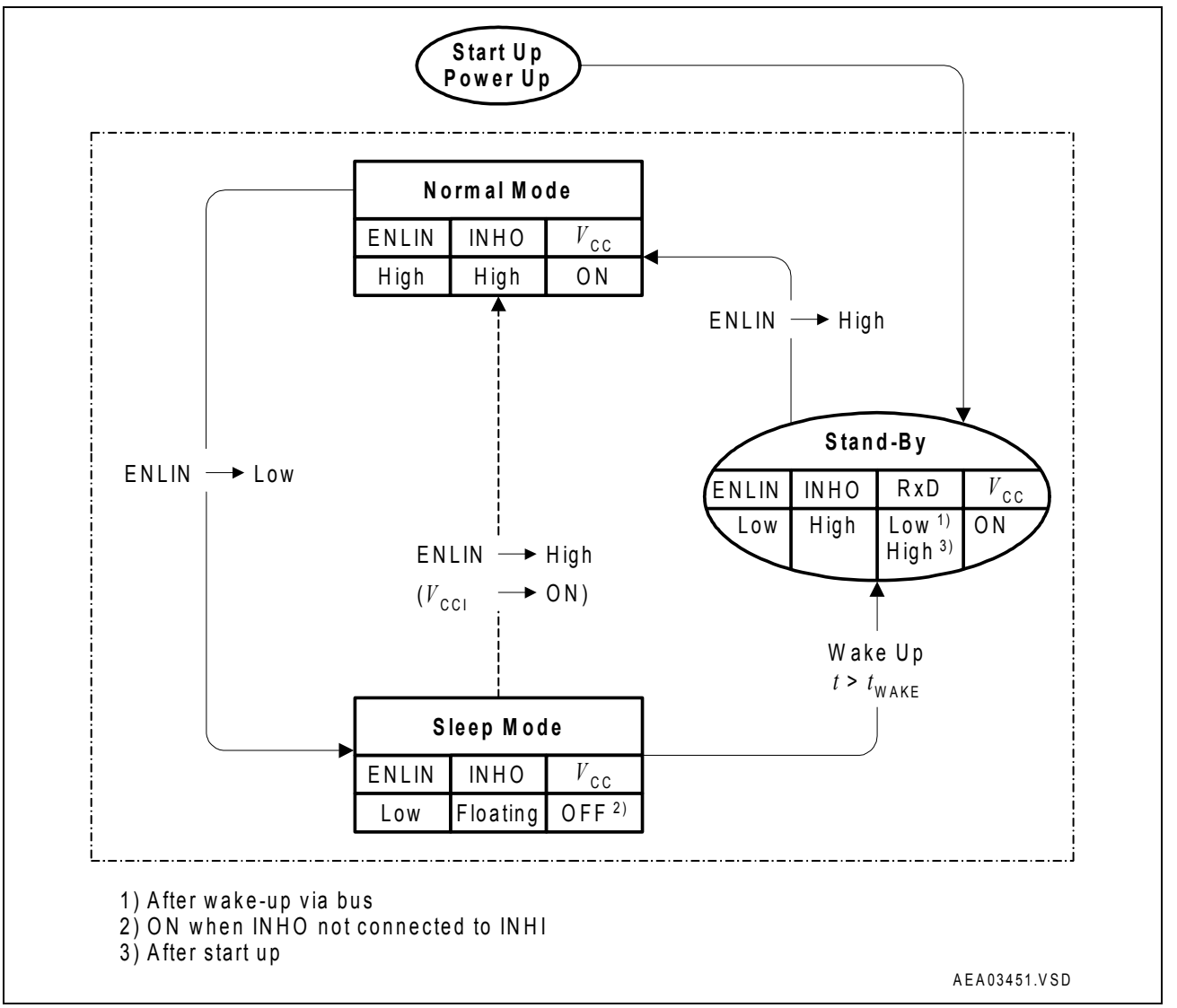


Figure 3 Operation Mode State Diagram

Operation Modes

In order to reduce the current consumption the TLE 6285 offers a sleep operation mode. This mode is selected by switching the enable input ENLIN low (see **Figure 3**, **Operation Mode State Diagram**). In the sleep mode a voltage regulator can be controlled via the INHO output in order to minimize the current consumption of the whole application. A wake-up caused by a message on the communication bus automatically enables the voltage regulator by switching the INHO output high. In parallel the wake-up is indicated by setting the RxD output low. When entering the normal mode this wake-up flag is reset and the RxD output is released to transmit the bus data.

In case the voltage regulator control input is not connected to INH output or the microcontroller is active respectively, the TLE 6285 can be set in normal operation mode without a wake-up via the communication bus.

LIN Transceiver

The LIN Transceiver has already a pull-up resistor of 30 kΩ as termination implemented. There is also a diode in this path, to protect the circuit from feedback of voltages from the bus line to the power supply. To configure the TLE 6285 as a master node, an additional external termination resistor of 1 kΩ is required. To avoid reverse currents from the bus line into the battery supply line in case of an unpowered node, it is also recommended to place a diode in series to the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF in the master node (see **Figure 5**, **Application Example**).

An capacitor of 10 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line.

Input Capacitor

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 5 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

Voltage Regulator

The TLE 6285 incorporates a PNP based very low drop linear voltage regular. It regulates the output voltage to V_{CC} = 5 V for an input voltage range of 6 V ≤ V_I ≤ 35V. The control circuit protects the device against potential caused by damages overcurrent and overtemperature.

The internal control circuit achieves a 5 V output voltage with a tolerance of ±2% in the temperature range of T_j = -40 to 125 °C.

The device includes a power on reset and an under voltage reset function with adjustable reset delay time and adjustable reset switching threshold as well as a sense control/early warning function. The device includes an inhibit function to disable it when the ECU is not used for example while the motor is off.

The reset logic compares the output voltage V_{CC} to an internal threshold. If the output voltage drops below this level, the external reset delay capacitor C_D is discharged. When V_D is lower than V_{LD}, the reset output RO is switched Low. If the output voltage drop is

very short, the V_{LD} level is not reached and no reset-signal is asserted. This feature avoids resets at short negative spikes at the output voltage e.g. caused by load changes.

As soon as the output voltage is more positive than the reset threshold, the delay capacitor is charged with constant current. When the voltage reaches V_{UD} the reset output RO is set High again.

The reset threshold is either the internal defined V_{RT} voltage (typical 4.6 V) or can be lowered by a voltage level at the RTh input down to 3.5 V. The reset delay time and the reset reaction time are defined by the external capacitor C_D. The reset function is active down to V_I = 1 V.

The device is capable to supply 150 mA. For protection at high input voltage above 25 V, the output current is reduced (SOA protection).

Reset

The power on reset feature is necessary for a defined start of the microprocessor when switching on the application. For the reset delay time after the output voltage of the regulator is above the reset threshold, the reset signal is set High again. The reset delay time is defined by the reset delay capacitor C_{RD} at pin RD (refer to **Figure 4** and **Figure 5**).

The undervoltage reset circuitry supervises the output voltage. In case V_Q decreases below the reset threshold the reset output is set LOW after the reset reaction time. The reset LOW signal is generated down to an output voltage V_Q to 1 V. Both the reset reaction time and the reset delay time is defined by the capacitor value.

The power on reset delay time is defined by the charging time of an external delay capacitor C_D.

$$C_D = (t_d \times I_D) / \Delta V \quad (1)$$

Definitions:

- C_D = reset delay capacitor
- t_d = reset delay time
- $\Delta V = V_{UD}$, typical 1.8 V for power up reset
- $\Delta V = V_{UD} - V_{LD}$, typical 1.35 V for undervoltage reset
- I_D = charge current typical 6.5 µA

For a delay capacitor C_D = 100 nF the typical power on reset delay time is 28 ms.

The reset reaction time t_{RR} is the time it takes the voltage regulator to set reset output LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 100 nF. For other values for C_D the reaction time can be estimated using the following equation:

$$t_{RR} = 10 \text{ ns / nF} \times C_D \quad (2)$$

The reset output is an open collector output with a pull-up resistor of typical 20 kΩ to Q. An external pull-up can be added with a resistor value of at least 5.6 kΩ.

In addition the reset switching threshold can be adjusted by an external voltage divider. The feature is useful for microprocessors which guarantee safe operation down to voltages below the internally set reset threshold of 4.65 V typical.

If the internal used reset threshold of typical 4.65 V is used, the pin RTh has to be connected to GND.

If a lower reset threshold is required by the system, a voltage divider defines the reset threshold V_{Rth} between 3.5 V and 4.60 V:

$$V_{Rth} = V_{RADJ\ TH} \times (R_1 + R_2) / R_2 \quad (3)$$

$V_{RADJ\ TH}$ is typical 1.36 V.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Supply voltage	V_{CC}	-0.3	6	V	–
Battery supply voltage	V_S	-0.3	40	V	–
Bus input voltage	V_{bus}	-20	32	V	–
Bus input voltage	V_{bus}	-20	40	V	t < 1 s
Logic voltages at EN, TxD, RxD	V_I	-0.3	V_{CC} + 0.3	V	0 V < V_{CC} < 5.5 V
Input voltages at INHO	V_{INHO}	-0.3	V_S + 0.3	V	–
Output current at INHO	I_{INHO}	–	20	mA	–
Reset output voltage	V_R	-0.3	7	V	–
Reset delay voltage	V_D	-0.3	7	V	–
Output voltage on V_{CCO}	V_Q	-0.3	7	V	–
INHI input voltage	V_{INH}	-40	40	V	–
Reset Threshold voltage	V_{Th}	-0.3	7	V	–
Reset Threshold current	I_{Th}	-10	10	mA	–
Electrostatic discharge voltage at V_S, Bus	V_{ESD}	-4	4	kV	human body model (100 pF via 1.5 kΩ)
Electrostatic discharge voltage	V_{ESD}	-2	2	kV	human body model (100 pF via 1.5 kΩ)
Temperatures					
Junction temperature	T_j	-40	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{CC}	4.5	5.5	V	–
Battery Supply Voltage	V_S	6	35	V	–
Junction temperature	T_j	-40	150	°C	–
Thermal Shutdown (junction temperature)					
Thermal shutdown temp.	T_{jSD}	150	170	190	°C
Thermal shutdown hyst.	ΔT	–	10	–	K
Thermal Resistances					
Junction ambient	$R_{thj\text{-}a}$	–	80	K/W	PCB heat sink area 300mm^2

Table 4 Electrical Characteristics

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Current Consumption						
Current consumption at V_{Bat} (LIN + Voltage Regulator)	I_{Bat}	–	1.1	3	mA	recessive state; INHI = INHO = HIGH; $V_{TxD} = V_{CC}$
	I_{Bat}	–	1.9	4	mA	dominant state; INHI = INHO = HIGH; $V_{TxD} = V_{CC}$
Current consumption at V_{CCI} (LIN only)	I_{CCI}	–	0.4	0.7	mA	recessive state; LDO sleep; $V_{TxD} = V_{CC}$
	I_{CCI}	–	0.4	0.8	mA	dominant state; LDO sleep; V_{TxD} = 0 V
Current consumption sleep mode (LIN + Voltage Regulator)	I_{Bat}	–	20	40	µA	sleep mode; INHI = INHO = LOW;
(LIN only)	I_{CCI}	–	3	10	µA	sleep mode; INHI = INHO = LOW
Current consumption LDO (Voltage Regulator, LIN in sleep mode)	I_{Bat}	–	170	500	µA	I_{CCO} = 10 mA;
	I_{Bat}	–	0.7	2	mA	I_{CCO} = 50 mA;
Enable Input (pin ENLIN)						
HIGH level input voltage threshold	$V_{EN,on}$	–	2.8	0.7 × V_{CC}	V	normal mode
LOW level input voltage threshold	$V_{EN,off}$	0.3 × V_{CC}	2.2	–	V	low power mode
EN input hysteresis	$V_{EN,hys}$	300	600	900	mV	–
EN pull-down resistance	R_{EN}	15	30	60	kΩ	–
Inhibit Output (pin INHO)						
Inhibit R_{on} resistance	R_{onINHO}		65	120	Ω	I_{INH} = - 15 mA

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Leakage current	$I_{INHO,lk}$	-5.0	–	5.0	µA	sleep mode; V_{INHO} = 0 V
V_Q Output (pin V_{CCO})						
Output voltage	V_Q	4.90	5.00	5.10	V	1 mA ≤ I_Q ≤ 100 mA; 6 V ≤ V_I ≤ 16 V
Output voltage	V_Q	4.85	5.00	5.15	V	I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 16 V
Current limit	I_Q	250	400	500	mA	–
Drop voltage	V_{dr}	–	0.22	0.5	V	I_Q = 100 mA[1)]
Load regulation	ΔV_Q	–	5	30	mV	I_Q = 1 mA to 100 mA
Line regulation	ΔV_Q	–	10	25	mV	V_I = 6 V to 28 V; I_Q = 1 mA
Power Supply Ripple rejection	$PSRR$	–	66	–	dB	[2)] f_r = 100 Hz; V_r = 1 Vpp; I_Q = 100 mA

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Reset Generator (pins RO, RD)						
Switching threshold	V_{rt}	4.50	4.60	4.80	V	–
Reset pull-up	R_{RO}	10	20	40	kΩ	–
Reset low voltage	V_R	–	0.17	0.40	V	[3] V_Q < 4.5 V; internal R_{RO}; I_R = 1 mA
External reset pull-up	$R_{RO\ ext}$	5.6	–	–	kΩ	Pull-up resistor pin RO to pin V_{CCO}
Delay switching threshold	V_{DT}	1.5	1.85	2.2	V	–
Switching threshold	V_{ST}	0.35	0.50	0.60	V	–
Reset delay low voltage	V_D	–	–	0.1	V	$V_Q < V_{RT}$
Charge current	I_{ch}	4.0	8.0	12.0	µA	V_D = 1 V
Reset delay time	t_d	17	28	35	ms	C_D = 100 nF
Reset reaction time	t_{RR}	0.5	1.2	3.0	µs	C_D = 100 nF
Reset adjust switching threshold	$V_{RADJ\ TH}$	1.26	1.36	1.44	V	V_Q > 3.5 V
Inhibit Input (pin INHI)						
Inhibit OFF voltage range	$V_{INHI\ OFF}$	–	–	0.8	V	V_Q off
Inhibit ON voltage range	$V_{INHI\ ON}$	3.5	–	–	V	V_Q on
High input current	$I_{INHI\ ON}$	–	3	8	µA	V_{INHI} = 5 V
Low input current	$I_{INHI\ OFF}$	–	0.5	2	µA	V_{INHI} = 0 V
Receiver Output RxD						
HIGH level output current	$I_{RD,H}$	-1.2	-0.8	-0.5	mA	$V_{RD} = 0.8 \times V_{CC}$
LOW level output current	$I_{RD,L}$	0.5	0.8	1.2	mA	$V_{RD} = 0.2 \times V_{CC}$

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TD,H}$	–	2.9	0.7 × V_{CC}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	300	700	900	mV	–
LOW level input voltage threshold	$V_{TD,L}$	0.3 × V_{CC}	2.1	–	V	dominant state
TxD pull-up current	I_{TD}	-150	-110	-70	µA	V_{TxD} < 0.3 V_{CC}
Bus Receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.44 × V_S	0.48 × V_S	–	V	-8 V < V_{bus} < $V_{bus,dom}$
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$	–	0.52 × V_S	0.60 × V_S	V	$V_{bus,rec}$ < V_{bus} < 20 V
Receiver hysteresis	$V_{bus,hys}$	0.02 × V_S	0.04 × V_S	0.1 × V_S	mV	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$
Receiver threshold center voltage	$V_{bus,cnt}$	0.475 × V_S	0.5 × V_S	0.525 × V_S		LIN2.0 table 3.1
Input leakage current	$I_{bus,lek}$	-1			mA	V_{bus} = 0V, V_{bat} = 12V, pull-up resistor as specified in LIN2.0
Wake-up threshold voltage	V_{wake}	0.40 × V_S	0.55 × V_S	0.60 × V_S	V	–
Bus Transmitter						
Bus recessive output voltage	$V_{bus,rec}$	0.9 × V_S	–	V_S	V	V_{TxD} = V_{CC}
Bus dominant output voltage	$V_{bus,dom}$	0	–	2	V	V_{TxD} = 0 V 7.3V<V_S<27V
		0	–	1.2	V	V_{TxD} = 0 V 6V<V_S<7.3V
Bus short circuit current	$I_{bus,sc}$	40	85	150	mA	$V_{bus,short}$ = 13.5 V

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Leakage current	$I_{bus,lk}$	-1	-	–	mA	V_{CC} = 0 V, V_S = 0 V, V_{bus} = -8 V,
		–	10	20	µA	V_{CC} = 0 V, V_S = 13.5V, V_{bus} = 20 V,
Bus pull-up resistance	R_{bus}	20	30	47	kΩ	–

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Dynamic Transceiver Characteristics						
Falling edge slew rate	$S_{bus(L)}$	-3	-2.0	-1	V/µs	60% > V_{bus} > 40% 1 µs<(τ = R_{BUS}× C_{BUS})<5µs[4] V_{CC} = 5 V; V_S = 13.5 V
Rising edge slew rate	$S_{bus(H)}$	1	1.5	3	V/µs	40% < V_{bus} < 60% 1 µs<(τ = R_{BUS}× C_{BUS})<5µs[4] V_{CC} = 5 V; V_S = 13.5 V
Slope symmetry	$t_{slopesym}$	-5	–	5	µs	t_{fslope} - t_{rslope}
Propagation delay TxD LOW to bus	$t_{d(L),T}$	–	1	4	µs	V_{CC} = 5 V
Propagation delay TxD HIGH to bus	$t_{d(H),T}$	–	1	4	µs	V_{CC} = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RxD} = 20 pF
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$
Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T}$ = $t_{d(L),T}$ - $t_{d(H),T}$
Duty cycle D1	t_{duty1}	0.396	–	–	µs	duty cycle 1[4] TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit};
Duty cycle D2	t_{duty2}	–	–	0.581	µs	duty cycle 2[4] TH_{Rec}(max) = 0.422× V_S; TH_{Dom}(max) = 0.264 × V_S V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit};
Wake-up delay time	t_{wake}	30	100	150	µs	T_j ≤ 125 °C
		–	–	170	µs	T_j ≤ 150 °C [2]

Table 4 Electrical Characteristics (cont'd)

V_{CC} = 5V; V_S = 13.5V; R_L = 500 Ω; $V_{EN} > V_{EN,ON}$; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Delay time for change sleep/stand by mode - normal mode	t_{snorm}	–	–	50	µs	–
Delay time for change normal mode - sleep mode	t_{nsleep}	–	–	50	µs	–

1) Drop voltage = V_I - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)
2) Not subject to production test, specified by design.
3) The reset output is low within the range V_Q = 1 V to V_{rt}
4) Bus load conditions concerning LIN spec 2.0 C_{bus}, R_{bus} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω

Diagrams

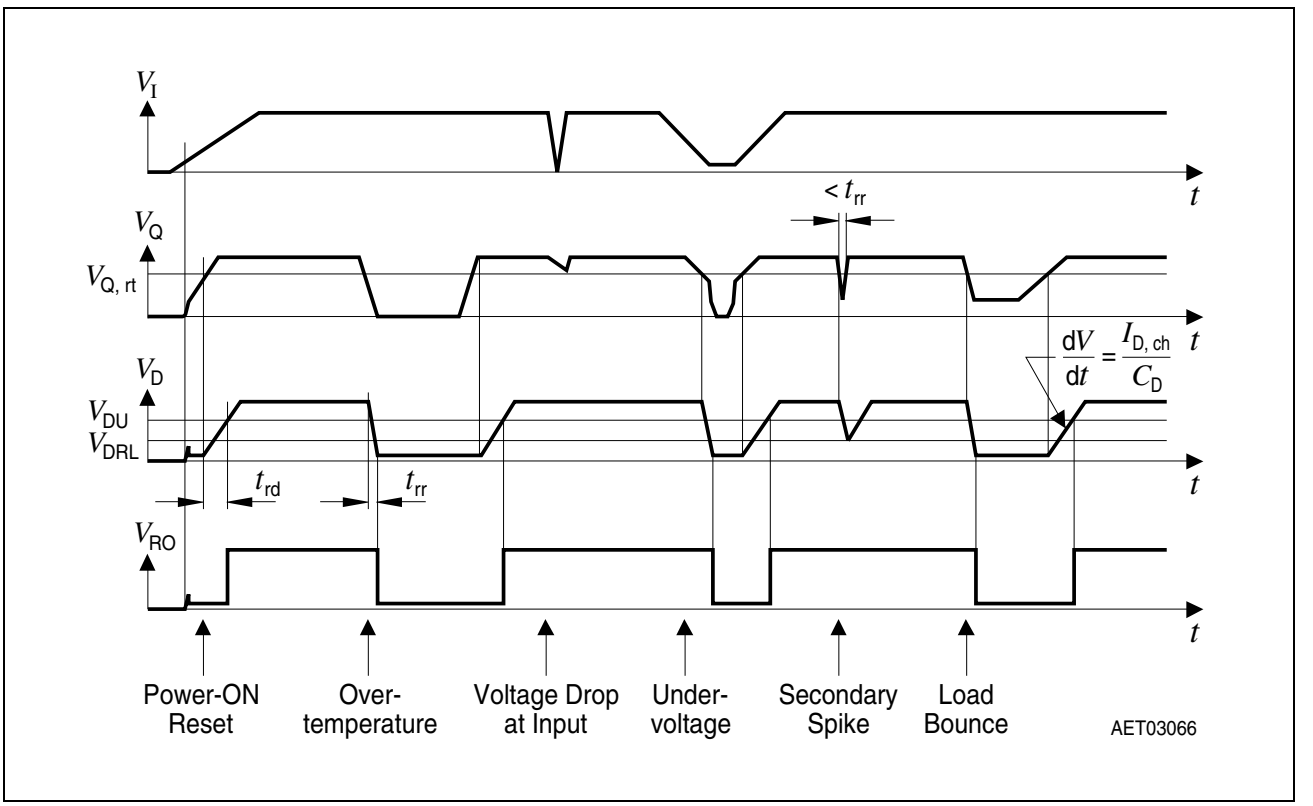
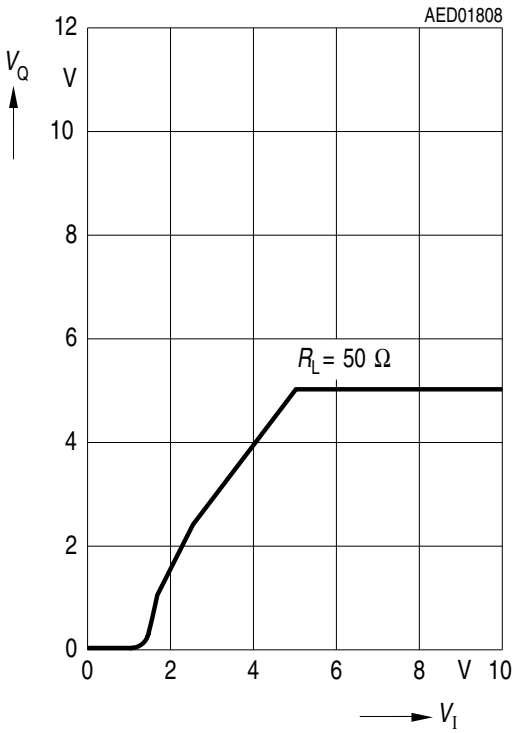


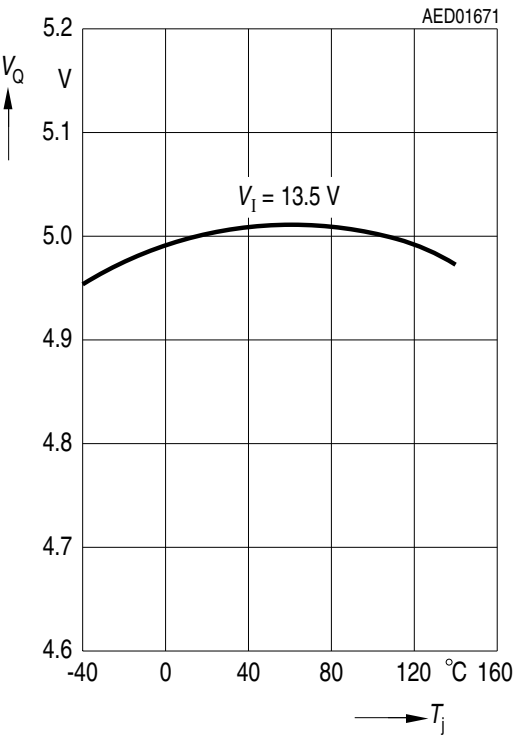
Figure 4 Time Response

Typical Performance Characteristics

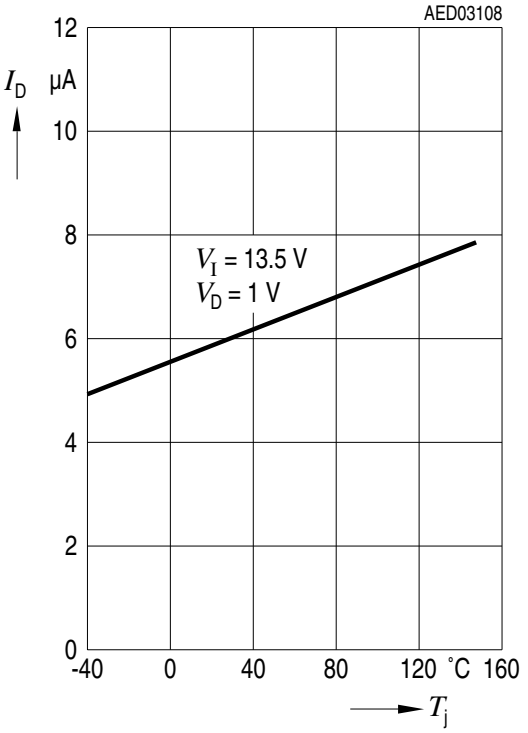
Output Voltage V_Q (PIN V_{CCO}) versus Input Voltage V_I (PIN V_{BAT})



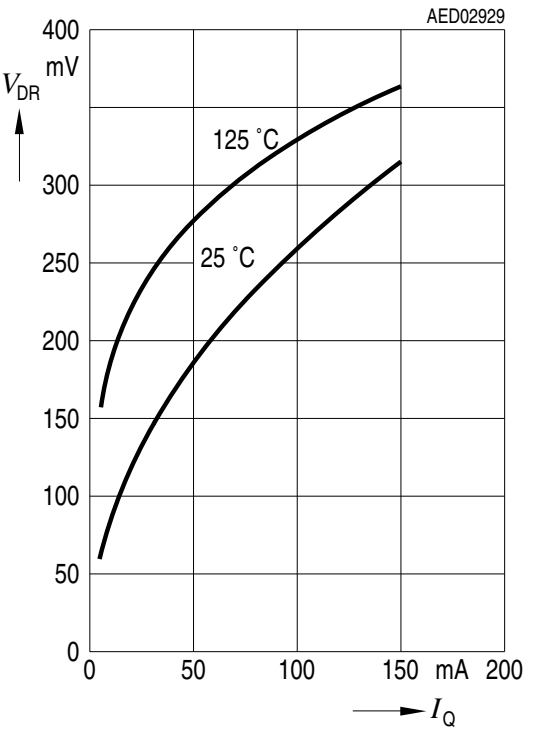
Output Voltage V_Q (PIN V_{CCO}) versus Temperature T_j



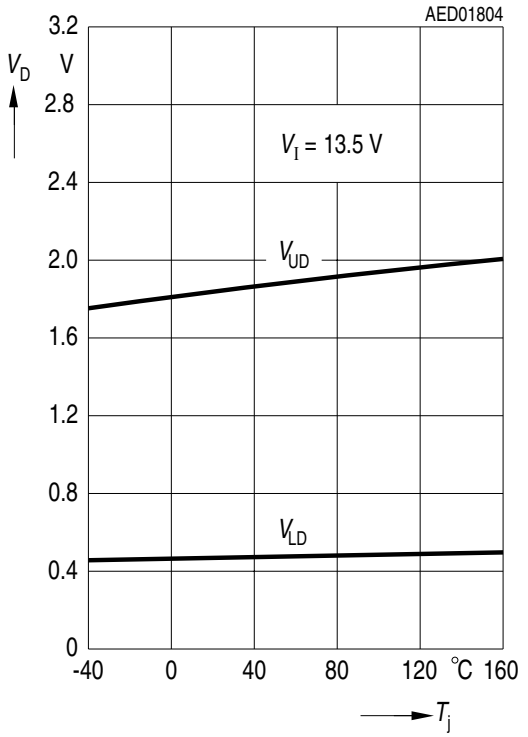
Charge Current I_{ch} versus Temperature T_j



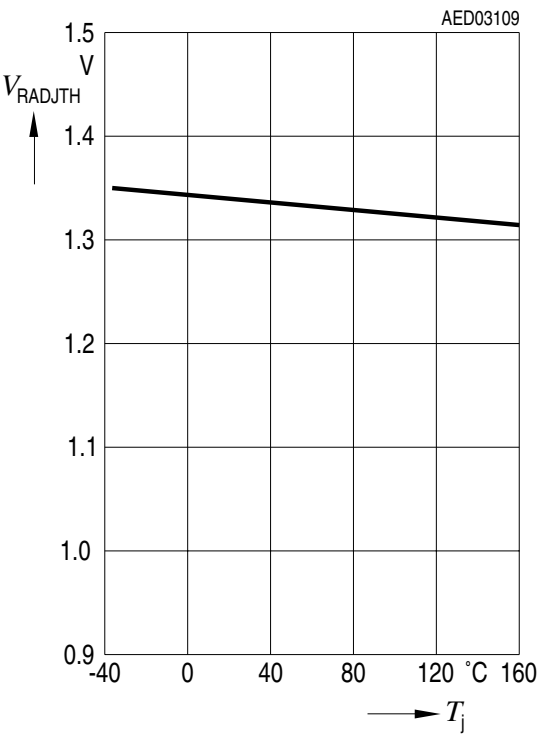
Drop Voltage V_{dr} versus Output Current I_Q (PIN V_{CCO})



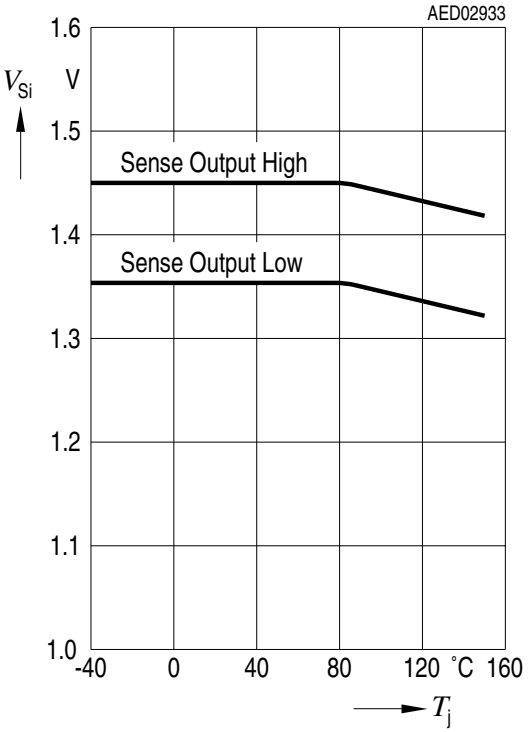
Switching Voltage V_{dt} and V_{st} versus Temperature T_j



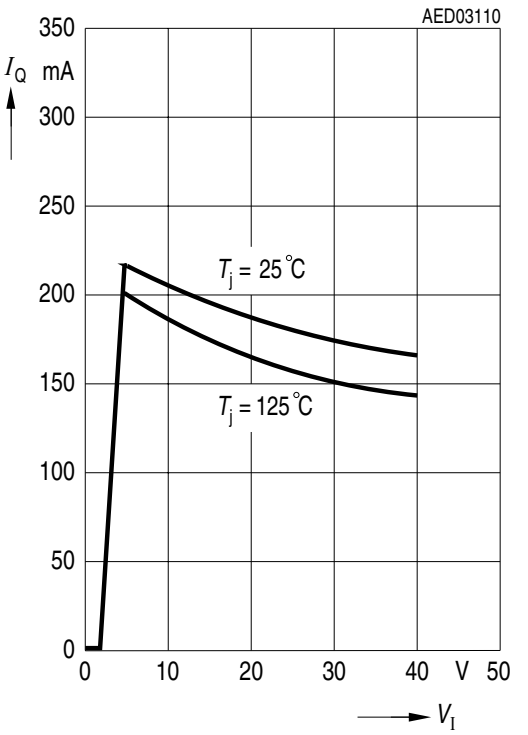
Reset Adjust Switching Threshold V_{RADJTH} versus Temperature T_j



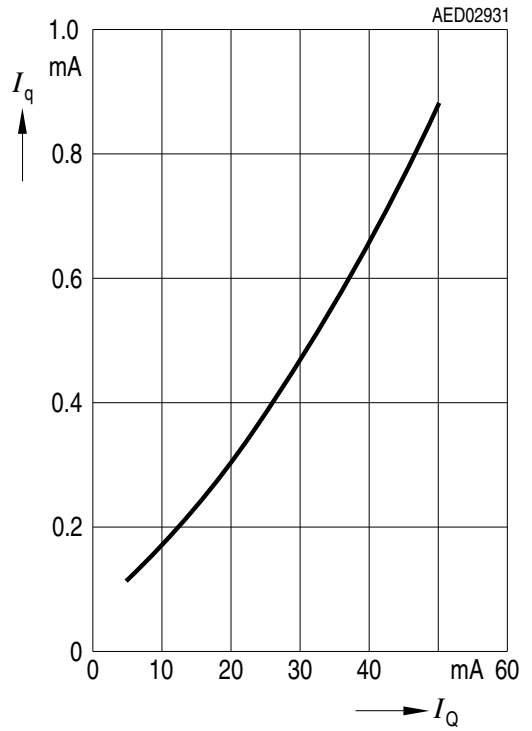
Sense Threshold V_{si} versus Temperature T_j



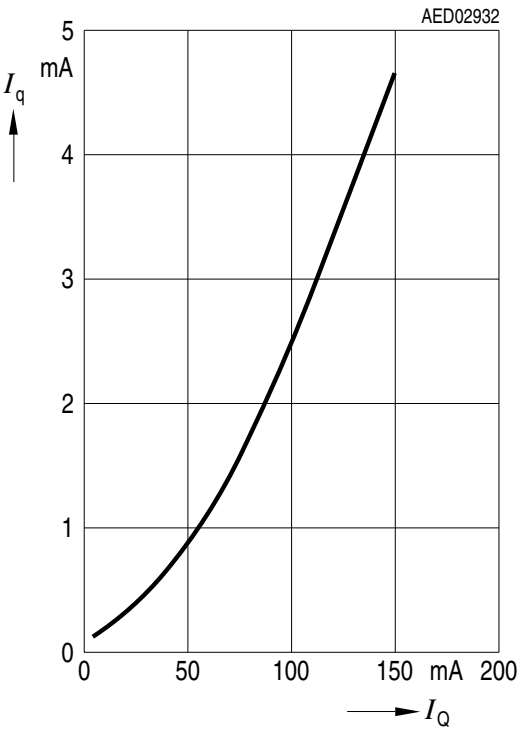
Output Current Limit I_Q (PIN V_{CCO}) versus Input Voltage V_I (PIN V_{BAT})



Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Output Current I_Q



Application

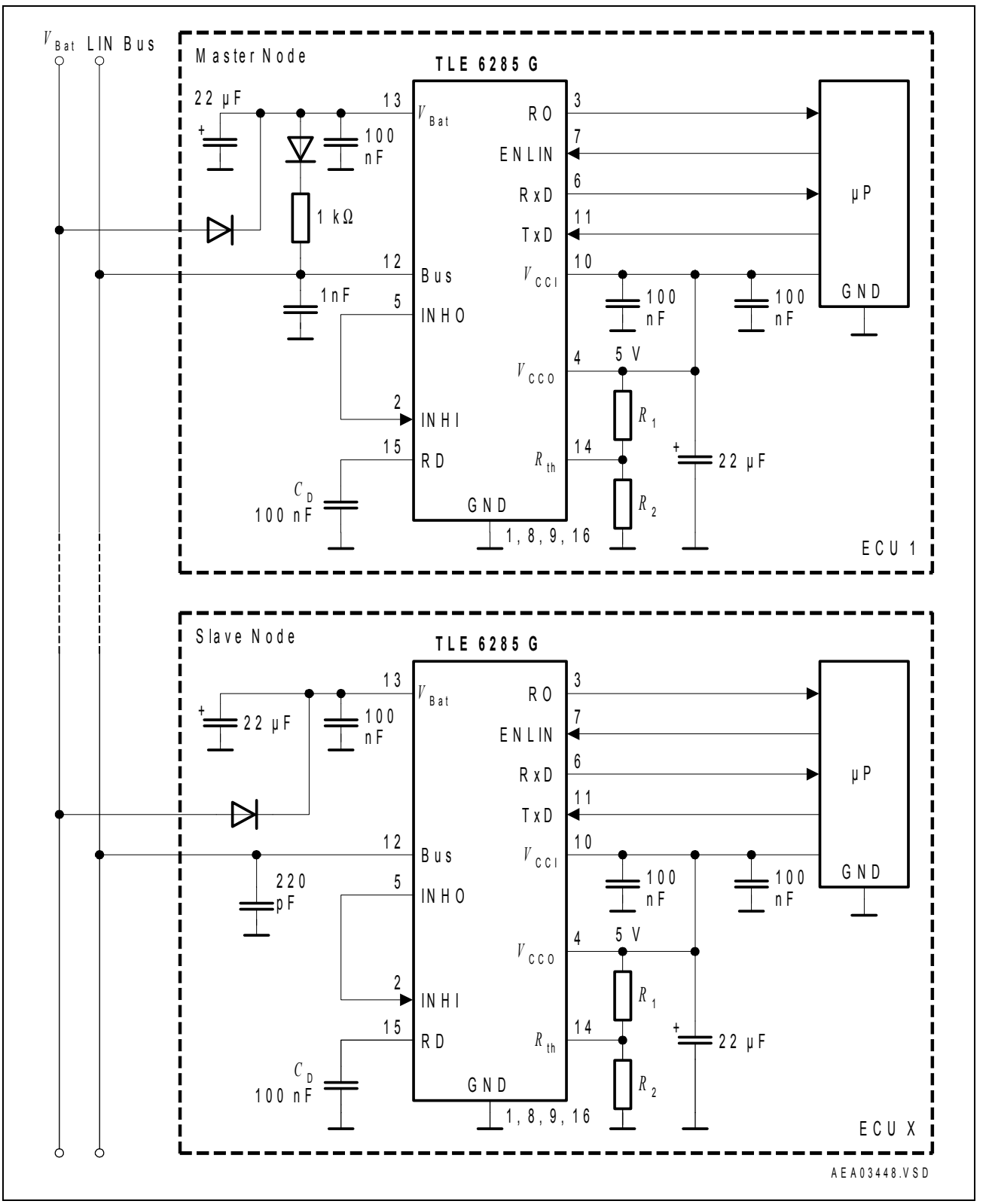
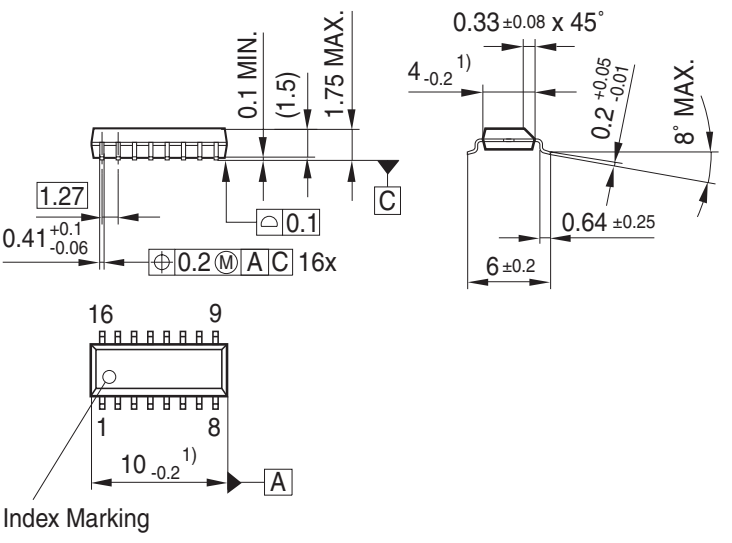


Figure 5 Application Example

Package Outlines



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPS09453

Figure 6 **P-DSO-16-11** (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm