

Data Sheet

High-Performance DrMOS

6mm x 6mm x 0.8mm IQFN

TDA21211- Data Sheet

August - 2009

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Power Management & Drive

Never stop thinking.

6x6 QFN High-Performance DrMOS

Features:

- Intel compliant DrMOS, Power MOSFET and Driver in one package
- For Synchronous Buck - step down voltage applications
- Maximum Average Current of 35A
- Wide input voltage range +5V to +30V
- Low power dissipation
- Extremely fast switching technology for improved performance at high switching frequencies (>1MHz)
- Remote Driver Disable function
- Switching Modulation (SMOD#) of low side MOS
- Includes active PMOS structure as integrated bootstrap circuit for reduced part count
- Shoot through protection
- +5V High and Low Side Driving voltage
- Compatible to standard PWM controller ICs with +3.3 and 5V logic
- Three-State PWM input functionality
- Small Package: IQFN40 (6 x 6 x 0.8 mm³)
- RoHS Compliant

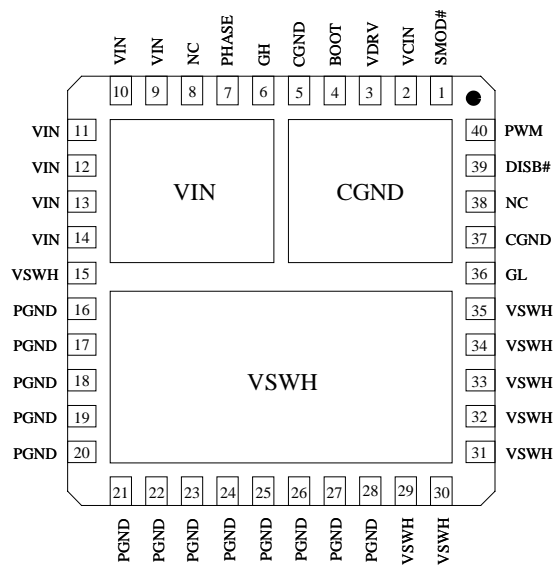


| Type | Package | Marking |
|----------|--|----------|
| TDA21211 | 6x6x0.8mm ³ PG-IQFN-40-1 | TDA21211 |

Applications:

- Desktop and Server VR11.X and VR12 Vcore and non-Vcore buck-converters
- Network and Telecom processor VR
- Single Phase and Multi-Phase POL
- CPU/GPU Regulation in Notebook, Graphics Cards, and Gaming
- Voltage Modules requiring high power density
- Memory (DDR2/3)

Pinout



Note:
Signals marked with "#" at the end are active low signals.

Figure 1. Pinout, numbering and name of pins (Transparent Top View)

Pin Description

| Pin Name | Pin No. | Description | Remarks |
|----------|------------------------|-----------------------------|---|
| CGND | 5, 37,CGND Pad | Control signal ground | Should be connected to PGND externally |
| SMOD# | 1 | Low side gate disable pin | when SMOD# is "low" the GL is OFF |
| VCIN | 2 | Logic supply voltage | 5V bias voltage for the internal logic. |
| VDRV | 3 | FET gate supply voltage | High & Low Side gate drive 5V |
| BOOT | 4 | Bootstrap voltage pin | Connect to boot capacitor |
| GH | 6 | High side gate signal | pin for monitoring gate of HS FET |
| PHASE | 7 | Switch node output | Internally connected to VSWH pin |
| NC | 8, 38 | No connect | Can be connected to any potential |
| VIN | 9 to 14, Vin Pad | Input Voltage | connection to the drain of the HS FET |
| VSWH | 15, 29 to 35, VSWH Pad | Switch node output | high current output switch node |
| PGND | 16 to 28 | Power ground | All of these pins must be connected to the power GND plane through multiple, low inductance vias. |
| GL | 36 | Low side gate signal | pin for monitoring gate of LS FET |
| DISB# | 39 | Disable Signal (active low) | pull to GND to disable the IC |
| PWM | 40 | PWM drive logic input | the three-state PWM input is compatible with 3.3V and 5V logic |

General Description

The Infineon TDA21211 is a multichip module that incorporates Infineon's premier MOSFET technology for a single high side and a single low side MOSFET coupled with a robust, high performance, high switching frequency gate driver in a single 40 pin QFN package. The optimized gate timing allows for significant light load efficiency improvements over discrete solutions. State of the art MOSFET technology provides exceptional full load performance. Thus this device has a clear advantage over existing approaches in the marketplace when both full load and light load efficiencies are important.

The Driver+MOSFET IC TDA21211 (DrMOS) is pin to pin compatible and compliant with the Intel 6x6 DrMOS specification. The device package height is only 0.8mm, and is an excellent choice for applications with critical height limitations.

BLOCK DIAGRAM

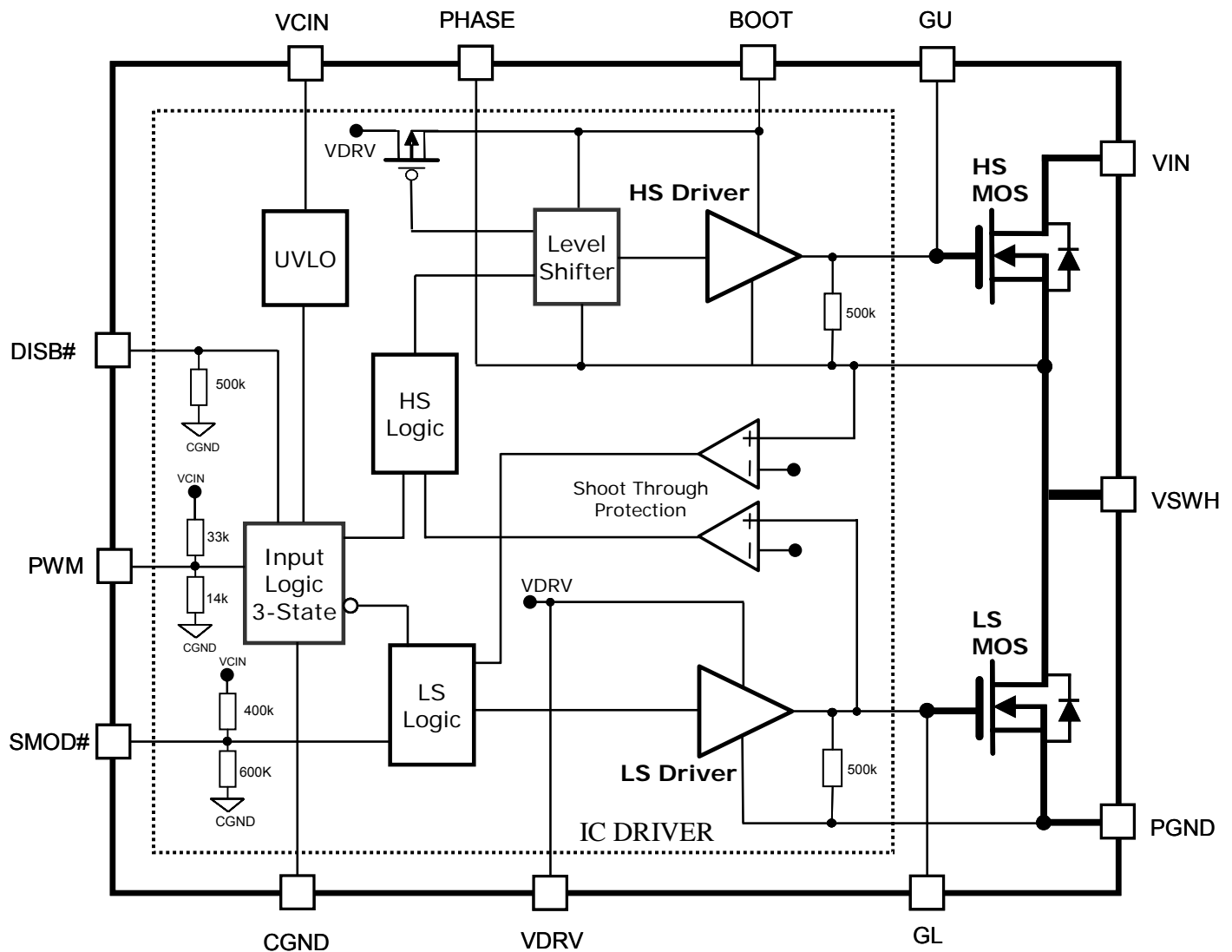


Figure 2. Simplified block diagram

Electrical Specification Table

Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Rating | Units |
|----------------------------------|------------------------------|--------------|-------|
| Frequency | f_{sw} | 1.2 | MHz |
| Average output current | I_{out} | 35 | A |
| Input voltage | VIN (DC) | -0.3 to +30 | V |
| Supply voltage | VCIN (DC) | -0.3 to +5.5 | V |
| High and Low side driver voltage | VDRV (DC) | -0.3 to +5.5 | V |
| Switch node voltage | VSWH (DC) | -1 to +30 | V |
| BOOT voltage | V _{BOOT-PHASE} (DC) | -1 to +5.5 | V |
| SMOD# voltage | V _{SMOD#} (DC) | -0.3 to +5.5 | V |
| DISB# voltage ¹ | VDISB | -0.3 to +5.5 | V |
| PWM voltage ¹ | V _{pwm} | -0.3 to +5.5 | V |
| Operating junction temperature | Tj-opr | -40 to +150 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

Note: All rated voltages are relative to voltages on the CGND and PGND pins unless otherwise specified.

¹ Latch Up class II- Level B (Jedec 78). Please refer to Quality Report for details.

Thermal Characteristics

| Parameter | Symbol | Values | | | Unit |
|---|-----------------|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| Thermal resistance, junction-soldering point ¹ | θ_{JS} | | 5 | | K/W |
| Thermal resistance, junction-top of package | θ_{Jtop} | | 20 | | |

¹ junction-soldering point is referred to the VSWH bottom exposed pad.

Recommended Operating Conditions and Electrical Characteristics (VCIN = 5V, Ta = 25°C)

| Parameter | | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---------------------------|--------------------------|-----|-----|------|-------|--|
| Input Voltage | | V _{IN} | 5 | | 25 | V | |
| Driving Voltage | | V _{DRV} | | 5 | | | |
| Bias Supply Voltage | | V _{CIN} | 4.5 | 5 | 5.5 | | |
| UVLO Rising | | V _{UVLO_R} | 2.9 | 3.5 | 3.9 | | VCIN rising |
| UVLO Falling | | V _{UVLO_F} | 2.5 | 3.1 | 3.3 | | VCIN falling |
| Driver Current | | I _{VDRV_300kHz} | | 10 | | mA | DISB# = 5V, f _{sw} = 300kHz |
| | | I _{VDRV_PWML} | | 25 | | μA | DISB# = 5V, PWM = 0V |
| IC Current (Control) | | I _{VCIN_PWML} | | 250 | | μA | DISB# = 5V, PWM = 0V SMOD# = Open |
| | | I _{VCIN_O} | | 370 | | μA | DISB# = 5V, PWM = Open SMOD# = Open |
| IC quiescent | | I _{CIN+IDRV} | | | 270 | μA | DISB# = 0V |
| Logic Inputs and Thresholds | | | | | | | |
| DISB# | Input low | V _{DISB_L} | 0.7 | 1.1 | 1.3 | V | V _{DISB} falling |
| | Input high | V _{DISB_H} | 1.9 | 2.1 | 2.4 | | V _{DISB} rising |
| | Sink Current | I _{DISB} | | 2 | | μA | V _{DISB} = 1V |
| SMOD# | Input low | V _{SMOD#_L} | 0.7 | 1.1 | 1.3 | V | V _{SMOD#} falling |
| | Input high | V _{SMOD#_H} | 1.9 | 2.1 | 2.4 | | V _{SMOD#} rising |
| | Open Voltage | V _{SMOD#_O} | | 3.0 | | | |
| | Sink Current | I _{SMOD#} | | -8 | | μA | V _{SMOD#} = 1V |
| PWM | Input low | V _{PWM_L} | | | 0.7 | V | V _{PWM} falling |
| | Input high | V _{PWM_H} | 2.4 | | | | V _{PWM} rising |
| | Input resistance | R _{IN-PWM} | 6.5 | 9.5 | 12.5 | kΩ | V _{PWM} = 1V |
| | Open Voltage | V _{PWM_O} | | 1.5 | | V | V _{PWM_O} |
| | Tri-state Shutdown Window | V _{PWM_S} | 1.2 | | 1.9 | | |
| Dynamic Characteristic | | | | | | | |
| Three State to GL/GH rising propagation delay | | T _{pts} | | 15 | | ns | GH, GL unloaded. |
| GL/GH Three State Shutdown Hold-Off time, | | T _{tsshd} | | 240 | | | |
| GH Turn-on propagation delay | | T _{pdhu} | | 15 | | | |
| GH Turn-off propagation delay | | T _{pdlu} | | 20 | | | |
| GL Turn-on propagation delay | | T _{pdhl} | | 20 | | | |
| GL Turn-off propagation delay | | T _{pdll} | | 10 | | | |
| DISB#Turn-off propogation delay falling | | T _{pdl_DISB} | | 20 | | | |
| DISB#Turn-on propogation delay rising | | T _{pdh_DISB} | | 20 | | | |

¹ Unless otherwise specified, VCIN=VDRV

Typical Application

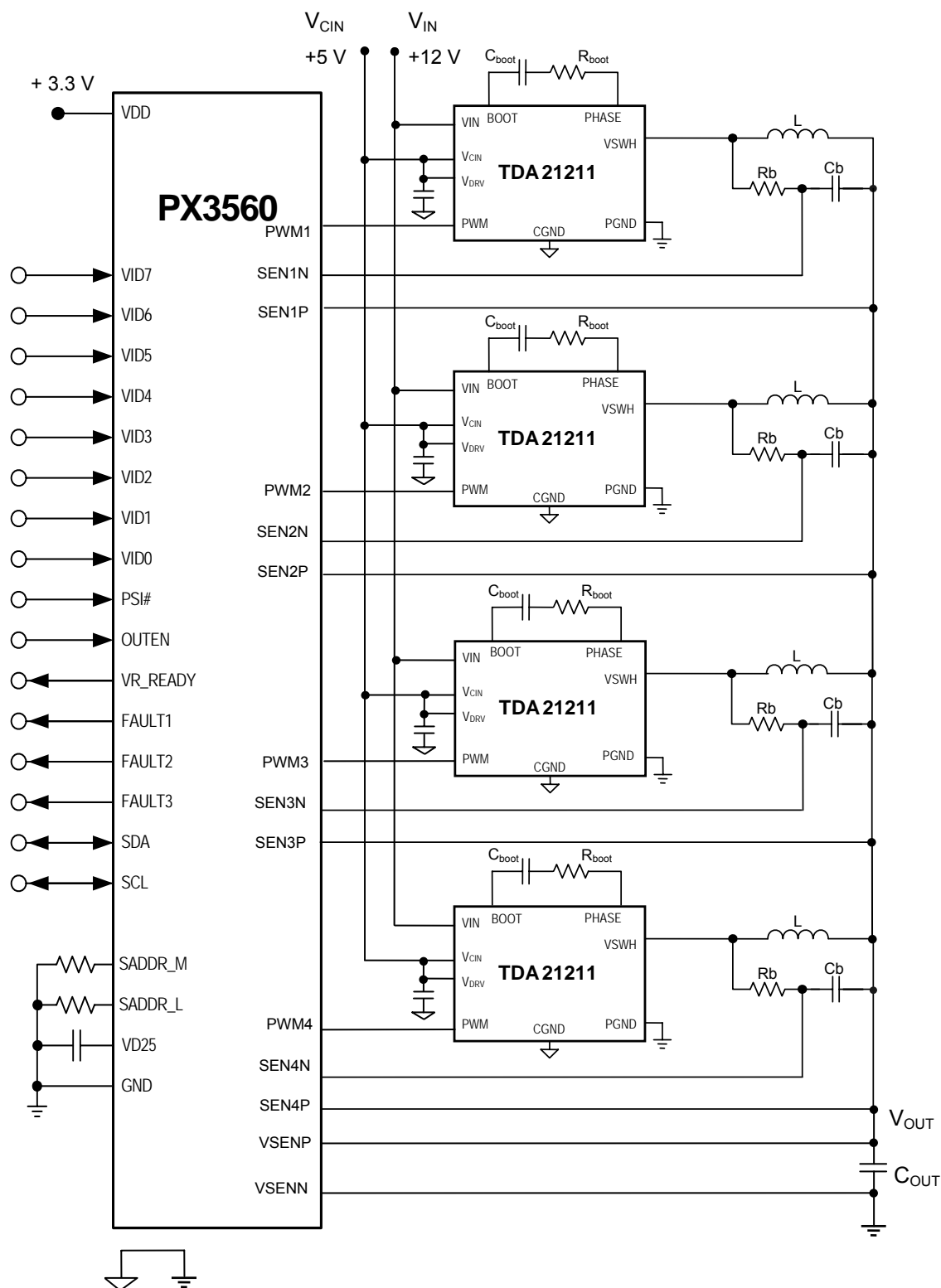


Figure 3. Four Phases Voltage Regulator Typical Application (Simplified Schematic)

Theory of Operation

The TDA21211 incorporates a high performance gate driver, one high side power MOSFET and one low-side power MOSFET in a single 40 lead QFN package. The advantages of this arrangement are found in the areas of increased performance, increased efficiency and lower overall package and layout inductance. This module is ideal for use in Synchronous Buck Regulators either as a stand-alone power stage that can deliver up to 35A or with an interleaved approach for higher current loads.

The power MOSFETs are tailored for this device. The gate driver is an extremely robust high-performance driver rated at the switching node for DC voltages ranging from -1V to +30V. The closely coupled driver and MOSFETs enable efficiency improvements that are hard to match using discrete components. The power density for transmitted power of this approach is approximately 30W within a 36mm² area.

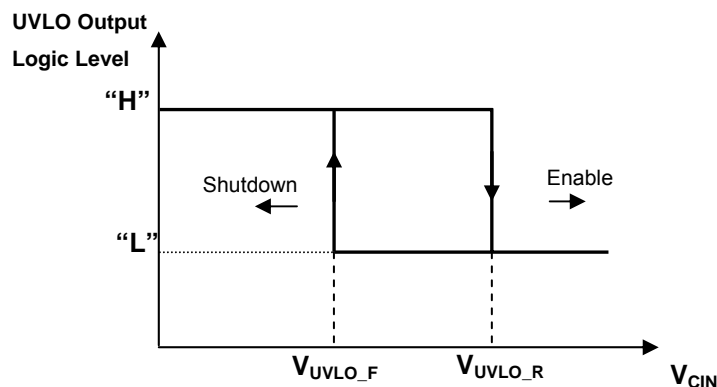
Driver Characteristics

The gate driver of the TDA21211 has 2 voltage inputs, VCIN and VDRV. VCIN is the 5V bias supply for the driver. VDRV is also 5V and is used to drive the High and Low Side MOSFETs. Ceramic capacitors should be placed very close to these input voltage pins to decouple the sensitive control circuitry from a noisy environment.

The MOSFETs selected for this application are optimized for 5V gate drive, thus giving the end user optimized high load as well as light load efficiency. The reference for the power circuitry including the driver output stage is PGND and the reference for the gate driver control circuit (VCIN) is CGND.

Referring to the Block Diagram, Figure 2 VCIN is internally connected to the UVLO circuit and for VCIN voltages less than required for proper circuit operation will provide shut-down. VDRV supplies both, the floating high side drive and the low-side drive circuits. An active boot circuit for the high side gate drive is also included. A second UVLO circuitry, sensing the BOOT voltage level, is implemented to prevent false GH turn on during insufficient power supply level condition (BOOT Cap charging/discharging sequence). During undervoltage both GH and GL are driven low actively; further passive pull down (500k Ohm) is placed on each gate.

Note: output signal from UVLO unit.



Inputs to the internal control circuit are **PWM**, **DISB#** and **SMOD#**:

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3V and 5V logic. The PWM input has three-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time T_{tsshd} , the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is internally fixed to $V_{PWM_O} = 1.5\text{ V}$ level

| PWM | Driver Output |
|------|---------------|
| L | GL=H, GH = L |
| H | GL=L, GH = H |
| Open | GL=L, GH = L |

The **DISB#** is an active low signal. When DISB# is pulled low, the power stage is disabled.

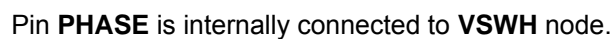
| DISB# | Driver Output |
|-------|----------------------------|
| L | Shutdown → GL, GH = L |
| H | Enable → GL, GH = "Active" |
| Open | Shutdown → GL, GH = L |

The **SMOD#** feature is provided to disable the low-side MOSFET during active operation. When synchronized with the PWM signal (as shown in Figure 7), SMOD# is intended to improve light load efficiency by saving the gate charge loss of the low-side MOSFET. Once left open, the pin is internally fixed to $V_{SMOD\#_O} = 3\text{ V}$ level.

| SMOD# | GL Status |
|-------|-----------------------|
| L | L |
| H | Enable → GL= "Active" |
| Open | Enable → GL= "Active" |

The TDA21211 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both HS and LS MOSFETs being on at the same time, the adaptive control circuitry monitors the voltage at the "VSWH" pin. When the PWM signal goes low, HS, the High-side MOSFET will begin to turn off, after the propagation delay (T_{pdlu}). Once the "VSWH" pin falls below 1V, LS, the Low-side MOSFET is gated on after the predefined delay time, (T_{pdhl}). Additionally, the gate to source voltage of the HS-MOSFET is also monitored. When $V_{GS}(HS)$ is discharged below 1V, a threshold known to turn HS off, a secondary delay is initiated, (T_{pdhl}), which results in LS being gated "ON" irregardless of the state of the "VSWH" pin. This way it will be ensured that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See Figure 5 for more detail.

GH and GL are monitoring pins to check the internal gate drive signals.



Gate Driver Timing Diagrams

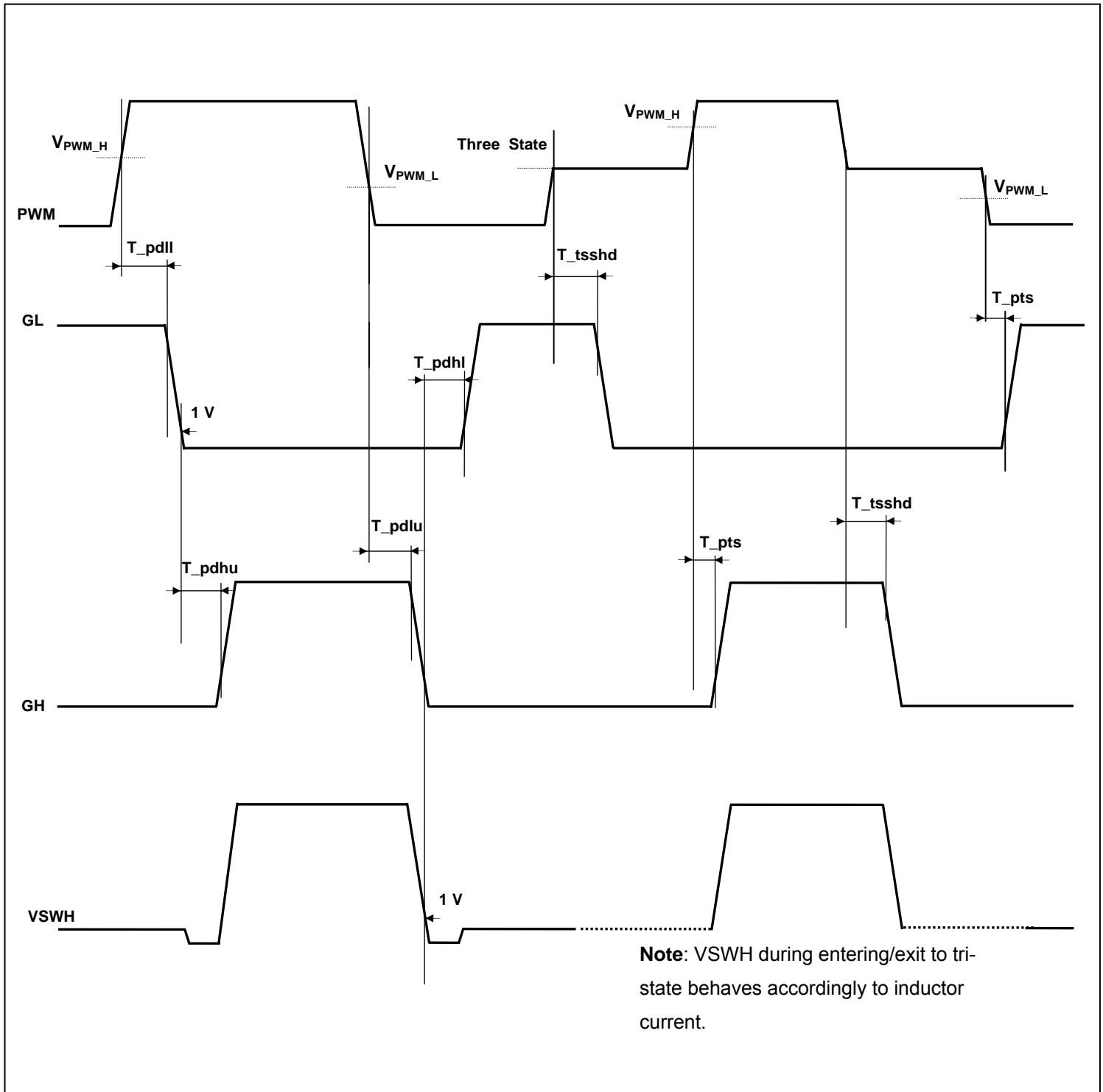


Figure 5: Adaptive Gate Driver Timing Diagram

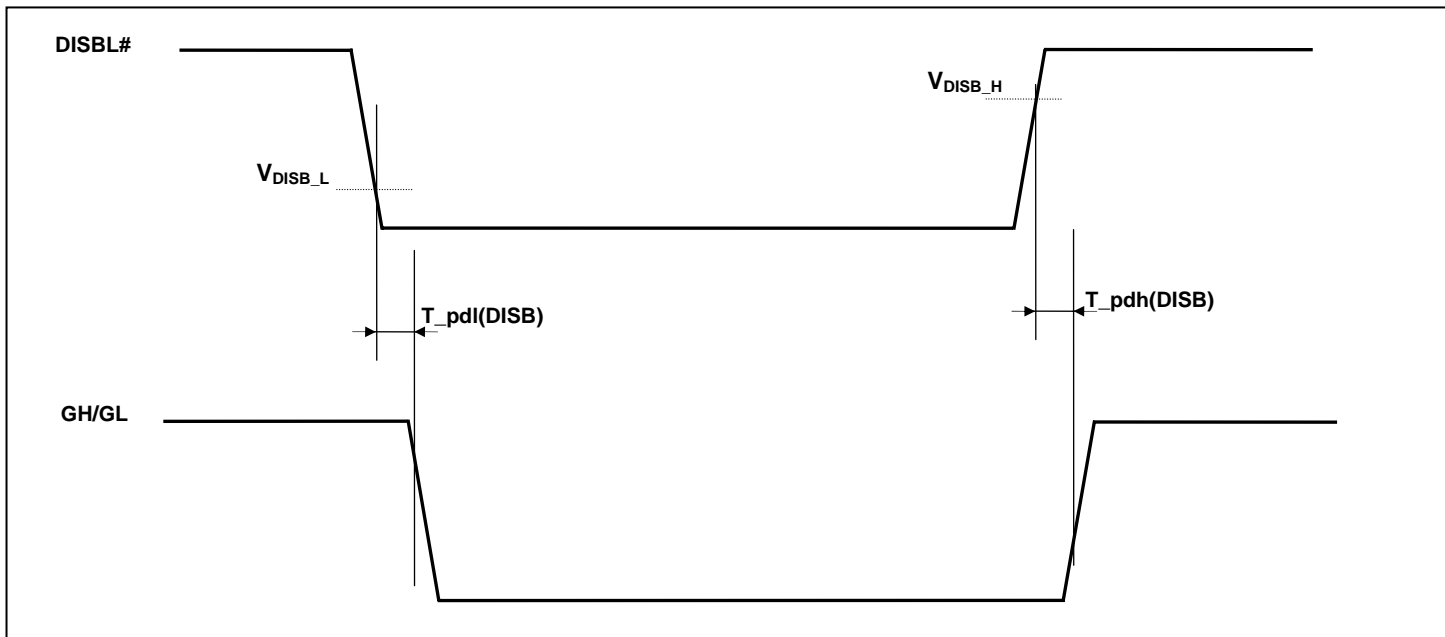


Figure 6: Disable Timing Diagram

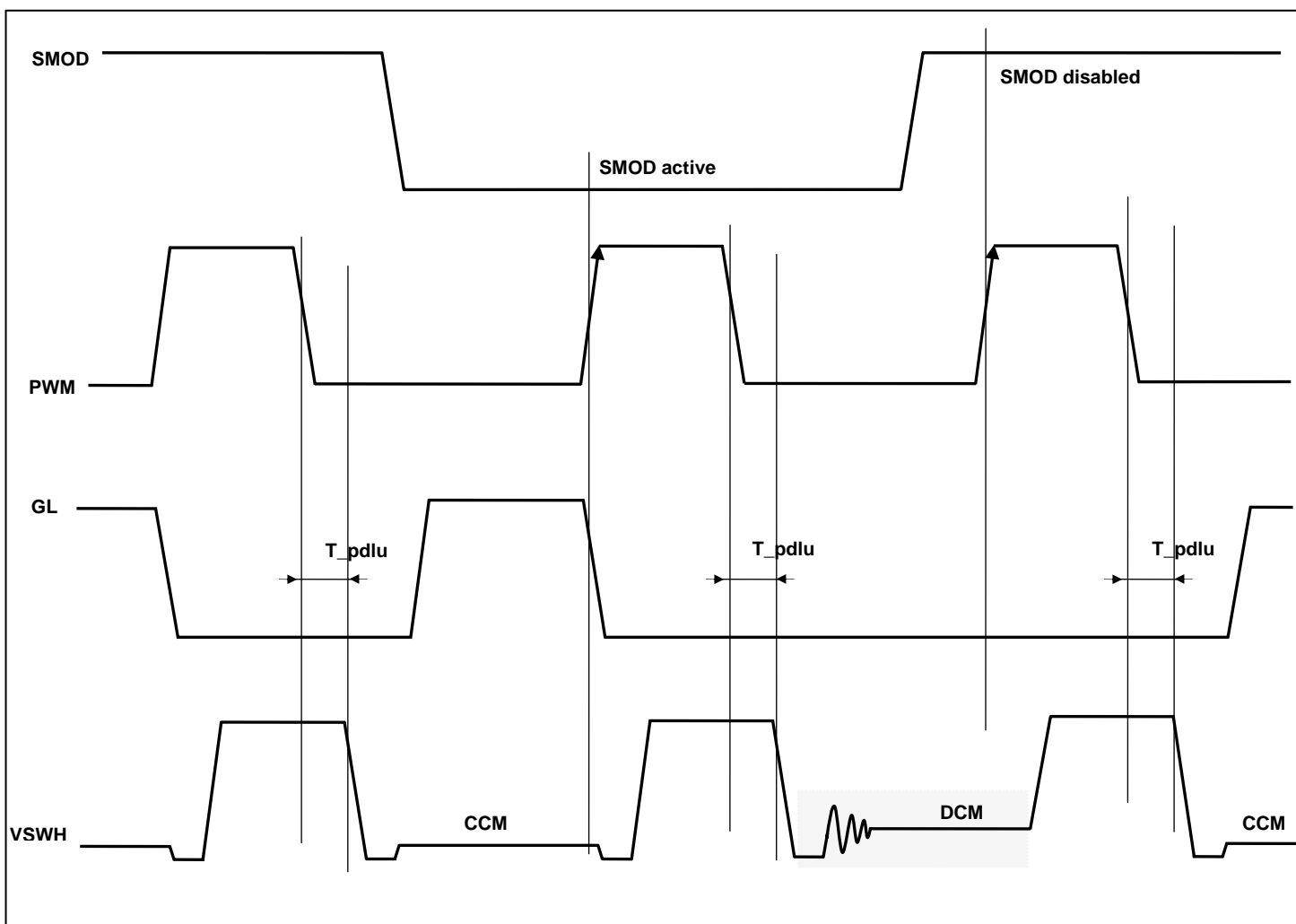


Figure 7 SMOD# Timing Diagram

Test Circuit

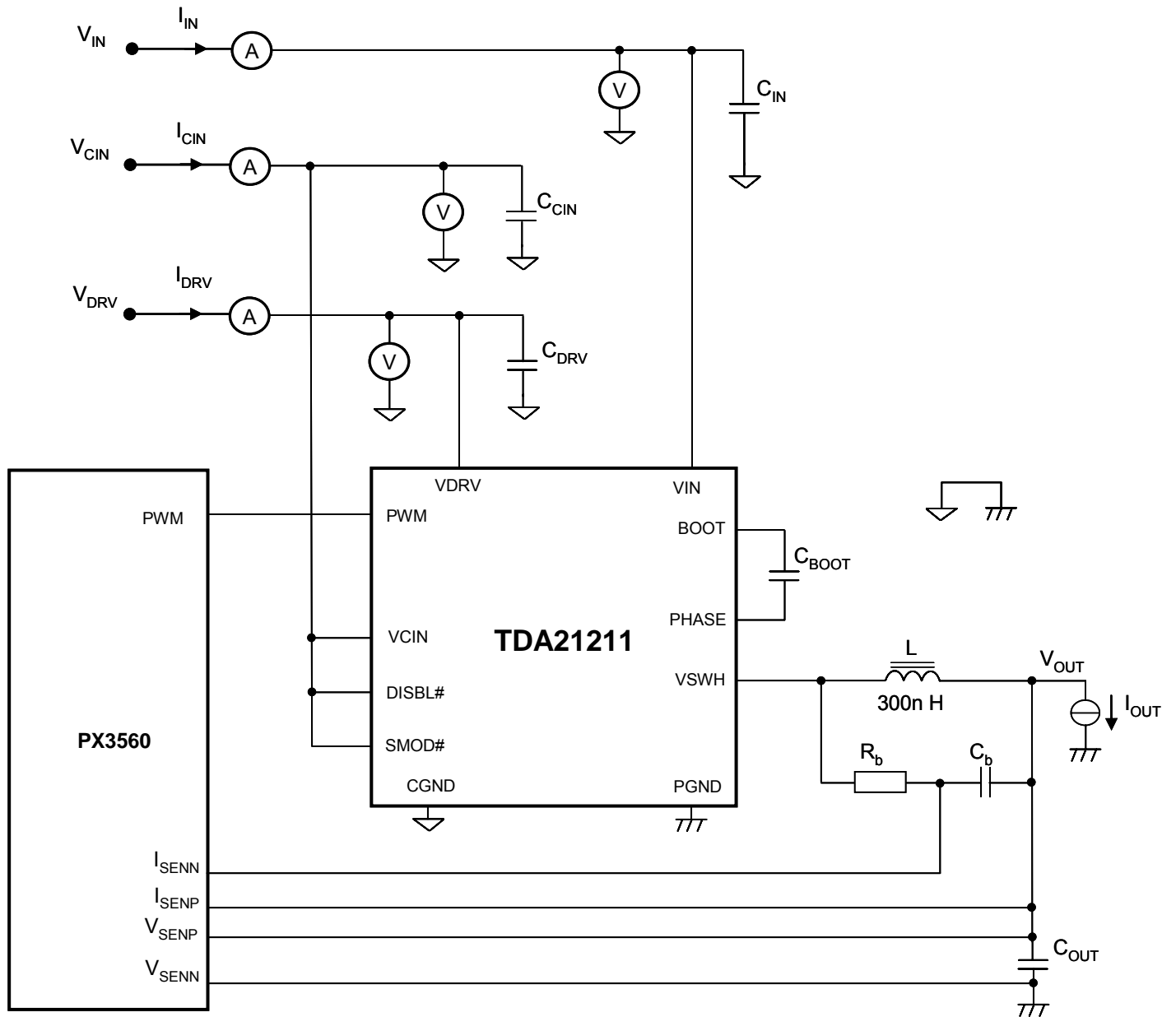


Figure 8. Test Circuit

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}}$$

$$P_{IN} = V_{DRV} \times I_{DRV} + V_{CIN} \times I_{CIN} + V_{IN} \times I_{IN}$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

$$P_{LOSS} = P_{IN} - P_{OUT}$$

Performance Curves – Typical Data

Operating conditions (unless otherwise specified): $V_{IN}= +12V$, $V_{CIN}=V_{DRV}= +5V$, $V_{OUT}=1.1 V$, $F=362k Hz$, 300nH inductor (VITEC-59P9081N01, DCR (typ) =0.43m Ω) $T_A=25^{\circ} C$, load line=0m Ω , airflow=100 LFM, no heatsink. Power Efficiency and Power Loss data reported herein includes TDA21211 and inductor losses but no other system losses (unless otherwise specified).

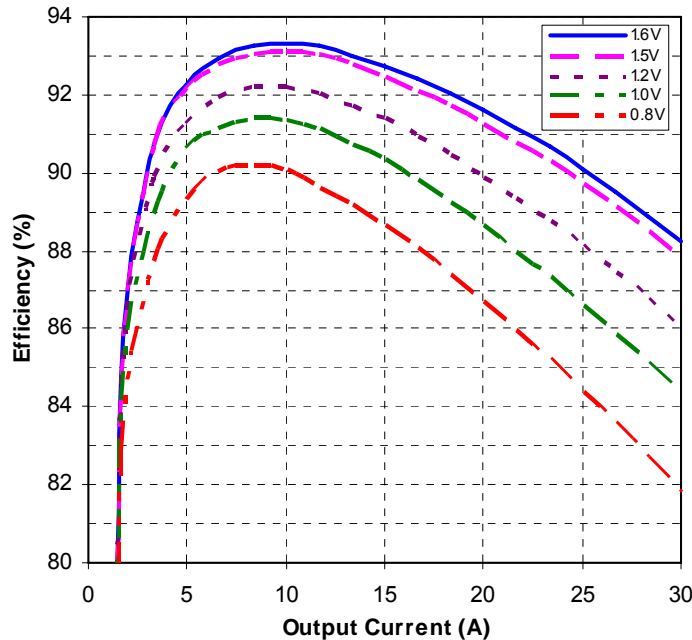


Figure 9. Efficiency vs. VOUT

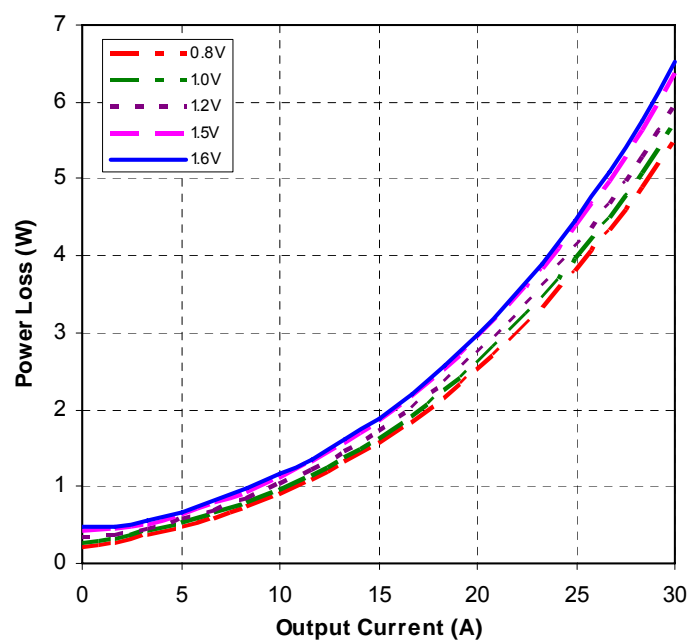


Figure 10. Power Loss vs. VOUT

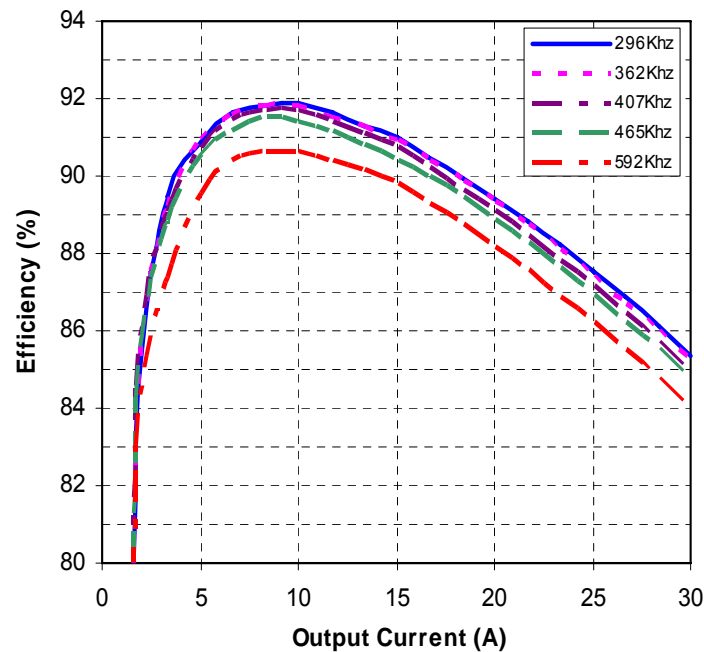


Figure 11. Efficiency vs. Switching Frequency

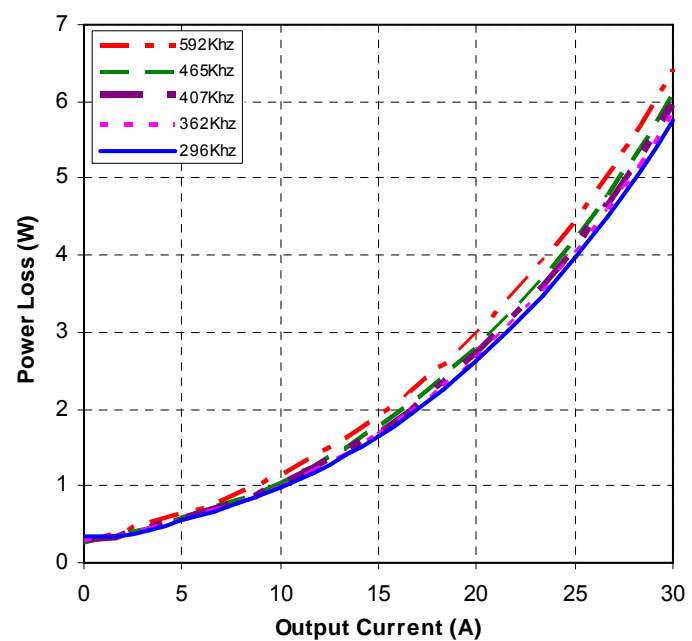


Figure 12. Power Loss vs. Switching Frequency

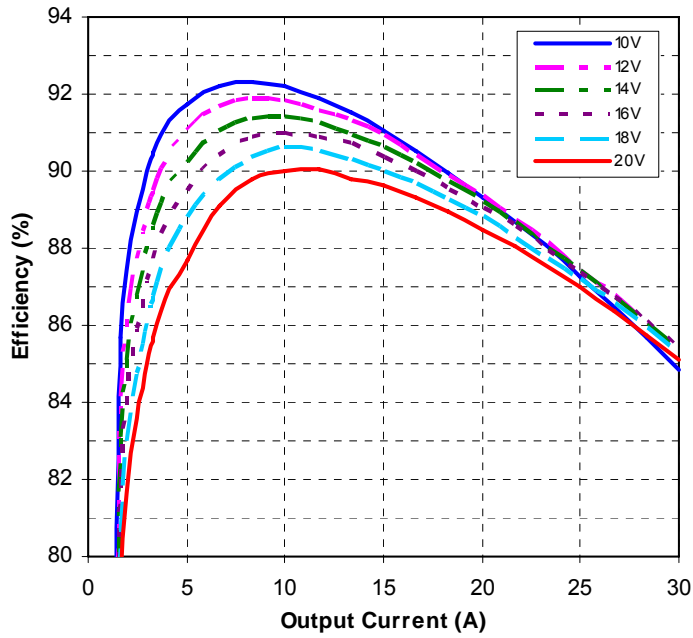


Figure 13. Efficiency vs. VIN

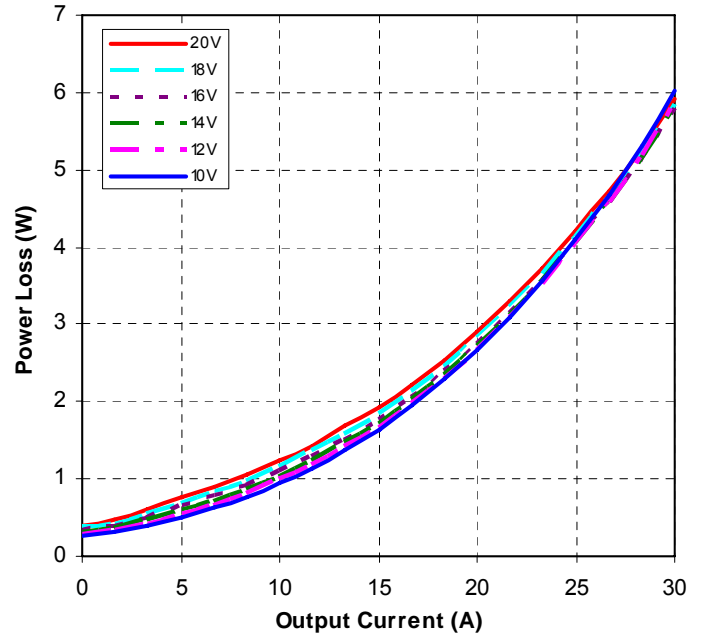


Figure 14. Power Loss vs. VIN

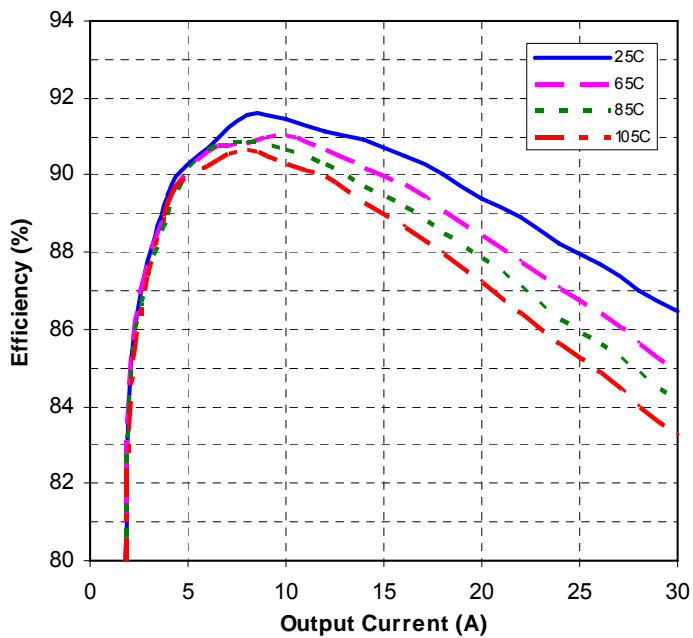


Figure 15. Efficiency vs. T_{CASE}

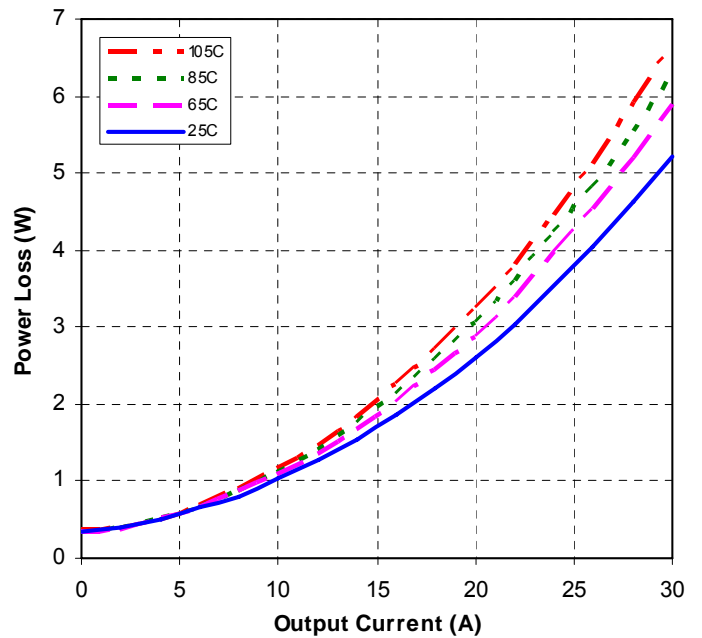


Figure 16. Power Loss vs. T_{CASE}

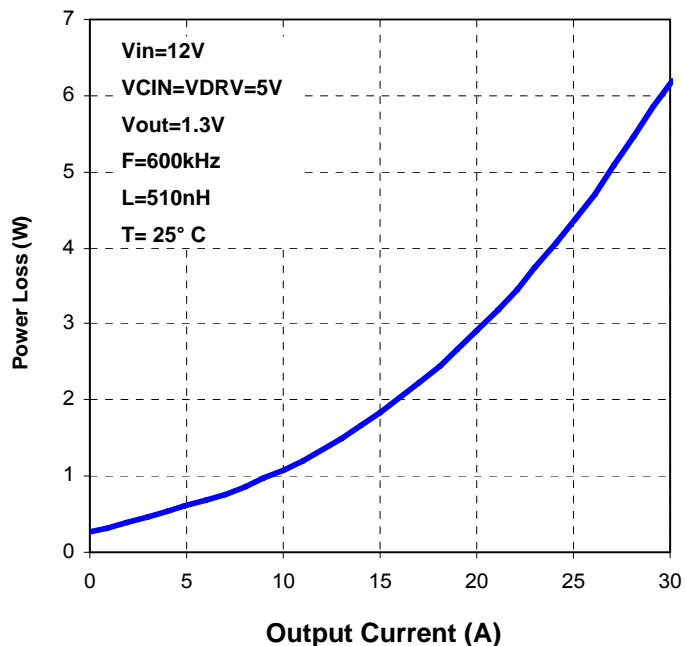


Figure 17. Power Loss vs. I_{out}
 (inductor losses not included)

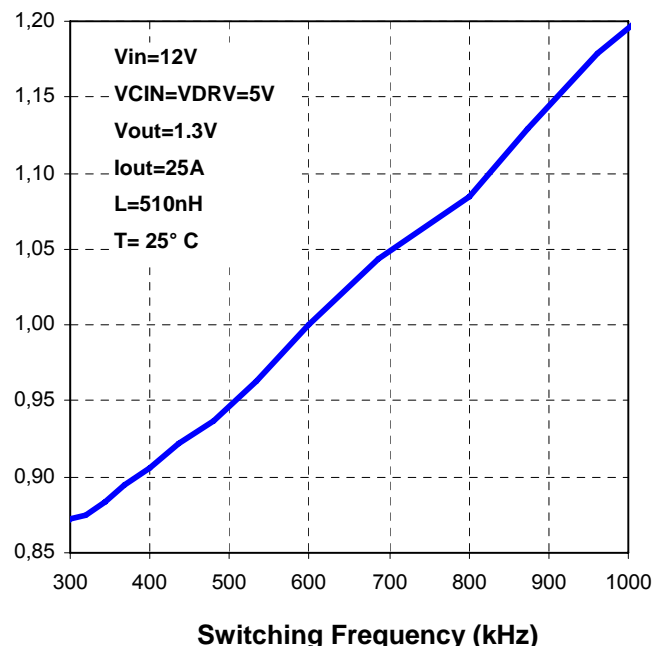


Figure 18. Normalized Power Loss @ $I_{out}=25$ A
 (inductor losses not included)

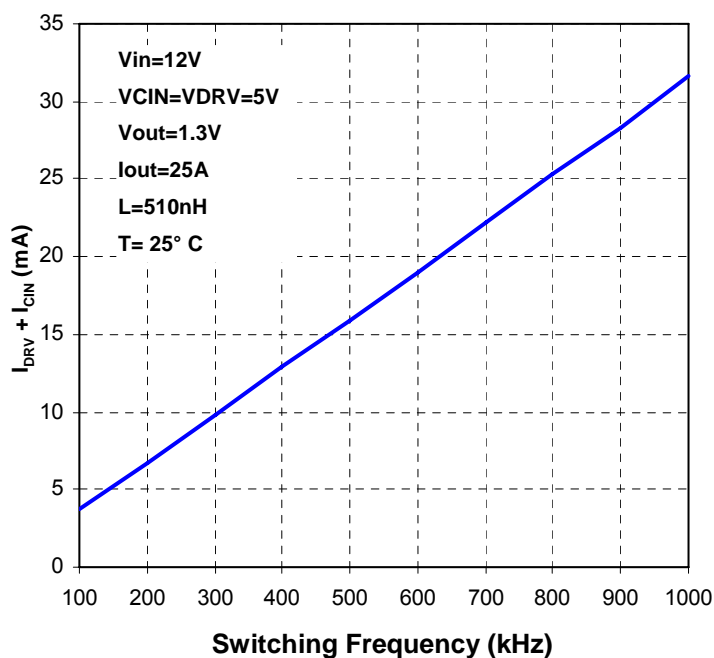
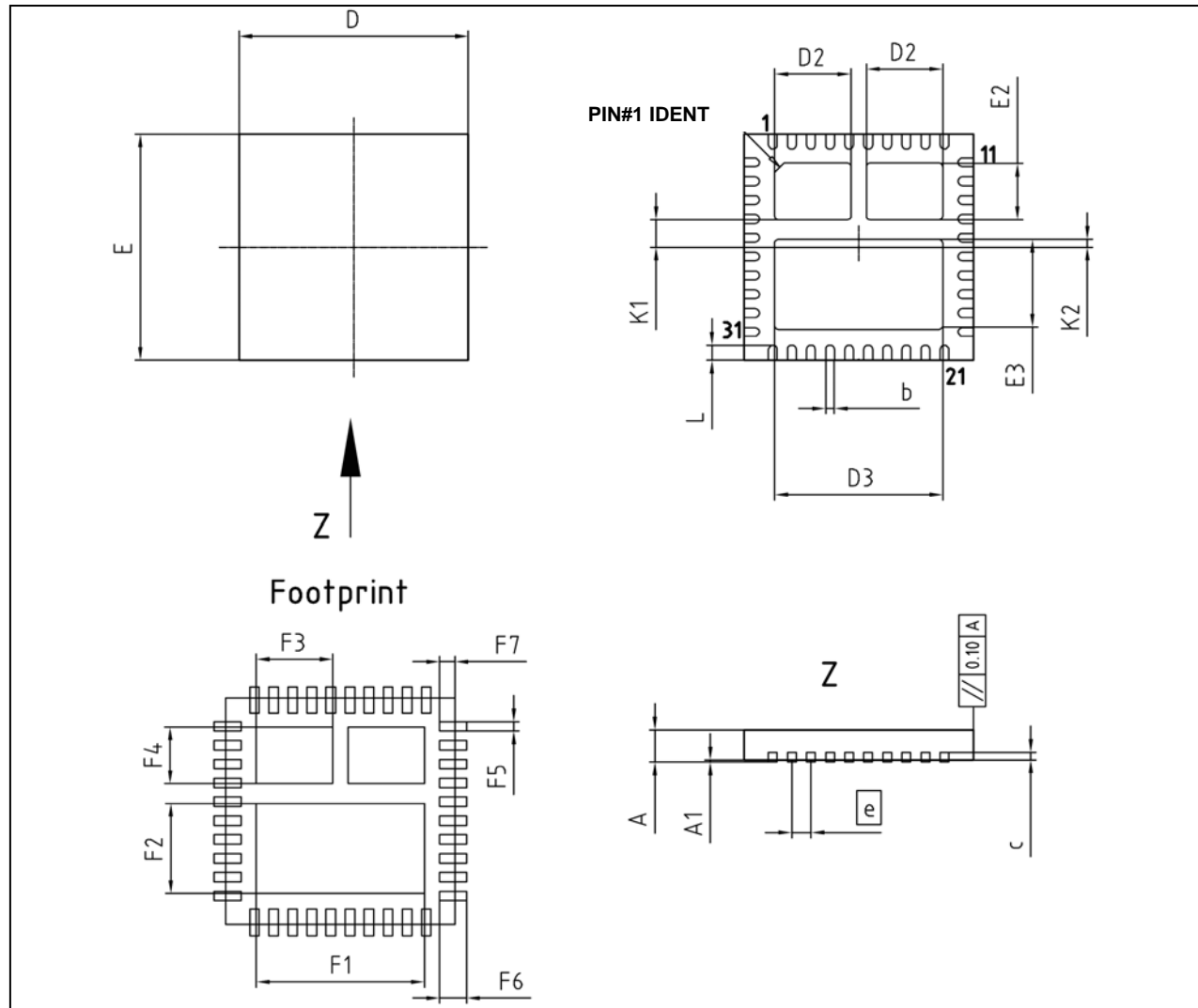


Figure 19. Power Supply Current ($I_{DRV} + I_{CIN}$) vs. F_{sw}

Package Outline



| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.75 | 0.85 | 0.030 | 0.033 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| b | 0.18 | 0.28 | 0.007 | 0.011 |
| c | 0.10 | 0.30 | 0.004 | 0.012 |
| D | 5.90 | 6.10 | 0.232 | 0.240 |
| D2 | 1.90 | 2.10 | 0.075 | 0.083 |
| D3 | 4.30 | 4.50 | 0.169 | 0.177 |
| E | 5.90 | 6.10 | 0.232 | 0.240 |
| E2 | 1.40 | 1.60 | 0.055 | 0.063 |
| E3 | 2.30 | 2.50 | 0.091 | 0.098 |
| e | 0.50 | | 0.020 | |
| N | 40 | | 40 | |
| L | 0.30 | 0.50 | 0.012 | 0.020 |
| K1 | 0.63 | 0.83 | 0.025 | 0.033 |
| K2 | 0.11 | 0.31 | 0.004 | 0.012 |
| F1 | 4.40 | | 0.173 | |
| F2 | 2.40 | | 0.094 | |
| F3 | 2.00 | | 0.079 | |
| F4 | 1.50 | | 0.059 | |
| F5 | 0.25 | | 0.010 | |
| F6 | 0.70 | | 0.028 | |
| F7 | 0.40 | | 0.016 | |

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SCALE

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02

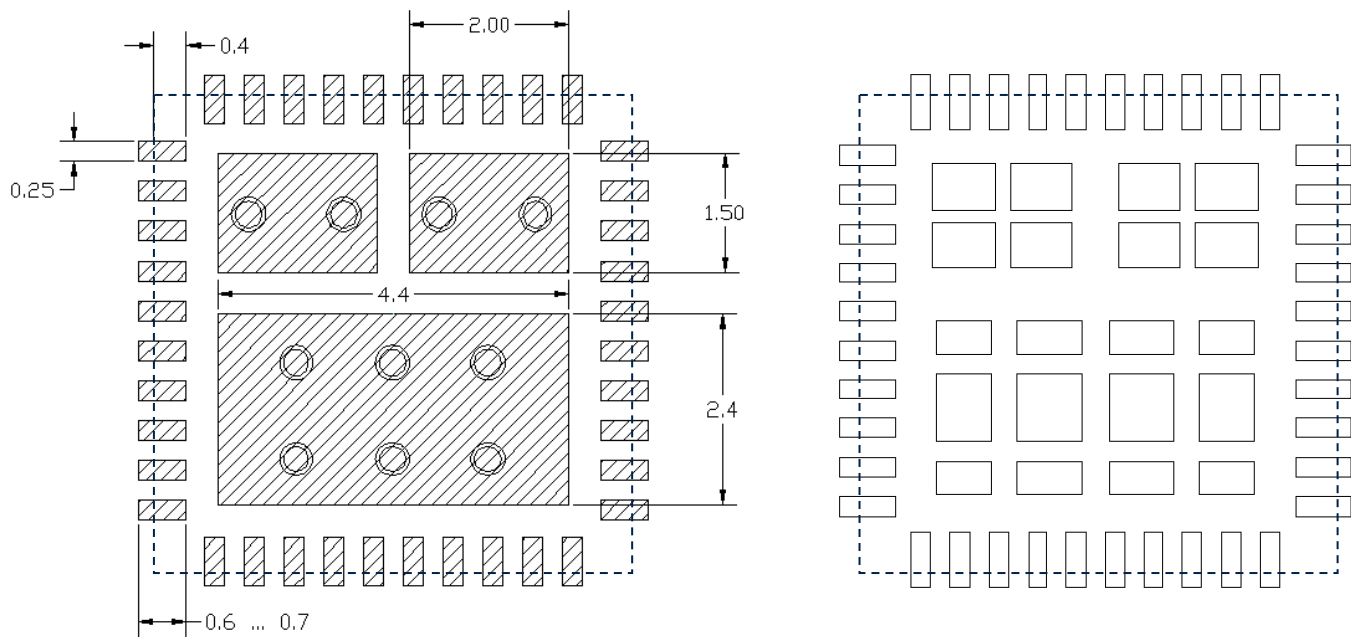


Figure 20: Footprint and Solder Stencil Recommendation

PCB Layout Example.

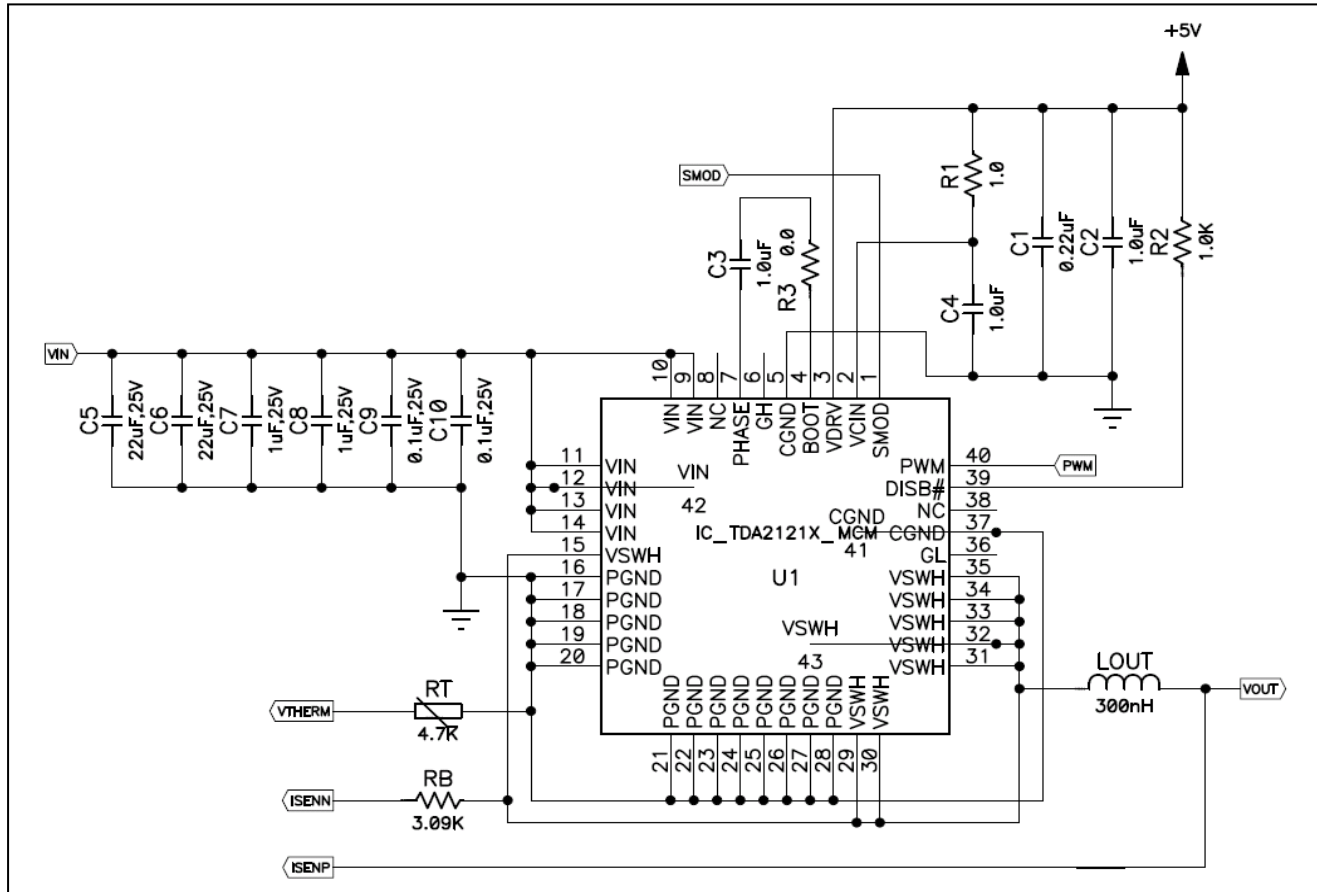


Figure 21 Single Phase DrMOS typical Application Circuit

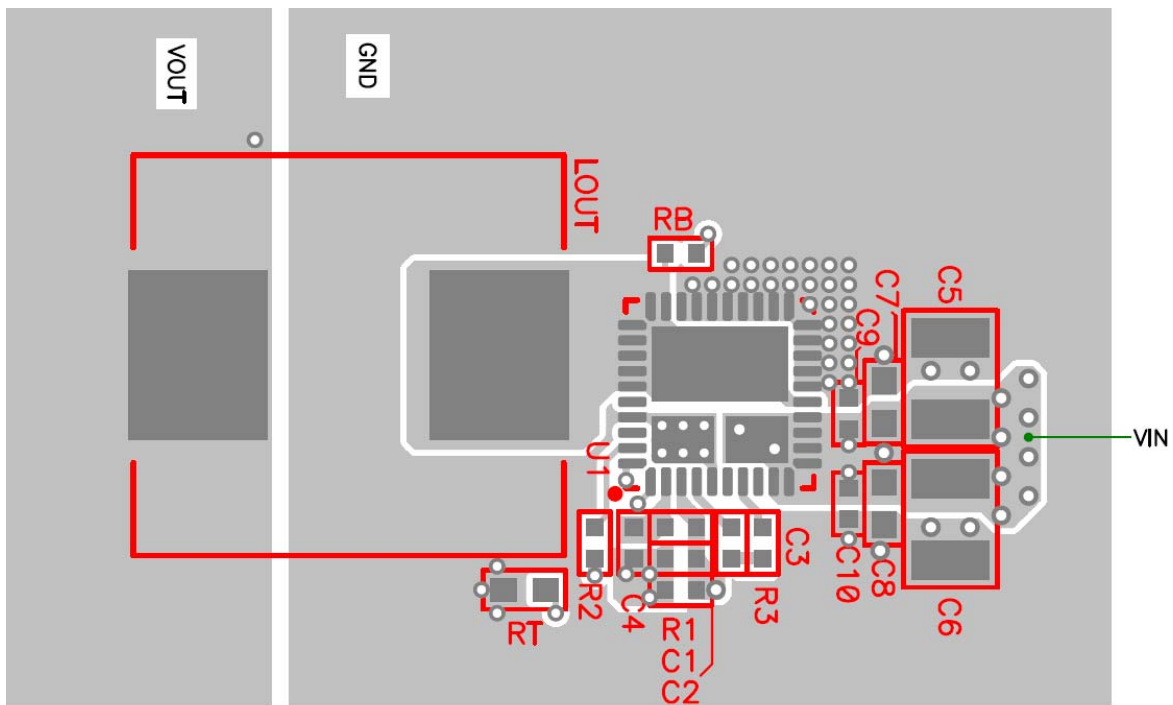


Figure 22 Single Phase DrMOS PCB Layout Example (Top Side View)
(for DrMOS Design support a customer PCB layout guide is available upon request)

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