

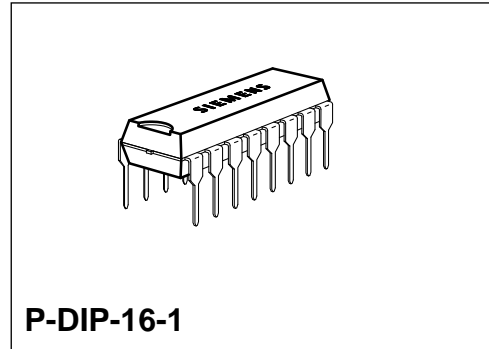
## Phase Control IC

**TCA 785**

**Bipolar IC**

### Features

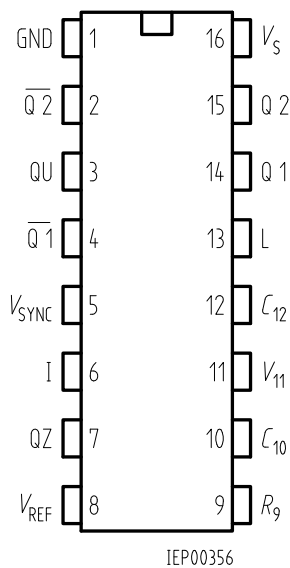
- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Wide temperature range



Type	Ordering Code	Package
TCA 785	Q67000-A2321	P-DIP-16-1

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0 ° and 180 °. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D.



### Pin Configuration (top view)

### Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	$\overline{Q2}$	Output 2 inverted
3	$\overline{Q U}$	Output U
4	$\overline{Q2}$	Output 1 inverted
5	$V_{SYNC}$	Synchronous voltage
6	I	Inhibit
7	Q Z	Output Z
8	$V_{REF}$	Stabilized voltage
9	$R_9$	Ramp resistance
10	$C_{10}$	Ramp capacitance
11	$V_{11}$	Control voltage
12	$C_{12}$	Pulse extension
13	L	Long pulse
14	Q 1	Output 1
15	Q 2	Output 2
16	$V_s$	Supply voltage

## Functional Description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage  $V_S$ ). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator, the capacitor  $C_{10}$  of which is charged by a constant current (determined by  $R_9$ ). If the ramp voltage  $V_{10}$  exceeds the control voltage  $V_{11}$  (triggering angle  $\varphi$ ), a signal is processed to the logic. Dependent on the magnitude of the control voltage  $V_{11}$ , the triggering angle  $\varphi$  can be shifted within a phase angle of  $0^\circ$  to  $180^\circ$ .

For every half wave, a positive pulse of approx.  $30 \mu s$  duration appears at the outputs Q 1 and Q 2. The pulse duration can be prolonged up to  $180^\circ$  via a capacitor  $C_{12}$ . If pin 12 is connected to ground, pulses with a duration between  $\varphi$  and  $180^\circ$  will result.

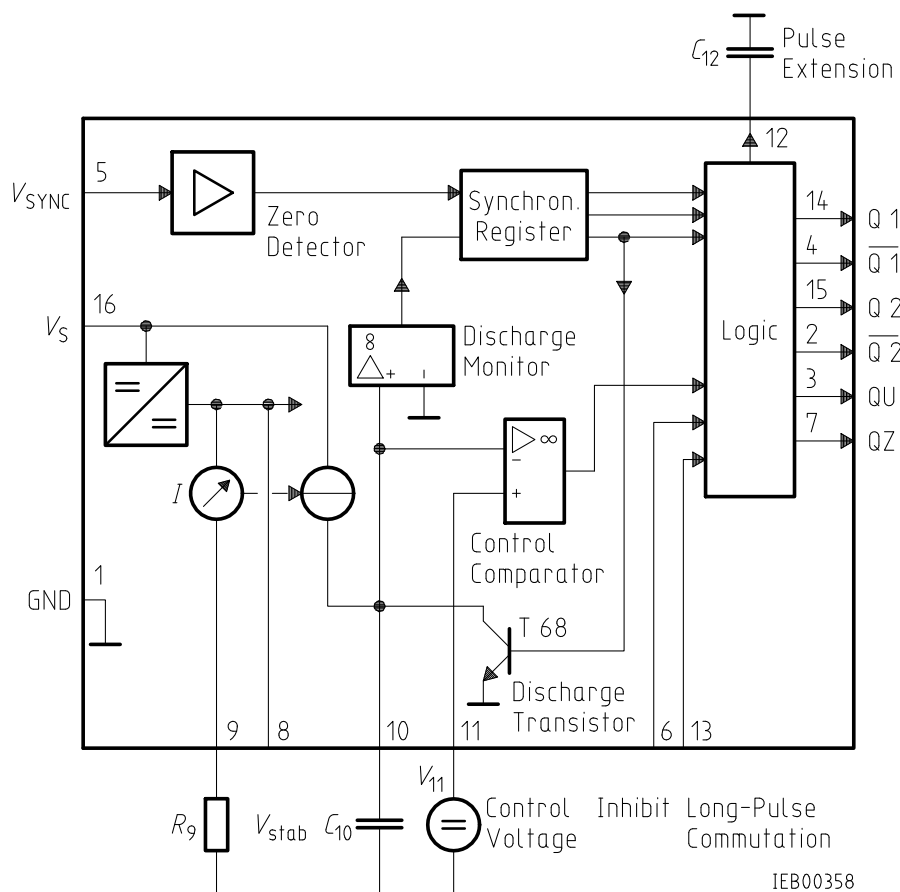
Outputs  $\overline{Q1}$  and  $\overline{Q2}$  supply the inverse signals of Q 1 and Q 2.

A signal of  $\varphi + 180^\circ$  which can be used for controlling an external logic, is available at pin 3.

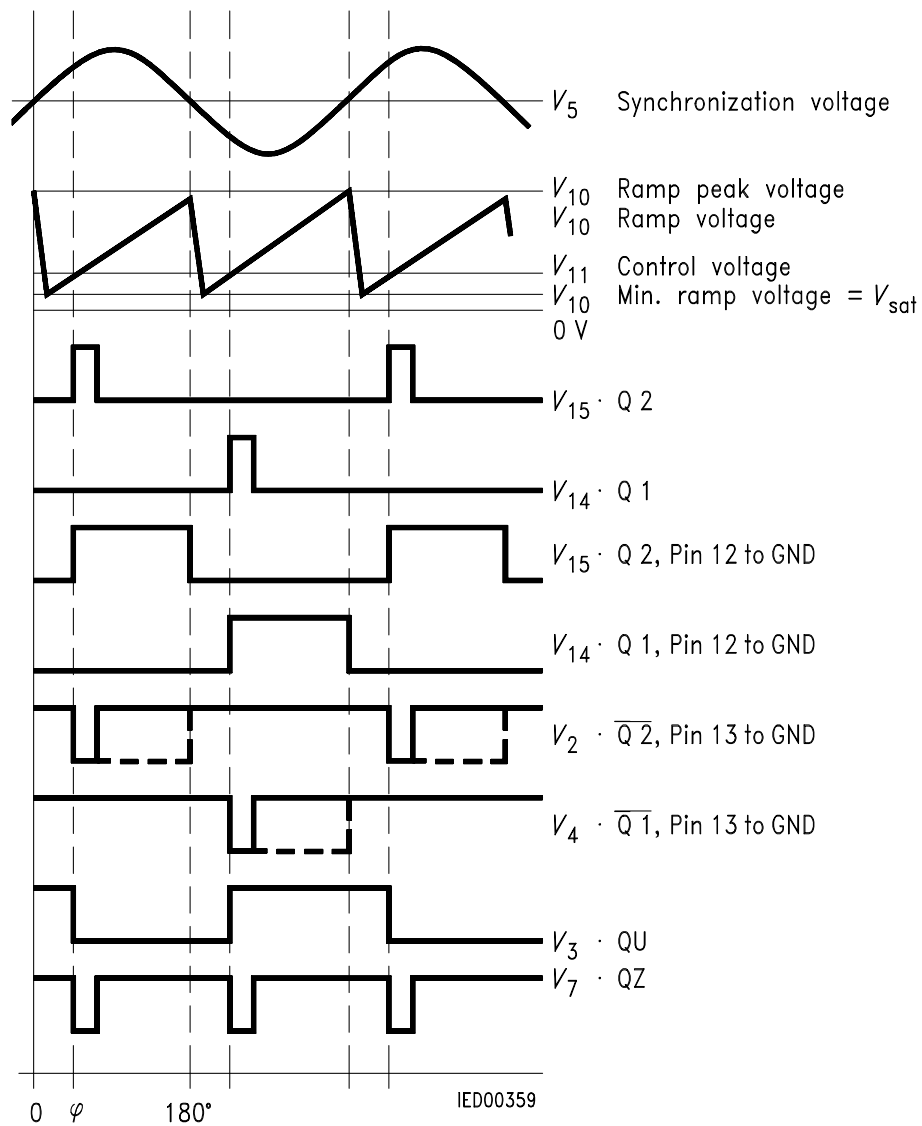
A signal which corresponds to the NOR link of Q 1 and Q 2 is available at output Q Z (pin 7).

The inhibit input can be used to disable outputs Q1, Q2 and  $\overline{Q1}$ ,  $\overline{Q2}$ .

Pin 13 can be used to extend the outputs  $\overline{Q1}$  and  $\overline{Q2}$  to full pulse length ( $180^\circ - \varphi$ ).



## Block Diagram



Pulse Diagram

## Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_S$	– 0.5	18	V
Output current at pin 14, 15	$I_Q$	– 10	400	mA
Inhibit voltage	$V_6$	– 0.5	$V_S$	V
Control voltage	$V_{11}$	– 0.5	$V_S$	V
Voltage short-pulse circuit	$V_{13}$	– 0.5	$V_S$	V
Synchronization input current	$V_5$	– 200	± 200	μA
Output voltage at pin 14, 15	$V_Q$		$V_S$	V
Output current at pin 2, 3, 4, 7	$I_Q$		10	mA
Output voltage at pin 2, 3, 4, 7	$V_Q$		$V_S$	V
Junction temperature	$T_j$		150	°C
Storage temperature	$T_{stg}$	– 55	125	°C
Thermal resistance system - air	$R_{th SA}$		80	K/W

## Operating Range

Supply voltage	$V_S$	8	18	V
Operating frequency	$f$	10	500	Hz
Ambient temperature	$T_A$	– 25	85	°C

## Characteristics

$8 \leq V_S \leq 18 \text{ V}$ ;  $-25 \text{ °C} \leq T_A \leq 85 \text{ °C}$ ;  $f = 50 \text{ Hz}$

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Supply current consumption S1 ... S6 open $V_{11} = 0 \text{ V}$ $C_{10} = 47 \text{ nF}$ ; $R_9 = 100 \text{ k}\Omega$	$I_S$	4.5	6.5	10	mA	1
Synchronization pin 5 Input current	$I_{5 \text{ rms}}$	30		200	μA	1
Offset voltage	$\Delta V_5$		30	75	mV	4
Control input pin 11 Control voltage range	$V_{11}$	0.2		$V_{10 \text{ peak}}$	V	1
Input resistance	$R_{11}$		15		kΩ	5

## Characteristics (cont'd)

$8 \leq V_S \leq 18 \text{ V}$ ;  $-25 \text{ }^\circ\text{C} \leq T_A \leq 85 \text{ }^\circ\text{C}$ ;  $f = 50 \text{ Hz}$

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Ramp generator						
Charge current	$I_{10}$	10		1000	$\mu\text{A}$	
Max. ramp voltage	$V_{10}$			$V_2 - 2$	V	1
Saturation voltage at capacitor	$V_{10}$	100	225	350	mV	1.6
Ramp resistance	$R_9$	3		300	$\text{k}\Omega$	1
Sawtooth return time	$t_f$		80		$\mu\text{s}$	1
Inhibit pin 6						
switch-over of pin 7						
Outputs disabled	$V_{6L}$		3.3	2.5	V	1
Outputs enabled	$V_{6H}$	4	3.3		V	1
Signal transition time	$t_r$	1		5	$\mu\text{s}$	1
Input current	$I_{6H}$		500	800	$\mu\text{A}$	1
$V_6 = 8 \text{ V}$						
Input current	$-I_{6L}$	80	150	200	$\mu\text{A}$	1
$V_6 = 1.7 \text{ V}$						
Deviation of $I_{10}$	$I_{10}$	-5		5	%	1
$R_9 = \text{const.}$						
$V_S = 12 \text{ V}$ ; $C_{10} = 47 \text{ nF}$						
Deviation of $I_{10}$	$I_{10}$	-20		20	%	1
$R_9 = \text{const.}$						
$V_S = 8 \text{ V to } 18 \text{ V}$						
Deviation of the ramp voltage between 2 following half-waves, $V_S = \text{const.}$	$\Delta V_{10 \text{ max}}$		$\pm 1$		%	
Long pulse switch-over pin 13						
switch-over of S8						
Short pulse at output	$V_{13H}$	3.5	2.5		V	1
Long pulse at output	$V_{13L}$		2.5	2	V	1
Input current	$I_{13H}$			10	$\mu\text{A}$	1
$V_{13} = 8 \text{ V}$						
Input current	$-I_{13L}$	45	65	100	$\mu\text{A}$	1
$V_{13} = 1.7 \text{ V}$						
Outputs pin 2, 3, 4, 7						
Reverse current	$I_{CEO}$			10	$\mu\text{A}$	2.6
$V_Q = V_S$						
Saturation voltage	$V_{\text{sat}}$	0.1	0.4	2	V	2.6
$I_Q = 2 \text{ mA}$						

## Characteristics (cont'd)

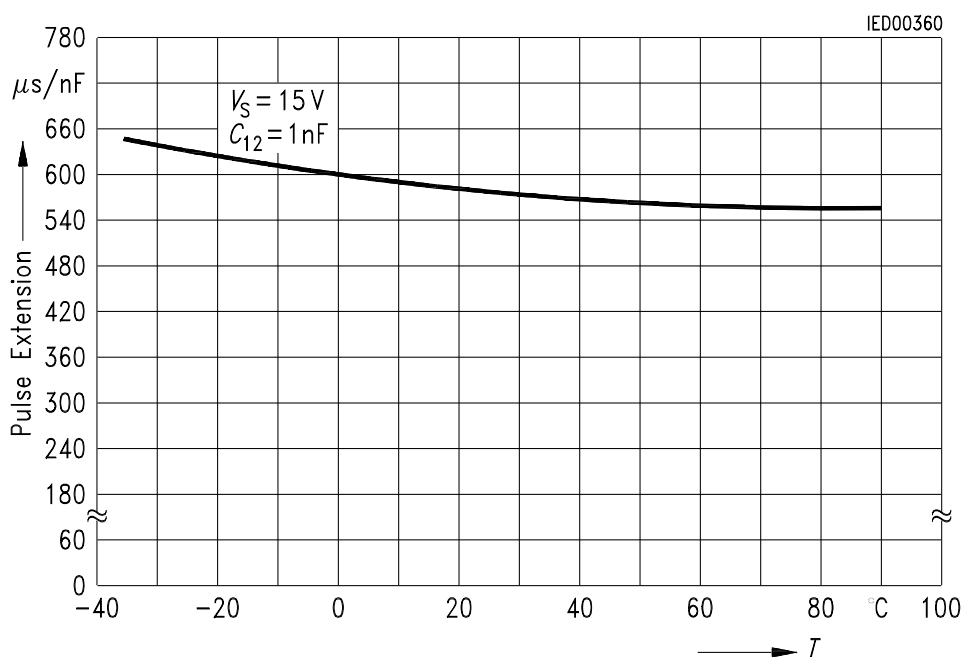
$8 \leq V_S \leq 18 \text{ V}$ ;  $-25 \text{ }^\circ\text{C} \leq T_A \leq 85 \text{ }^\circ\text{C}$ ;  $f = 50 \text{ Hz}$

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Outputs pin 14, 15						
H-output voltage – $I_Q = 250 \text{ mA}$	$V_{14/15 \text{ H}}$	$V_S - 3$	$V_S - 2.5$	$V_S - 1.0$	V	3.6
L-output voltage $I_Q = 2 \text{ mA}$	$V_{14/15 \text{ L}}$	0.3	0.8	2	V	2.6
Pulse width (short pulse) S9 open	$t_p$	20	30	40	$\mu\text{s}$	1
Pulse width (short pulse) with $C_{12}$	$t_p$	530	620	760	$\mu\text{s}/\text{nF}$	1
Internal voltage control						
Reference voltage	$V_{\text{REF}}$	2.8	3.1	3.4	V	1
Parallel connection of 10 ICs possible						
TC of reference voltage	$\alpha_{\text{REF}}$		$2 \times 10^{-4}$	$5 \times 10^{-4}$	1/K	1

## Application Hints for External Components

Ramp capacitance	$C_{10}$	min 500 pF	max 1 $\mu\text{F}$ <sup>1)</sup>	The minimum and maximum values of $I_{10}$ are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{REF} \times K}$		<sup>2)</sup>	
Charge current	$I_{10} = \frac{V_{REF} \times K}{R_9}$		<sup>2)</sup>	Ramp voltage $V_{10 \max} = V_S - 2 \text{ V}$ $V_{10} = \frac{V_{REF} \times K \times t}{R_9 \times C_{10}}$ <sup>2)</sup>

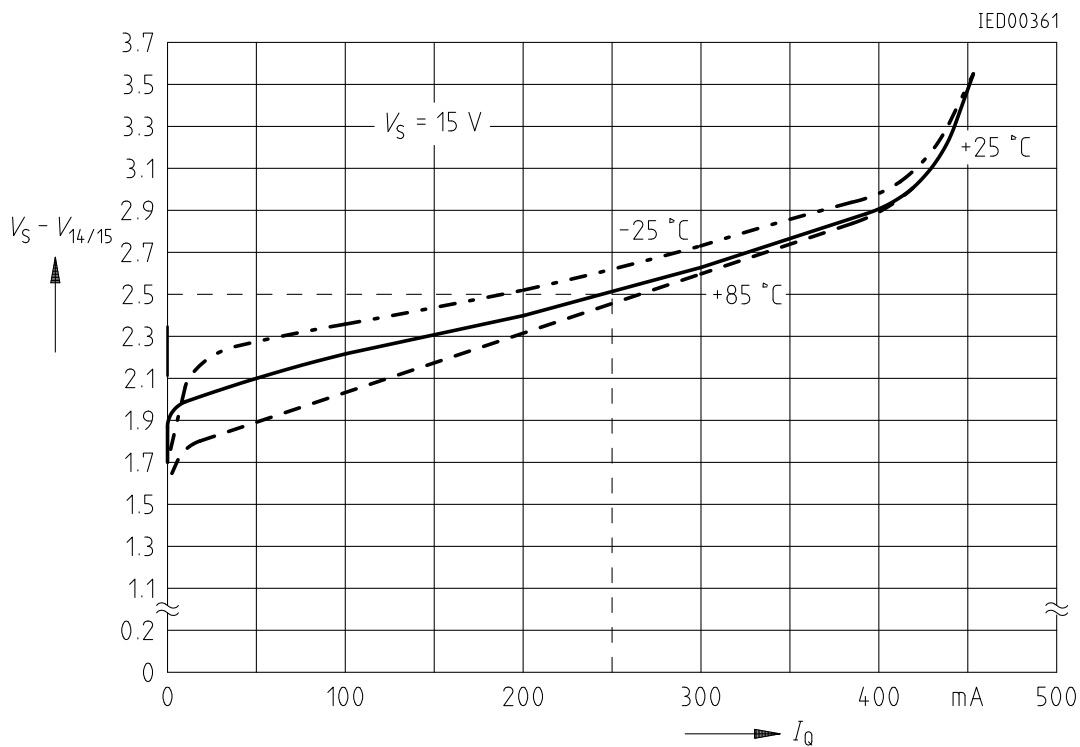
## Pulse Extension versus Temperature



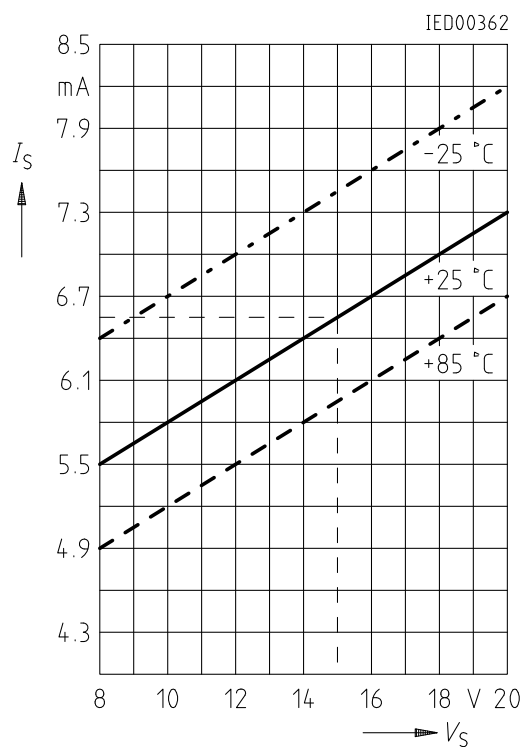
<sup>1)</sup> Attention to flyback times

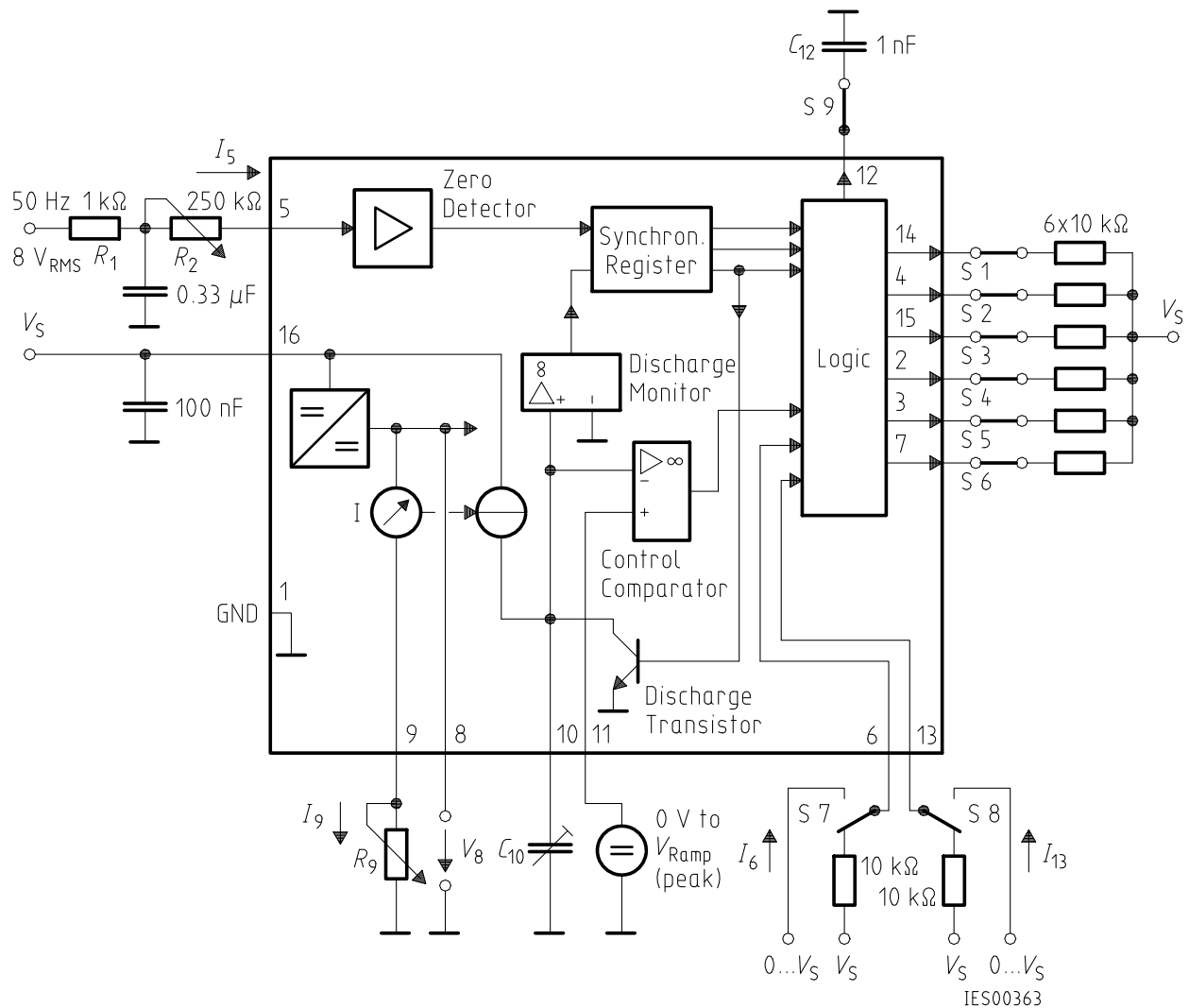
<sup>2)</sup>  $K = 1.10 \pm 20 \%$

## Output Voltage measured to + $V_S$



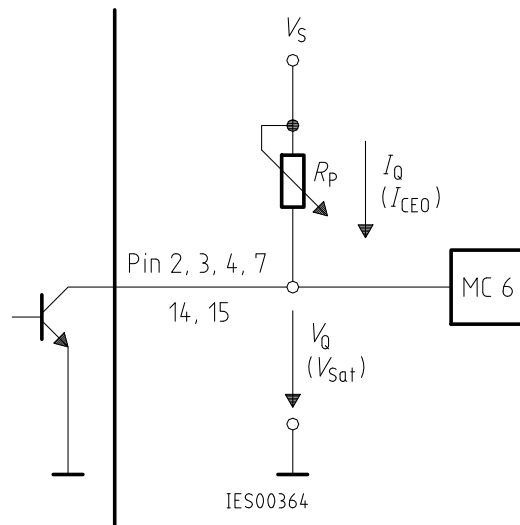
## Supply Current versus Supply Voltage





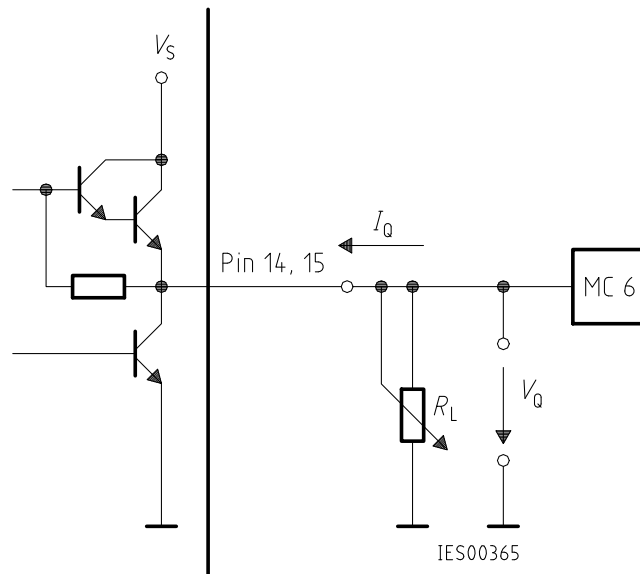
It is necessary for all measurements to adjust the ramp with the aid of  $C_{10}$  and  $R_9$  in the way that  $3\text{ V} \leq V_{\text{ramp max}} \leq V_S - 2\text{ V}$   
 e.g.  $C_{10} = 47\text{ nF}$ ;  $18\text{ V}$ :  $R_9 = 47\text{ k}\Omega$ ;  $8\text{ V}$ :  $R_9 = 120\text{ k}\Omega$

## Test Circuit 1



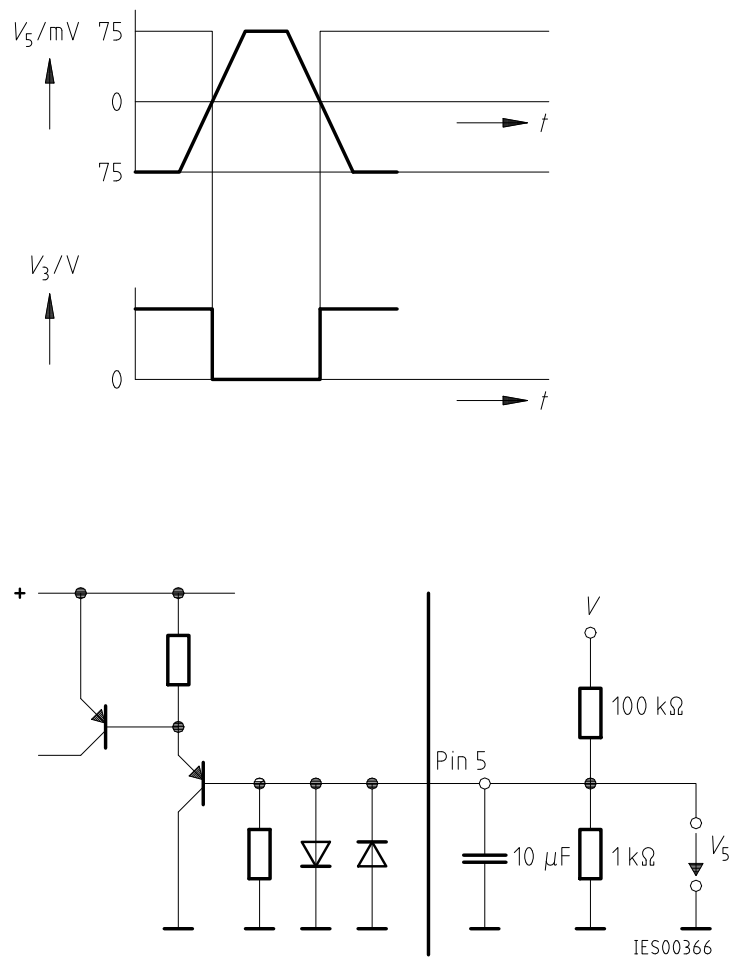
The remaining pins are connected as in test circuit 1

## Test Circuit 2



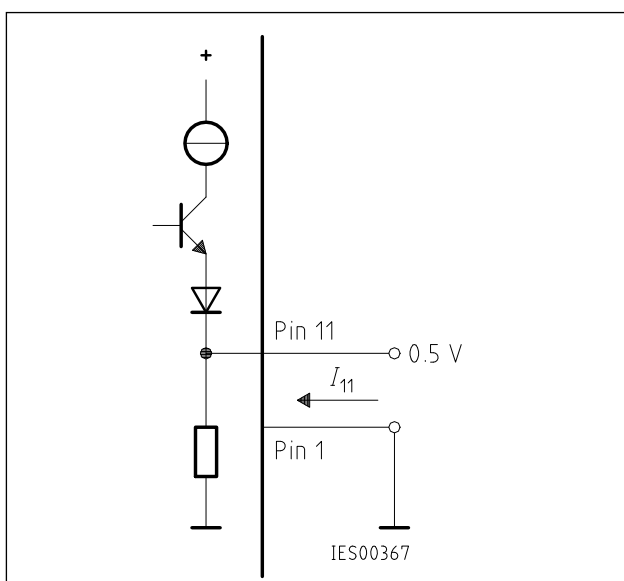
The remaining pins are connected as in test circuit 1

## Test Circuit 3

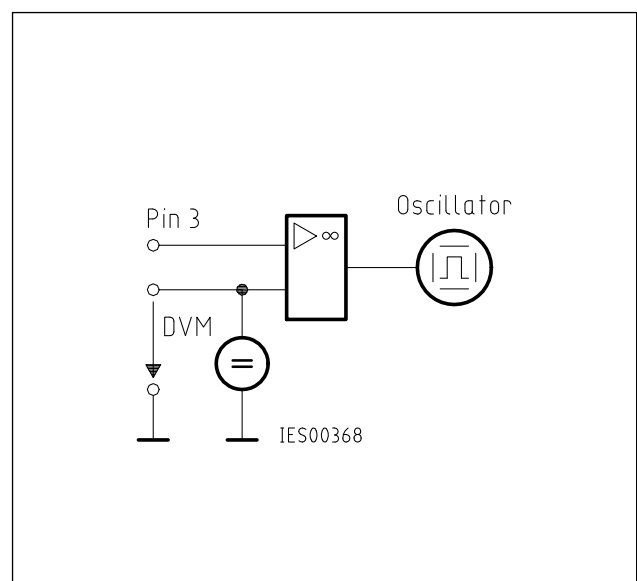


Remaining pins are connected as in test circuit 1  
The 10  $\mu\text{F}$  capacitor at pin 5 serves only for test purposes

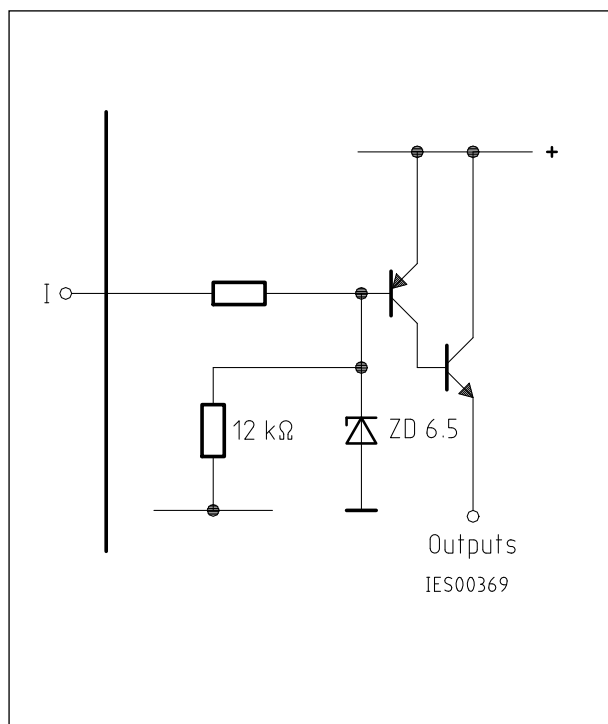
## Test Circuit 4



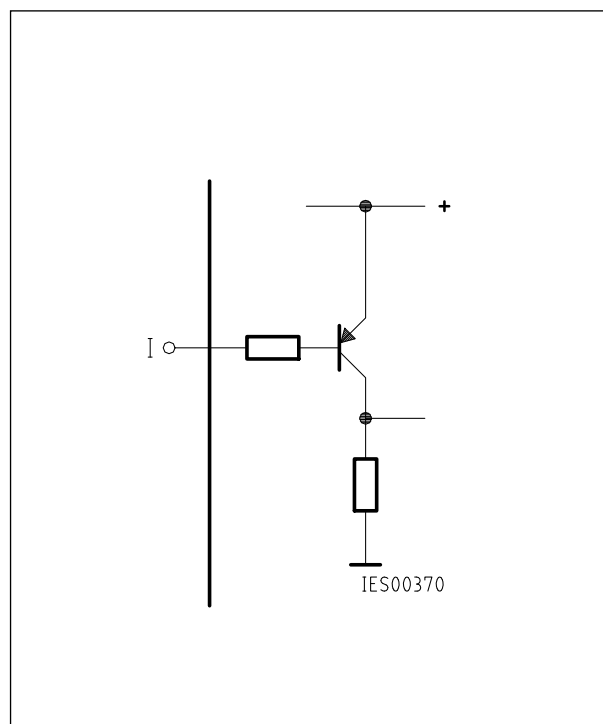
## Test Circuit 5



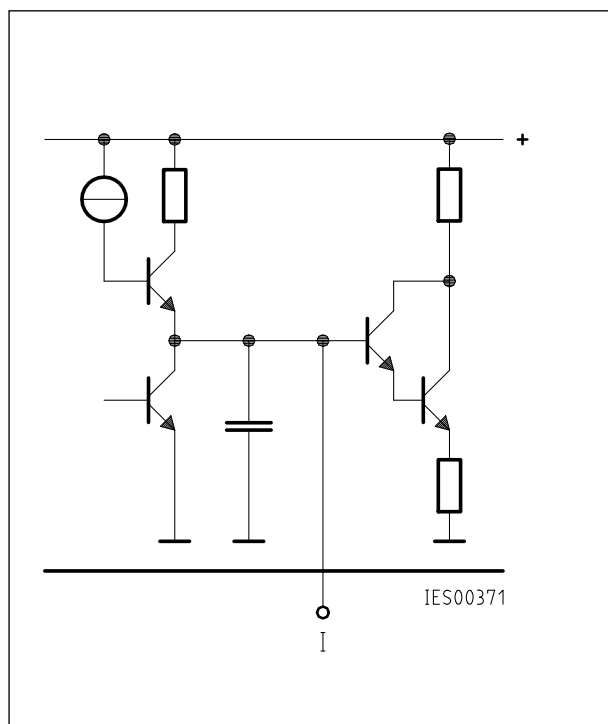
## Test Circuit 6



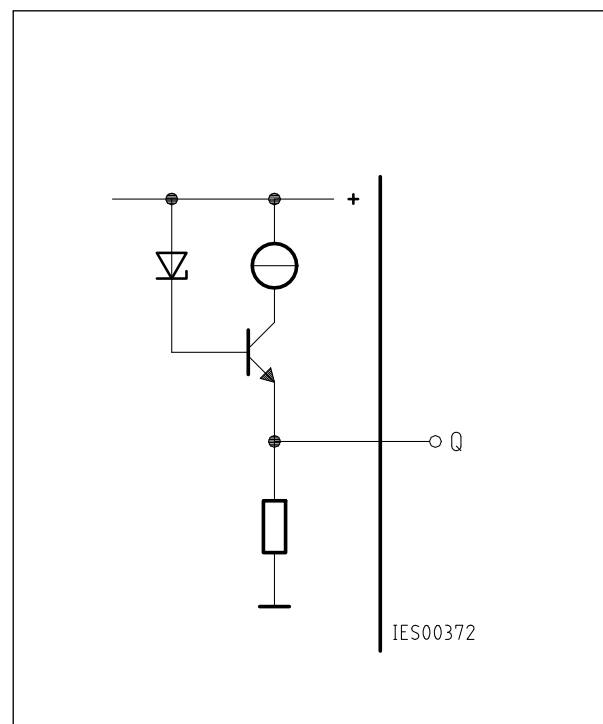
**Inhibit 6**



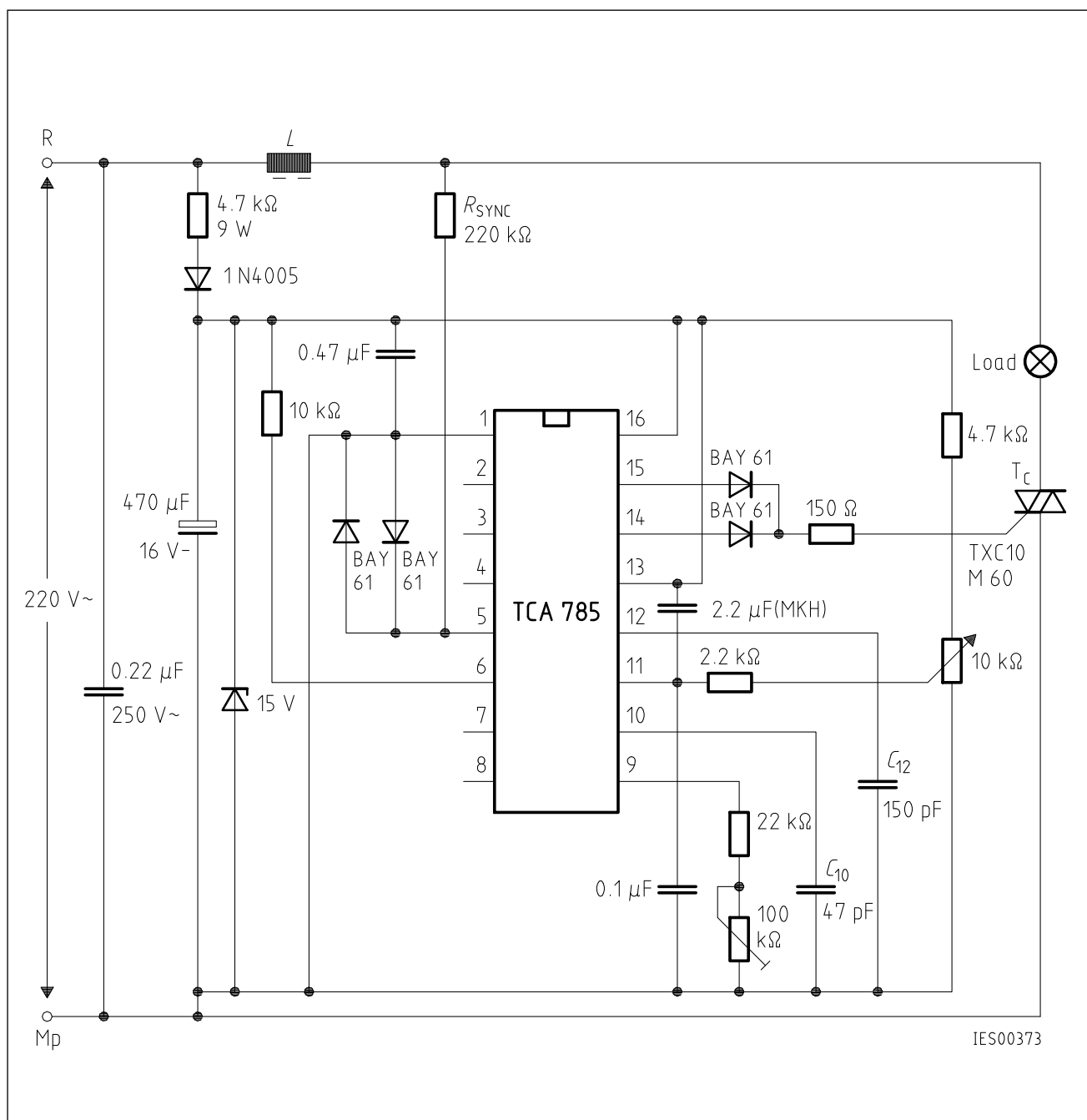
**Long Pulse 13**



**Pulse Extension 12**



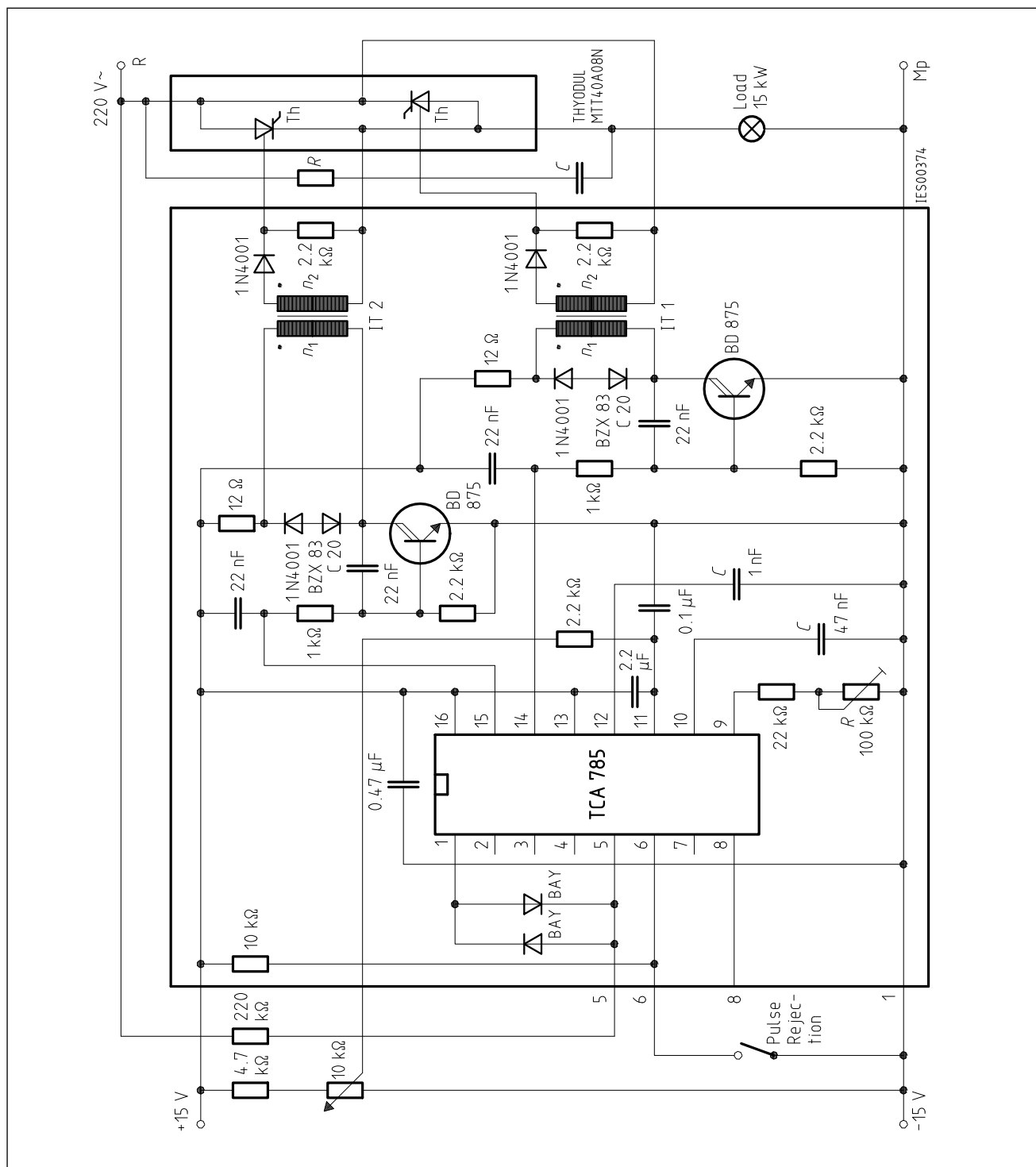
**Reference Voltage 8**



## Application Examples

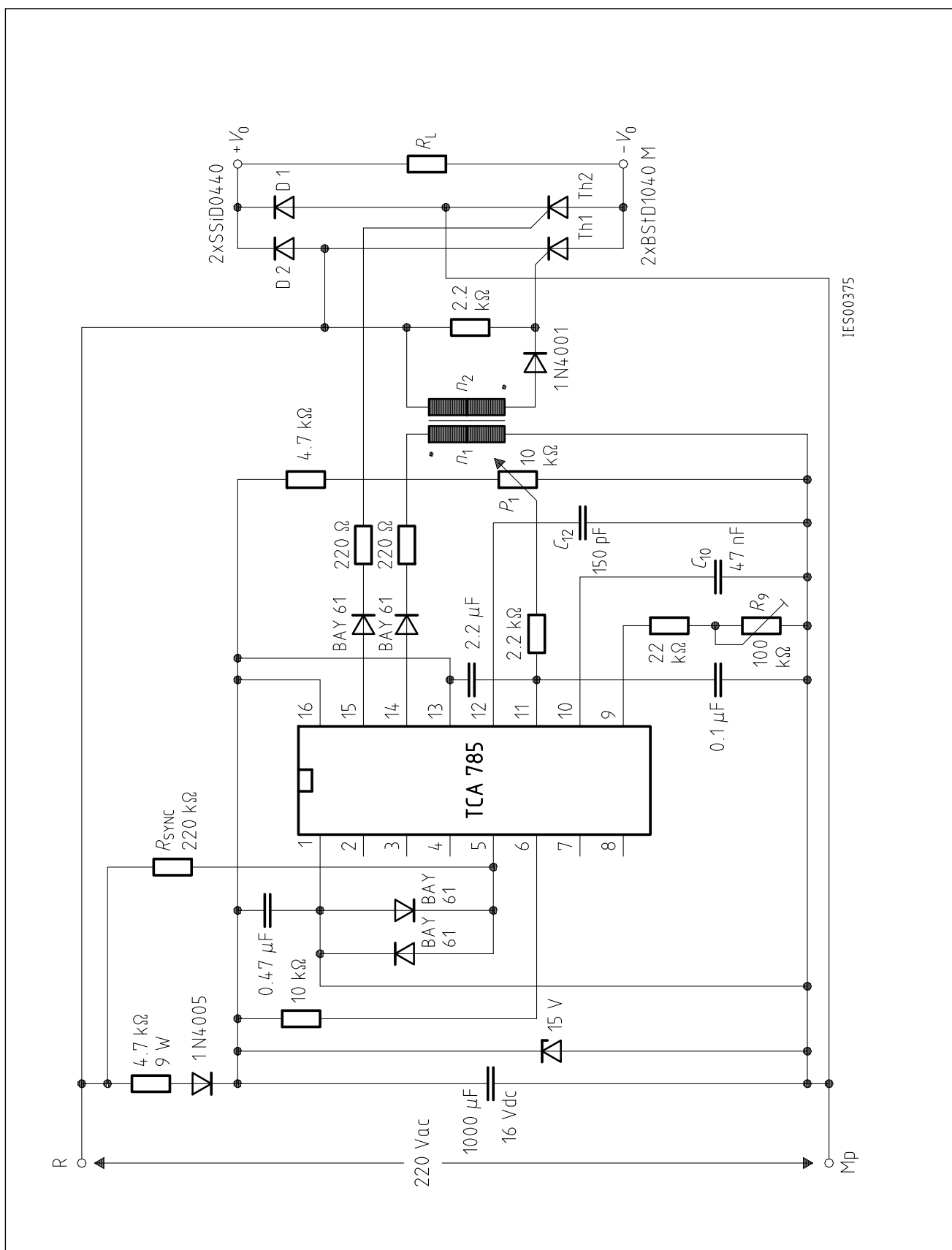
### Triac Control for up to 50 mA Gate Trigger Current

A phase control with a directly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between  $0^\circ$  and  $180^\circ$  with the aid of an external potentiometer. During the positive half-wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half-wave, it also receives a positive trigger pulse from pin 14. The trigger pulse width is approx.  $100\text{ }\mu\text{s}$ .

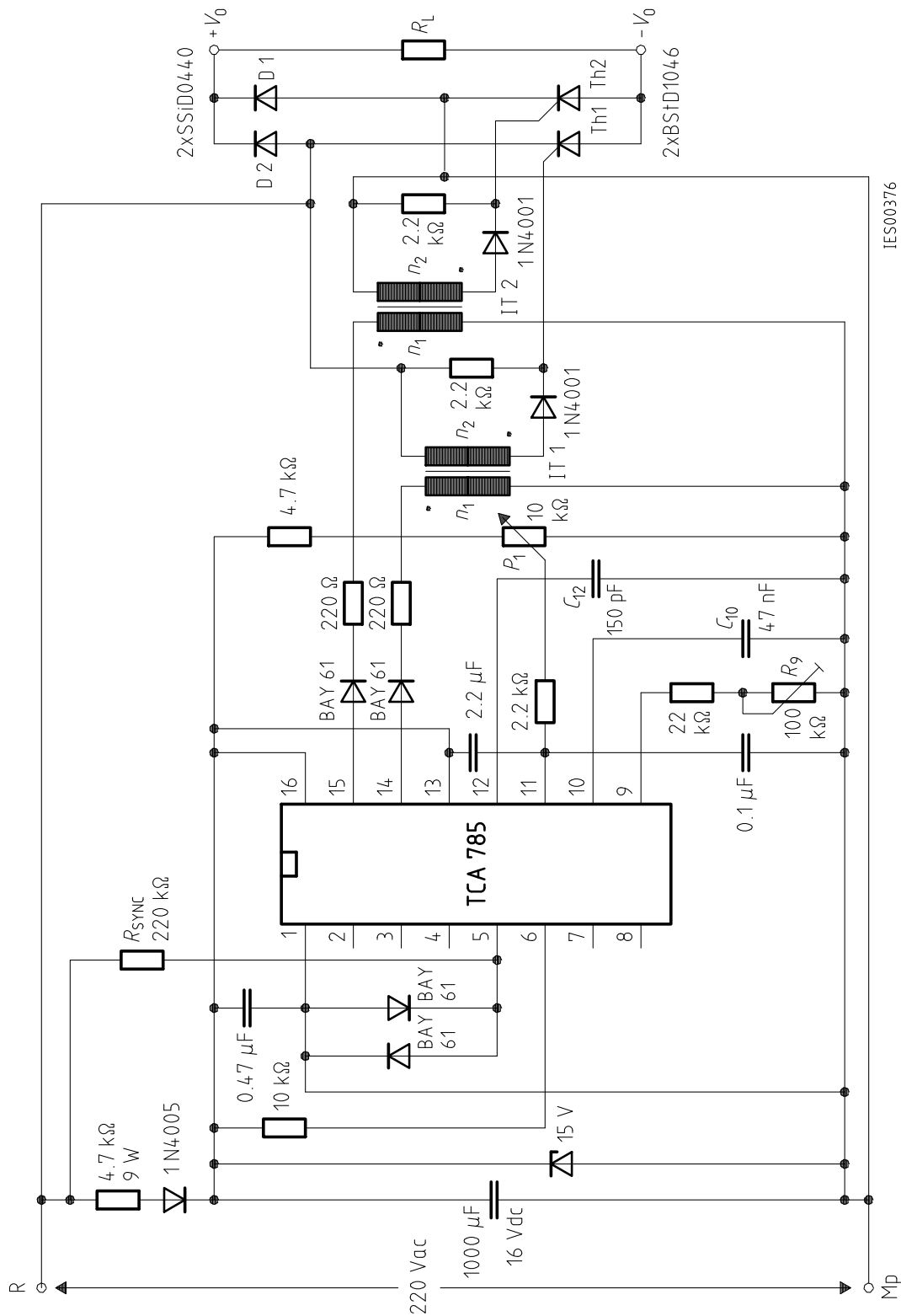


## Fully Controlled AC Power Controller Circuit for Two High-Power Thyristors

Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulse can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half-wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half-wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.



Half-Controlled Single-Phase Bridge Circuit with Trigger Pulse Transformer and Direct Control for Low-Power Thyristors



Half-Controlled Single-Phase Bridge Circuit with Two Trigger Pulse Transformers for Low-Power Thyristors