Preliminary PTFA181001GL
PTFA181001HL

green Product

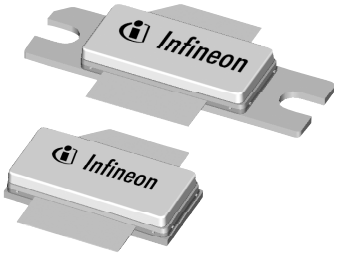
Thermally-Enhanced High Power RF LDMOS FETs
100 W, 1805 – 1880 MHz

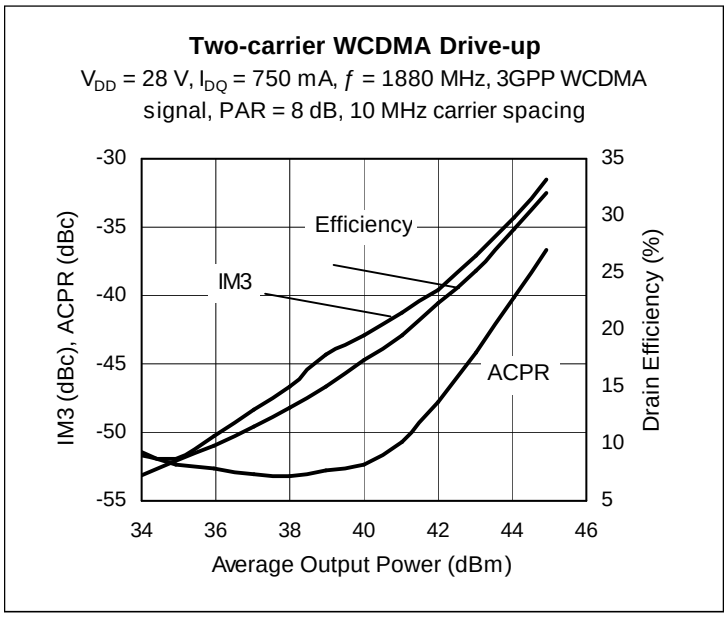
Description

The PTFA181001GL and PTFA181001GL are 100-watt LDMOS FETs designed for EDGE and WCDMA power amplifier applications in the 1805 to 1880 MHz band. Features include input and output matching, and thermally-enhanced open-cavity packages with copper flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA181001GL*
Package PG-63248-2

PTFA181001HL*
Package PG-64248-2





Features

- Thermally-enhanced, plastic open-cavity (EPOC™) packages with copper flanges, Pb-free and RoHS compliant
- Broadband internal matching
- Typical EDGE performance at 1879.8 MHz, 28 V
  - Average output power = 45 W
  - Linear Gain = 16.5 dB
  - Efficiency = 36%
  - EVM RMS = 1.8%
- Typical CW performance, 1880 MHz, 28 V
  - Output power at P–1dB = 120 W
  - Gain 15.5 dB
  - Efficiency = 52%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability
- Capable of handling 10:1 VSWR @ 28 V, 100 W (CW) output power

RF Characteristics

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 750 mA, P_{OUT} = 45 W (AVG), f = 1879.8 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Error Vector Magnitude	RMS EVM	—	1.8	—	%
Modulation Spectrum @ 400 KHz	ACPR	—	–61	—	dBc
Modulation Spectrum @ 600 KHz	ACPR	—	–73	—	dBc
Gain	G_{ps}	—	16.5	—	dB
Drain Efficiency	η_D	—	36	—	%

All published data at T_{CASE} = 25°C unless otherwise indicated

**See Infineon distributor for future availability.*

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 750 mA, P_{OUT} = 100 W PEP, f = 1850 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	16.5	—	dB
Drain Efficiency	η_D	—	41	—	%
Intermodulation Distortion	IMD	—	–30	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.085	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_D = 750 mA	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	TBD	W
Above 25°C derate by		TBD	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 100 W CW)	$R_{\theta JC}$	TBD	°C/W

Ordering Information

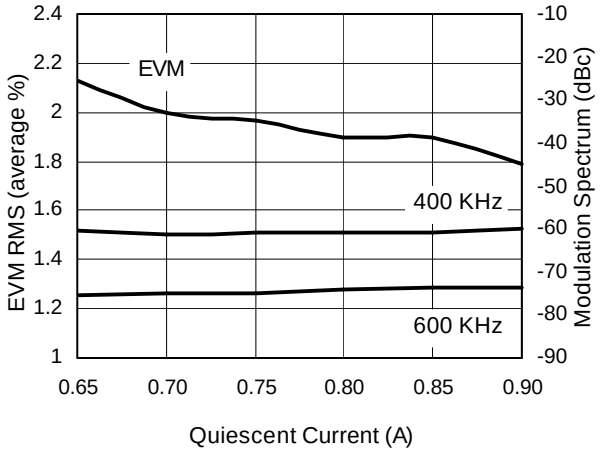
Type and Version	Package Type	Package Description	Shipping	Marking
PTFA181001GL* V1	PG-63248-2	Thermally-enhanced, plastic open-cavity, slotted flange, single-ended	Tray	PTFA181001GL
PTFA181001HL* V1	PG-64248-2	Thermally-enhanced, plastic open-cavity, earless flange, single-ended	Tray	PTFA181001HL

**See Infineon distributor for future availability.*

Typical Performance (data taken in a production test fixture)

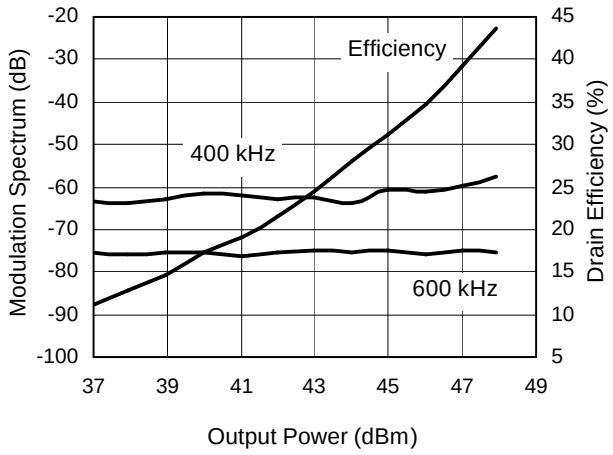
Edge EVM and Modulation Spectrum vs. Quiescent Current

V_{DD} = 28V, f = 1879.8 MHz, P_{OUT} = 46.5 dBm



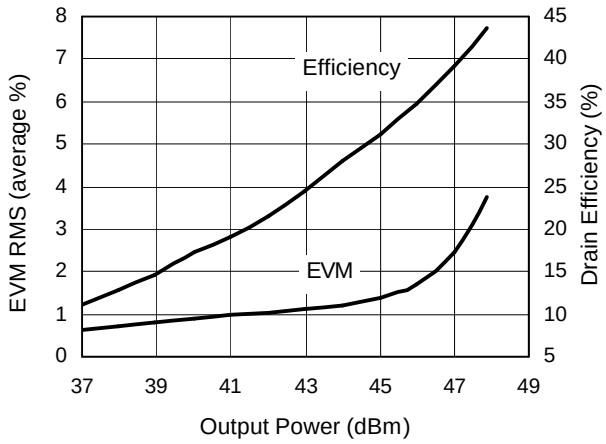
EDGE Modulation Spectrum Performance

V_{DD} = 28 V, I_{DQ} = 750 mA, f = 1879.8 MHz



EDGE EVM Performance

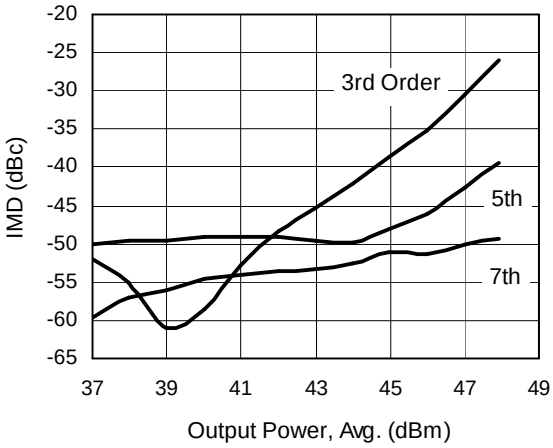
V_{DD} = 28 V, I_{DQ} = 750 mA, f = 1879.8 MHz



Intermodulation Distortion vs. Output Power

(as measured in a broadband circuit)

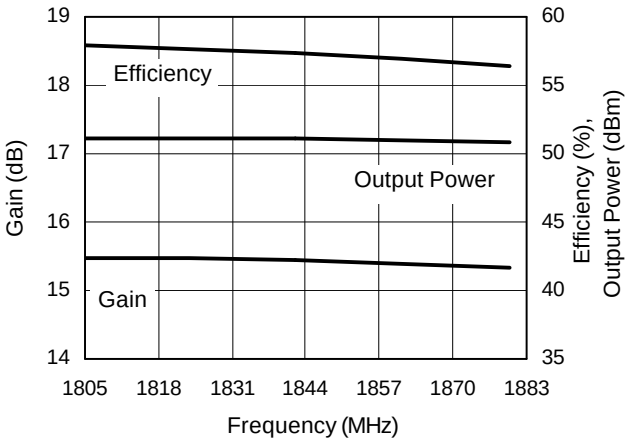
V_{DD} = 28 V, I_{DQ} = 750 mA, f_1 =1879 MHz, f_2 = 1880 MHz



Typical Performance (cont.)

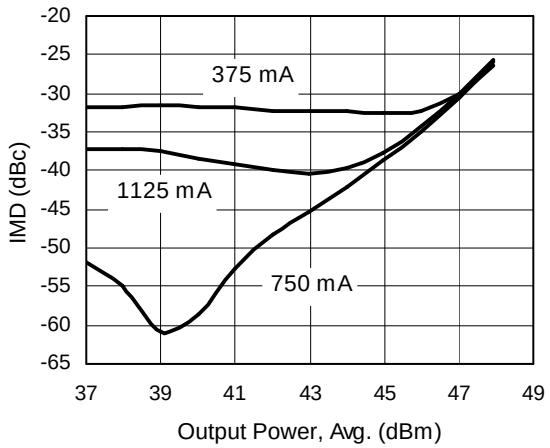
Broadband CW Performance (at P-1dB)

V_{DD} = 28 V, I_{DQ} = 750 m



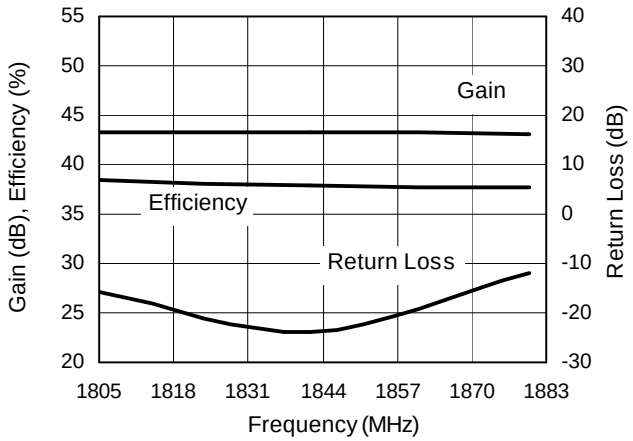
IM3 vs. Output Power at Selected Biases

V_{DD} = 28 V, f_1 = 1879, f_2 = 1880 MHz



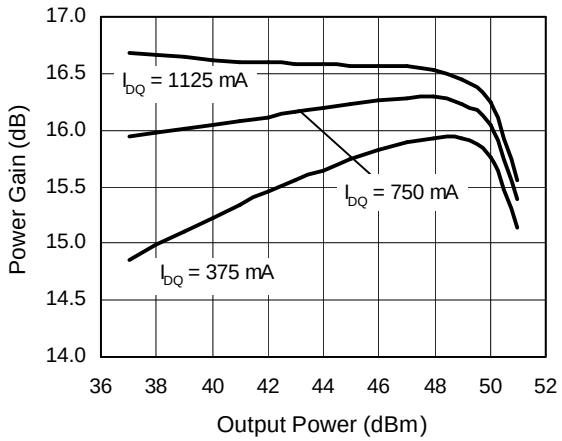
CW Broadband Performance

V_{DD} = 28 V, I_{DQ} =750 mA, P_{OUT} = 47 dBm



Power Sweep

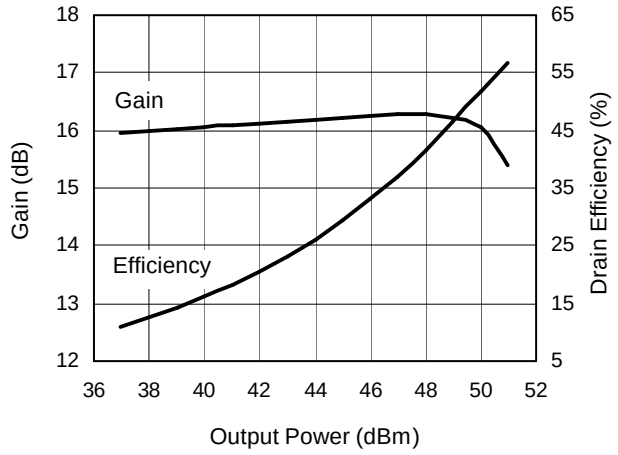
V_{DD} = 28 V, f = 1880 MHz



Typical Performance (cont.)

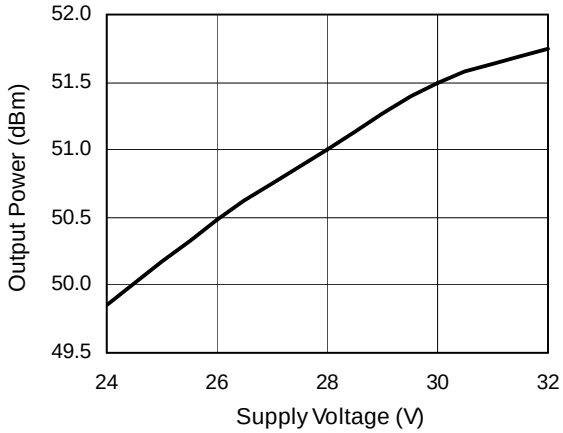
Gain & Efficiency vs. Output Power

V_{DD} = 28 V, I_{DQ} = 750 mA, f = 1880 MHz



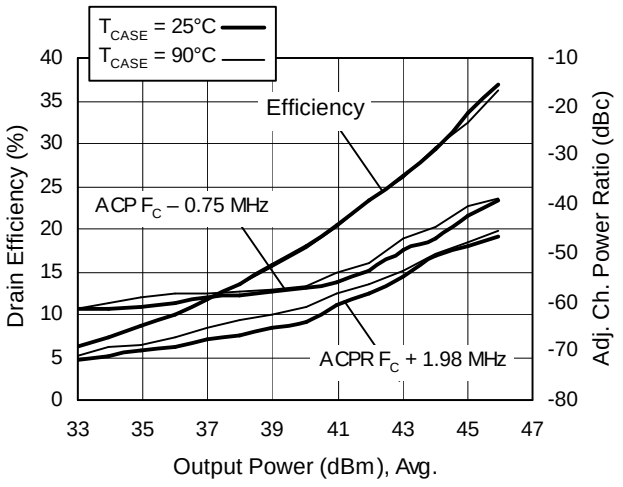
Output Power (at 1 dB Compression) vs. Supply Voltage

I_{DQ} = 750 mA, f =1880 MHz

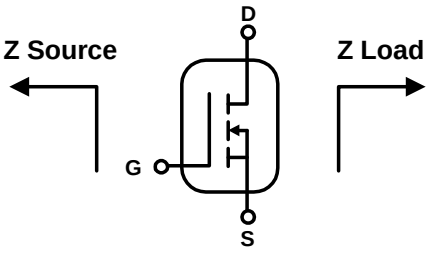


IS-95 CDMA Performance

V_{DD} = 28 V, I_{DQ} = 750 mA, f = 1880 MHz



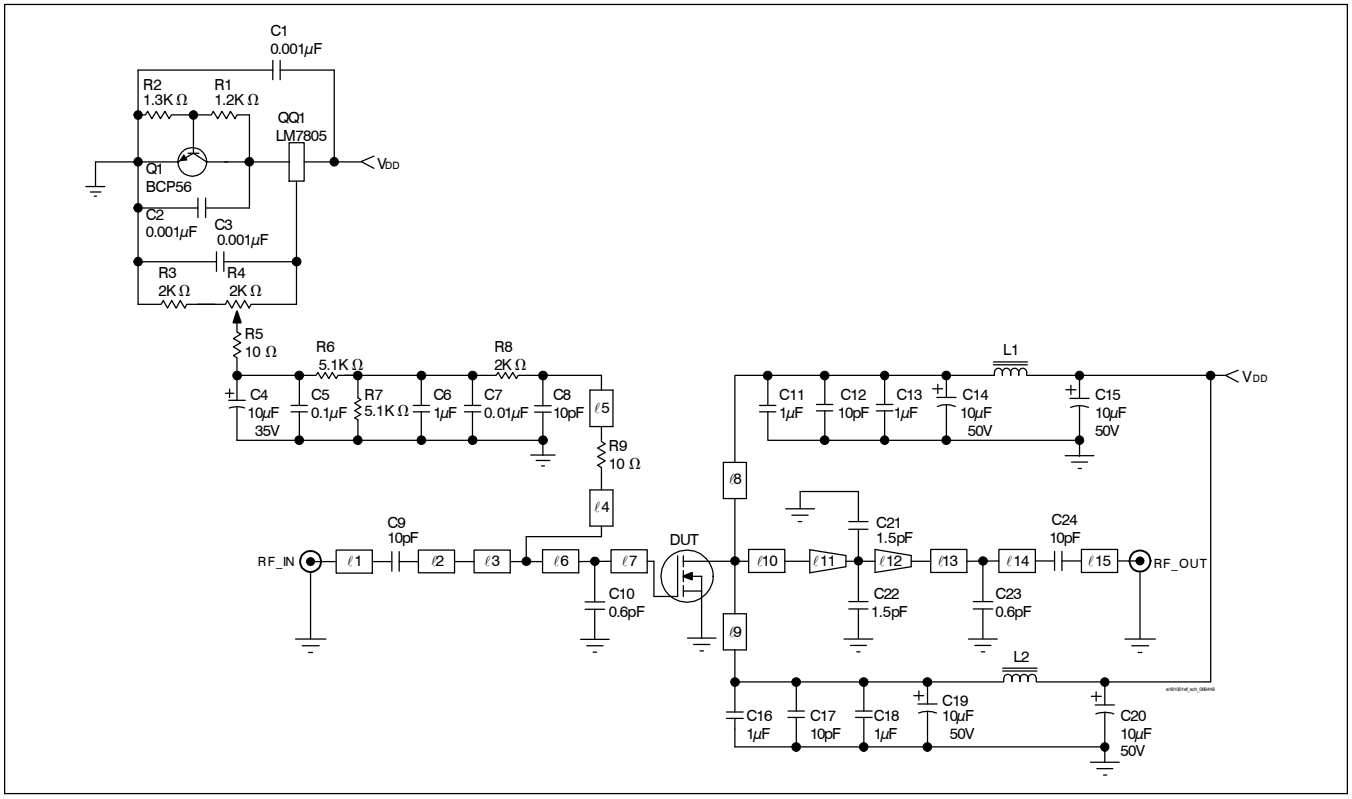
Broadband Circuit Impedance



Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
1805	4.62	–6.23	1.50	–3.87
1830	4.18	–6.10	1.51	–3.46
1850	4.20	–6.13	1.50	–3.16
1860	4.58	–6.20	1.49	–3.00
1880	4.42	–6.36	1.48	–2.62

See next page for reference circuit

Reference Circuit



Reference circuit schematic for ƒ = 1880 MHz

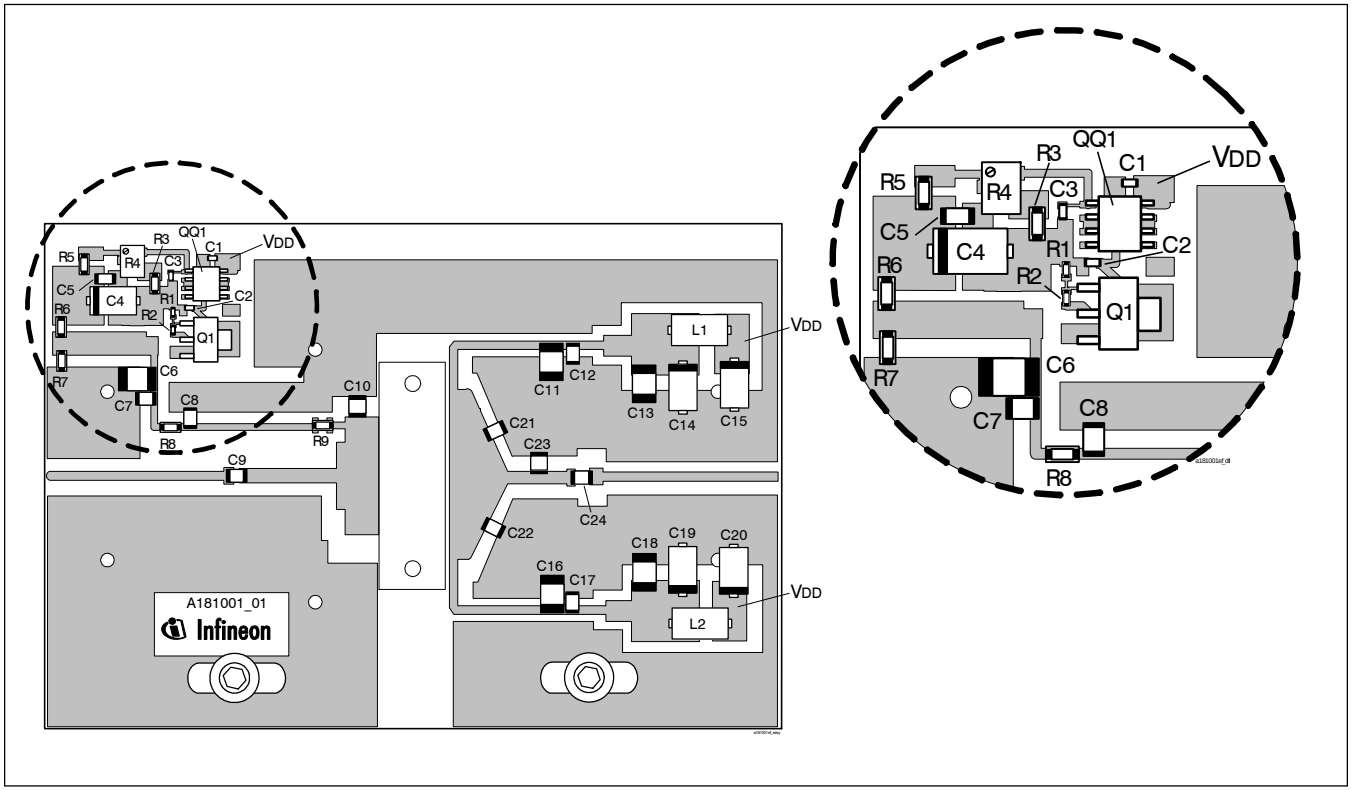
Circuit Assembly Information

DUT	PTFA181001GL or PTFA181001HL	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 1880 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.314 λ, 50.0 Ω	27.43 x 1.37	1.080 x 0.054
ℓ2	0.172 λ, 38.0 Ω	14.73 x 2.16	0.580 x 0.085
ℓ3	0.016 λ, 11.4 Ω	1.27 x 10.16	0.050 x 0.400
ℓ4	0.024 λ, 60.0 Ω	2.24 x 0.99	0.088 x 0.039
ℓ5	0.218 λ, 60.0 Ω	19.33 x 0.99	0.761 x 0.039
ℓ6	0.019 λ, 6.9 Ω	1.52 x 17.78	0.060 x 0.700
ℓ7	0.044 λ, 6.9 Ω	3.43 x 17.78	0.135 x 0.700
ℓ8, ℓ9	0.233 λ, 53.0 Ω	20.45 x 1.24	0.805 x 0.049
ℓ10	0.039 λ, 4.9 Ω	3.10 x 25.65	0.122 x 1.010
ℓ11 (taper)	0.037 λ, 4.9 Ω / 10.3 Ω	2.92 x 25.65 / 11.43	0.115 x 1.010 / 0.450
ℓ12 (taper)	0.033 λ, 10.3 Ω / 41.0 Ω	2.79 x 11.43 / 1.91	0.110 x 0.450 / 0.075
ℓ13	0.069 λ, 41.0 Ω	6.35 x 1.91	0.250 x 0.075
ℓ14	0.038 λ, 41.0 Ω	3.25 x 1.91	0.128 x 0.075
ℓ15	0.331 λ, 50.0 Ω	28.98 x 1.37	1.141 x 0.054

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	399-1655-2-ND
C5	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C11, C13, C16, C18	Capacitor, 1.0 µF	ATC	920C105
C7	Capacitor, 0.01 µF	ATC	200B 103
C8, C9, C12, C17, C24	Ceramic capacitor, 10 pF	ATC	100B 100
C10, C23	Ceramic capacitor, 0.6 pF	ATC	100B 0R6
C14, C15, C19, C20	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPSE106K050R0400
C21, C22	Ceramic capacitor, 1.5 pF	ATC	100B 1R5
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infinion Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip Resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip Resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R8	Chip Resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R9	Chip Resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip Resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND

**Gerber files for this circuit available on request*

Package Outline Specifications

Package PG-63248-2

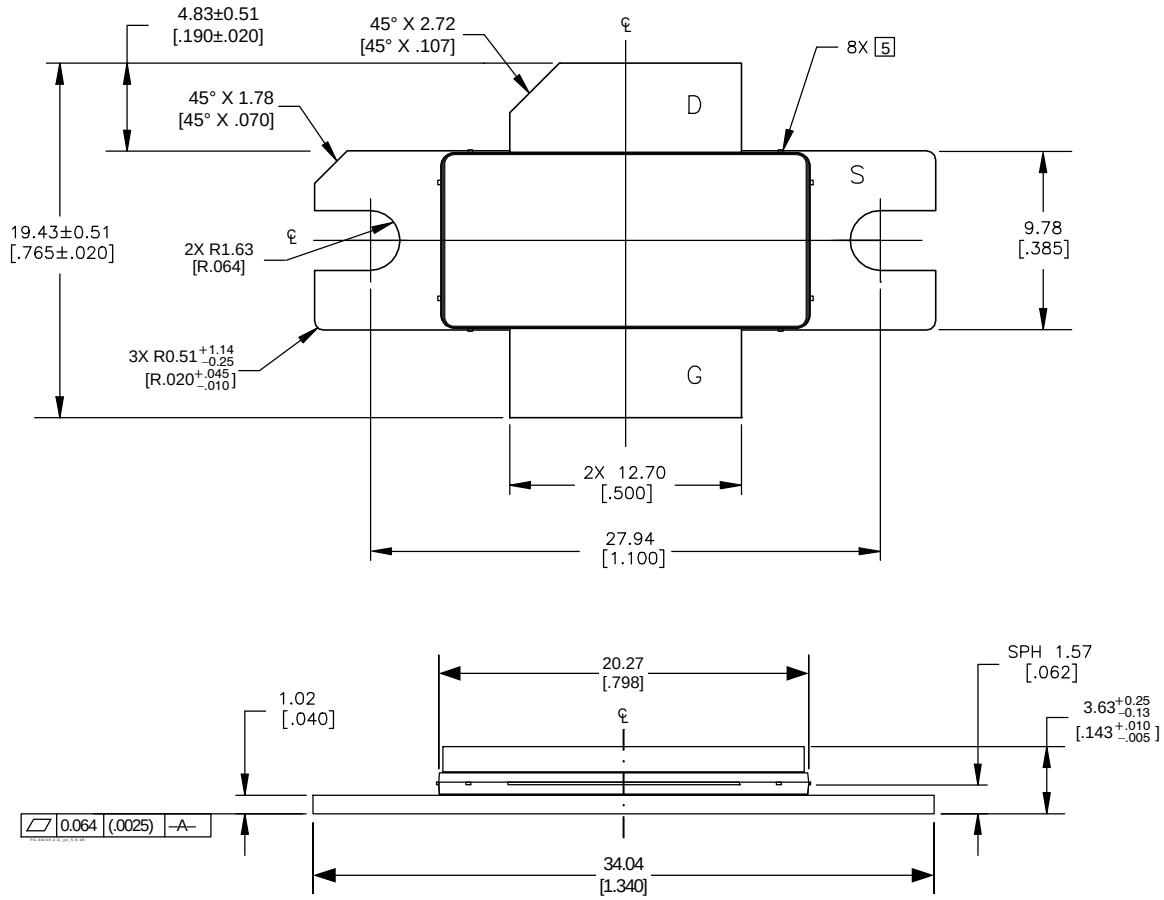
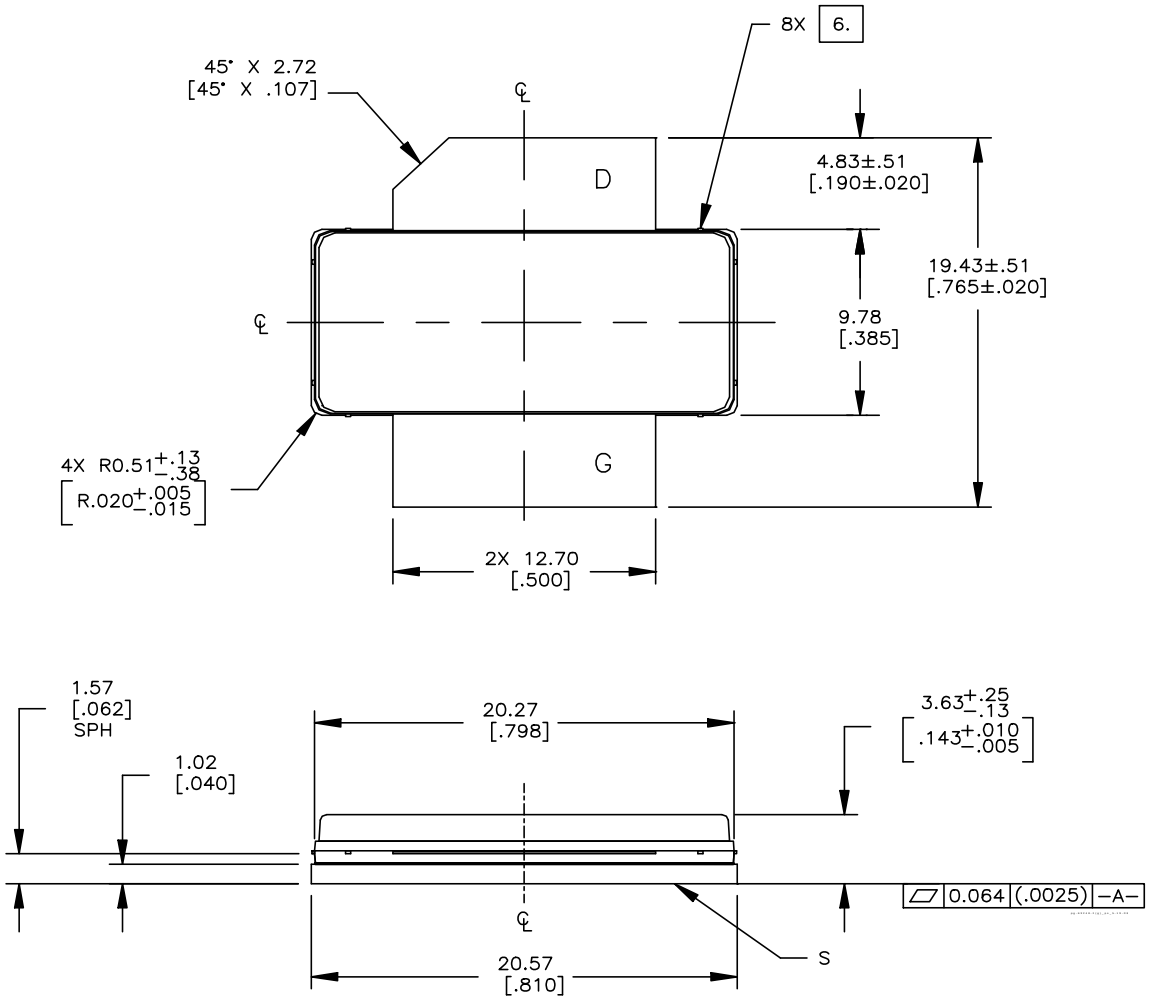


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Pins: D = drain, S = source, G = gate.
3. Lead thickness: 0.10 + 0.051/–0.025 mm [.004 +0.002/–0.001 inch].
4. Gold plating thickness: < 0.254 micron [< 10 microinch]
5. Tabs may protrude 0.13 [.005] max from body.
6. All tolerances: TBD.
7. Primary dimensions are mm. Alternate dimensions are inches.

Package Outline Specifications (cont.)

Package PG-63248-2



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Revision History:	2008-06-15	PreliminaryData Sheet
Previous Version:	none	

Page	Subjects (major changes since last revision)

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highpowerRF@infineon.com

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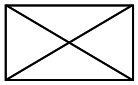

Edition 2008-06-15

Published by
Infineon Technologies AG
81726 Munich, Germany

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