

Thermally-Enhanced High Power RF LDMOS FETs

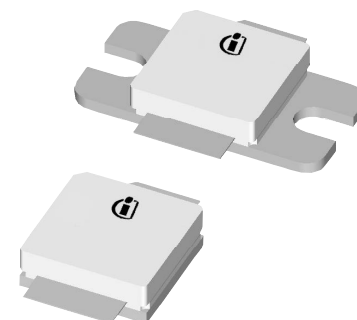
55 W, 869 – 960 MHz

Description

The PTFA080551E and PTFA080551F are 55-watt, internally matched **GOLDMOS®** FETs intended for EDGE and CDMA applications in the 869 to 960 MHz band. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

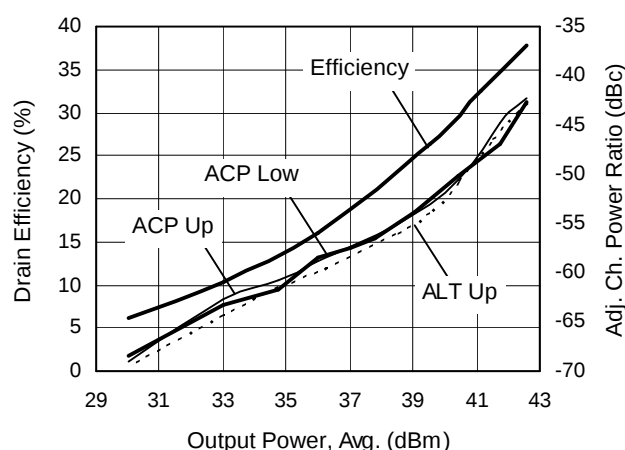
PTFA080551E
Package 30265

PTFA080551F
Package 31265



Three-Carrier CDMA2000 Performance

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$, $f = 960\text{ MHz}$



Features

- Broadband internal matching
- Typical EDGE performance
 - Average output power = 26 W
 - Gain = 18 dB
 - Efficiency = 44%
- Typical CW performance
 - Output power at P-1dB = 75 W
 - Gain = 17 dB
 - Efficiency = 67%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 55 W (CW) output power
- Pb-free and RoHS compliant

RF Characteristics

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$, $P_{OUT} = 26\text{ W}$, $f = 959.8\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Error Vector Magnitude	EVM (RMS)	—	2.5	—	%
Modulation Spectrum @ 400 kHz	ACPR	—	-60	—	dBc
Modulation Spectrum @ 600 kHz	ACPR	—	-75	—	dBc
Gain	G_{ps}	—	18	—	dB
Drain Efficiency	η_D	—	44	—	%

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$, $P_{OUT} = 55\text{ W PEP}$, $f = 960\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18	18.5	—	dB
Drain Efficiency	η_D	46.5	48	—	%
Intermodulation Distortion	IMD	—	−31	−29	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ }\mu\text{A}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.15	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$	V_{GS}	2.0	2.3	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

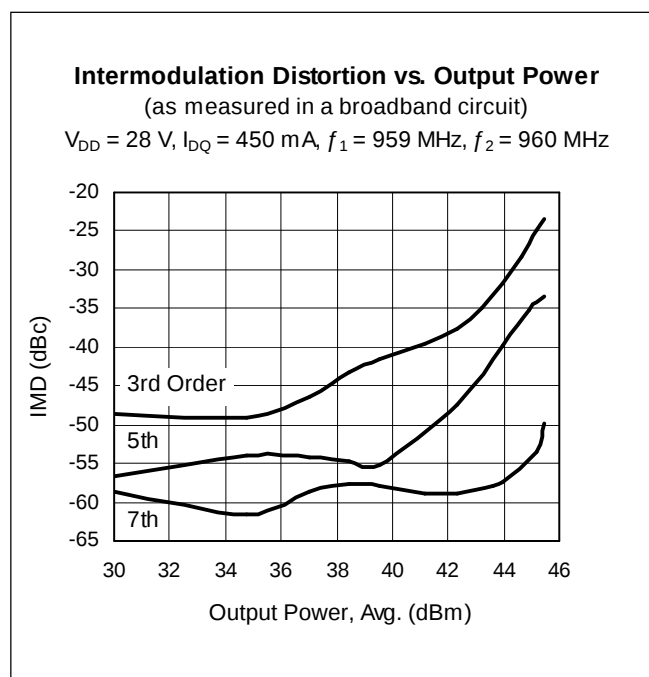
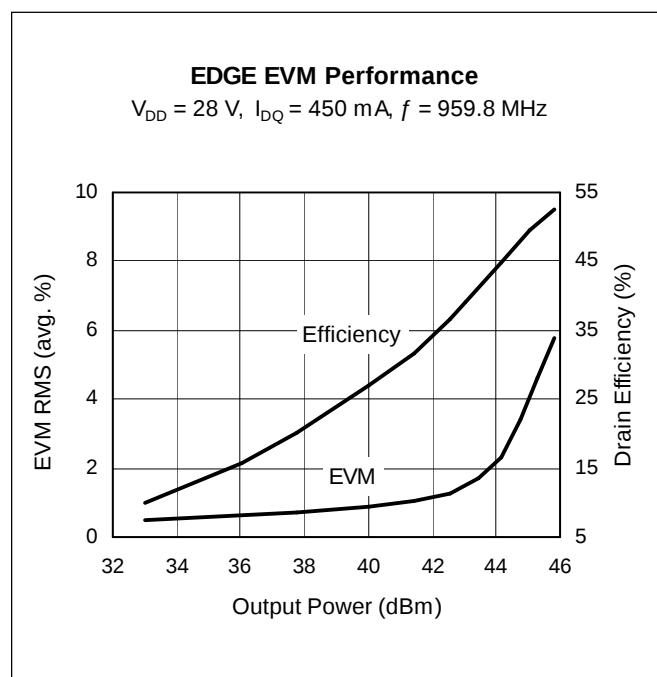
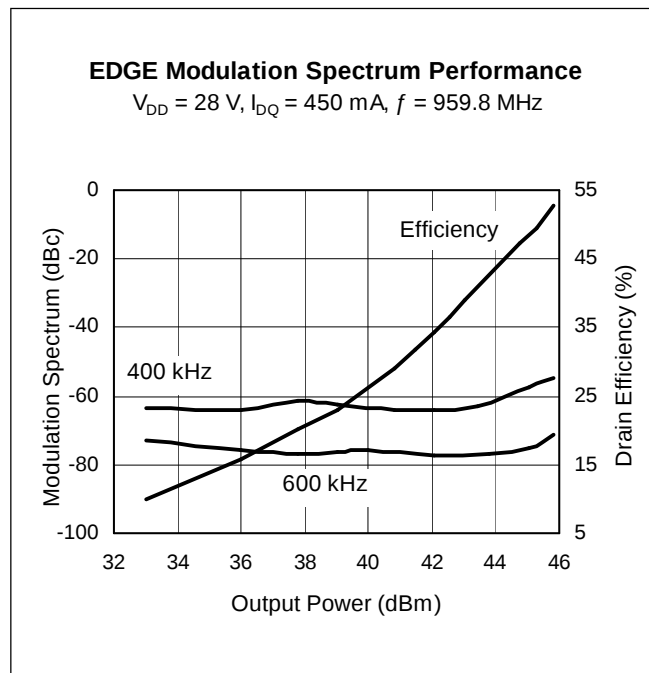
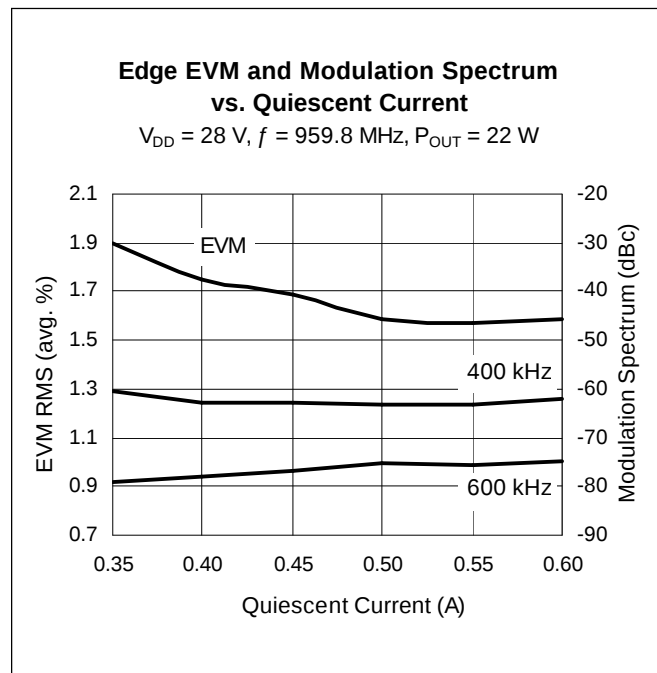
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	−0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Total Device Dissipation	P_D	219	W
Above 25 $^{\circ}\text{C}$ derate by		1.25	W/ $^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$)	$R_{\theta JC}$	0.8	$^{\circ}\text{C/W}$

Ordering Information

Type	Package Outline	Package Description	Marking
PTFA080551E	30265	Thermally-enhanced slotted flange, single-ended	PTFA080551E
PTFA080551F	31265	Thermally-enhanced earless flange, single-ended	PTFA080551F

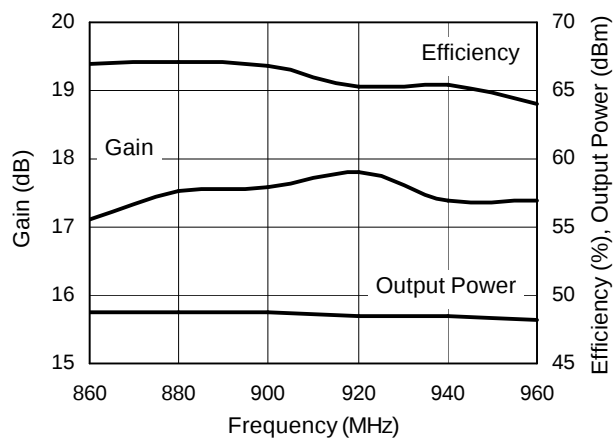
Typical Performance (data taken in a production test fixture)



Typical Performance (cont.)

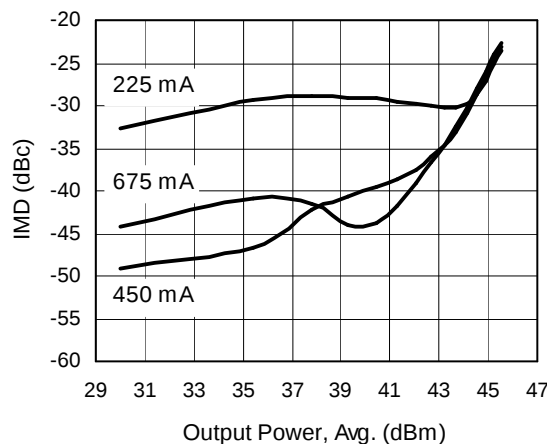
Broadband CW Performance (at P-1dB)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$



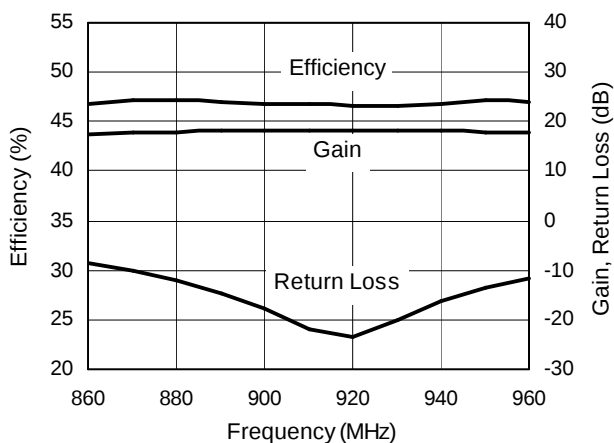
IM3 vs. Output Power at Selected Biases

$V_{DD} = 28\text{ V}$, $f_1 = 959\text{ MHz}$, $f_2 = 960\text{ MHz}$



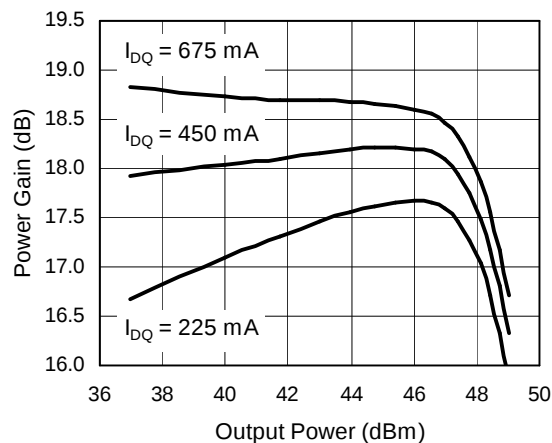
Linear Broadband Performance

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$, $P_{OUT\text{ Avg}} = 44.39\text{ dBm}$



Power Sweep

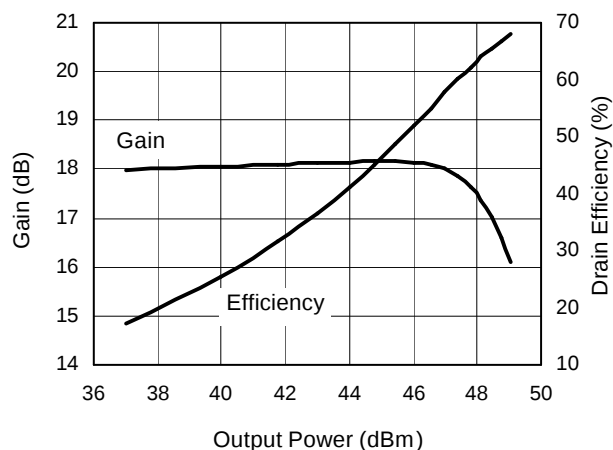
$V_{DD} = 28\text{ V}$, $f = 960\text{ MHz}$



Typical Performance (cont.)

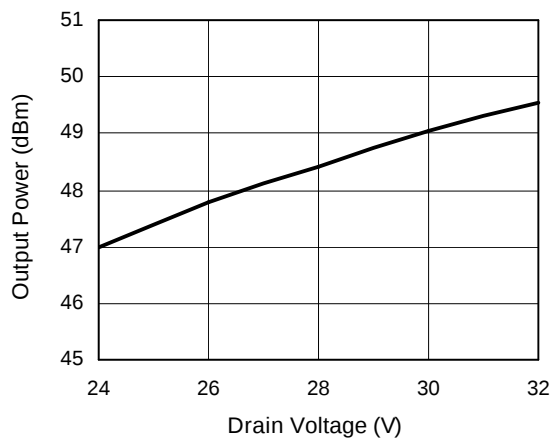
Gain & Efficiency vs. Output Power

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$, $f = 960\text{ MHz}$



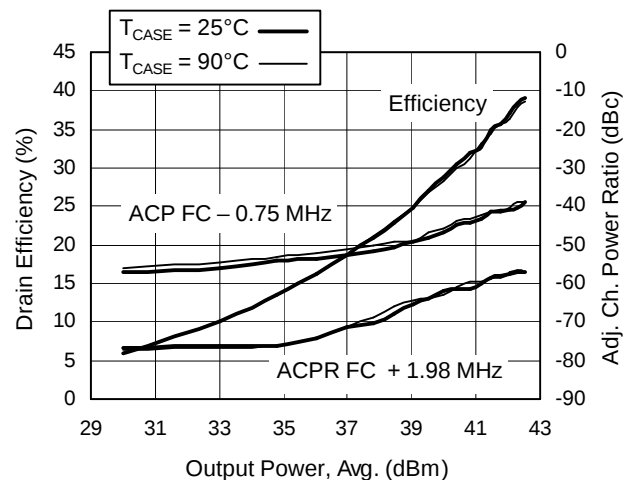
Output Power (P-1dB) vs. Drain Voltage

$I_{DQ} = 450\text{ mA}$, $f = 960\text{ MHz}$



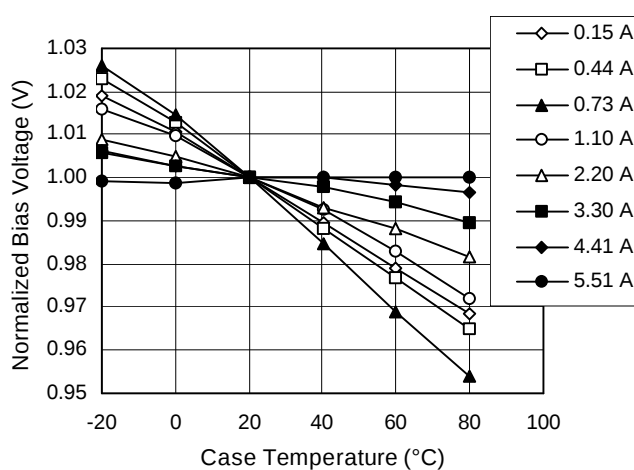
IS-95 CDMA Performance

$V_{DD} = 28\text{ V}$, $I_{DQ} = 450\text{ mA}$, $f = 960\text{ MHz}$

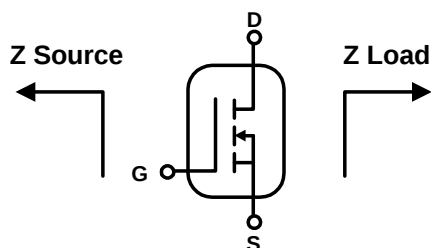


Bias Voltage vs. Temperature

Voltage normalized to typical gate voltage, series show current



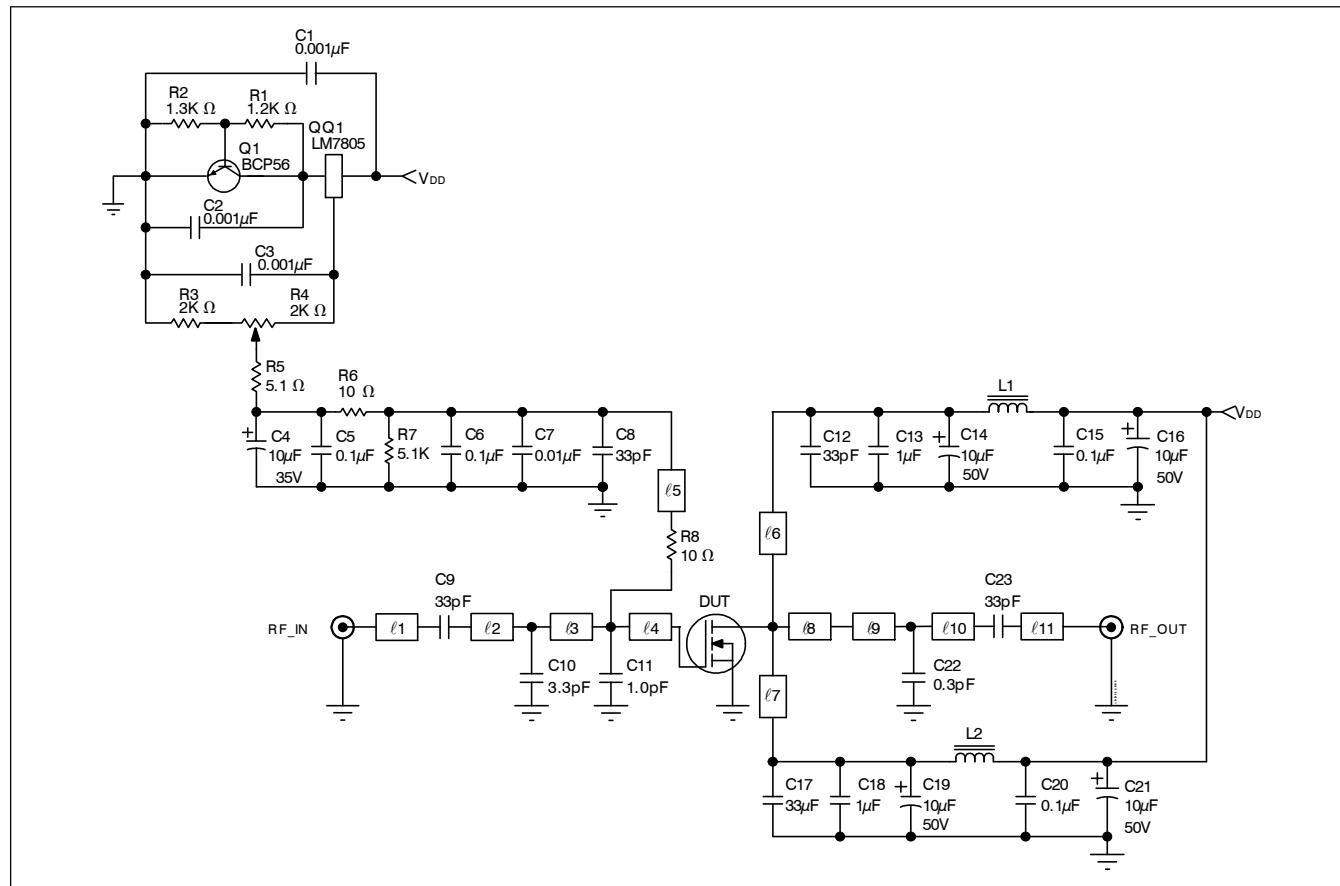
Broadband Circuit Impedance



Frequency	Z Source W		Z Load W	
MHz	R	jX	R	jX
869	8.91	-10.93	7.42	-1.63
880	3.72	-8.28	4.65	-1.74
894	5.93	-5.43	4.61	0.16
920	4.87	-7.16	4.88	-0.59
960	6.05	-5.57	4.89	0.86

See next page for circuit information

Reference Circuit



Reference circuit schematic diagram for $f = 960 \text{ MHz}$

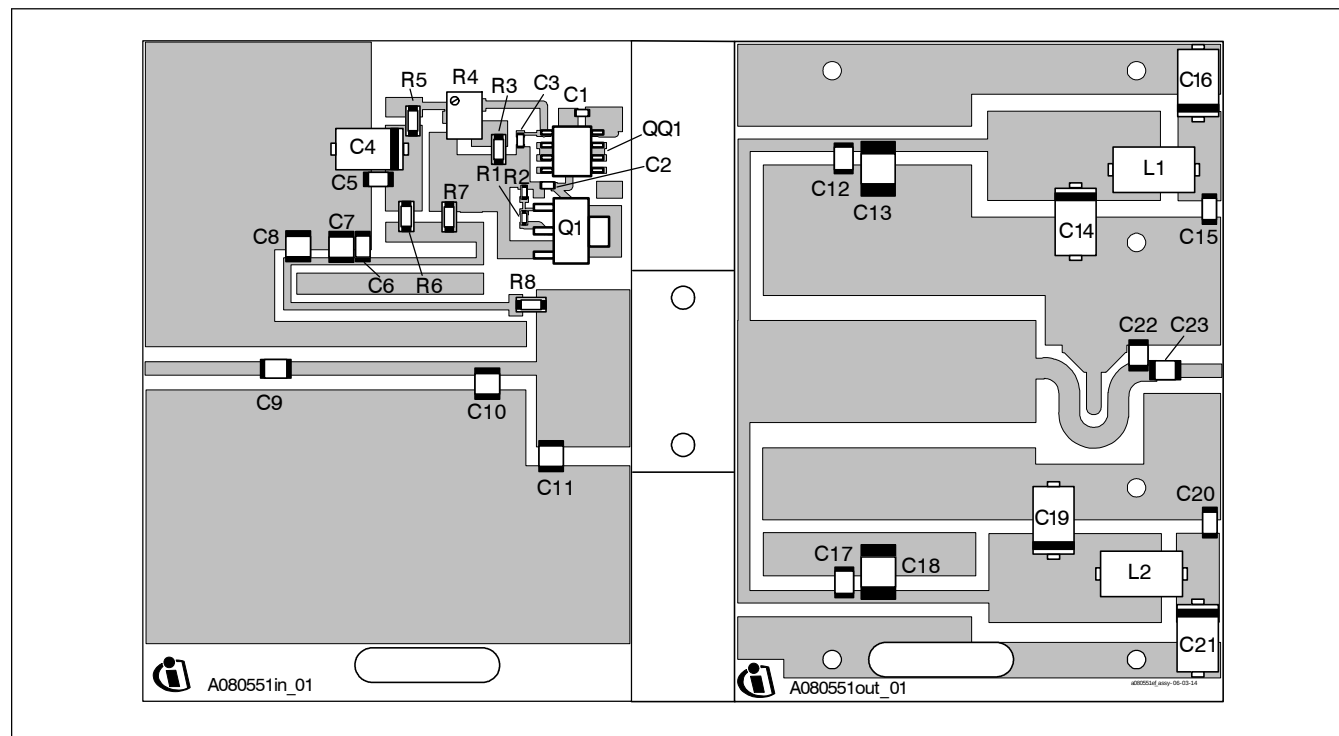
Circuit Assembly Information

DUT	PTFA080551E or PTFA080551F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 4.5$	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 960 MHz ¹	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ_1	0.070λ , 50.0Ω	12.19 x 1.37	0.480 x 0.054
ℓ_2	0.122λ , 50.0Ω	20.93 x 1.37	0.824 x 0.054
ℓ_3	0.031λ , 50.0Ω	5.31 x 1.37	0.209 x 0.054
ℓ_4	0.063λ , 7.5Ω	9.58 x 16.21	0.377 x 0.638
ℓ_5	0.162λ , 67.0Ω	28.45 x 0.79	1.120 x 0.031
ℓ_6, ℓ_7	0.150λ , 55.0Ω	25.65 x 1.17	1.010 x 0.046
ℓ_8	0.198λ , 11.1Ω	30.73 x 10.46	1.210 x 0.412
ℓ_9	0.145λ , 38.0Ω	24.21 x 2.16	0.953 x 0.085
ℓ_{10}	0.009λ , 38.0Ω	1.52 x 2.16	0.060 x 0.085
ℓ_{11}	0.026λ , 50.0Ω	4.50 x 1.37	0.177 x 0.054

¹Electrical characteristics are rounded.

Reference Circuit (cont.)

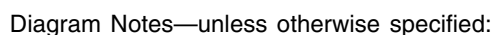


Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 μ F, 35 V	Digi-Key	399-1655-2-ND
C5, C6, C15, C20	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C8, C9, C12, C17, C23	Ceramic capacitor, 33 pF	ATC	100B 330
C7	Capacitor, 0.01 μ F	ATC	200B 103
C10	Ceramic capacitor, 3.3 pF	ATC	100B 3R3
C11	Ceramic capacitor, 1.0 pF	ATC	100B 1R0
C13, C18	Capacitor, 1.0 μ F	ATC	920C105
C14, C16, C19, C21	Tantalum capacitor, 10 μ F, 50 V	Garrett Electronics	TPSE106K050R0400
C22	Ceramic capacitor, 0.3 pF	ATC	100B 0R3
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infinition Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip Resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip Resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3	Chip Resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R7	Chip Resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R6, R8	Chip Resistor 10 ohms	Digi-Key	P10ECT-ND

*Gerber Files for this circuit available on request

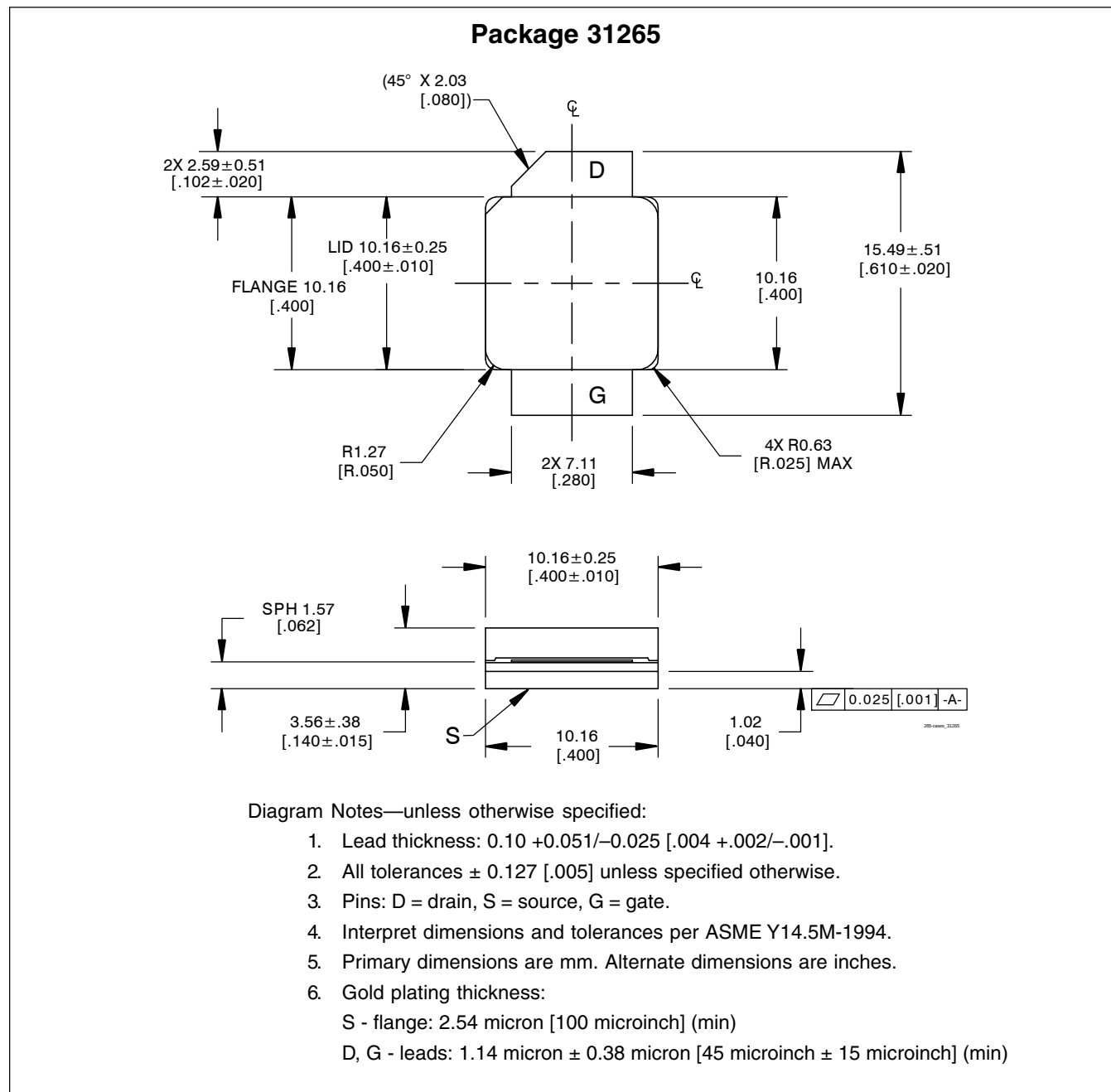
Package 30265



1. Lead thickness: $0.10 +0.051/-0.025$ [$.004 +.002/-0.001$].
2. All tolerances ± 0.127 [$.005$] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
S - flange: 2.54 micron [100 microinch] (min)
D, G - leads: $1.14 \text{ micron} \pm 0.38 \text{ micron}$ [$45 \text{ microinch} \pm 15 \text{ microinch}$] (min)

Rev. 01, 2006-03-16

Package Outline Specifications (cont.)



Find the latest and most complete information about products and packaging at the Infineon Internet page
<http://www.infineon.com/products>

Revision History: 2006-03-16

Data Sheet

Previous Version: none

Page	Subjects (major changes since last revision)

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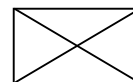
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Edition 2006-03-16

Published by Infineon Technologies AG,

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