# QuadLIU™

## Quad E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications

## PEF 22504 E, PEF 22504 HT, Version 2.1

Communications

Never stop thinking

**Edition 2006-01-25**

**Published by Infineon Technologies AG,
81726 München, Germany**



### Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

### Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

**PEF 22504 E, Quad E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications**

**Revision History: 2006-01-25, Rev. 1.3**

| Previous Version: Preliminary Data Sheet 2005-11-07 | |
|---|---|
| **Chapter, Table** | **Subjects (major changes since last revision)** |
| Chapter 2.3, Chapter 5 | The QuadLIU™ is now available in PG-TQFP-144-17 package also |

**Table of Contents**


| | | |
|---|---|---|
| | **Preface** | 11 |
| **1** | **Introduction** | 12 |
| 1.1 | Features | 13 |
| 1.2 | Logic Symbol | 15 |
| 1.3 | Typical Applications | 16 |
| **2** | **Pin Descriptions** | 17 |
| 2.1 | Ball Diagram P/PG-LBGA-160-1 (top view) | 17 |
| 2.2 | Ball Diagram P/PG-LBGA-160-1 (bottom view) | 17 |
| 2.3 | Pin Diagram P-TQFP-144 | 19 |
| 2.4 | Pin Definitions and Functions | 20 |
| 2.5 | Pin Strapping | 64 |
| **3** | **Functional Description** | 65 |
| 3.1 | Hardware | 65 |
| 3.2 | Software | 66 |
| 3.3 | Functional Overview | 66 |
| 3.4 | Block Diagram | 67 |
| 3.5 | Functional Blocks | 67 |
| 3.5.1 | Asynchronous Micro Controller Interface (Intel or Motorola mode) | 67 |
| 3.5.1.1 | Mixed Byte/Word Access | 68 |
| 3.5.2 | Serial Micro Controller Interfaces | 69 |
| 3.5.2.1 | SCI Interface | 69 |
| 3.5.2.2 | SPI Interface | 73 |
| 3.5.3 | Interrupt Interface | 74 |
| 3.5.4 | Boundary Scan Interface | 76 |
| 3.5.5 | Master Clocking Unit | 78 |
| 3.5.5.1 | PLL (Reset and Configuring) | 79 |
| 3.6 | Line Coding and Framer Interface Modes | 80 |
| 3.6.1 | Bipolar Violation Detection | 81 |
| 3.7 | Receive Path | 83 |
| 3.7.1 | Receive Line Interface | 84 |
| 3.7.2 | Receive Line Coding | 84 |
| 3.7.3 | Receive Line Interface | 84 |
| 3.7.3.1 | “Generic” Receiver Interface | 85 |
| 3.7.3.2 | Receive Line Monitoring Mode (RLM) | 86 |
| 3.7.3.3 | Monitoring Application using RLM | 86 |
| 3.7.3.4 | Redundancy Application using RLM | 87 |
| 3.7.3.5 | General Redundancy Applications | 89 |
| 3.7.4 | Loss-of-Signal Detection | 91 |
| 3.7.5 | Receive Equalization Network | 92 |
| 3.7.6 | Receive Line Attenuation Indication | 92 |
| 3.7.7 | Receive Clock and Data Recovery | 92 |
| 3.7.8 | Receive Jitter Attenuator | 92 |
| 3.7.8.1 | Receive Jitter Attenuation Performance | 95 |
| 3.7.8.2 | Jitter Tolerance (E1) | 96 |
| 3.7.8.3 | Output Jitter | 98 |
| 3.7.8.4 | Output Wander | 98 |
| 3.7.9 | Dual Receive Elastic Buffer | 99 |
| 3.8 | Additional Receiver Functions | 100 |
| 3.8.1 | Error Monitoring and Alarm Handling | 100 |
| 3.8.2 | Automatic Modes | 101 |
| 3.8.3 | Error Counter | 101 |
| 3.8.4 | One-Second Timer | 101 |

**Table of Contents**


3.9 Transmit Path . . . 102
3.9.1 Transmit Line Interface . . . 102
3.9.2 Transmit Clock TCLK . . . 103
3.9.3 Automatic Transmit Clock Switching . . . 103
3.9.4 Transmit Jitter Attenuator . . . 104
3.9.5 Dual Transmit Elastic Buffer . . . 105
3.9.6 Programmable Pulse Shaper and Line Build-Out . . . 105
3.9.6.1 QuadFALC™ V2.1 Compatible Programming with XPM(2:0) Registers . . . 106
3.9.6.2 Programming with TXP(16:1) Registers . . . 107
3.9.7 Transmit Line Monitor . . . 108
3.10 Framer Interface . . . 109
3.11 Test Functions . . . 110
3.11.1 Pseudo-Random Binary Sequence Generation and Monitor . . . 110
3.11.2 In-Band Loop Generation, Detection and Loop Switching . . . 111
3.11.3 Remote Loop . . . 112
3.11.4 Local Loop . . . 113
3.11.5 Payload Loop-Back . . . 113
3.11.6 Alarm Simulation . . . 114
3.12 Multi Function Ports . . . 114

**4 Register Description** . . . 116
4.1 Detailed Control Register Description . . . 116
4.1.1 Control Registers . . . 120
4.2 Detailed Status Register Description . . . 191
4.2.1 Status Registers . . . 194

**5 Package Outlines** . . . 220

**6 Electrical Characteristics** . . . 222
6.1 AC Characteristics . . . 226
6.1.1 Master Clock Timing . . . 226
6.1.2 JTAG Boundary Scan Interface . . . 226
6.1.3 Reset . . . 227
6.1.4 Asynchronous Microprocessor Interface . . . 228
6.1.4.1 Intel Bus Interface Mode . . . 228
6.1.4.2 Motorola Bus Interface Mode . . . 230
6.1.4.3 SCI Interface . . . 232
6.1.4.4 SPI Interface . . . 233
6.1.5 Digital Interface (Framer Interface) . . . 233
6.1.6 Pulse Templates - Transmitter . . . 236
6.1.6.1 Pulse Template E1 . . . 236
6.1.6.2 Pulse Template T1 . . . 237
6.2 Capacitances . . . 239
6.3 Package Characteristics . . . 239
6.4 Test Configuration . . . 240
6.4.1 AC Tests . . . 240
6.4.2 Power Supply Test . . . 240

**7 Operational Description** . . . 243
7.1 Operational Overview . . . 243
7.2 Device Reset . . . 243
7.3 Device Initialization . . . 244
7.4 Device Configuration in E1 Mode . . . 244
7.5 Device Configuration in T1/J1 Mode . . . 245
7.6 Device Configuration for Digital Clock Interface Mode (DCIM) . . . 248

**Table of Contents**

**8 Appendix** . . . . . 249
8.1 Protection Circuitry . . . . . 249
8.2 Application Notes . . . . . 249
8.3 Software Support . . . . . 249
**Terminology** . . . . . 252

## List of Figures

Figure 1 Logic Symbol . . . 15
Figure 2 Typical Multiple Link Application . . . 16
Figure 3 Typical Multiple Repeater Application between line #1 and Line #2 . . . 16
Figure 4 Top View of the Pin Configuration (Ball Layout) P/PG-LBGA-160-1 . . . 17
Figure 5 Bottom View of the Pin Configuration (Ball Layout) P/PG-LBGA-160-1 . . . 18
Figure 6 Pin Configuration P-TQFP-144-8 . . . 19
Figure 7 Single Voltage Supply . . . 65
Figure 8 Dual Voltage Supply . . . 66
Figure 9 Block Diagram . . . 67
Figure 10 SCI Interface Application with Point To Point Connections . . . 70
Figure 11 SCI Interface Application with Multipoint To Multipoint Connection . . . 70
Figure 12 SCI Message Structure of QuadLIU™ . . . 71
Figure 13 Frame Structure of QuadLIU™ SCI Messages . . . 72
Figure 14 Principle of Building Addresses and RSTA bytes in the SCI ACK Message of the QuadLIU™ . . . 72
Figure 15 Read Status Byte (RSTA) byte of the SCI Acknowledge (ACK) . . . 73
Figure 16 SPI Read Operation . . . 74
Figure 17 SPI Write Operation . . . 74
Figure 18 Interrupt Status Registers . . . 75
Figure 19 Block Diagram of Test Access Port and Boundary Scan . . . 77
Figure 20 Flexible Master Clock Unit . . . 79
Figure 21 Behaviour of Bipolar Violation Detection . . . 82
Figure 22 Receive System of one Channel . . . 83
Figure 23 Recovered and Receive Clock Selection . . . 84
Figure 24 General Receiver Configuration with Integrated Resistor and Analog Switches for Receive Impedance Matching . . . 85
Figure 25 Principle of Receive Line Monitoring RLM (shown for one line) . . . 86
Figure 26 Monitoring Application using RLM (shown for one line) . . . 87
Figure 27 Redundancy Application using RLM (shown for one line) . . . 89
Figure 28 General Redundancy Application (shown for one line) . . . 90
Figure 29 Principle of Configuring the DCO-R and DCO-X Corner Frequencies . . . 94
Figure 30 Jitter Attenuation Performance (E1) . . . 96
Figure 31 Jitter Attenuation Performance (T1/J1) . . . 96
Figure 32 Jitter Tolerance (E1) . . . 97
Figure 33 Jitter Tolerance (T1/J1) . . . 97
Figure 34 Output Wander . . . 98
Figure 35 The Receive Elastic Buffer as Circularly Organized Memory . . . 100
Figure 36 Transmit System of one Channel . . . 102
Figure 37 Transmit Line Interface . . . 103
Figure 38 Clocking and Data in Remote Loop Configuration . . . 105
Figure 39 Measurement Configuration for E1 Transmit Pulse Template . . . 106
Figure 40 Measurement Configuration for T1/J1 Transmit Pulse Template . . . 106
Figure 41 Transmit Line Monitor Configuration . . . 108
Figure 42 Framer Interface (shown for one channel) . . . 109
Figure 43 Remote Loop . . . 112
Figure 44 Local Loop . . . 113
Figure 45 Payload Loop . . . 114
Figure 46 P/PG-LBGA-160-1 (Plastic Green Low Profile Ball Grid Array Package) . . . 220
Figure 47 PG-TQFP-144-17 (Plastic Thin Quad Flat Package) . . . 221
Figure 48 MCLK Timing . . . 226
Figure 49 JTAG Boundary Scan Timing . . . 227
Figure 50 Reset Timing . . . 227
Figure 51 Intel Non-Multiplexed Address Timing . . . 228
Figure 52 Intel Multiplexed Address Timing . . . 228

## List of Figures

Figure 53 Intel Read Cycle Timing . . . 229
Figure 54 Intel Write Cycle Timing . . . 229
Figure 55 Motorola Read Cycle Timing . . . 230
Figure 56 Motorola Write Cycle Timing . . . 231
Figure 57 SCI Interface Timing . . . 232
Figure 58 SPI Interface Timing . . . 233
Figure 59 FCLKX Output Timing . . . 234
Figure 60 FCLKR Output Timing . . . 234
Figure 61 SYNC Timing . . . 235
Figure 62 FSC Timing . . . 235
Figure 63 E1 Pulse Shape at Transmitter Output . . . 237
Figure 64 T1 Pulse Shape at the Cross Connect Point . . . 237
Figure 65 Thermal Behavior of Package . . . 239
Figure 66 Input/Output Waveforms for AC Testing . . . 240
Figure 67 Device Configuration for Power Supply Testing . . . 241
Figure 68 Protection Circuitry Examples (shown for one channel) . . . 249
Figure 69 Screen Shot of the “Master Clock Frequency Calculator” . . . 250
Figure 70 Screen Shot of the “External Line Frontend Calculator” . . . 251

## List of Tables

Table 1 I/O Signals for P/PG-LBGA-160-1 . . . 20
Table 2 I/O Signals for P-TQFP-144-8 . . . 36
Table 3 Overview about the Pin Strapping . . . 64
Table 4 Data Bus Access (16-Bit Intel Mode) . . . 68
Table 5 Data Bus Access (16-Bit Motorola Mode) . . . 68
Table 6 Selectable asynchronous Bus and Microprocessor Interface Configuration . . . 68
Table 7 Read Status Byte (RSTA) Byte of the SCI Acknowledge (ACK) . . . 73
Table 8 Definition of Control Bits in Commands (CMD) . . . 73
Table 9 SCI Configuration Register Content . . . 73
Table 10 Interrupt Modes . . . 76
Table 11 TAP Controller Instruction Codes . . . 78
Table 12 Conditions for a PLL Reset . . . 80
Table 13 Line Coding and Framer Interface Modes . . . 80
Table 14 Controlling of the Receive Interface Switches . . . 85
Table 15 Generic Receiver Configuration Example . . . 86
Table 16 External Component Recommendations for Monitoring Applications using RLM . . . 87
Table 17 Tristate Configurations for the RDO, RSIG, SCLKR and RFM Pins . . . 88
Table 18 Configuration for Redundancy Application using RLM, switching with only one board signal . . . 89
Table 19 General (proposed) Configuration for Redundancy Applications, Switching with only one Board Signal 90
Table 20 Configuration for “non-generic” Redundancy Applications, Switching with only one Board Signal 91
Table 21 Configuration for “generic” Redundancy Applications, Switching with only one Board Signal . . . 91
Table 22 Switching in “Generic” Redundancy Application . . . 91
Table 23 Overview DCO-R (DCO-X) Programming . . . 93
Table 24 Clocking Modes of DCO-R . . . 95
Table 25 Output Jitter . . . 98
Table 26 Receive (Transmit) Elastic Buffer Modes . . . 99
Table 27 Summary of Alarm Detection and Release . . . 100
Table 28 Recommended Transmitter Configuration Values . . . 103
Table 29 Recommended Pulse Shaper Programming for T1/J1 with Registers XPM(2:0) (Compatible to QuadFALC V2.1 ) 106
Table 30 Recommended Pulse Shaper Programming for E1 with Registers XPM(2:0) (Compatible to QuadFALC V2.1) 107
Table 31 Recommended Pulse Shaper Programming for T1 with Registers TXP(16:1) . . . 107
Table 32 Recommended Pulse Shaper Programming for E1 with registers TXP(16:1) . . . 108
Table 33 Supported PRBS Polynomials . . . 111
Table 34 Multi Function Port Selection . . . 115
Table 35 Registers Overview . . . 116
Table 36 Registers Access Types . . . 119
Table 37 IMRn Overview . . . 122
Table 38 Interrupt Mask Registers . . . 122
Table 39 CCBn Overview . . . 135
Table 40 Clear Channel Registers . . . 135
Table 41 FLLB Constant Values (Case 1) . . . 144
Table 42 FLLB Constant Values (Case 2) . . . 144
Table 43 LLBP Constant Values (Case 1) . . . 144
Table 44 LLBP Constant Values (Case 2) . . . 144
Table 45 RPC1 Constant Values . . . 160
Table 46 XPC1 Constant Values . . . 161
Table 47 PCn Overview . . . 162
Table 48 Port Configuration Registers . . . 162
Table 49 Clock Mode Register Settings for E1 or T1/J1 . . . 174
Table 50 TXP Overview. . . . 182

## List of Tables

Table 51 Registers Overview . . . 191
Table 52 Registers Access Types . . . 192
Table 53 Alarm Simulation States . . . 200
Table 54 Absolute Maximum Ratings . . . 222
Table 55 Operating Range . . . 223
Table 56 DC Characteristics . . . 223
Table 57 MCLK Timing Parameter Values . . . 226
Table 58 JTAG Boundary Scan Timing Parameter Values . . . 227
Table 59 Reset Timing Parameter Value . . . 228
Table 60 Intel Bus Interface Timing Parameter Values . . . 229
Table 61 Motorola Bus Interface Timing Parameter Values . . . 231
Table 62 SCI Timing Parameter Values . . . 232
Table 63 SPI Timing Parameter Values . . . 233
Table 64 FCLKX Timing Parameter Values . . . 234
Table 65 FCLKR Timing Parameter Values . . . 235
Table 66 SYNC Timing Parameter Values . . . 235
Table 67 FSC Timing Parameter Values . . . 236
Table 68 T1 Pulse Template at Cross Connect Point (T1.102 ) . . . 238
Table 69 Capacitances . . . 239
Table 70 Package Characteristic Values . . . 239
Table 71 AC Test Conditions . . . 240
Table 72 Power Supply Test Conditions E1 . . . 241
Table 73 Power Supply Test Conditions T1/J1 . . . 241
Table 74 Initial Values after Reset . . . 244
Table 75 Configuration Parameters (E1) . . . 245
Table 76 Line Interface Configuration (E1) . . . 245
Table 77 Configuration Parameters (T1/J1) . . . 246
Table 78 Line Interface Configuration (T1/J1) . . . 246
Table 79 Device Configuration for DCIM Mode . . . 248

# Preface

The QuadLIU™ is four channel E1/T1/J1 Line interface Component, it is designed to fulfill all required interfacing between four analog E1/T1/J1 lines and four digital framers.

The digital functions as well as the analog characteristics can be configured either via a flexible microprocessor interface, SPI interface or via a SCI interface.

### Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1**, “Introduction”: Gives a general description of the product and its family, lists the key features, and presents some typical applications.
- **Chapter 2**, “Pin Descriptions”: Lists pin locations with associated signals, categorizes signals according to function, and describe signals.
- **Chapter 3**, “Functional Description”: Describes the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation
- **Chapter 4**, “Registers”: Gives a detailed description of all implemented registers and how to use them in different applications/configurations.
- **Chapter 5**, “Package Outlines”: Shows the mechanical characteristics of the device packages.
- **Chapter 6**, “Electrical Characteristics”: Specifies maximum ratings, DC and AC characteristics.
- **Chapter 7**, “Operational Description”: Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).
- **Chapter 8**, “Appendix”: Gives an example for over voltage protection and information about application notes and tool support.

### Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.231
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETSI ETS 300 233
ETSI TBR12
ETSI TBR13
FCC Part68
H.100
H-MVIP
IEEE 1149.1
TR-TSY-000009
TR-TSY-000253
TR-TSY-000499
ITU-T G.703
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU.T G.733
ITU-T G.775
ITU-T G.823
ITU-T G.824
ITU-T I.431
JT-G703
JT-G704
JT-G706
JT-G33
JT-I431
MIL-Std. 883D
UL 1459

# 1 Introduction

The QuadLIU™ is the latest addition to Infineon's family of sophisticated E1/T1/J1 Line interface Components. This monolithic four channel device is designed to fulfill all required interfacing between four analog E1/T1/J1 lines and four digital framer interfaces for world market telecommunication systems.

The device is supplied in P/PG-LBGA-160-1 package (P/PG-LBGA-160-1 is RoHS compliant) and in a PG-TQFP-144-17 package, and is designed to minimize the number of external components required, so reducing system costs and board space.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards.

Crystal-less jitter attenuation with only one master clock source reduces the amount of required external components.

Equipped with a flexible microprocessor interface, a SCI and a SPI interface, it connects to various control processor environment. A standard boundary scan interface is provided to support board level testing. LBGA device packaging, minimum number of external components and low power consumption lead to reduced overall system costs.

The QuadLIU™ is not hardware and software compatibel to older versions!

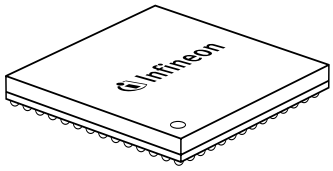
Other members of the FALC® family are the OctalLIU™ supporting eight line interface components on a single chip, the OctalFALC™ and the QuadFALC® E1/T1/J1 Framer And Line interface Components for long-haul and short-haul applications, supporting 8 or 4 channels on a single chip respectively.

# Quad E1/T1/J1 Line Interface Component for Long- and Short-Haul Applications QuadLIU™

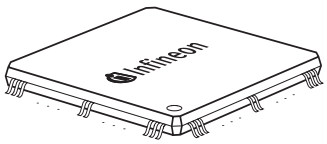
**PEF 22504 E**

**Version 2.1**

## 1.1 Features



P/PG-LBGA-160-1



P-TQFP-144-6, -8, -14

### Line Interface

- High-density, generic interface for all E1/T1/J1 applications
- Four Analog receive and transmit circuits for long-haul and short-haul applications
- E1 or T1/J1 mode selectable
- Data and clock recovery using an integrated digital phase-locked loop
- Clock generator for jitter-free transmit clocks per channel
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) and PUB 62411 are met
- Maximum line attenuation up to -43 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Flexible programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1. 403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22.5 dB (T1/J1)
- Programmable low transmitter output impedances for high transmit return loss and generic E1/T1/J1 applications
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Flexible tristate functions of the digital receive outputs
- Receive line monitor mode
- Integrated switchtable 300 Ω receive resistors for generic E1/T1/J1 applications to meet termination resistance 75/120 Ω for E1, 100 Ω for T1 and 110 Ω for J1
- Integrated multi purpose analog switch at line receive interface to support generic redundancy applications (only supported in P/PG-LBGA-160-1 package)
- Crystal-less wander and jitter attenuation/compensation according to TR 62411, ETS-TBR 12/13, PUB 62411
- Common master clock reference for E1 and T1/J1 with any frequency within 1.02 and 20 MHz
- Power-down function
- Support of automatic protection switching
- Dual-rail or single-rail digital inputs and outputs
- Unipolar CMI for interfacing fiber-optical transmission routes
- Selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- Optional data stream muting upon LOS detection
- Programmable receive slicer threshold

| Type | Package |
|---|---|
| PEF 22504 HT | PG-TQFP-144-17 |
| PEF 22504 E | P/PG-LBGA-160-1 |

- Local loop, digital loop and remote loop for diagnostic purposes. Automatic remote loop switching is possible with In-Band and Out-Band loop codes
- Low power device, two power supply voltages 1.8 V and 3.3 V or a single supply of 3.3 V
- Alarm and performance monitoring per second 16-bit counter for code violations, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS)
- Single-bit defect insertion
- Flexible clock frequency for receiver and transmitter
- Dual elastic stores for both, receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Programmable In-band loop code detection and generation (TR62411)
- Local loop back, payload loop back land remote loop back capabilities (TR54016)
- Flexible pseudo-random binary sequence generator and monitor

**Microprocessor Interfaces**

- Asynchronous 8/16-bit microprocessor bus interface (Intel or Motorola type selectable)
- SPI bus interface
- SCI bus interface
- All registers directly accessible
- Multiplexed and non-multiplexed address bus operations on asynchronous 8/16-bit microprocessor bus interface
- Hard/software reset options
- Extended interrupt capabilities
- One-second timer (internal or external timing reference)

**General**

- Boundary scan standard IEEE 1149.1
- PG-TQFP-144-17P-BGA-160-1 package
- Temperature range from -40 to +85 °C
- 1.8 V and 3.3 V power supply or single 3.3 V power supply
- Typical power consumption 140 mW per channel

**Applications**

- Wireless base stations
- E1/T1/J1 ATM gateways, multiplexer
- E1/T1/J1 **C**hannel & **D**ata **S**ervice **U**nits (CSU, DSU)
- E1/T1/J1 Internet access equipment
- LAN/WAN router
- ISDN PRI, PABX
- **D**igital **A**ccess **C**rossconnect **S**ystems (DACS)
- SONET/SDH add/drop multiplexer

## 1.2 Logic Symbol

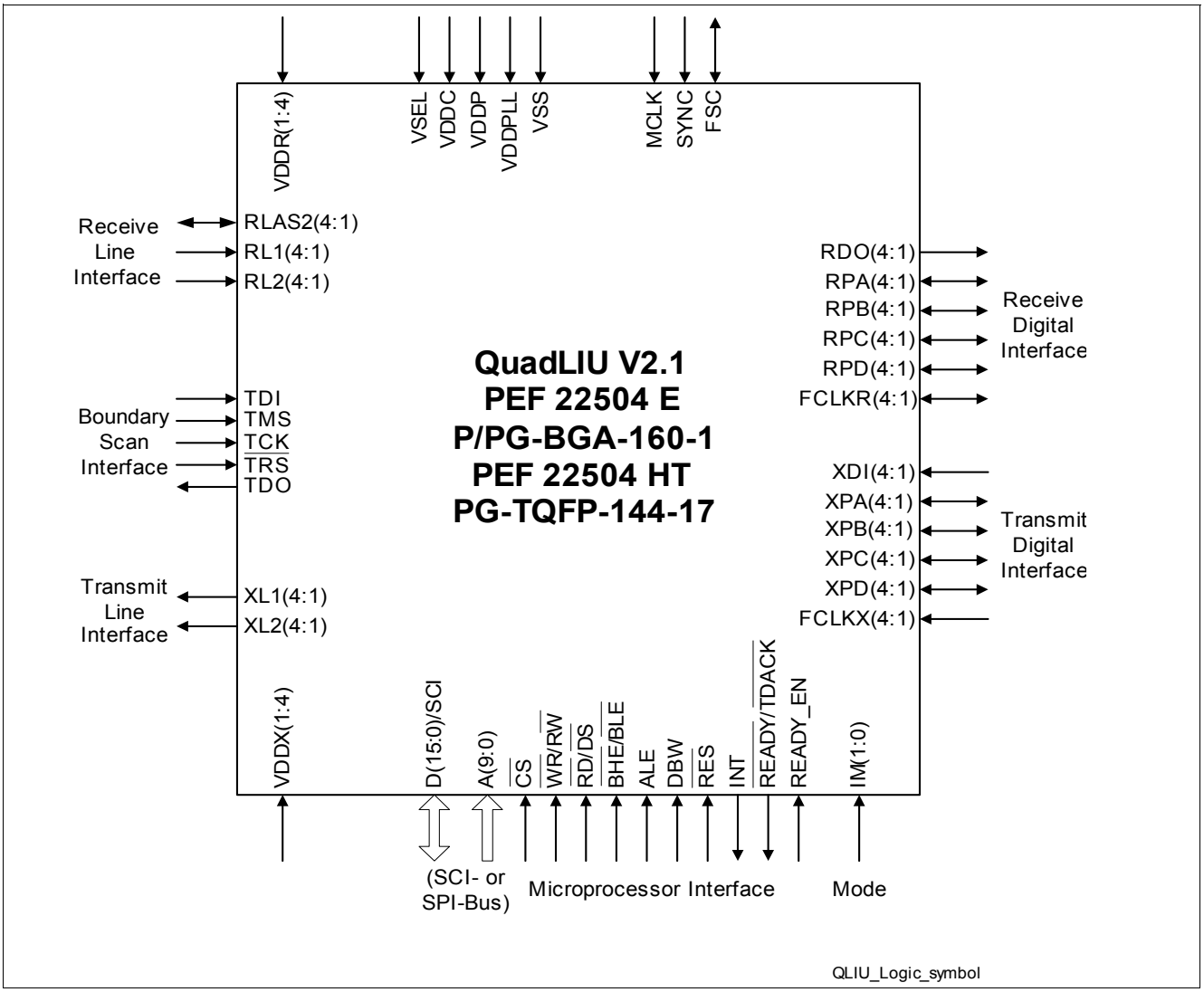



**Figure 1 Logic Symbol**

## 1.3 Typical Applications

**Figure 2** shows a multiple link application, **Figure 3** a repeater application using the QuadLIU™.

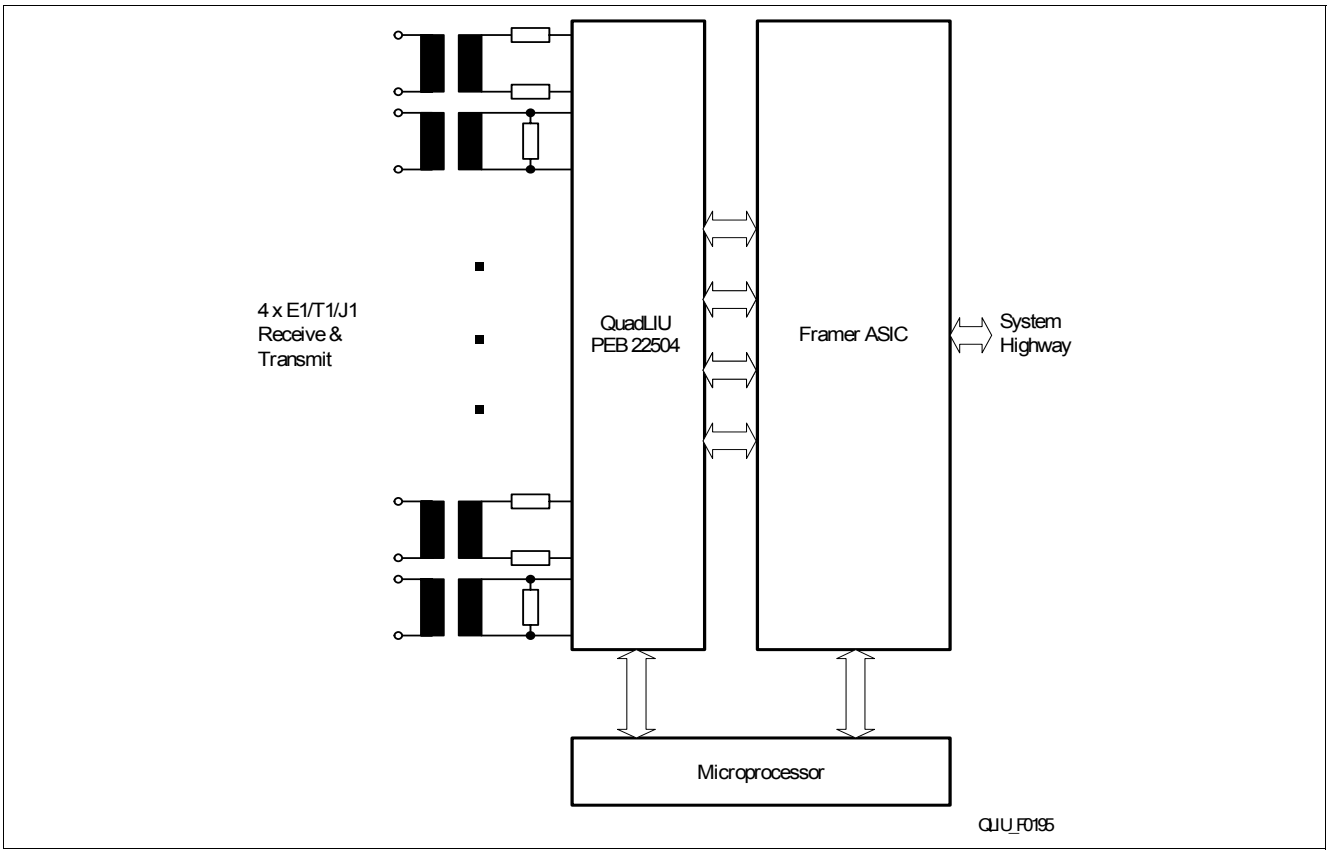



**Figure 2 Typical Multiple Link Application**

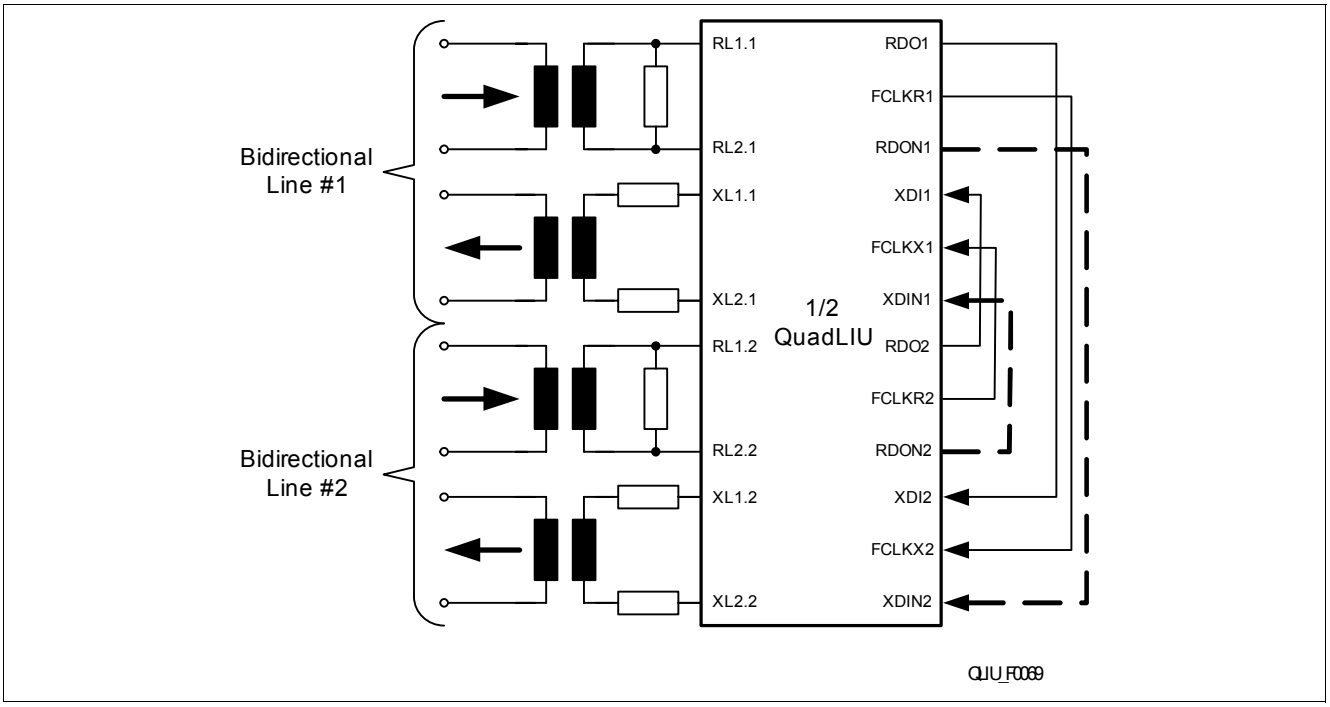



**Figure 3 Typical Multiple Repeater Application between line #1 and Line #2**

# 2 Pin Descriptions

In this chapter the function and placement of all pins are described.

## 2.1 Ball Diagram P/PG-LBGA-160-1 (top view)

**Figure 4** shows the ball layout of the QuadLIU™ in a P/PG-LBGA-160-1 package.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | ● | XL1_2 | XL2_2 | VDDR | VSSR | RL1_2 | RL2_2 | RL2_1 | RL1_1 | VSSR | VDDR | XL2_1 | XL1_1 | |
| B | VSSX (RLAS22 | VSSX | XDI1 | MCLK | XPC2 | $\overline{TRS}$ | XPD2 | VDD | XPA1 | VDDP | XPB1 | D15 | VSSX | VSSX (RLAS21) |
| C | VDDX | VDDX | FCLKX 1 | TCK | VSSP | VDDP | XPA2 | XPB2 | XPC1 | VDDC | TDO | D14 | VDDX | VDDX |
| D | RPC1 | RPA1 | RPB1 | RPD1 | TMS | VSEL | RCLK2 | VSS | XPD1 | RCLK1 | TDI | D12 | D13 | D11 |
| E | RDO1 | FCLKR 1 | VDD | VDD | | | | | | | VSS | VDD | VDD | D10 |
| F | RDO2 | VSS | FCLKR 2 | RPA2 | | | | | | | D9 | D7 | D8 | D6 |
| G | RPC2 | RPB2 | FCLKX 2 | RPD2 | | | VSS | VSS | | | D5 | $\overline{READY}$ /DTACK (VDD) | D4 | D3 |
| H | XDI3 | FCLKX 3 | XDI2 | RPA3 | | | VSS | VSS | | | D2 | READY EN (VSS) | D0 | D1 |
| J | RPB3 | RPD3 | RPC3 | FCLKR 3 | | | | | | | $\overline{BHE}$/ $\overline{BLE}$ | $\overline{CS}$ | $\overline{WR}$/ $\overline{RW}$ | $\overline{RD}$/$\overline{DS}$ |
| K | RDO3 | IM1 (VSS) | VDD | RDO4 | | | | | | | A9 | A8 | A6 | A7 |
| L | FCLKR 4 | RPB4 | RPA4 | DBW | RCLK3 | XPA3 | XPD3 | XPB4 | ALE | SEC/ FSC | A5 | A3 | A2 | A4 |
| M | VDDX | VDDX | RPC4 | INT | $\overline{RES}$ | FCLKX 4 | VDD | VDD | XPD4 | VDDC | IM | A1 | VDDX | VDDX |
| N | VSSX (RLAS23 | VSSX | RPD4 | XDI4 | XPC3 | SYNC | XPB3 | XPA4 | RCLK4 | VSS | XPC4 | A0 | VSSX | VSSX (RLAS24) |
| P | | XL1_3 | XL2_3 | VDDR | VSSR | RL1_3 | RL2_3 | RL2_4 | RL1_4 | VSSR | VDDR | XL2_4 | XL1_4 | |

QUIU_F0213_2

**Figure 4 Top View of the Pin Configuration (Ball Layout) P/PG-LBGA-160-1**

## 2.2 Ball Diagram P/PG-LBGA-160-1 (bottom view)

**Figure 4** shows the ball layout of the QuadLIU™ in a P/PG-LBGA-160-1 package.

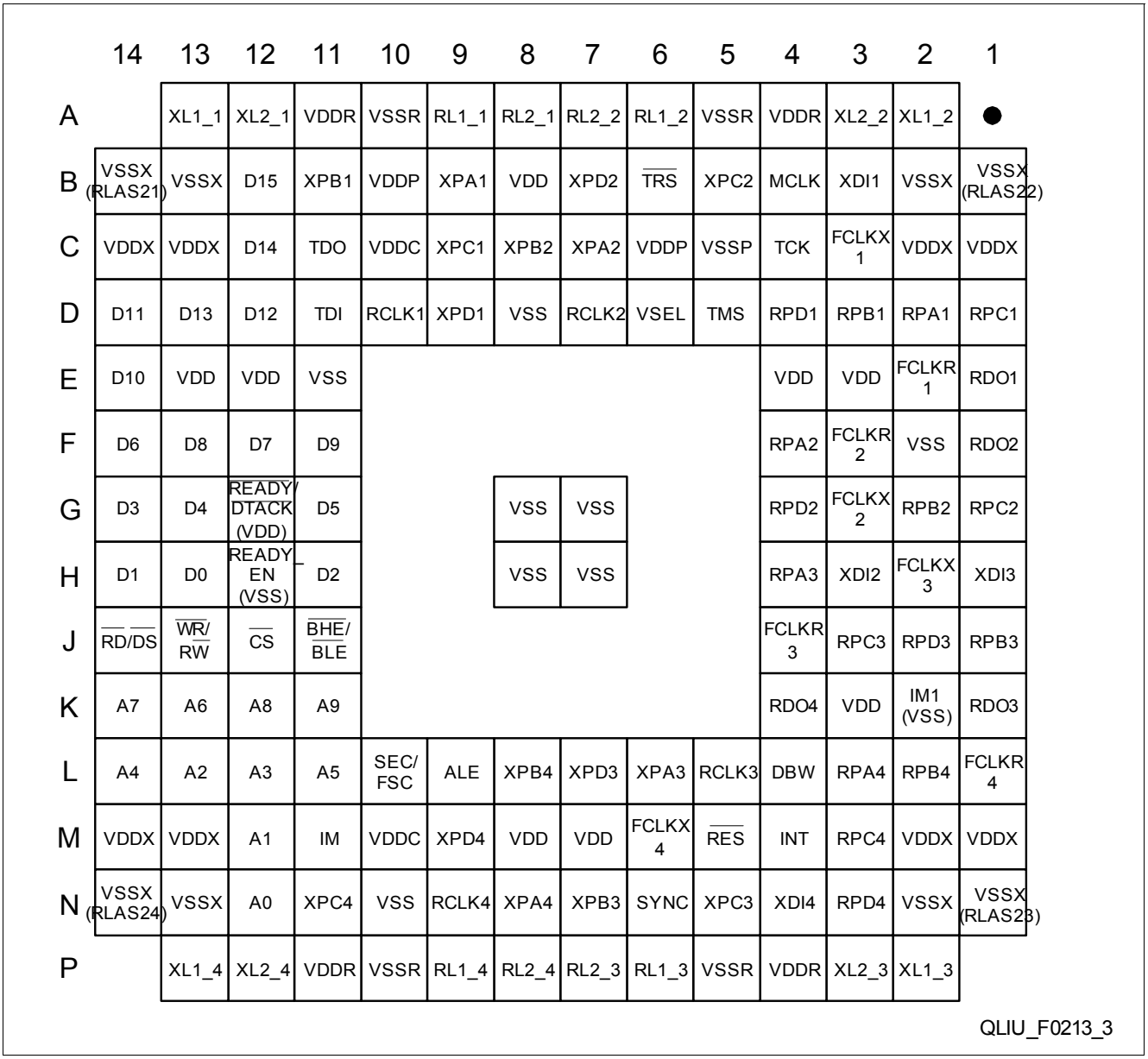



**Figure 5 Bottom View of the Pin Configuration (Ball Layout) P/PG-LBGA-160-1**

## 2.3 Pin Diagram P-TQFP-144

**Figure 6** shows the pin diagram of the QuadLIU™.

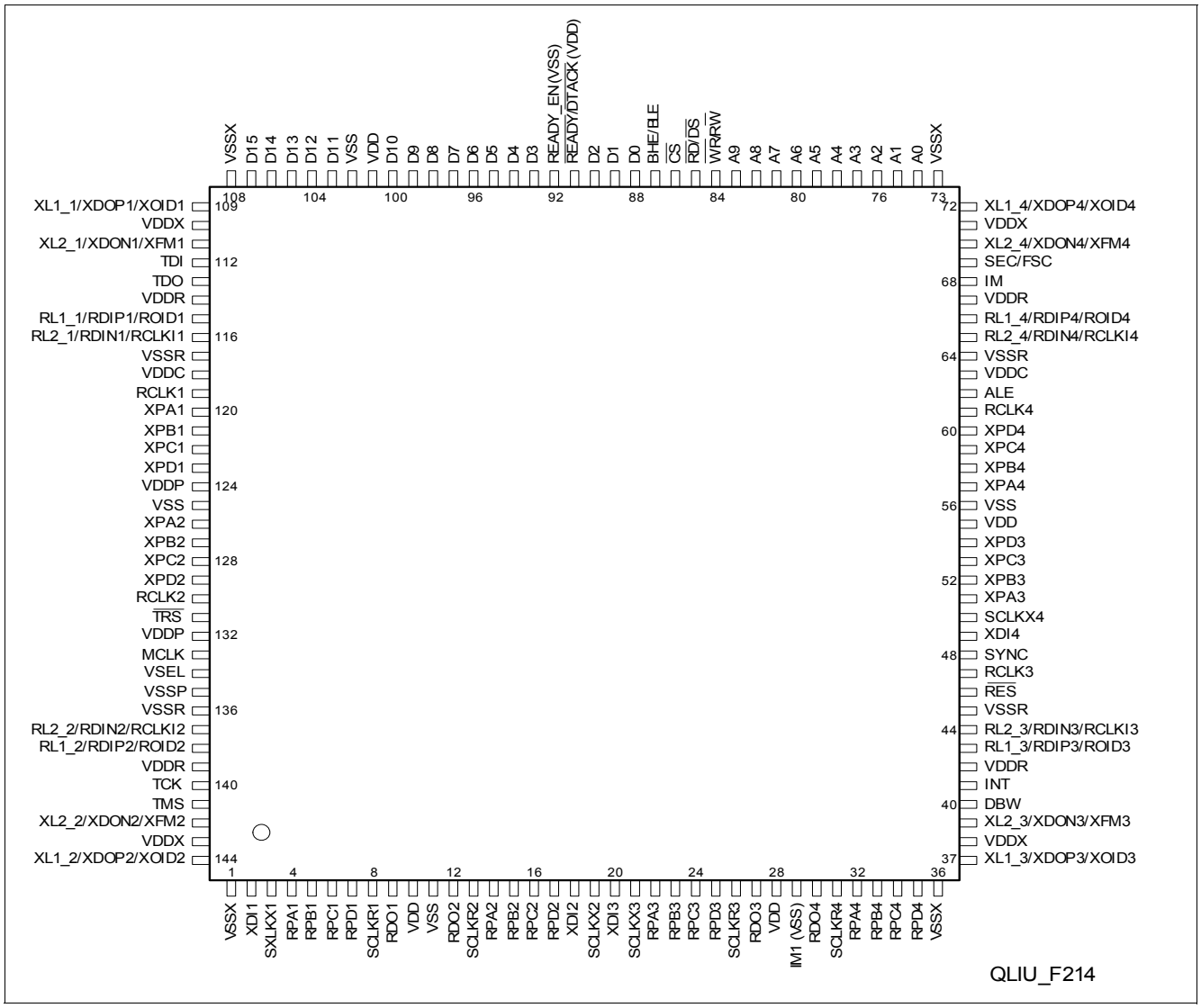



**Figure 6 Pin Configuration P-TQFP-144-8**

## 2.4 Pin Definitions and Functions

The following table describes all pins and their functions:

**Table 1 I/O Signals for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Operation Mode Selection and Device Initialization** | | | | |
| M5 | $\overline{\text{RES}}$ | I | PU | **Hardware Reset**<br>Active low |
| K2 | IM1 | I | PD | **Interface Mode Selection**<br>$'00_B'$: Asynchronous Intel Bus Mode.<br>$'01_B'$: Asynchronous Motorola Bus Mode<br>$'10_B'$: SPI Bus Slave Mode.<br>$'11_B'$: SCI Bus Slave Mode |
| M11 | IM0 | I | PU | |
| **Asynchronous and Serial Micro Controller Interfaces** | | | | |
| K11 | A9 | I | PU | **Address Bus Line 9 (MSB)** |
| K12 | A8 | I | PU | **Address Bus Line 8** |
| K14 | A7 | I | PU | **Address Bus Line 7** |
| K13 | A6 | I | PU | **Address Bus Line 6** |
| L11 | A5 | I | PU | **Address Bus Line 5** |
| | A5 | I | PU | **SCI source address bit 5 (MSB)**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| L14 | A4 | I | PU | **Address Bus Line 4** |
| | A4 | I | PU | **SCI source address bit 4**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| L12 | A3 | I | PU | **Address Bus Line 3** |
| | A3 | I | PU | **SCI source address bit 3**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| L13 | A2 | I | PU | **Address Bus Line 2** |
| | A2 | I | PU | **SCI source address bit 2**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| M12 | A1 | I | PU | **Address Bus Line 1** |
| | A1 | I | PU | **SCI source address bit 1**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| N12 | A0 | I | PU | **Address Bus Line 0** |
| | A0 | I | PU | **SCI source address bit 0 (LSB)**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| B12 | D15 | IO | PU | **Data Bus Line 15** |
| | PLL10 | I | PU | **PLL programming bit 10**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| C12 | D14 | IO | PU | **Data Bus Line 14** |
| | PLL9 | I | PU | **PLL programming bit 9**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| D13 | D13 | IO | PU | **Data Bus Line 13** |
| | PLL8 | I | PU | **PLL programming bit 8**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| D12 | D12 | IO | PU | **Data Bus Line 12** |
| | PLL7 | I | PU | **PLL programming bit 7**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| D14 | D11 | IO | PU | **Data Bus Line 11** |
| | PLL6 | I | PU | **PLL programming bit 6**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| E14 | D10 | IO | PU | **Data Bus Line 10** |
| | PLL5 | I | PU | **PLL programming bit 5**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| F11 | D9 | IO | PU | **Data Bus Line 9** |
| | PLL4 | I | PU | **PLL programming bit 4**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| F13 | D8 | IO | PU | **Data Bus Line 8** |
| | PLL3 | I | PU | **PLL programming bit 3**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| F12 | D7 | IO | PU | **Data Bus Line 7** |
| | PLL2 | I | PU | **PLL programming bit 2**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| F14 | D6 | IO | PU | **Data Bus Line 6** |
| | PLL1 | I | PU | **PLL programming bit 1**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| G11 | D5 | IO | PU | **Data Bus Line 5** |
| | PLL0 | I | PU | **PLL programming bit 0**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = ´1Xb´. |
| G13 | D4 | IO | PU | **Data Bus Line 4** |
| G14 | D3 | IO | PU | **Data Bus Line 3** |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| H11 | D2 | IO | PU | **Data Bus Line 2** |
| | SCI_CLK | I | – | **SCI Bus Clock**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| | SCLK | I | – | **SPI Bus Clock**<br>Only used if SPI interface mode is selected by IM(1:0) = ´10b´. |
| H14 | D1 | IO | PU | **Data Bus Line 1** |
| | SCI_RXD | I | PU | **SCI Bus Serial Data In**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| | SDI | I | PU | **SPI Serial Data In**<br>Only used if SPI interface mode is selected by IM(1:0) = ´10b´. |
| H13 | D0 | IO | PU | **Data Bus Line 0** |
| | SCI_TXD | I | PP or oD | **SCI Bus Serial Data Out**<br>Only used if SCI interface mode is selected by IM(1:0) = ´11b´. |
| | SDO | I | PU | **SPI Bus Serial Data Out**<br>Only used if SPI interface mode is selected by IM(1:0) = ´10b´. |
| L9 | ALE | I | PU | **Address Latch Enable**<br>A high on this line indicates an address on an external multiplexed address/data bus. The address information provided on lines A(10:0) is internally latched with the falling edge of ALE. This function allows the QuadLIU™ to be connected to a multiplexed address/data bus without the need for external latches. In this case, pins A(7:0) must be connected to the data bus pins externally. In case of demultiplexed mode this pin can be connected directly to VDD or can be left open. |
| J14 | $\overline{RD}$ | I | PU | **Read Enable**<br>Intel bus mode.<br>This signal indicates a read operation. When the QuadLIU™ is selected via CS, the RD signal enables the bus drivers to output data from an internal register addressed by A(10:0) to the Data Bus. |
| | $\overline{DS}$ | I | PU | **Data Strobe**<br>Motorola bus mode.<br>This pin serves as input to control read/write operations. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| J13 | $\overline{WR}$ | I | PU | **Write Enable**<br>Intel bus mode.<br>This signal indicates a write operation. When CS is active the QuadLIU™ loads an internal register with data provided on the data bus. |
| | $\overline{RW}$ | I | PU | **Read/Write Select**<br>Motorola bus mode.<br>This signal distinguishes between read and write operation. |
| L4 | DBW | I | PU | **Data Bus Width select**<br>Bus interface mode<br>A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{BHE}$/$\overline{BLE}$. |
| J11 | $\overline{BHE}$ | I | PU | **Bus High Enable**<br>Intel bus mode.<br>If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus D(15:8). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open. |
| | $\overline{BLE}$ | I | PU | **Bus Low Enable**<br>Motorola bus mode.<br>If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus D(7:0). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open. |
| J12 | $\overline{CS}$ | I | PU | **Chip Select**<br>Low active chip select. |
| M4 | INT | O | – | **Interrupt Request**<br>Interrupt request.<br>INT serves as general interrupt request for all interrupt sources. These interrupt sources can be masked via registers IMR(7:0). Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR(7:0). Output characteristics (push-pull active low/high, open drain) are determined by programming register IPC. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| G12 | $\overline{\text{READY}}$ | O | oD (PU) | **Data Ready** oD output only if activated by READY_EN = $1_B$ and if Intel bus mode is selected. If not activated (READY_EN = $0_B$) the pull-up resistor is active. Asynchronous handshake signal to indicate successful read or write cycle. |
| | $\overline{\text{DTACK}}$ | O | oD (PU) | **Data Acknowledge** oD output only if activated by READY_EN = $1_B$ and if motorola bus mode is selected. If not activated (READY_EN = $0_B$) the pull-up resistor is active. Asynchronous handshake signal to indicate successful read or write cycle. |
| H12 | READY_EN | I | PD | **Ready Enable** Activates the oD functionality of $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$. $0_B$: $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is not activated (only pull-up resistor is active). Pin $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ can be connected to VDD. $1_B$: $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is an active oD output |
| **Separate Analog Switches (only supported in BGA package)** | | | | |
| B14 | RLAS21 | IO (analog) | – | **Analog Switch Connector port 1** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1) |
| B1 | RLAS22 | IO (analog) | – | **Analog Switch Connector port 2** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1) |
| N1 | RLAS23 | IO (analog) | – | **Analog Switch Connector port 3** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1) |
| N14 | RLAS24 | IO (analog) | – | **Analog Switch Connector port 4** Can be connected to VSSX if analog switch is not used (HW compatibel to QuadFALC® v2.1) |
| **Line Interface Receiver** | | | | |
| A9 | RL1.1 | I (analog) | – | **Line Receiver input 1, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | ROID1 | I | – | **Receive Optical Interface Data, port 1** Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´$01_b$´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required. |
| A8 | RL2.1 | I (analog) | – | **Line Receiver input 2, port 1** Analog input from the external transformer. Selected if LIM1.DRS is cleared. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| A6 | RL1.2 | I (analog) | – | **Line Receiver input 1, port 1**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | ROID2 | I | – | **Receive Optical Interface Data, port 2**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´$01_b$´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required. |
| A7 | RL2.2 | I (analog) | – | **Line Receiver input 2, port 2**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| P6 | RL1.3 | I (analog) | – | **Line Receiver input 1, port 3**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | ROID3 | I | – | **Receive Optical Interface Data, port 3**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´$01_b$´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required. |
| P7 | RL2.3 | I (analog) | – | **Line Receiver input 2, port 3**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| P9 | RL1.4 | I (analog) | – | **Line Receiver input 1, port 4**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | ROID4 | I | – | **Receive Optical Interface Data, port 4**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). If CMI coding is selected (MR0.RC(1:0) = ´$01_b$´ and LIM0.DRS = ´1´), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required. |
| P8 | RL2.4 | I (analog) | – | **Line Receiver input 2, port 4**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Line Interface Transmitter** | | | | |
| A13 | XL1.1 | O (analog) | – | **Transmit Line 1, port 1**<br>Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| | XOID1 | O | – | **Transmit Optical Interface Data, port 1**<br>Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK2 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| A12 | XL2.1 | O (analog) | – | **Transmit Line 2, port 1**<br>Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| A2 | XL1.2 | O (analog) | – | **Transmit Line 1, port 2**<br>Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| | XOID2 | O | – | **Transmit Optical Interface Data, port 2**<br>Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK2 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| A3 | XL2.2 | O (analog) | – | **Transmit Line 2, port 2**<br>Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| P2 | XL1.3 | O (analog) | – | **Transmit Line 1, port 3** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| | XOID3 | O | – | **Transmit Optical Interface Data, port 3** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK3 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| P3 | XL2.3 | O (analog) | – | **Transmit Line 2, port 3** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| P13 | XL1.4 | O (analog) | – | **Transmit Line 1, port 4** Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| | XOID4 | O | – | **Transmit Optical Interface Data, port 4** Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK4 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and MR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| P12 | XL2.4 | O (analog) | – | **Transmit Line 2, port 4** Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit MR0.XC1 is set and XPM2.XLT is cleared. |
| **Clock Signals** | | | | |
| B4 | MCLK | I | – | **Master Clock** A reference clock of better than ±32 ppm accuracy in the range of 1.02 to 20 MHz must be provided on this pin. The QuadLIU™ internally derives all necessary clocks from this master (see registers GCM(6:1)). |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| N6 | SYNC | I | PU | **Clock Synchronization of DCO-R**<br>If a clock is detected on pin SYNC the DCO-R circuitry of the QuadLIU™ synchronizes to this 1.544/2.048 MHz clock (see LIM0.MAS, CMR1.DCS and CMR2.DCF). Additionally, in master mode the QuadLIU™ is able to synchronize to an 8 kHz reference clock (IPC.SSYF = ´1´). If not connected, an internal pull-up transistor ensures high input level. |
| L10 | FSC | O | – | **8 kHz Frame Synchronization**<br>The optionally synchronization pulse is active high or low for one 2.048/1.544 MHz cycle (pulse width = 488 ns for E1and 648 ns or T1/J1). |
| D10, D7, L5, N9 | RCLK(1:4) | O | – | **Receive Clock Out, ports 1 to 4**<br>After reset this ports are configured to be internally pulled up weakly. Setting of register bit PC5.CRPR will switch this ports to be active outputs. |
| **Digital (Framer) Interface Receive** | | | | |
| E1 | RDO1 | O | – | **Receive Data Out, port 1**<br>Received data at RL1, RL2 is sent to RDOP, RDON. Clocking of data is done with the rising or falling edge of RCLK. |
| E2 | FCLKR1 | I/O | PU | **Framer Data Clock Receive, port 1**<br>Input if PC5.CSRP = ´0´, output if PC5.CSRP = ´1´. |
| F1 | RDO2 | O | – | **Receive Data Out, port 2**<br>See description of RDOP1. |
| F3 | FCLKR2 | I/O | PU | **Framer Data Clock Receive, port 2**<br>See description of FCLKR1. |
| K1 | RDO3 | O | – | **Receive Data Out, port 3**<br>See description of RDOP1. |
| J4 | FCLKR3 | I/O | PU | **Framer Data Clock Receive, port 3**<br>See description of FCLKR1. |
| K4 | RDO4 | O | – | **Receive Data Out, port 4**<br>See description of RDOP1. |
| L1 | FCLKR4 | I/O | PU | **Framer Data Clock Receive, port 4**<br>See description of FCLKR1. |
| **Digital (Framer) Interface Transmit** | | | | |
| B3 | XDI1 | I | – | **Transmit Data In, port 1**<br>NRZ transmit data received from the framer. Latching of data is done with rising or falling transitions of FCLKX1 according to bit DIC3.RESX. |
| C3 | FCLKX1 | I/O | – | **Framer Data Clock Transmit, port 1** |
| H3 | XDI2 | I | – | **Transmit Data In, port 2**<br>See description of XDI1. |
| G3 | FCLKX2 | I/O | – | **Framer Data Clock Transmit, port 2**<br>See description of FCLKX1. |
| H1 | XDI3 | I | – | **Transmit Data In, port 3**<br>See description of XDI1. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| H2 | FCLKX3 | I/O | – | **Framer Data Clock Transmit, port 3**<br>See description of FCLKX1. |
| N4 | XDI4 | I | – | **Transmit Data In, port 4**<br>See description of XDI1. |
| M6 | FCLKX4 | I/O | – | **Framer Data Clock Transmit, port 4**<br>See description of FCLKX1. |
| **Multi Function Pins** | | | | |
| D2 | RPA1 | I/O | PU/– | **Receive Multifunction Pins A to D, port 1**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level.<br>An input function must not be selected twice or more. Selectable pin functions are described below. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| D2 | RPA1 | I | PU | **Receive Line Termination (RLT), port 1**<br>PC(1:4).RPC(3:0) = ´$1000_b$´.<br>These input function controls together with LIM0.RTRS the analog switch of the receive line interface: A logical equivalence is build out of LIM0.RTRS and RLT. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| D2 | RPA1 | I | PU | **General Purpose Input (GPI), port 1**<br>PC(1:4).RPC(3:0) = ´$1001_b$.<br>The pin is set to input. The state of this input is reflected in the register bits MFPI.RPA, MFPI.RPB or MFPI.RPC respectively. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| D2 | RPA1 | O | – | **General Purpose Output High (GPOH), port 1**<br>PC(1:4).RPC(3:0) = ´$1010_b$´.<br>The pin level is set fix to high level. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| D2 | RPA1 | O | – | **General Purpose Output Low (GPOL), port 1**<br>PC(1:4).RPC(3:0) = ´$1011_b$´.<br>The pin level is set fix to low-level. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| D2 | RPA1 | O | – | **Loss of Signal Indication Output (LOS), port 1**<br>PC(1:3).RPC(3:0) = ´$1100_b$.<br>The output reflects the Loss of Signal status as readable in LSR0.LOS. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| D2 | RPA1 | O | – | **Receive Data Output Negative (RDON), port 1**<br>PC(1:4).RPC(3:0) = ´1110$_b$´.<br>Receive data output negative for dual rail mode on digital (framer) interface (LIM3.DRR = ´1´).<br>Bipolar violation output for single rail mode on digital (framer) interface (LIM3.DRR = ´0´). |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| D2 | RPA1 | O | – | **Receive Clock Output (RCLK), port 1**<br>PC(1:4).RPC(3:0) = ´1111$_b$´. Default setting after reset<br>Receive clock output RCLK. After reset RCLK is configured to be internally pulled up weekly. By setting of PC5.CRP RCLK is an active output.<br>RCLK source and frequency selection is made by CMR1.RS(1:0) if COMP = ´1´ or by CMR4.RS(2:0) if COMP = ´0´. |
| D3 | RPB1 | | | |
| D1 | RPC1 | | | |
| D4 | RPD1 | | | |
| F4 | RPA2 | I/O | PU/– | **Receive Multifunction Pins A to D, port 2**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level.<br>An input function must not be selected twice or more.<br>Selectable pin functions as described for port 1. |
| G2 | RPB2 | | | |
| G1 | RPC2 | | | |
| G4 | RPD2 | | | |
| H4 | RPA3 | I/O | PU/– | **Receive Multifunction Pins A to D, port 3**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level.<br>An input function must not be selected twice or more.<br>Selectable pin functions as described for port 1. |
| J1 | RPB3 | | | |
| J3 | RPC3 | | | |
| J2 | RPD3 | | | |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| L3 | RPA4 | I/O | PU/– | **Receive Multifunction Pins A to D, port 4**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESR latching/transmission of data is done with the rising or falling edge of FCLKR. If not connected, an internal pull-up transistor ensures a high input level.<br>An input function must not be selected twice or more.<br>Selectable pin functions as described for port 1. |
| L2 | RPB4 | | | |
| M3 | RPC4 | | | |
| N3 | RPD4 | | | |
| B9 | XPA1 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 1**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level.<br>Each input function (TCLK, XDIN, XLT or $\overline{XLT}$) may only be selected once.<br>Selectable pin functions are described below. |
| B11 | XPB1 | | | |
| C9 | XPC1 | | | |
| D9 | XPD1 | | | |
| B9 | XPA1 | I | PU | **Transmit Clock (TCLK), port 1**<br>PC(1:4).XPC(3:0) = ´$0011_b$´<br>A 2.048/8.192 MHz (E1) or 1.544/6.176 MHz (T1/J1) clock has to be sourced by the framer if the internally generated transmit clock (generated by DCO-X) shall not be used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 (E1) or 1.544 MHz (T1/J1). |
| B11 | XPB1 | | | |
| C9 | XPC1 | | | |
| D9 | XPD1 | | | |
| B9 | XPA1 | O | – | **Transmit Clock (XCLK), port 1**<br>PC(1:4).XPC(3:0) = ´$0111_b$´<br>Transmit line clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1) derived from FCLKX/R, RCLK or generated internally by DCO circuitries. |
| B11 | XPB1 | | | |
| C9 | XPC1 | | | |
| D9 | XPD1 | | | |
| B9 | XPA1 | I | PU | **Transmit Line Tristate (XLT), port 1**<br>PC(1:4).XPC(3:0) = ´$1000_b$´<br>A high level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically OR´d with register bit XPM2.XLT. |
| B11 | XPB1 | | | |
| C9 | XPC1 | | | |
| D9 | XPD1 | | | |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| B9<br>B11<br>C9<br>D9 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **General Purpose Input (GPI), port 1**<br>PC(1:4).XPC(3:0) = ´$1001_b$.<br>The pin is set to input. The state of this input is reflected in the register bits MFPI.XPA, MFPI.XPB or MFPI.XPC respectively. |
| B9<br>B11<br>C9<br>D9 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **General Purpose Output High (GPOH), port 1**<br>PC(1:4).XPC(3:0) = ´$1010_b$´.<br>The pin level is set fix to high level. |
| B9<br>B11<br>C9<br>D9 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **General Purpose Output Low (GPOL), port 1**<br>PC(1:4).XPC(3:0) = ´$1011_b$´.<br>The pin level is set fix to high level. |
| B9<br>B11<br>C9<br>D9 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Transmit Data Input Negative (XDIN), port 1**<br>PC(1:2).XPC(3:0) = ´$1101_b$.<br>Transmit data input negative for dual rail mode on framer side (LIM3.DRX = ´1´). Depending on bit DIC3.RESX latching of data is done with the rising or falling edge of FCLKX. |
| B9<br>B11<br>C9<br>D9 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Transmit Line Tristate, low active, port 1**<br>**$\overline{\text{XLT}}$** : PC(1:4).XPC(3:0) = ´$1110_b$´.<br>A low level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically OR´d with register bit XPM2.XLT. |
| C7<br>C8<br>B5<br>B7 | XPA2,<br>XPB2<br>XPC2<br>XPD2 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 2**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level.<br>Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once.<br>Selectable pin functions as described for port 1. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| L6<br>N7 | XPA3<br>XPB3 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 3**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level.<br>Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once.<br>Selectable pin functions as described for port 1. |
| N5 | XPC3 | | | |
| L7 | XPD3 | | | |
| N8<br>L8 | XPA4<br>XPB4 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 4**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the framer interface or from the framer to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit DIC3.RESX latching/transmission of data is done with the rising or falling edge of FCLKX. If not connected, an internal pull-up transistor ensures a high input level.<br>Each input function (TCLK, XDIN, XLT or $\overline{\text{XLT}}$) may only be selected once.<br>Selectable pin functions as described for port 1. |
| N11 | XPC4 | | | |
| M9 | XPD4 | | | |
| **Power Supply** | | | | |
| A11 | $V_{DDR1}$ | S | – | **Positive Power Supply**<br>For the analog receiver 1 (3.3 V) |
| A4 | $V_{DDR2}$ | S | – | **Positive Power Supply**<br>For the analog receiver 2 (3.3 V) |
| P4 | $V_{DDR3}$ | S | – | **Positive Power Supply**<br>For the analog receiver 3 (3.3 V) |
| P11 | $V_{DDR4}$ | S | – | **Positive Power Supply**<br>For the analog receiver 4 (3.3 V) |
| C13, C14 | $V_{DDX1}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 1 |
| C1, C2 | $V_{DDX2}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 2 |
| M1, M2 | $V_{DDX3}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 3 |
| M13, M14 | $V_{DDX4}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 4 |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| M10, C10 | $V_{DDC}$ | S | – | **Positive Power Supply**<br>For the digital core (1.8 V).<br>These pins can either be positive power supply input or output, dependent on VSEL:<br>VSEL connected to $V_{SS}$ : 1.8 V power supply inputs, require decoupling.<br>VSEL connected to $V_{DD}$: 1.8 V outputs for decoupling to $V_{SS}$ . **These pins must not be used to supply external devices.** |
| B10<br>C6 | $V_{DDPLL}$ | S | – | **Positive Power Supply**<br>For the analog PLL |
| E3, E4<br>K3<br>M7, M8<br>E12, E13, B8 | $V_{DDP}$ | S | – | **Positive Power Supply**<br>For the digital pads(3.3 V)<br>For correct operation, all $V_{DDP}$ pins have to be connected to positive power supply. |
| P5<br>P10<br>A10<br>A5<br>B2<br>N2<br>N13<br>B13<br>F2<br>N10<br>E11<br>D8<br>G7<br>G8<br>H7<br>H8<br>C5 | $V_{SS}$ | S | – | **Power Ground**<br>Common for all sub circuits (0 V)<br>For correct operation, all $V_{SS}$ pins have to be connected to ground. |
| B1, B14, N1, N14 | $V_{SS}$ | S | – | **Only for P/PG-LBGA-160-1 Package**<br>Either usage as power ground or usage as connectors RLAS2 of the analog switches |
| **Power Supply Configuration** | | | | |
| D6 | $V_{SEL}$ | I + PU | – | **Voltage Select**<br>Enables the internal voltage regulator for 3.3 V only operation mode if connected to $V_{DD}$ (recommended) or left open.<br>Disables the internal voltage regulator for dual power supply mode (1.8 V and 3.3 V) if connected to $V_{SS}$. |

**Table 1 I/O Signals** (cont'd)**for P/PG-LBGA-160-1**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Boundary Scan/Joint Test Access Group (JTAG)** | | | | |
| B6 | $\overline{\text{TRS}}$ | I | PD | **Test Reset**<br>For Boundary Scan (active low). If not connected, an internal pull-down transistor ensures low input level. |
| D11 | TDI | | PU | **Test Data Input**<br>For Boundary Scan.<br>If not connected an internal pull-up transistor ensures high input level. |
| D5 | TMS | | | **Test Mode Select**<br>For Boundary Scan.<br>If not connected an internal pull-up transistor ensures high input level. |
| C4 | TCK | | | **Test Clock**<br>For Boundary Scan.<br>If not connected an internal pull-up transistor ensures high input level. |
| C11 | TDO | O | – | **Test Data Output**<br>For Boundary Scan |

*Note: oD = open drain output PU = input or input/output comprising an internal pull-up device To override the internal pull-up by an external pull-down, a resistor value of 22 kΩ is recommended. The pull-up devices are activated during reset, this means their state is undefined until the reset signal has been applied. Unused pins containing pull-ups can be left open.*

**Table 2 I/O Signals for P-TQFP-144-8**

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Operation Mode Selection and Device Initialization** | | | | |
| 46 | $\overline{\text{RES}}$ | I | PU | **Hardware Reset**<br>Active low. |
| 29 | IM1 | I | PD | **Interface Mode Selection**<br>$00_B$ Asynchronous Intel Bus Mode<br>$01_B$ Asynchronous Motorola Bus Mode<br>$10_B$ SPI Bus Slave Mode<br>$11_B$ SCI Bus Slave Mode |
| 68 | IM | I | PU | |
| **Asynchronous and Serial Microcontroller Interfaces** | | | | |
| 83 | A9 | I | PU | **Address Bus Line 9 (MSB)** |
| 82 | A8 | I | PU | **Address Bus Line 8** |
| 81 | A7 | I | PU | **Address Bus Line 7** |
| 80 | A6 | I | PU | **Address Bus Line 6** |
| 79 | A5 | I | PU | **Address Bus Line 5** |
| | A5 | I | PU | **SCI Source address bit 5 (MSB)**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| 78 | A4 | I | PU | **Address Bus Line 4** |
| | A4 | I | PU | **SCI Source Address bit 4**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| 77 | A3 | I | PU | **Address Bus Line 3** |
| | A3 | I | PU | **SCI Source Address bit 3**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| 76 | A2 | I | PU | **Address Bus Line 2** |
| | A2 | I | PU | **SCI Source Address bit 2**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| 75 | A1 | I | PU | **Address Bus Line 1** |
| | A1 | I | PU | **SCI Source Address bit 1**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| 74 | A0 | I | PU | **Address Bus Line 0** |
| | A0 | I | PU | **SCI Source Address Bit 0 (LSB)**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| 107 | D15 | IO | PU | **Data Bus Line 15** |
| | PLL10 | I | PU | **PLL Programming Bit 10**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 106 | D14 | IO | PU | **Data Bus Line 14** |
| | PLL9 | I | PU | **PLL Programming Bit 9**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 105 | D13 | IO | PU | **Data Bus Line 13** |
| | PLL8 | I | PU | **PLL programming bit 8**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 104 | D12 | IO | PU | **Data Bus Line 12** |
| | PLL7 | I | PU | **PLL programming bit 7**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 103 | D11 | IO | PU | **Data Bus Line 11** |
| | PLL6 | I | PU | **PLL programming bit 6**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 100 | D10 | IO | PU | **Data Bus Line 10** |
| | PLL5 | I | PU | **PLL programming bit 5**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 99 | D9 | IO | PU | **Data Bus Line 9** |
| | PLL4 | I | PU | **PLL programming bit 4**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 98 | D8 | IO | PU | **Data Bus Line 8** |
| | PLL3 | I | PU | **PLL programming bit 3**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 97 | D7 | IO | PU | **Data Bus Line 7** |
| | PLL2 | I | PU | **PLL programming bit 2**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 96 | D6 | IO | PU | **Data Bus Line 6** |
| | PLL1 | I | PU | **PLL programming bit 1**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 95 | D5 | IO | PU | **Data Bus Line 5** |
| | PLL0 | I | PU | **PLL programming bit 0**<br>Only used if SCI or SPI interface mode is selected by IM(1:0) = $1X_B$. |
| 94 | D4 | IO | PU | **Data Bus Line 4** |
| 93 | D3 | IO | PU | **Data Bus Line 3** |
| 90 | D2 | IO | PU | **Data Bus Line 2** |
| | SCI_CLK | I | – | **SCI Bus Clock**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| | SCLK | I | – | **SPI Bus Clock**<br>Only used if SPI interface mode is selected by IM(1:0) = $10_B$. |
| 89 | D1 | IO | PU | **Data Bus Line 1** |
| | SCI_RXD | I | PU | **SCI Bus Serial Data In**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| | SDI | I | PU | **SPI Serial Data In**<br>Only used if SPI interface mode is selected by IM(1:0) = $10_B$. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 88 | D0 | IO | PU | **Data Bus Line 0** |
| | SCI_TXD | I | PP or oD | **SCI Bus Serial Data Out**<br>Only used if SCI interface mode is selected by IM(1:0) = $11_B$. |
| | SDO | I | PU | **SPI Bus Serial Data Out**<br>Only used if SPI interface mode is selected by IM(1:0) = $10_B$. |
| 62 | ALE | I | PU | **Address Latch Enable**<br>A high on this line indicates an address on an external multiplexed address/data bus. The address information provided on A(9:0) is internally latched with the falling edge of ALE. This function allows the QuadLIU™ to be connected to a multiplexed address/data bus without the need for external latches. In this case, pins A(7:0) must be connected to the data bus pins externally. In case of demultiplexed mode this pin can be connected directly to VDD or can be left open. |
| 85 | $\overline{RD}$ | I | PU | **Read Enable**<br>Intel bus mode.<br>This signal indicates a read operation. When the QuadLIU™ is selected via CS, the RD signal enables the bus drivers to output data from an internal register addressed by A(10:0) to the Data Bus. |
| | $\overline{DS}$ | I | PU | **Data Strobe**<br>Motorola bus mode.<br>This pin serves as input to control read/write operations. |
| 84 | $\overline{WR}$ | I | PU | **Write Enable**<br>Intel bus mode.<br>This signal indicates a write operation. When CS is active the QuadLIU™ loads an internal register with data provided on the data bus. |
| | $\overline{RW}$ | I | PU | **Read/Write Select**<br>Motorola bus mode.<br>This signal distinguishes between read and write operation. |
| 40 | DBW | I | PU | **Data Bus Width select**<br>Bus interface mode<br>A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{BHE}$/$\overline{BLE}$. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 87 | $\overline{\text{BHE}}$ | I | PU | **Bus High Enable**<br>Intel bus mode.<br>If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus D(15:8). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open. |
| | $\overline{\text{BLE}}$ | I | PU | **Bus Low Enable**<br>Motorola bus mode.<br>If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus D(7:0). In 8-bit bus interface mode this signal has no function and should be tied to VDD or left open. |
| 86 | $\overline{\text{CS}}$ | I | PU | **Chip Select**<br>Low active chip select. |
| 41 | INT | O | – | **Interrupt Request**<br>INT serves as general interrupt request for all interrupt sources. These interrupt sources can be masked via registers IMR(7:0). Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR(7:0).<br>Output characteristics (push-pull active low/high, open drain) are determined by programming register IPC. |
| 91 | $\overline{\text{READY}}$ | O | oD (PU) | **Data Ready**<br>oD output only if activated by READY_EN = $1_B$ and if Intel bus mode is selected. If not activated (READY_EN = $0_B$) the pull-up resistor is active.<br>Asynchronous handshake signal to indicate successful read or write cycle. |
| | $\overline{\text{DTACK}}$ | O | oD (PU) | **Data Acknowledge**<br>oD output only if activated by READY_EN = $1_B$ and if motorola bus mode is selected. If not activated (READY_EN = $0_B$) the pull-up resistor is active.<br>Asynchronous handshake signal to indicate successful read or write cycle. |
| 92 | READY_EN | I | PD | **Ready Enable**<br>Activates the oD functionality of $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$.<br>$0_B$: $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is not activated (only pull-up resistor is active). Pin $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ can be connected to VDD.<br>$1_B$: $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is an active oD output |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Line Interface Receiver** | | | | |
| 115 | RL1.1 | I (analog) | – | **Line Receiver input 1, port 1**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIP1 | I | – | **Receive Data Input Positive, port 1**<br>Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | ROID1 | I | – | **Receive Optical Interface Data, port 1**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = $01_B$), an internal DPLL recovers clock an data; no clock signal on RCLKI1 is required. |
| 116 | RL2.1 | I (analog) | – | **Line Receiver input 2, port 1**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIN1 | I | – | **Receive Data Input Negative, port 1**<br>Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%.<br>The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | RCLKI1 | I | – | **Receive Clock Input, port 1**<br>Receive clock input for the optical interface if LIM1.DRS is set and<br>FMR0.RC(1:0) = $00_B$.<br>Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1).<br>RCLKI1 is ignored if CMI coding is selected. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 138 | RL1.2 | I (analog) | – | **Line Receiver input 1, port 2**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIP2 | I | – | **Receive Data Input Positive, port 2**<br>Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | ROID2 | I | – | **Receive Optical Interface Data, port 2**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = $01_B$), an internal DPLL recovers clock an data; no clock signal on RCLKI2 is required. |
| 137 | RL2.2 | I (analog) | – | **Line Receiver input 2, port 2**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIN2 | I | – | **Receive Data Input Negative, port 2**<br>Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%.<br>The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | RCLKI2 | I | – | **Receive Clock Input, port 2**<br>Receive clock input for the optical interface if LIM1.DRS is set and<br>FMR0.RC(1:0) = $00_B$.<br>Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1).<br>RCLKI2 is ignored if CMI coding is selected. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 43 | RL1.3 | I (analog) | – | **Line Receiver input 1, port 3**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIP3 | I | – | **Receive Data Input Positive, port 3**<br>Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | ROID3 | I | – | **Receive Optical Interface Data, port 3**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = $01_B$), an internal DPLL recovers clock an data; no clock signal on RCLKI3 is required. |
| 44 | RL2.3 | I (analog) | – | **Line Receiver input 2, port 3**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIN3 | I | – | **Receive Data Input Negative, port 3**<br>Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%.<br>The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | RCLKI3 | I | – | **Receive Clock Input, port 3**<br>Receive clock input for the optical interface if LIM1.DRS is set and<br>FMR0.RC(1:0) = $00_B$.<br>Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1).<br>RCLKI3 is ignored if CMI coding is selected. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 66 | RL1.4 | I (analog) | – | **Line Receiver input 1, port 4**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIP4 | I | – | **Receive Data Input Positive, port 4**<br>Digital input for received dual-rail PCM(+) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%. The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | ROID4 | I | – | **Receive Optical Interface Data, port 4**<br>Unipolar data received from a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The single-rail mode is selected if LIM1.DRS is set and FMR0.RC1 is cleared. If CMI coding is selected (FMR0.RC(1:0) = $01_B$), an internal DPLL recovers clock an data; no clock signal on RCLKI4 is required. |
| 65 | RL2.4 | I (analog) | – | **Line Receiver input 2, port 4**<br>Analog input from the external transformer. Selected if LIM1.DRS is cleared. |
| | RDIN4 | I | – | **Receive Data Input Negative, port 4**<br>Input for received dual-rail PCM(-) route signal which is latched with the internally recovered receive route clock. An internal DPLL extracts the receive route clock from the incoming data pulses. The duty cycle of the received signal has to be close to 50%.<br>The dual-rail mode is selected if LIM1.DRS and FMR0.RC1 are set. Input polarity is selected by bit RC0.RDIS (after reset: active low), line coding is selected by FMR0.RC(1:0). |
| | RCLKI4 | I | – | **Receive Clock Input, port 4**<br>Receive clock input for the optical interface if LIM1.DRS is set and<br>FMR0.RC(1:0) = $00_B$.<br>Clock frequency: 2.048 MHz (E1) or 1.544 MHz (T1/J1).<br>RCLKI4 is ignored if CMI coding is selected. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 109 | XL1.1 | O (analog) | – | **Transmit Line 1, port 1**<br>Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDOP1 | O | – | **Transmit Data Output Positive, port 1**<br>This digital output for transmitted dual-rail PCM(+) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked with positive transitions of XCLK1 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| | XOID1 | O | – | **Transmit Optical Interface Data, port 1**<br>Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK1. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 111 | XL2.1 | O (analog) | – | **Transmit Line 2, port 1**<br>Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDON1 | O | – | **Transmit Data Output Negative, port 1**<br>This digital output for transmitted dual-rail PCM(-) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked on positive transitions of XCLK1 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low).<br>The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. |
| | XFM1 | O | – | **Transmit Frame Marker, port 1**<br>This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = $1_B$ and FMR0.XC1 = $0_B$). Data is clocked on positive transitions of XCLK1. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.<br>In remote loop configuration the XFM1 marker is not valid. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 144 | XL1.2 | O (analog) | – | **Transmit Line 1, port 2**<br>Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDOP2 | O | – | **Transmit Data Output Positive, port 2**<br>This digital output for transmitted dual-rail PCM(+) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked with positive transitions of XCLK2 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| | XOID2 | O | – | **Transmit Optical Interface Data, port 2**<br>Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK2 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 142 | XL2.2 | O (analog) | – | **Transmit Line 2, port 2**<br>Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDON2 | O | – | **Transmit Data Output Negative, port 2**<br>This digital output for transmitted dual-rail PCM(-) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked on positive transitions of XCLK2 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low).<br>The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. |
| | XFM2 | O | – | **Transmit Frame Marker, port 2**<br>This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = $1_B$ and FMR0.XC1 = $0_B$). Data is clocked on positive transitions of XCLK2. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.<br>In remote loop configuration the XFM2 marker is not valid. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 37 | XL1.3 | O (analog) | – | **Transmit Line 1, port 3**<br>Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDOP3 | O | – | **Transmit Data Output Positive, port 3**<br>This digital output for transmitted dual-rail PCM(+) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked with positive transitions of XCLK3 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| | XOID3 | O | – | **Transmit Optical Interface Data, port 3**<br>Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK3 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 39 | XL2.3 | O (analog) | – | **Transmit Line 2, port 3**<br>Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDON3 | O | – | **Transmit Data Output Negative, port 3**<br>This digital output for transmitted dual-rail PCM(-) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked on positive transitions of XCLK3 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low).<br>The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. |
| | XFM3 | O | – | **Transmit Frame Marker, port 3**<br>This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = 1 and FMR0.XC1 = $0_B$). Data is clocked on positive transitions of XCLK3. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.<br>In remote loop configuration the XFM3 marker is not valid. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 72 | XL1.4 | O (analog) | – | **Transmit Line 1, port 4**<br>Analog output to the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDOP4 | O | – | **Transmit Data Output Positive, port 4**<br>This digital output for transmitted dual-rail PCM(+) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked with positive transitions of XCLK4 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |
| | XOID4 | O | – | **Transmit Optical Interface Data, port 4**<br>Unipolar data sent to a fiber-optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which is clocked on the positive transitions of XCLK. Clocking of data in NRZ code is done with 100% duty cycle. Data in CMI code is shifted out with 50% or 100% duty cycle on both transitions of XCLK4 according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single-rail mode is selected if LIM1.DRS is set and FMR0.XC1 is cleared. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT is cleared. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 70 | XL2.4 | O (analog) | – | **Transmit Line 2, port 4**<br>Analog output for the external transformer. Selected if LIM1.DRS is cleared. After reset this pin is in high-impedance state until bit FMR0.XC1 is set and XPM2.XLT is cleared. |
| | XDON4 | O | – | **Transmit Data Output Negative, port 4**<br>This digital output for transmitted dual-rail PCM(-) route signals can provide<br>• Half bauded signals with 50% duty cycle (LIM0.XFB = $0_B$) or<br>• Full bauded signals with 100% duty cycle (LIM0.XFB = $1_B$)<br>The data is clocked on positive transitions of XCLK4 in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low).<br>The dual-rail mode is selected if LIM1.DRS and FMR0.XC1 are set. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared. |
| | XFM4 | O | – | **Transmit Frame Marker, port 4**<br>This digital output marks the first bit of every frame transmitted on port XDOP. This function is only available in the optical interface mode (LIM1.DRS = $1_B$ and FMR0.XC1 = $0_B$). Data is clocked on positive transitions of XCLK4. After reset this pin is in high-impedance state until register LIM1.DRS is set and XPM2.XLT cleared.<br>In remote loop configuration the XFM4 marker is not valid. |
| **Clock Signals** | | | | |
| 133 | MCLK | I | – | **Master Clock**<br>A reference clock of better than ±32 ppm accuracy in the range of 1.02 to 20 MHz must be provided on this pin. The QuadLIU™ internally derives all necessary clocks from this master<br>(see registers GCM(8:1)). |
| 48 | SYNC | I | PU | **Clock Synchronization of DCO-R**<br>If a clock is detected on pin SYNC the DCO-R circuitry of the OctalFALCTM synchronizes to this 1.544/2.048 MHz clock (see LIM0.MAS, CMR1.DCS and CMR2.DCF). Additionally, in master mode the OctalFALCTM is able to synchronize to an 8 kHz reference clock (IPC.SSYF = $1_B$). If not connected, an internal pullup transistor ensures high input level. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 69 | SEC | I | PU | **One-Second Timer Input**<br>A pulse with logical high level for at least two 2.048 MHz cycles triggers the internal one-second timer. After reset this pin is configured to be an input. If not connected, an internal pullup transistor ensures high input level (see register GPC1). |
| | SEC | O | – | **One-Second Timer Output**<br>Activated high every second for two 2.048 MHz clock cycles. |
| | FSC | O | – | **8 kHz Frame Synchronization**<br>The optionally synchronization pulse is active high or low for one 2.048/1.544 MHz cycle (pulse width = 488 ns for E1and 648 ns or T1/J1). |
| 119, 130, 47, 61 | RCLK(1:4) | O | – | **Receive Clock Out, ports 1 to 4**<br>After reset this ports are configured to be internally pulled up weakly. Setting of register bit PC5.CRP will switch this ports to be active outputs. |
| **System Interface Receive** | | | | |
| 9 | RDO1 | O | – | **Receive Data Out, port 1**<br>Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR1, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR1 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0.<br>If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO1 is cleared (driven to low level, not tristate). |
| 8 | SCLKR1 | I/O | PU | **System Clock Receive, port 1**<br>Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface.<br>If SCLKR1 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. |
| 12 | RDO2 | O | – | **Receive Data Out, port 2**<br>Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR2, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR2 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0.<br>If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO2 is cleared (driven to low level, not tristate). |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 13 | SCLKR2 | I/O | PU | **System Clock Receive, port 2**<br>Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface.<br>If SCLKR2 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. |
| 27 | RDO3 | O | – | **Receive Data Out, port 3**<br>Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR3, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR3 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0.<br>If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO3 is cleared (driven to low level, not tristate). |
| 26 | SCLKR3 | I/O | PU | **System Clock Receive, port 3**<br>Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface.<br>If SCLKR3 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. |
| 30 | RDO4 | O | – | **Receive Data Out, port 4**<br>Received data that is sent to the system highway. Clocking of data is done with the rising or falling edge (SIC3.RESR) of SCLKR4, if the receive elastic store is bypassed. The delay between the beginning of time slot 0 and the initial edge of SCLKR4 (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0.<br>If received data is shifted out with higher (more than 2.048/1.544 Mbit/s) data rates, the active channel phase is defined by bits SIC2.SICS(2:0). During inactive channel phases RDO4 is cleared (driven to low level, not tristate). |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 31 | SCLKR4 | I/O | PU | **System Clock Receive, port 4**<br>Working clock for the receive system interface with a frequency of 16.384/8.192/4.096/2.048 MHz in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. If the receive elastic store is bypassed, the clock supplied on this pin is ignored, because RCLK is used to clock the receive system interface.<br>If SCLKR4 is configured to be an output, the internal working clock of the receive system interface sourced by DCO-R or RCLK is output. |
| **System Interface Transmit** | | | | |
| 2 | XDI1 | I | – | **Transmit Data In, port 1**<br>Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX1 according to bit SIC3.RESX.<br>The delay between the beginning of time slot 0 and the initial edge of SCLKX1 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0).<br>In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0). |
| 3 | SCLKX1 | I | PU | **System Clock Transmit, port 1**<br>Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. |
| 18 | XDI2 | I | – | **Transmit Data In, port 2**<br>Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX2 according to bit SIC3.RESX.<br>The delay between the beginning of time slot 0 and the initial edge of SCLKX2 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0).<br>In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0). |
| 19 | SCLKX2 | I | PU | **System Clock Transmit, port 2**<br>Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 20 | XDI3 | I | – | **Transmit Data In, port 3**<br>Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX3 according to bit SIC3.RESX.<br>The delay between the beginning of time slot 0 and the initial edge of SCLKX3 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0).<br>In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0). |
| 21 | SCLKX3 | I | PU | **System Clock Transmit, port 3**<br>Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. |
| 49 | XDI4 | I | – | **Transmit Data In, port 4**<br>Transmit data received from the system highway. Latching of data is done with rising or falling transitions of SCLKX4 according to bit SIC3.RESX.<br>The delay between the beginning of time slot 0 and the initial edge of SCLKX4 (after $\overline{\text{SYPX}}$ goes active) is determined by the registers XC(1:0).<br>In higher (more than 1.544/2.048 Mbit/s) data rates sampling of data is defined by bits SIC2.SICS(2:0). |
| 50 | SCLKX4 | I | PU | **System Clock Transmit, port 4**<br>Working clock for the transmit system interface with a frequency of 16.384/8.192/4.096/2.048 in E1 mode and 16.384/8.192/4.096/2.048 MHz (SIC2.SSC2 = $0_B$) or 12.352/6.176/3.088/1.544 MHz (SIC2.SSC2 = $1_B$) in T1/J1 mode. |
| **Multi Function Pins** | | | | |
| 4 | RPA1 | I/O | PU/– | **Receive Multifunction Pins A to D, port 1**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level.<br>The input function must not be selected twice or more.<br>Selectable pin functions are described below. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 4<br>5<br>6<br>7 | RPA1<br>RPB1<br>RPC1<br>RPD1 | I | PU | **Synchronous Pulse Receive, port 1**<br>$\overline{SYPR}$, PC(1:4).RPC(3:0) = $0000_B$<br>Together with the values of registers RC(1:0) this signal defines the beginning of time slot 0 on system highway port RDO.<br>Only one multifunction port may be selected as $\overline{SYPR}$ input. After reset, $\overline{SYPR}$ of port A is used, the other lines are ignored.<br>In system interface multiplex mode, $\overline{SYPR}$ has to be provided at port RPA1 for four or all four channels dependent if 4:1 or 8:1 multiplex mode is selected. $\overline{SYPR}$ defines the beginning of the time slot 0 on port RDO/RSIG.<br>The pulse cycle is an integer multiple of 125 µs. |
| 4<br>5<br>6<br>7 | RPA1<br>RPB1<br>RPC1<br>RPD1 | O | – | **Receive Frame Marker (RFM), port 1**<br>PC(1:4).RPC(3:0) = $0001_B$<br>**CMR2.IRSP = $0_B$**<br>The receive frame marker can be active high for a 2.048 MHz (E1) or 1.544 MHz (T1/J1) period during any bit position of the current frame. It is clocked off with the rising or falling edge of SCLKR or RCLK, depending on SIC3.RESR. Offset programming is done by using registers RC(1:0).<br>**CMR2.IRSP = $1_B$**<br>Frame synchronization pulse generated by the DCO-R circuitry internally. This pulse is active low for a 2.048 MHz (E1) or 1.544 MHz (T1/J1) period. |
| 4<br>5<br>6<br>7 | RPA1<br>RPB1<br>RPC1<br>RPD1 | O | – | **Receive Multiframe Begin (RMFB), port 1**<br>PC(1:4).RPC(3:0) = $0010_B$<br>In E1 mode RMFB marks the beginning of every received multiframe (RDO). Optionally the time slot 16 CAS multiframe begin can be marked (SIC3.CASMF). Active high for one 2.048 MHz period.<br>In T1/J1 mode the function depends on bit XC0.MFBS:<br>**MFBS = $1_B$**<br>RMFB marks the beginning of every received multiframe (RDO).<br>**MFBS = $0_B$**<br>RMFB marks the beginning of every received superframe. Additional pulses are provided every 12 frames when using ESF/F24 or F72 format. |
| 4<br>5<br>6<br>7 | RPA1<br>RPB1<br>RPC1<br>RPD1 | O | – | **Receive Signaling Marker (RSIGM), port 1**<br>PC(1:4).RPC(3:0) = $0011_B$<br>E1: Marks the time slots which are defined by register RTR(4:1) of every received frame on port RDO.<br>T1/J1: Marks the time slots which are defined by register RTR(4:1) of every received frame on port RDO, if CAS-BR is not used.<br>When using the CAS-BR signaling scheme, the robbed bit of each channel every sixth frames is marked, if CAS-BR is enabled by XC0.BRM = $1_B$. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 4 | RPA1 | O | – | **Receive Signaling Data (RSIG), port 1**<br>PC(1:4).RPC(3:0) = $0100_B$<br>The received CAS signaling data is sourced by this pin. Time slots on RSIG correlate directly to the time slot assignment on RDO.<br>In 4:1 system interface multiplex mode four received signaing data streams are merged into a single data stream respectively which is transmitted on RPB1 (bit- or byte-interleaved). |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | O | – | **Data Link Bit Receive (DLR), port 1**<br>PC(1:4).RPC(3:0) = $0101_B$<br>E1: Marks the Sa(8:4)-bits within the data stream on RDO. The Sa(8:4)-bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0.<br>T1/J1: Marks the DL-bit position within the data stream on RDO. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | O | – | **Freeze signaling (FREEZE), port 1**<br>PC(1:4).RPC(3:0) = $0110_B$<br>The freeze signaling status is set active high by detecting a loss of signal alarm, a loss of CAS frame alignment or a receive slip (positive or negative). It will stay high for at least one complete multiframe after the alarm disappears. Setting SIC2.FFS enforces a high on pin FREEZE. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | O | – | **Frame Synchronous Pulse (RFSP) , port 1**<br>$\overline{\text{RFSP}}$, PC(1:4).RPC(3:0) = $0111_B$<br>Active low framing pulse derived from the received PCM route signal (line side, RCLK). During loss of synchronization (bit FRS0.LFA = $1_B$), this pulse is suppressed (not influenced during alarm simulation).<br>Pulse frequency: 8 kHz<br>Pulse width: 488 ns (E1) or 648 ns (T1/J1). |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | I | PU | **Receive Line Termination (RLT), port 1**<br>PC(1:4).RPC(3:0) = $1000_B$. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | I | PU | **General Purpose Input (GPI), port 1**<br>PC(1:4).RPC(3:0) = $1001_B$.<br>The pin is set to input. The state of this input is reflected in the register bits MFPI.RPA, MFPI.RPB or MFPI.RPC respectively. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | O | – | **General Purpose Output High (GPOH), port 1**<br>PC(1:4).RPC(3:0) = $1010_B$.<br>The pin level is set fix to high level. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 4 | RPA1 | O | – | **General Purpose Output Low (GPOL), port 1**<br>PC(1:4).RPC(3:0) = $1011_B$.<br>The pin level is set fix to low level. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | O | – | **Loss of Signal Indication Output (LOS), port 1**<br>PC(1:4).RPC(3:0) = $1100_B$.<br>The output reflects the Loss of Signal status as readable in FRS0.LOS. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | I | PU | **Receive TDM System Interface Tristate (RTDMT), port 1**<br>PC(1:4).RPC(3:0) = $1101_B$.<br>Controlling of tristate mode for RDO, RSIG,SCLKR and RFM. The RTDMT value is logically exored with the register bit SIC3.RRTRI. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 4 | RPA1 | O | – | **Receive Clock Output (RCLK), port 1**<br>PC(1:4).RPC(3:0) = $1111_B$. Default setting after reset Receive clock output RCLK. After reset RCLK is configured to be internally pulled up weekly. By setting of PC5.CRP RCLK is an active output.<br>RCLK source and frequency selection is made by CMR1.RS(1:0) if GPC6.COMP_DIS = $0_B$ or by CMR4.RS(2:0) if GPC6.COMP_DIS = $1_B$. |
| 5 | RPB1 | | | |
| 6 | RPC1 | | | |
| 7 | RPD1 | | | |
| 14 | RPA2 | I/O | PU/– | **Receive Multifunction Pins A to D, port 2**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level.<br>The input function must not be selected twice or more. Selectable pin functions as described for port 1. |
| 15 | RPB2 | | | |
| 16 | RPC2 | | | |
| 17 | RPD2 | | | |
| 22 | RPA3 | I/O | PU/– | **Receive Multifunction Pins A to D, port 3**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level.<br>The input function must not be selected twice or more. Selectable pin functions as described for port 1. |
| 23 | RPB3 | | | |
| 24 | RPC3 | | | |
| 25 | RPD3 | | | |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 32<br>33<br>34<br>35 | RPA4<br>RPB4<br>RPC4<br>RPD4 | I/O | PU/– | **Receive Multifunction Pins A to D, port 4**<br>Depending on programming of bits PC(1:4).RPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset these ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESR latching/transmission of data is done with the rising or falling edge of SCLKR. If not connected, an internal pullup transistor ensures a high input level.<br>The input function must not be selected twice or more.<br>Selectable pin functions as described for port 1. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 1**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level.<br>Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel.<br>Selectable pin functions are described below. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Synchronous Pulse Transmit, port 1**<br>$\overline{\text{SYPX}}$, PC(1:4).XPC(3:0) = ´$0000_B$´<br>Together with the values of registers XC(0:1) this signal defines the beginning of time slot 0 at system highway port XDI.<br>The pulse cycle is an integer multiple of 125 µs.<br>$\overline{\text{SYPX}}$ must not be used in parallel with XMFS. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Tran4mit Multiframe Synchronization (XMFS), port 1**<br>PC(1:4).XPC(3:0) = $0001_B$<br>This port defines the frame and multiframe begin on the transmit system interface ports XDI and XSIG.<br>Depending on PC5.CXMFS the signal on XMFS is active high or low.<br>XMFS must not be used in parallel with $\overline{\text{SYPX}}$.<br>*Note: A new multiframe position has settled at least one multiframe after pulse XMFS has been supplied.* |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Transmit Signaling Data (XSIG), port 1**<br>PC(1:4).XPC(3:0) = $0010_B$<br>Input for transmit signaling data received from the signaling highway. Optionally, (SIC3.TTRF = 1), sampling of XSIG data is controlled by the active high XSIGM marker. At higher data rates sampling of data is defined by bits SIC2.SICS(2:0). |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Transmit Clock (TCLK) input, port 1**<br>PC(1:4).XPC(3:0) = $0011_B$<br>A 2.048/8.192 MHz (E1) or 1.544/6.176 MHz (T1/J1) clock has to be sourced by the system if the internally generated transmit clock (generated by DCO-X) shall not be used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 (E1) or 1.544 MHz (T1/J1). |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **Transmit Multiframe Begin (XMFB), port 1**<br>PC(1:4).XPC(3:0) = $0100_B$<br>XMFB marks the beginning of every transmitted multiframe on XDI. The signal is active high for one 2.048 (E1) or 1.544 MHz (T1/J1) period. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **Transmit Signaling Marker (XSIGM), port 1**<br>PC(1:4).XPC(3:0) = $0101_B$<br>**E1**<br>Marks the transmit time slots on XDI of every frame which are defined by register TTR(1:4).<br>**T1/J1**<br>Marks the transmit time slots on XDI of every frame which are defined by register TTR(1:4) (if not CAS-BR is used).<br>When using the CAS-BR signaling scheme the robbed bit of each channel in every sixth frame is marked. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **Data Link Bit Transmit (DLX), port 1**<br>PC(1:4).XPC(3:0) = $0110_B$<br>**E1**<br>Marks the Sa(8:4)-bits within the data stream on XDI. The Sa(8:4)-bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA8E to XC0.SA4E.<br>**T1/J1**<br>This output provides a 4 kHz signal which marks the DL-bit position within the data stream on XDI (in ESF mode only). |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **Tran4mit Clock (XCLK), port 1**<br>PC(1:4).XPC(3:0) = $0111_B$<br>Transmit line clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1) derived from SCLKX/R, RCLK or generated internally by DCO circuitries. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Transmit Line Tristate (XLT), port 1**<br>PC(1:4).XPC(3:0) = $1000_B$<br>A high level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically ored with register bit XPM2.XLT. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **General Purpose Input (GPI), port 1**<br>PC(1:4).XPC(3:0) = $1001_B$.<br>The pin is set to input. The state of this input is reflected in the register bits MFPI.XPA, MFPI.XPB or MFPI.XPC respectively. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **General Purpose Output High (GPOH), port 1**<br>PC(1:4).XPC(3:0) = $1010_B$.<br>The pin level is set fix to high level. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | O | – | **General Purpose Output Low (GPOL), port 1**<br>PC(1:4).XPC(3:0) = $1011_B$.<br>The pin level is set fix to high level. |
| 120<br>121<br>122<br>123 | XPA1<br>XPB1<br>XPC1<br>XPD1 | I | PU | **Transmit Line Tristate, low active, port 1**<br>$\overline{XLT}$ : PC(1:2).XPC(3:0) = $1110_B$.<br>A low level on this port sets the transmit lines XL1/2 or XDOP/N into tristate mode. This pin function is logically ored with register bit XPM2.XLT. |
| 126,<br>127,<br>128,<br>129 | XPA2<br>XPB2<br>XPC2<br>XPD2 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 2**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level.<br>Each input function ($\overline{SYPX}$, XMFS, XSIG,TCLK, XLT or $\overline{XLT}$) may only be selected once. SYPX and XMFS must not be used in parallel.<br>Selectable pin functions as described for port 1. |
| 51,<br>52,<br>53,<br>54 | XPA3<br>XPB3<br>XPC3<br>XPD3 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 3**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level.<br>Each input function ($\overline{SYPX}$, XMFS, XSIG,TCLK, XLT or $\overline{XLT}$) may only be selected once. SYPX and XMFS must not be used in parallel.<br>Selectable pin functions as described for port 1. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 57,<br>58,<br>59,<br>60 | XPA4<br>XPB4<br>XPC4<br>XPD4 | I/O | PU/– | **Transmit Multifunction Pins A to D, port 4**<br>Depending on programming of bits PC(1:4).XPC(3:0) these multifunction ports carry information to the system interface or from the system to the QuadLIU™. After reset the ports are configured to be inputs. With the selection of the appropriate pin function, the corresponding input/output configuration is achieved automatically. Depending on bit SIC3.RESX latching/transmission of data is done with the rising or falling edge of SCLKX. If not connected, an internal pullup transistor ensures a high input level.<br>Each input function ($\overline{\text{SYPX}}$, XMFS, XSIG,TCLK, XLT or $\overline{\text{XLT}}$) may only be selected once. SYPX and XMFS must not be used in parallel.<br>Selectable pin functions as described for port 1. |
| **Power Supply** | | | | |
| 114 | $V$DDR1 | S | – | **Positive Power Supply**<br>For the analog receiver 1 (3.3 V) |
| 139 | $V_{DDR2}$ | S | – | **Positive Power Supply**<br>For the analog receiver 2 (3.3 V) |
| 42 | $V_{DDR3}$ | S | – | **Positive Power Supply**<br>For the analog receiver 3 (3.3 V) |
| 67 | $V_{DDR4}$ | S | – | **Positive Power Supply**<br>For the analog receiver 4 (3.3 V) |
| 110 | $V_{DDX1}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 1 (3.3 V) |
| 143 | $V_{DDX2}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 2(3.3 V) |
| 38 | $V_{DDX3}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 3 (3.3 V) |
| 71 | $V_{DDX4}$ | S | – | **Positive Power Supply**<br>For the analog transmitter 4 (3.3 V) |
| 63<br>118 | $V_{DDC}$ | S | – | **Positive Power Supply**<br>For the digital core (1.8 V).<br>These pins can either be positive power supply input or output, dependent on VSEL:<br>VSEL connected to $V_{SS}$ : 1.8 V power supply inputs, require decoupling.<br>VSEL connected to $V_{DD}$: 1.8 V outputs for decoupling to $V_{SS}$.<br>**These pins must not be used to supply external devices.** |
| 124<br>132 | $V$ | S | – | **Positive Power Supply**<br>For the analog PLL (3.3 V) |
| 10<br>28<br>55<br>101 | $V_{DDP}$ | S | – | **Positive Power Supply**<br>For the digital pads (3.3 V)<br>For correct operation, all $V_{DDP}$ pins have to be connected to positive power supply. |

**Table 2 I/O Signals for P-TQFP-144-8** (cont'd)

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 45<br>64<br>117<br>136<br>1<br>36<br>73<br>108<br>11<br>56<br>102<br>125<br>135 | $V_{SS}$ | S | – | **Power Ground**<br>Common for all sub circuits (0 V)<br>For correct operation, all $V_{SS}$ pins have to be connected to ground. |
| **Power Supply Configuration** | | | | |
| 134 | $V_{SEL}$ | I + PU | – | **Voltage Select**<br>Enables the internal voltage regulator for 3.3 V only operation mode if connected to $V_{DD}$ (recommended) or left open.<br>Disables the internal voltage regulator for dual power supply mode (1.8 V and 3.3 V) if connected to $V_{SS}$. |
| **Boundary Scan/Joint Test Access Group (JTAG)** | | | | |
| 131 | $\overline{TRS}$ | I | PD | **Test Reset**<br>For Boundary Scan (active low). If not connected, an internal pulldown transistor ensures low input level. |
| 112 | TDI | | PU | **Test Data Input**<br>For Boundary Scan.<br>If not connected an internal pullup transistor ensures high input level. |
| 141 | TMS | | | **Test Mode Select**<br>For Boundary Scan.<br>If not connected an internal pullup transistor ensures high input level. |
| 140 | TCK | | | **Test Clock**<br>For Boundary Scan.<br>If not connected an internal pullup transistor ensures high input level. |
| 113 | TDO | O | – | **Test Data Output**<br>For Boundary Scan |

## 2.5 Pin Strapping

Some pins are used for selection of functional modes of the QuadLIU™:

**Table 3 Overview about the Pin Strapping**

| PIN | Pin Strapping is used | Pin Strapping Function |
|---|---|---|
| IM(1:0) | Always | Defines the used micro controller interface |
| A(5:0) | Only in SCI interface mode | Defines the six LBSs of the SCI source address, see **Chapter 3.5.2.1** |
| D(15:5) | Only in SCI or SPI interface mode | Programs the parameters N and M of the PLL in the master clocking unit instead of registers GCM5 and GCM6, see **Chapter 3.5.5**:<br>- D(15:11) values programs PLL dividing factor M<br>- D(10:5) values programs PLL dividing factor N<br>Programming by pin strapping is equivalent to programming by register bits GCM5.PLL_M(4:0) and GCM6.PLL_N(5:0) which is used in asynchronous micro controller modes. |

# 3 Functional Description

## 3.1 Hardware

The QuadLIU™ requires either two supply voltages, 1.8 V and 3.3 V, see **Figure 8**, or a single 3.3 V supply, with the 1.8 V supply being generated internally by an on-chip regulator, see **Figure 7**. In order to minimize power dissipation, it is recommended to operate the device using separate external 3.3 V and 1.8 V supplies. Please note that the 1.8 V supply requires de-coupling whether generated on-chip or externally. Supply voltage selection is done by the pin VSEL.

The pin IM1 is used to select the additional serial interfaces SPI and SCI bus, see also **Chapter 2.5**.

The pin READY_EN can be used to activate the output functionality of the additional pin $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$. for the asynchronous micro controller interface. Because the READY_EN pin is used for $V_{SS}$ in version 2.1, the pin $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is not active (is in tri-state mode) if no change is made on the board. Therefore for the $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ pin also no change must be made on the board. See also **Chapter 3.5.1**.

Some pins of the micro controller interface have different functions if the SPI or SCI bus is selected as interface to the micro controller.

The pins RLAS2(1:4) of the additional separate analog switches at the receive line interfaces (supported only in P/PG-LBGA-160-1 package) can be connected to VSSX if the analog switches are not used.

To accommodate the package several signals can be configured at the multifunction ports. Four multifunction ports exist for the receive direction and four for the transmit direction for each of the four channels.

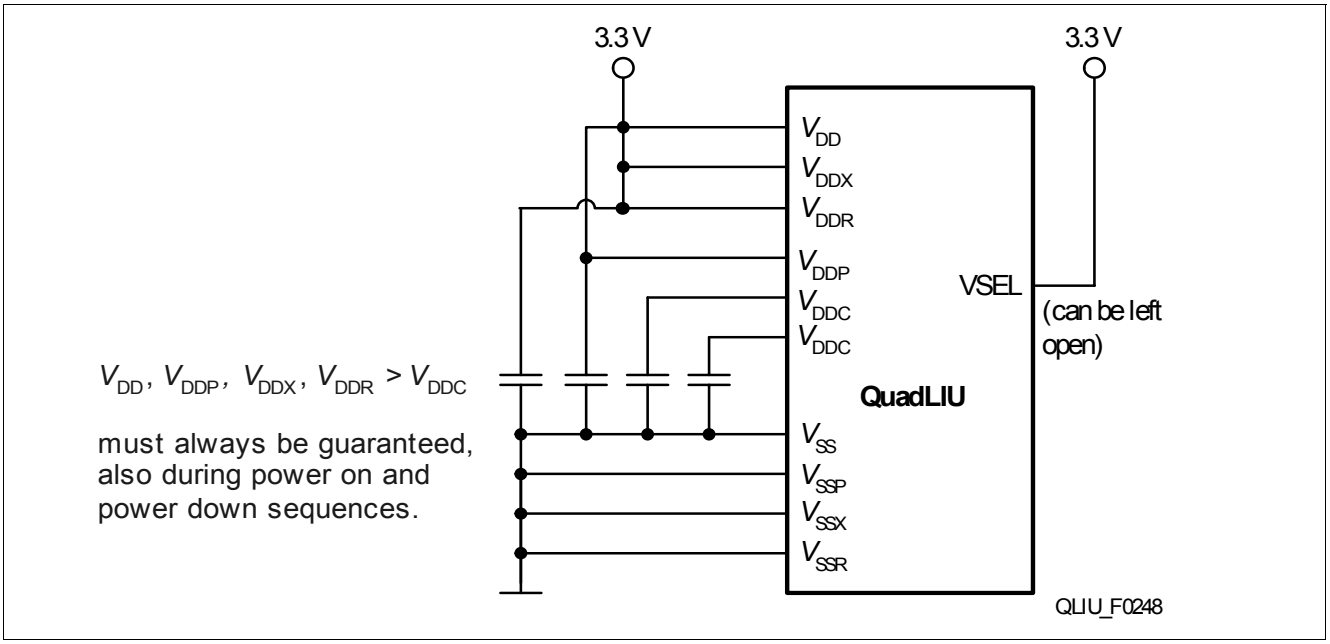



**Figure 7 Single Voltage Supply**

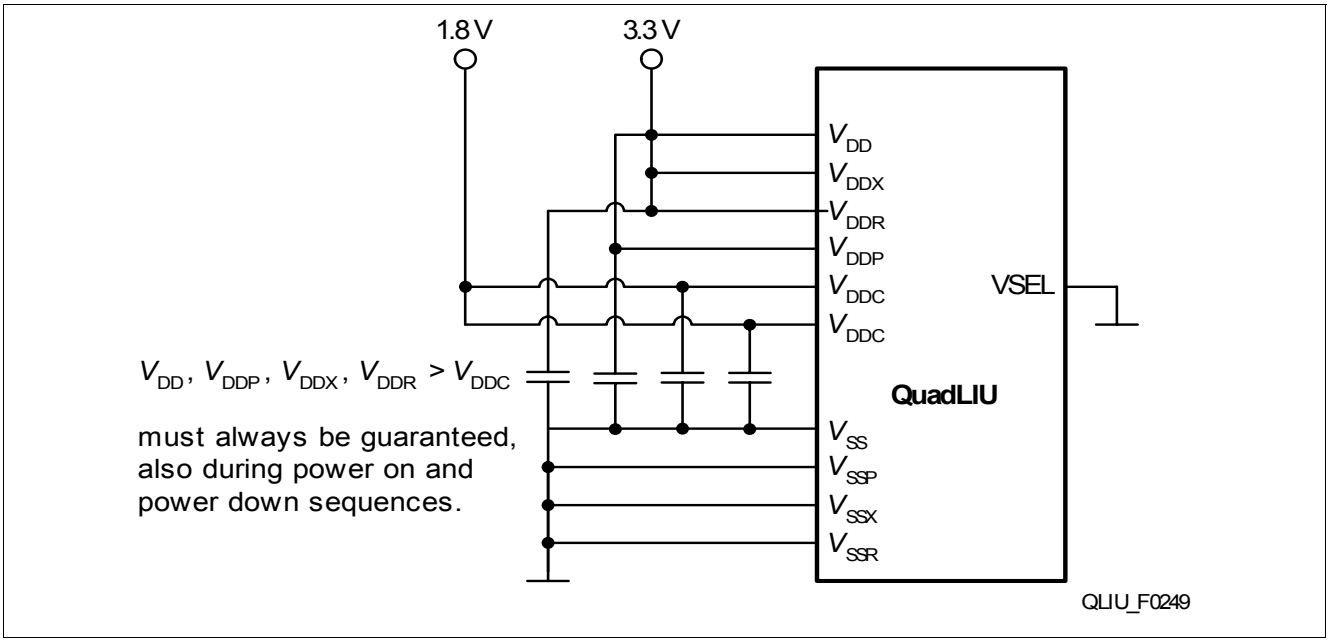



**Figure 8 Dual Voltage Supply**

## 3.2 Software

The QuadLIU™ device contains analog and digital function blocks that are configured and controlled by an external microprocessor or micro controller, using either the asynchronous interface, SPI bus or SCI bus.

The register address range is 10 bit wide.

## 3.3 Functional Overview

The main interfaces are

- Receive and transmit line interface
- Asynchronous Microprocessor interface with two modes: Intel or Motorola
- SPI Bus interface
- SCI Bus interface
- Framer interface
- Boundary scan interface

As well as several control lines for reset, mode and clocking purpose.

The main internal functional blocks are

- Analog line receiver with equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper and line build out
- Master clock generation unit
- Dual elastic buffers for receive and transmit direction, controlled by the appropriate jitter attenuators
- Receive line decoding, alarm detection and PRBS monitoring
- Transmit line encoding, alarm and PRBS generation
- Receive jitter attenuator
- Transmit jitter attenuator
- Available test loops: Local loop, remote loop and payload loop
- Boundary scan control

## 3.4 Block Diagram

**Figure 9** shows the block diagram of the QuadLIU™.

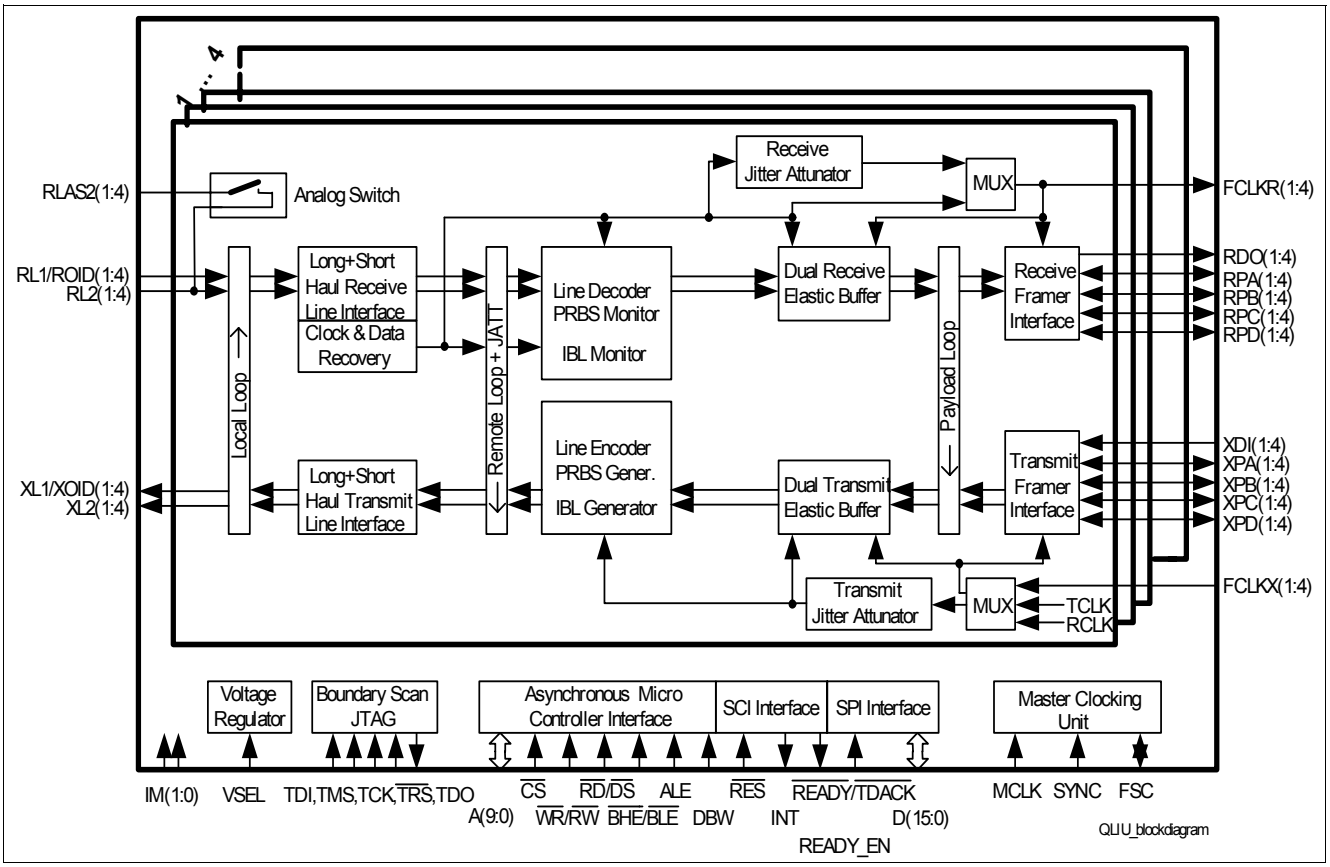



**Figure 9 Block Diagram**

## 3.5 Functional Blocks

The four possible micro controller interface modes - two asynchronous modes (Intel, Motorola) and two serial interface modes (SPI bus or SCI bus) - are selected by using the interface mode selection pins IM(1:0). This selection is valid immediately after reset becomes inactive.

After changing of the interface mode by IM(1:0), a hardware reset must be applied.

### 3.5.1 Asynchronous Micro Controller Interface (Intel or Motorola mode)

The asychronous micro controller interface is selected if IM(1:0) is strapped to ´00B´ (Intel mode) or ´01B´ (Motorola mode).

An handshake signal (data acknowledge $\overline{\text{DTACK}}$ for Motorola- and $\overline{\text{READY}}$ for Intel-mode) is provided indicating successful read or write cycle. By using $\overline{\text{DTACK}}$ or $\overline{\text{READY}}$ respectively no counter is necessary in the micro controller to finish the access, see also timing diagrams **Figure 51** ff.

If activated, $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ is an open Drain (oD) output and will be only driven to low if $\overline{\text{CS}}$ is low. Therefore the $\overline{\text{READY}}$/ $\overline{\text{DTACK}}$ signals of two or more QuadLIU™ v3.1 can be connect together, using a common external pull-up resistor (wired or).

The generation of $\overline{\text{READY}}$ /$\overline{\text{DTACK}}$ is asynchronous:

In Intel mode read access $\overline{\text{READY}}$ will be set to low by the QuadLIU™ after the data output is stable at the QuadLIU™. After the rising edge of RD (which is driven by the micro controller), $\overline{\text{READY}}$ is low for a “hold time”, before it will be set to high by the QuadLIU™.

In the Intel mode write access $\overline{\text{READY}}$ will be set to low by the QuadLIU™ after the falling edge of WR (which is driven by the micro controller). After WR is high and data are written successfully into the registers of the QuadLIU™, $\overline{\text{READY}}$ will be set to high by the QuadLIU™.

The general timing diagrams are shown in **Figure 51** to **Figure 56**.

The communication between the external micro controller and the QuadLIU™ is done using a set of directly accessible registers. The interface can be configured as Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The external micro controller transfers data to and from the QuadLIU™, sets the operating modes, controls function sequences, and gets status information by writing or reading control and status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal BHE / $\overline{\text{BLE}}$ as shown in **Table 4** and **Table 5**.

**Table 6** shows how the ALE (**A**ddress **L**atch **E**nable) line is used to control the bus structure and interface type. The switching of ALE allows the QuadLIU™ to be directly connected to a multiplexed address/data bus.

#### 3.5.1.1 Mixed Byte/Word Access

Reading from or writing to the internal registers can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access is allowed without any restrictions.

**Table 4 Data Bus Access (16-Bit Intel Mode)**

| $\overline{\text{BHE}}$ | A0 | Register Access | QuadLIU™ Data Pins Used |
|---|---|---|---|
| 0 | 0 | Register word access (even addresses) | D(15:0) |
| 0 | 1 | Register byte access (odd addresses) | D(15:8) |
| 1 | 0 | Register byte access (even addresses) | D(7:0) |
| 1 | 1 | No transfer performed | None |

**Table 5 Data Bus Access (16-Bit Motorola Mode)**

| $\overline{\text{BLE}}$ | A0 | Register Access | QuadLIU™ Data Pins Used |
|---|---|---|---|
| 0 | 0 | Register word access (even addresses) | D(15:0) |
| 0 | 1 | Register byte access (odd addresses) | D(7:0) |
| 1 | 0 | Register byte access (even addresses) | D(15:8) |
| 1 | 1 | No transfer performed | None |

**Table 6 Selectable asynchronous Bus and Microprocessor Interface Configuration**

| ALE | IM(1:0) | Asynchronous Microprocessor Interface Mode | Bus Structure |
|---|---|---|---|
| Constant level | 01 | Motorola | De-multiplexed |
| | 00 | Intel | De-multiplexed |
| Switching | 00 | Intel | Multiplexed |

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected asynchronous microprocessor interface mode:

| | | | | |
|---|---|---|---|---|
| **Intel** | (Address n + 1) | | (Address n) | |
| Motorola | (Address n) | | (Address n + 1) | |
| | ↑ | | ↑ | |
| | ↓ | | ↓ | |
| Data lines | D15 | D8 | D7 | D0 |

n: even address

### 3.5.2 Serial Micro Controller Interfaces

Two serial interfaces are included to enable device programming and controlling:- Slave Serial Control Interface (SCI) - Slave Serial Peripheral Interface (SPI)

By using the SCI Interface, the QuadLIU™ can be easily connected to Infineon interworking devices plus Infineon SHDSL- and ADSL-PHYs so that implementation of different line transmission technologies on the same line card easily is possible. The SCI interface is a three-wire bus and optionally replaces the parallel processor interface to reduce wiring overhead on the PCB, especially if multiple devices are used on a single board. Data on the bus is HDLC encapsulated and uses a message-based communication protocol.

If SCI interface with multipoint to multipoint configuration is used, address pins A(5:0) are used for SCI source (slave) address pin strapping, see **Table 3**.

Note that after a reset writing into or reading from QuadLIU™ registers using the SCI- or SPI-Interface is not possible until the PLL is locked: If the SCI-Interface is used no acknowledge message will be sent by the QuadLIU™. If the SPI-Interface is used pin SDO has high impedance (SDO is pulled up by external resistor). To trace if the SPI interface is accessible, the micro controller should poll for example the register DSTR so long as it read no longer the value ´$F_H$´.

#### 3.5.2.1 SCI Interface

The Serial Control Interface (SCI) is selected if IM(1:0) is strapped to ´$11_H$´.

The QuadLIU™ SCI interface is always a slave.

**Figure 57** shows the timing diagram of the SCI interface, **Table 62** gives the appropriate values of the timing parameters.

**Figure 10** shows a first application using the SCI interfaces of some QuadLIU™s where point to point full duplex connections are realized between every QuadLIU™ and the micro controller. Here the data out pins of the SCI interfaces (SCI_TXD) of the QuadLIU™s must be configured as push-pull (PP), see configuration register bit PP in **Table 9**.

**Figure 11** shows an application with Multipoint to multipoint connections between the QuadLIU™s and the micro controller (half duplex). Here the data out pin of the SCI interfaces (SCI_TXD) of all QuadLIU™s must be configured as an open Drain (oD), see configuration register bit PP in **Table 9**. The data out and data in pins (SCI_RXD, SCI_TXD) of each QuadLIU™ are connected together to form a common data line. Together with a common pull up resistor for the data line, all open Drain data out pins are building a wired And.

The Infineon proprietary Daisy-Chain approach is not supported

The group address of the SCI interface is ´$00_H$´ after reset. Recommendation for configuring is ´$C4_H$´ to be different to the group addresses of all other Infineon devices.

In case of multipoint to multipoint applications the 6 MSBs of the SCI source address will be defined by pinstrapping of the address pins A5 to A0. The two LSBs of the SCI source address are constant ´10B´, see **Table 9**. The SCI source address can be overwritten by a write command into the SCI configuration register. For applications with point to point connections for the SCI interface the source address is not valid.

Because 14 bits are used for the register addresses in the SCI interface macro the two MSBs of the 16 bit wide register addresses are set fixed to zero.

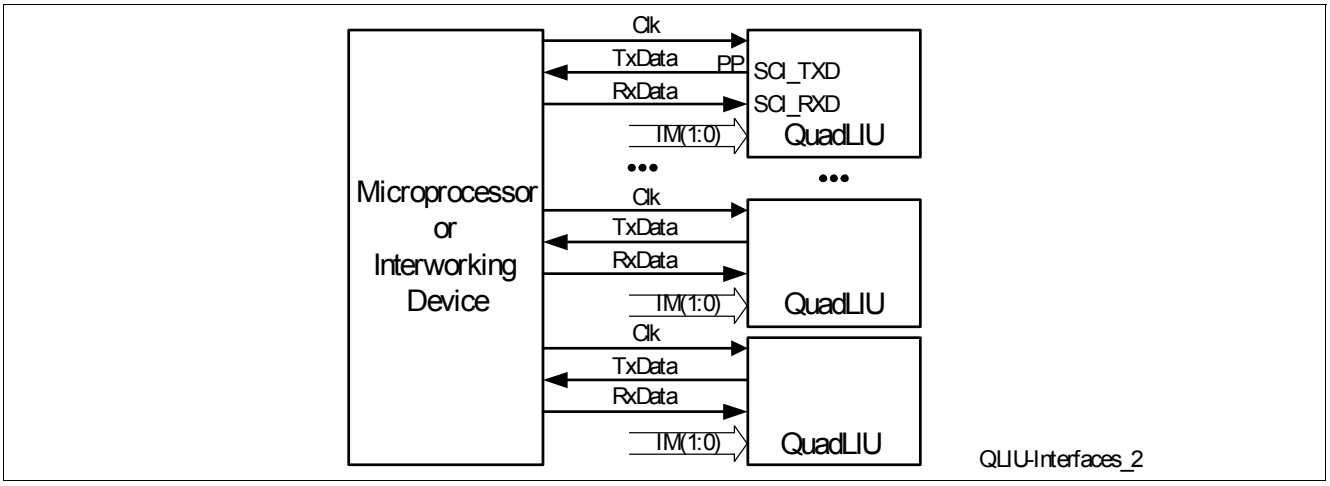



**Figure 10 SCI Interface Application with Point To Point Connections**

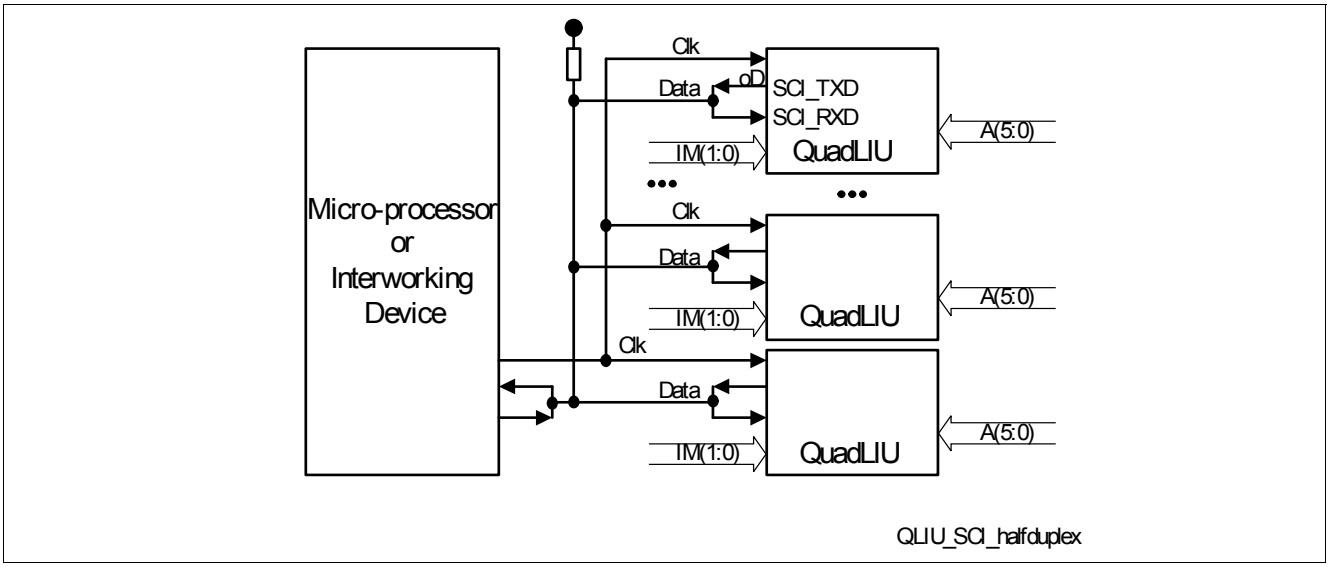



**Figure 11 SCI Interface Application with Multipoint To Multipoint Connection**

The following configurations of the SCI interface of the QuadLIU™ can be set by the micro controller by a write command into the SCI configuration register (control bits ´10B´, see **Table 9**, SCI register address is ´0000H´, see **Table 4** and **Figure 13**):

- Half duplex/full duplex (reset value: Half duplex), bit DUP.
- OpenDrain/push-pull (configuration of output pin to openDrain/push-pull is in general independent of the duplex mode and must be set appropriately in application) (reset value: open Drain), bit PP.
- CRC for transmit and receive on/off (reset value: off), bit CRC_EN.
- Automatic acknowledgement of CMD messages on/off (reset value: off), bit ACK_EN.
- Clock edge rising/falling (reset value: falling), bit CLK_POL.
- Clock gating (reset value: off), bit CLK_GAT.

The following SCI configurations are fixed and cannot be set by the micro controller:

- Interrupt feature is disabled, bit INT_EN = ´0´.
- Arbitration always made with LAPD (only SCI applications like in **Figure 10** and **Figure 11** are possible), bit ARB = ´0´.

The maximum possible SCI clock frequency is 6 MHz for point to point applications (full duplex) and about 2 MHz for multipoint to multipoint applications, dependent on the electrical capacity of the bus lines of the PCB.

**Figure 12** shows the message structure of the QuadLIU™. The SCI interface uses HDLC frames for communication. The HDLC flags mark beginning and end of all messages.

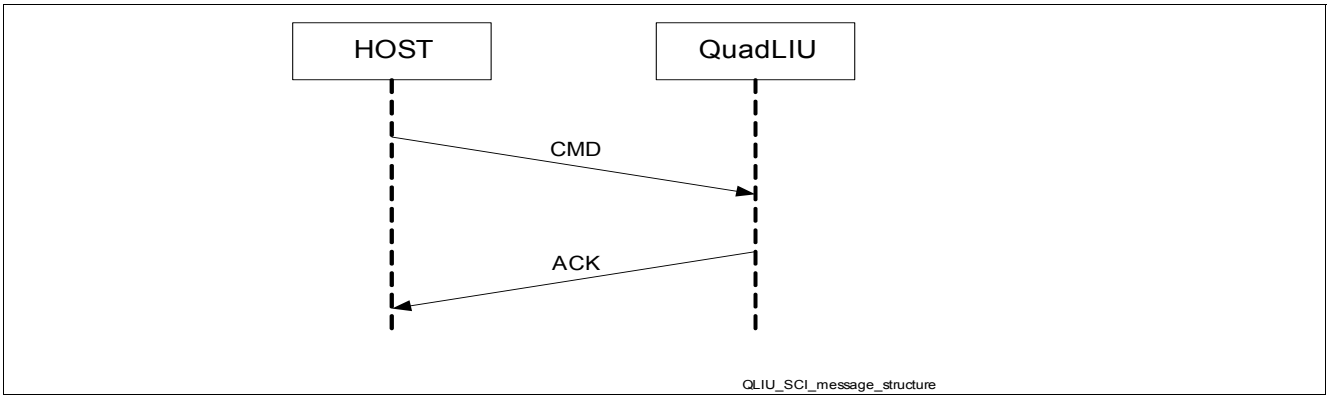



**Figure 12 SCI Message Structure of QuadLIU™**

Every write into or read from a register of the QuadLIU™ is initiated by a command message CMD from the Host (micro con roller) and is then confirmed by an acknowledge message ACK from the QuadLIU™ if in the SCI configuration automatic acknowledgement is set (bit ACK_EN, see **Table 9**). Read commands are always confirmed, independent on the bit ACK_EN.

The frame structure of this messages are shown in **Figure 13**.

In general the LSB of every byte is transmitted first and lower bytes are transmitted before higher bytes (regarding the register address)

Source and destination addresses are 8 bits long. Only the first 6 bits are really used for addressing. The bit C/R (Command/Response) distinguishes between a command and a response. The bit MS (Master/Slave) is ´0B´ for all Slaves and ´1B´ for all masters, see **Table 9** and **Figure 13**

The source address is defined by pinstrapping of A5 to A0 after reset, but other values can be configured by programming of the SCI configuration register.

The payload of the write CMD includes two control bits (MSBs of the payload), which distinguish between the different kind of commands, see **Table 8**, the 14 bit wide register address and the 8 bit wide data whereas the read CMD payload includes only the control bits and the register address. Register addresses can be either QuadLIU™ register addresses or SCI configuration register addresses. Because of the address space of the QuadLIU™, really 10 LSBs of the 14 bit address are used in the QuadLIU™. The 4 MSBs are ignored

The payload of the read ACK includes the content of the register (one byte) in addition to the payload of the write ACK.

The Frame Check Sequence FCS has 16 bits and is build (or checked) over the address and payload according to ISO 3309-1984.

The Read Status Byte RSTA of the acknowledge message shows the status of the received message and is built by the SCI interface of the QuadLIU™, see **Figure 15** and **Table 7**.

The destination address in the ACK message is always the source address of the corresponding CMD (the address of the micro controller), see **Figure 14**, because no CMD messages will be sent by the QuadLIU™ SCI interface

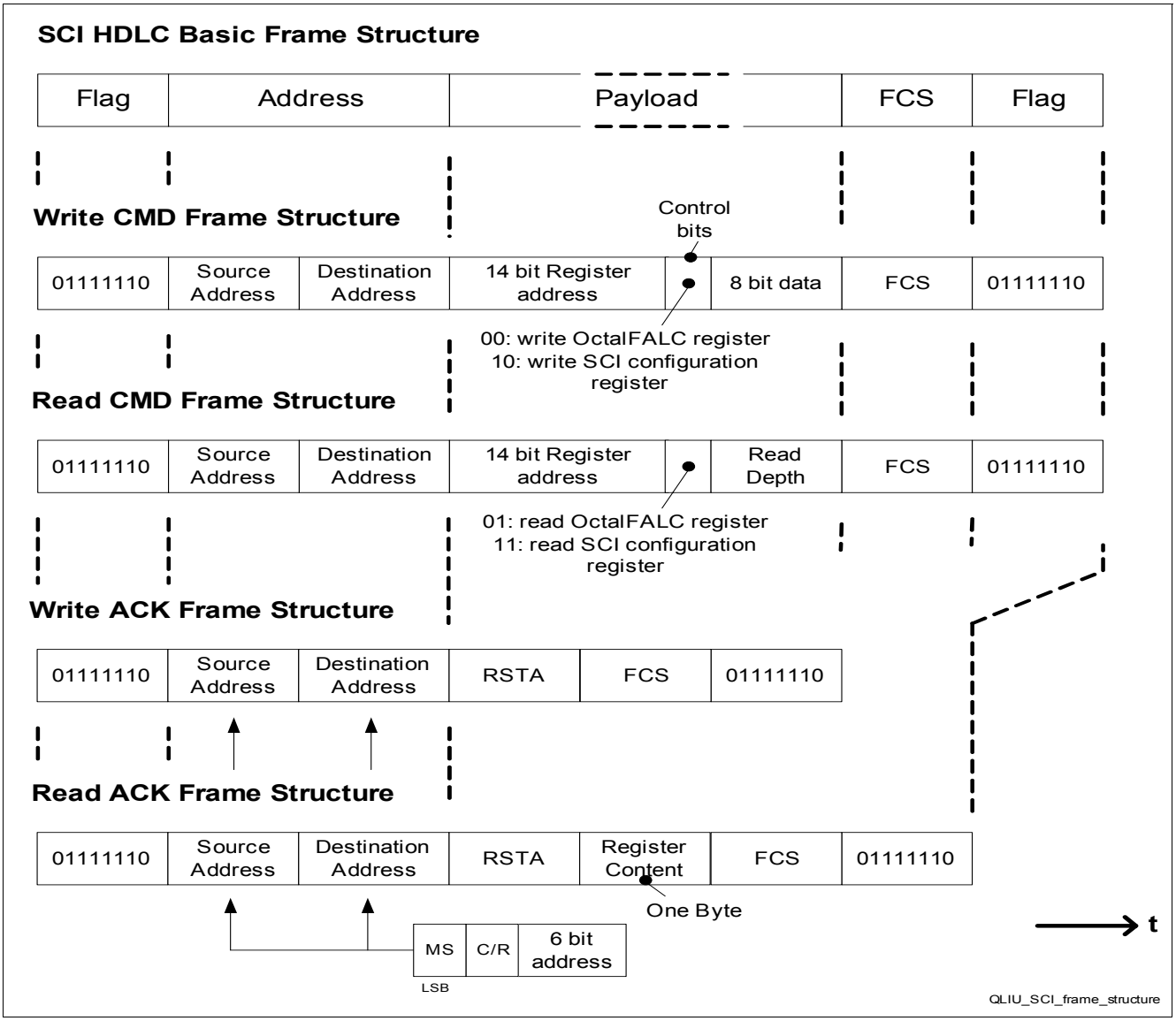



**Figure 13 Frame Structure of QuadLIU™ SCI Messages**

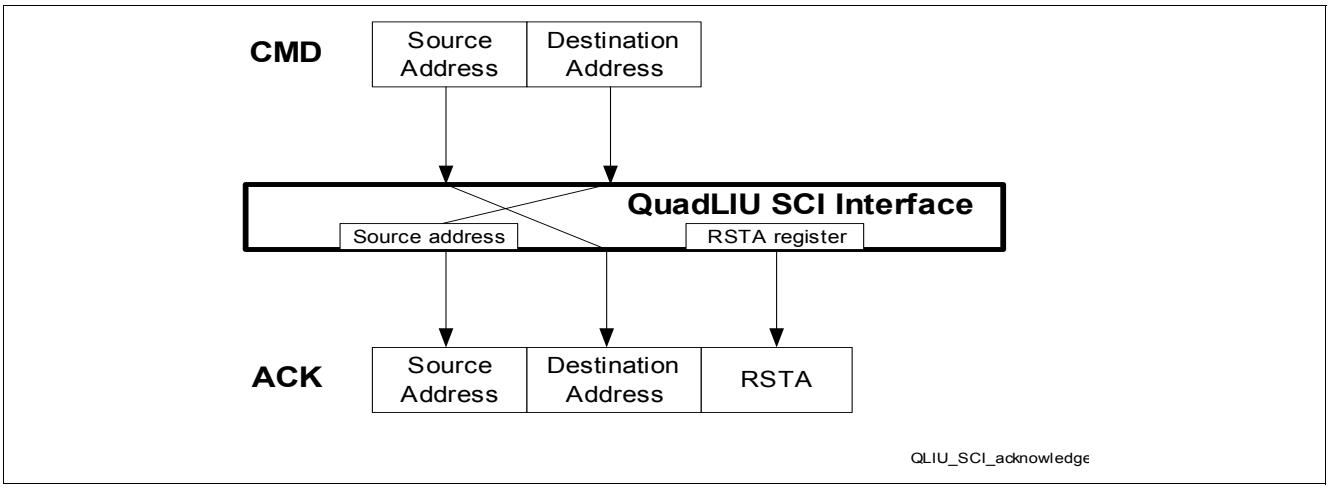



**Figure 14 Principle of Building Addresses and RSTA bytes in the SCI ACK Message of the QuadLIU™**

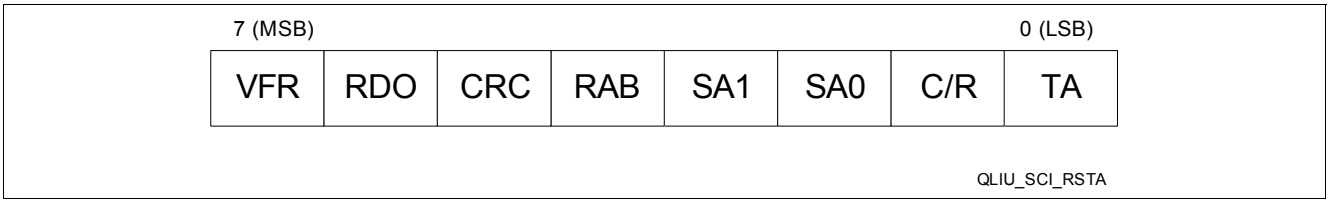



**Figure 15 Read Status Byte (RSTA) byte of the SCI Acknowledge (ACK)**

**Table 7 Read Status Byte (RSTA) Byte of the SCI Acknowledge (ACK)**

| Field | Bit | Description |
|---|---|---|
| VFR | 7 | Valid Frame. Indicates whether a valid frame has received.<br>´0´: Received frame is invalid.<br>´1´: Received frame is valid. |
| RDO | 6 | Reserved |
| CRC | 5 | CRC compare check. Indicates whether a CRC check is failed or not.<br>´0´: CRC error check failed on the received frame.<br>´1´: Received frame is free of CRC errors. |
| RAB | 4 | Received message aborted. CMD message abortion is declared. The receive message was aborted by the HOST. A sequence of 7 consecutive ´1´ was detected before closing the flag. Note that ACK message and therefore RAB will not be send before destination address was received.<br>´0´: Data reception is in progress.<br>´0´: Data reception has been aborted. |
| SA1 | 3 | Reserved |
| SA0 | 2 | Reserved |
| C/R | 1 | Reserved |
| TA | 0 | Reserved |

**Table 8 Definition of Control Bits in Commands (CMD)**

| Control Bits (MSB LSB) | Command type |
|---|---|
| 01 | Read QuadLIU™ registers |
| 00 | Write QuadLIU™ register1 |
| 10 | Write SCI configuration register |
| 11 | Read SCI configuration register |

**Table 9 SCI Configuration Register Content**

| Address | Bit 7 (MSB) | Bit6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| ´$0000_H$´ | PP | CLK_POL | CLK_GAT | ACK_EN | INT_EN | CRC_EN | ARB | DUP |
| ´$0001_H$´ | 1 | Destination Address | | | | | 1 (=C/R) | 0 (=MS) |
| ´$0002_H$´ | 0 | Group Address | | | | | 1 (=C/R) | 0 (=MS) |

### 3.5.2.2 SPI Interface

The Serial Peripheral Interface (SPI) is selected if IM(1:0) is strapped to ´$10_H$´.

The SPI interface of the QuadLIU™ is always a slave.

Figure 16 and Figure 17 show the read and the write operation respectively. The start of a read or write operation is marked by the falling edge of the chip select signal CS whereas the end of the operations is marked by the rising edge of CS. Because of CS the SPI interface has no slave address.

The first bit of the serial data in (SDI) is ´1´ for a read operation and ´0´ for a write operation. The first four bits of the 15 bit address are not valid for the QuadLIU™.

In read operation the QuadLIU™ delivers the 8 bit wide content of the addressed register at the serial data out (SDO).

In general SPI data are driven with the negative edge of the serial clock (SCLK) and sampled with the positive edge of SCLK. Figure 58 shows the timing of the SPI interface and Table 63 the appropriate timing parameter values.

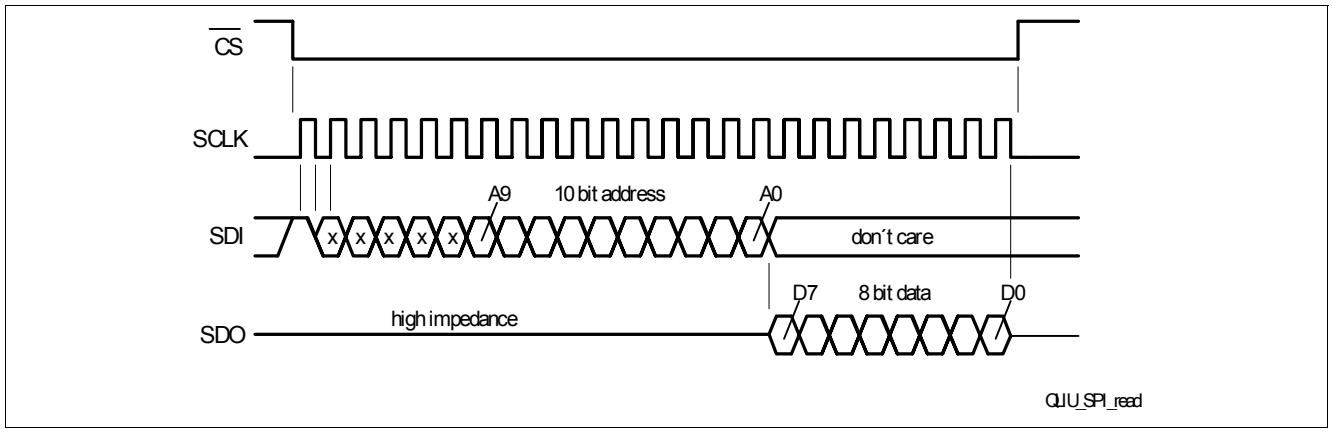



**Figure 16 SPI Read Operation**

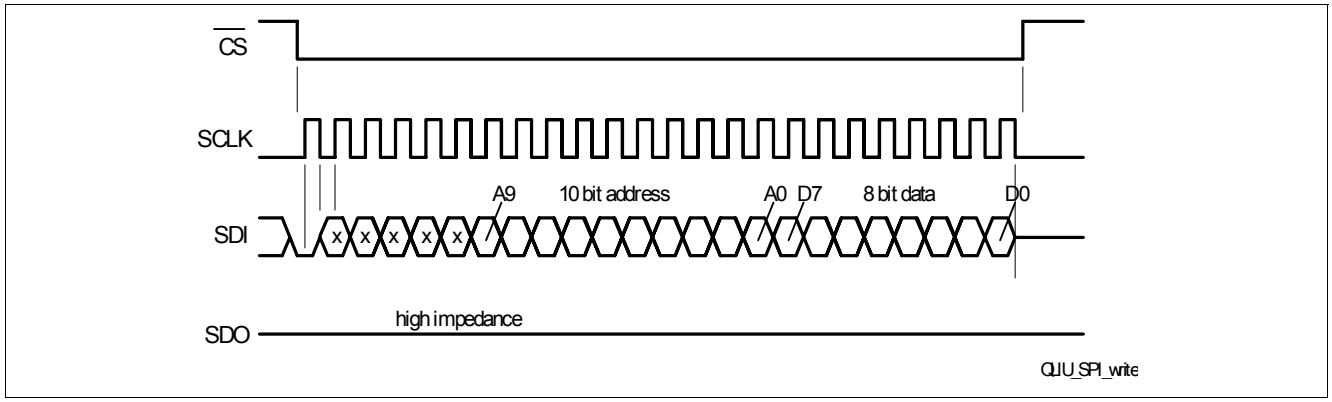



**Figure 17 SPI Write Operation**

### 3.5.3 Interrupt Interface

Special events in the QuadLIU™ are indicated by means of an interrupt output INT, which requests the external micro controller to read status information from the QuadLIU™, or to transfer data from/to the QuadLIU™. The electrical characteristics (open drain or push-pull) is programmed defined by the register bits IPC.IC(1:0), see IPC.

The QuadLIU™ has a single interrupt output pin INT with programmable characteristics (open drain or push-pull, defined by registers IPC) too.

Since only one INT request output is provided, the cause of an interrupt must be determined by the external micro controller by reading the QuadLIU™'s interrupt status registers (GIS, ISR(1:4), ISR6 and ISR7). The interrupt on pin INT and the interrupt status bits are reset by reading the interrupt status registers. The interrupt status registers ISR are of type “clear on read“ (“rsc”).

The structure of the interrupt status registers is shown in Figure 18.

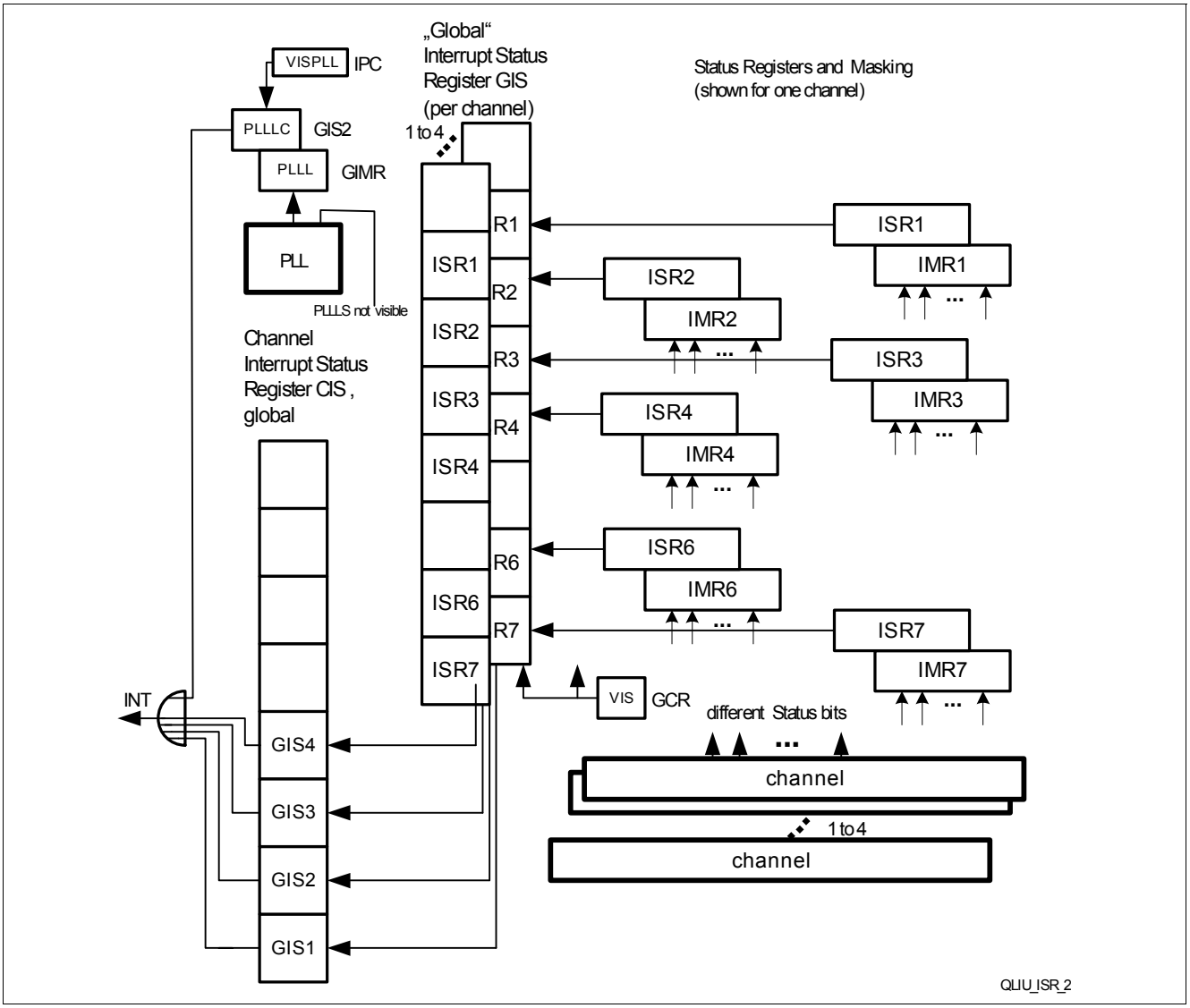



**Figure 18 Interrupt Status Registers**

Each interrupt indication bit of the registers ISR can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR. If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR. **All reserved bits in the mask registers IMR must not be written with the value ´0´.**

GIS, the non-maskable “Global” Interrupt Status Register per channel, serves as pointer to pending interrupts sourced by registers ISR(1:4), ISR6 and ISR7.

The non-maskable Channel Interrupt Status Register CIS serves as channel pointer to pending interrupts sourced by registers GIS.

After the QuadLIU™ has requested an interrupt by activating its INT pin, the external micro controller should first read the register CIS to identify the requesting interrupt source channel. Then it should read the Global Interrupt Status register GIS to identify the requesting interrupt source register ISR of that channel.

After reading the assigned interrupt status registers ISR(1:4), ISR6 and ISR7, the pointer bit in register GIS is cleared or updated if another interrupt requires service. After all bits ISR(7:0) of a register GIS are cleared, the assigned bit in register CIS is cleared. After all bits in register CIS are cleared the INT pin will be deactivated.

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR(1:4), ISR6 and ISR7 and GIS is only prohibited during read access.

**Masked Interrupts Visible in Status Registers**

- The “Global” Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (bits GIS.ISR(7:0)).
- An additional interrupt mode can be selected per port via bit GCR.VIS (**GCR**). In this mode, masked interrupt status bits neither generate an interrupt on pin INT nor are they visible in GIS, **but are displayed in the corresponding interrupt status registers ISR(1:4), ISR6 and ISR7.**

**PLL Interrupt Status Register**

- The bit n (n = 1 to 4) of the register CIS pointers an interrupt on channel n.
- The Global Interrupt Status register GIS2 indicates the lock status of the (global) PLL. Masking can be done by the register GIMR.
- An additional interrupt mode can be selected per port via bit IPC.VISPLL (**IPC**) where the masked interrupt status bit GIS2.PLLLS does not generate an interrupt on pin INT, **but is displayed in the corresponding interrupt status register bit GIS2.PLLLC**.

The additional interrupt mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

**Table 10 Interrupt Modes**

| GCR.VIS; IPC.VISPLL | Appropriate Mask bit | Interrupt active | Visibility in ISR(1:4), ISR(6:7) and GIS2 |
|---|---|---|---|
| 0 | 0 | Yes | Yes |
| 0 | 1 | No | No |
| 1 | 0 | Yes | Yes |
| 1 | 1 | No | Yes |

*Note:*

1. *In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.*
2. *All unmasked interrupt statuses are treated as before.*

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated, i.e. unmasked interrupts.

### 3.5.4 Boundary Scan Interface

In the QuadLIU™ a **T**est **A**ccess **P**ort (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard IEEE 1149.1-2001. **Figure 19** gives an overview, **Figure 49** shows the timing diagram and **Table 58** gives the appropriate values of the timing parameters.

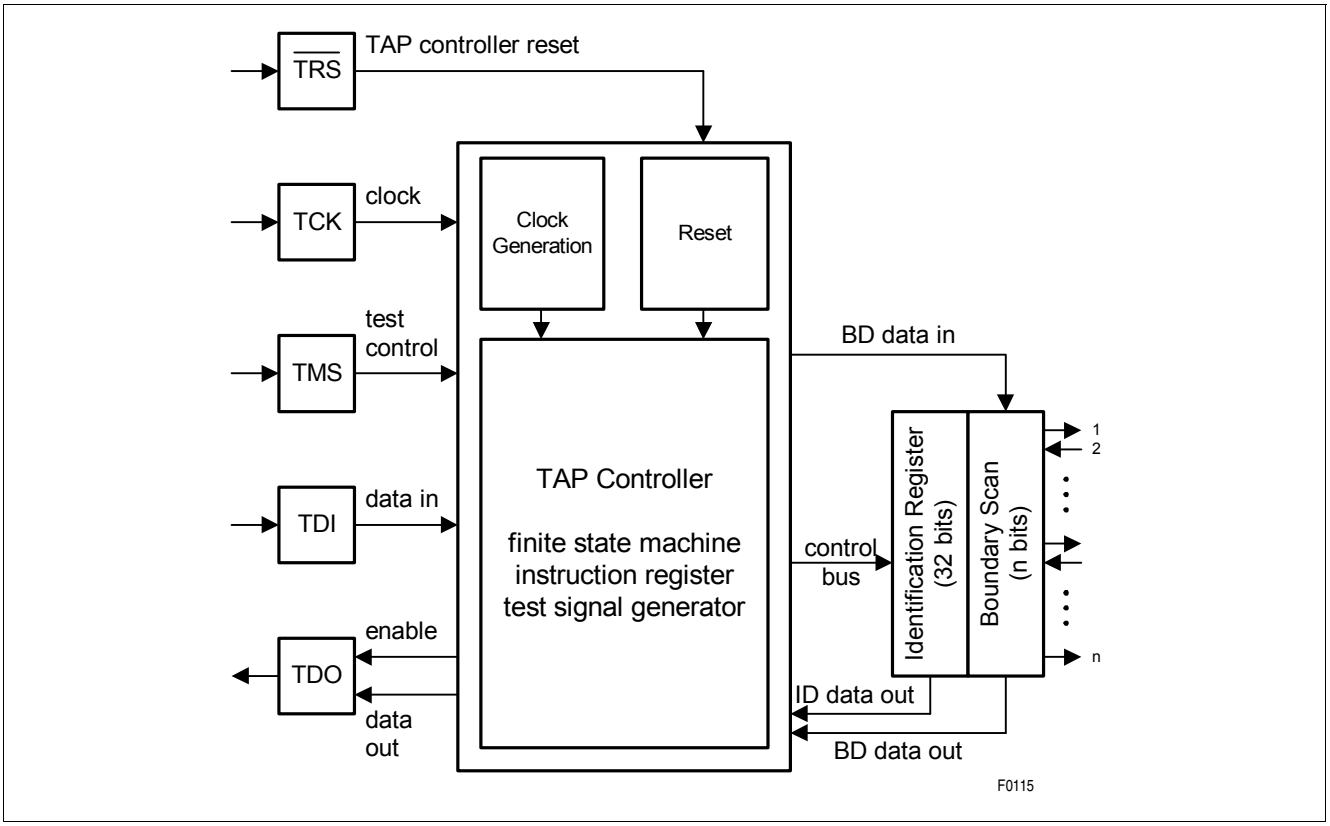



**Figure 19 Block Diagram of Test Access Port and Boundary Scan**

After switching on the device (power-on), a reset signal has to be applied to $\overline{TRS}$, which forces the TAP controller into test logic reset state.

The boundary length is t.b.d..

If no boundary scan operation is used, $\overline{TRS}$, TMS, TCK and TDI do not need to be connected since pull-up or pulldown transistors ensure default input levels in this case.

Test handling (boundary scan operation) is performed using the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, that means $\overline{TRS}$ is connected to $V_{DD}$ or it remains unconnected due to its internal pull up. Test data at TDI is loaded with a clock signal connected to TCK. "1" or "0" on TMS causes a transition from one controller state to another; constant "1" on TMS leads to normal operation of the chip.

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out and enable) and an I/O-pin (I/O) uses three cells (data in, data out and enable). Note that most functional output and input pins of the QuadLIU™ are tested as I/O pins in boundary scan, hence using three cells.

The desired test mode is selected by serially loading a 8-bit instruction code into the instruction register through TDI (LSB first), see **Table 11**. The test modes are:

### EXTEST

Extest is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values ("0" or "1"). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

### SAMPLE

Is a test mode which provides a snapshot of pin levels during normal operation.

**IDCODE**

A 32-bit identification register is serially read out on pin TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

The ID code field is set to (MSB to LSB): t.b.d.

Version number (first 4 bits) = ´$0001_B$´

Part Number (next 16 bits) = ´$0000\ 0001\ 0000\ 0100_B$´

Manufacturer ID (next 11 bits) = $0000\ 1000\ 001_B$´

LSB fixed to ´1´.

**BYPASS**

A bit entering TDI is shifted to TDO after one TCK clock cycle.

An alphabetical overview of all TAP controller operation codes is given in **Table 11**.

**Table 11 TAP Controller Instruction Codes**

| TAP Instruction | Instruction Code |
|---|---|
| BYPASS | 11111111 |
| EXTEST | 00000000 |
| IDCODE | 00000100 |
| SAMPLE | 00000001 |
| Reserved for device test | 01010011 |

## 3.5.5 Master Clocking Unit

The QuadLIU™ provides a flexible clocking unit, which references to any clock in the range of 1.02 to 20 MHz supplied on pin MCLK, see **Figure 20**.

The clocking unit has two different modes:

- In the so called “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´, **GCM2**) the clocking unit has to be tuned to the selected reference frequency by setting the global clock mode registers GCM(8:1) accordingly, see formulas in **GCM6**. All four ports can work in E1 or T1 mode individually. After reset the clocking unit is in “flexible master clocking mode”.
- In the so called “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) the tuning of the clocking unit is done internally so that no setting of the global clock mode registers GCM(8:1) is necessary. All four ports must work together either in E1 or in T1 mode.

For the calculation for the appropriate register settings see **GCM6**. Calculation can be done easy by using the flexible Master Clock Calculator which is part of the software support of the QuadLIU™, see **Chapter 8.3**.

All required clocks for E1 or T1/J1 operation are generated by this circuit internally. The global setting depends only on the selected master clock frequency and is the same for E1 and T1/J1 because both clock rates are provided simultaneously.

To meet the E1 requirements the MCLK reference clock must have an accuracy of better than ± 32 ppm. The synthesized clock can be controlled on pins RCLK and FCLKR.

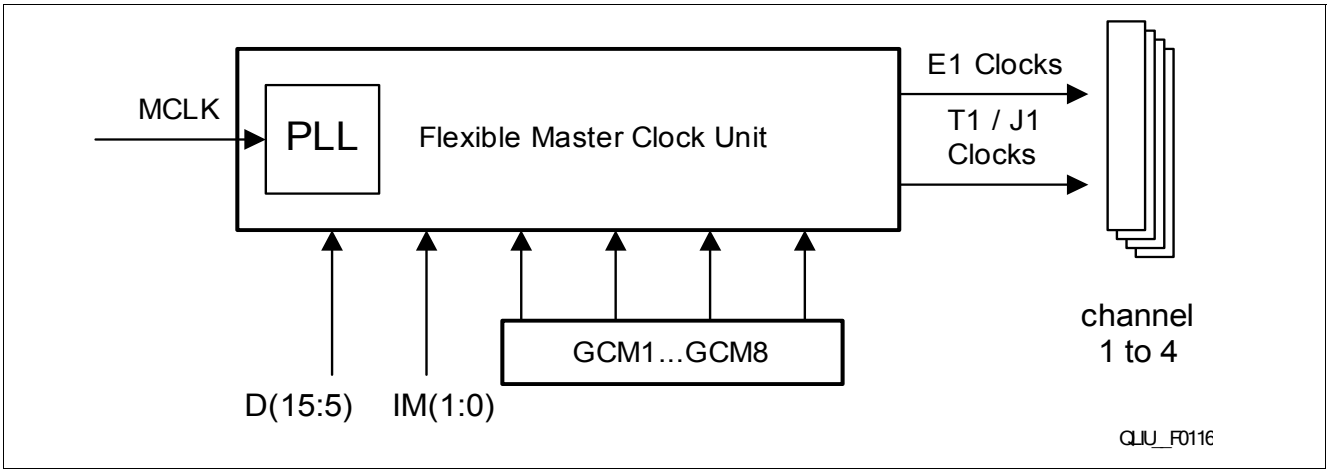



**Figure 20 Flexible Master Clock Unit**

### 3.5.5.1 PLL (Reset and Configuring)

If the (asynchronous) micro controller interface mode is selected by IM(1:0) the PLL must be configured

- By programming of the registers GCM5 and GCM6 in “flexible master clocking mode”. Every change of the contents of these registers - the divider factors N and M of the PLL - causes a reset of the PLL. Switching between E1 and T1 modes in arbitrary channels causes a reset of the clock unit but not of the PLL itself.
- Or by enabling of the ”fixed mode”: GCM2.VFREQ_EN = ´0´ (**GCM2**). Programming of registers GCM5 and GCM6 is not necessary. Any programming of GCM5 and GCM6 does NOT cause a reset of the PLL. Switching between E1 and T1 modes (for all channels) causes a reset of the clock unit but not of the PLL itself.

The SPI and SCI are synchronous interfaces and therefore need defined clocks immediately after reset, before any configuration is done. So to enable access to serial interfaces, the clock MCLK must be active and must have a defined frequency before reset becomes inactive. Dependent on the MCLK frequency the internal PLL must be configured if the SCI- or SPI-Interface mode is selected by IM(1:0)

- By strapping of the pins D(15:5) if “fixed mode” is not enabled (GCM2.VFREQ_EN = ´1´), see also **Table 3**. Because “fixed mode” is not enabled after reset, pinstrapping at D(15:5) is always necessary! Every new value at this pins causes a reset of the PLL. Configuring by the registers GCM5 and GCM6 is not taken into account and causes not a reset of the PLL
- Or by enabling of the ” fixed mode”.This is only allowed if the values of N and M defined by pinstrapping are identical to that values which are internally used for the “fixed mode”. That avoids changing of N and M by switching into the ”fixed mode” and therefore a new reset of the PLL. (A new reset of the PLL can cause a hang up of the whole system!) In ”fixed mode” the values are: N = ´$33_{10}$´, M = ´$0_{10}$´ so that the pinstrapping must be: D(10:5) = ´HLLLLH´, D(15:11) = ´LLLLL´. In ”fixed mode” programming of registers GCM1 to GCM8 is no longer necessary and values at the pins D(15:5) are no longer taken into account and causes NOT a reset of the PLL. A switching between E1 and T1 modes causes a reset of the clock unit but not of the PLL itself.

The configuration of the PLL by pinstrapping (see **Table 3**) in case of serial interface modes is done in the same way as by using the registers GCM5 and GCM6 if asynchronous micro controller interface mode (Intel or Motorola) is selected. So calculation of the pinstrapping values can be done also by using the formulas in **GCM6** or by using the “flexible Master Clock Calculator” which is part of the software support of the QuadLIU™, see **Chapter 8.3**. If the serial interfaces are selected, pinstrapping of D(15:5) configure the PLL directly, so changes causes always a reset of the PLL.

The conditions to trigger a reset of the central clock PLL are listed in **Table 12**. Every reset of the PLL causes a reset of the clock system.

**Table 12 Conditions for a PLL Reset**

| Reset Pin | GCM2.VFREQ_EN | Used controller interface | A PLL reset is made if ... |
|---|---|---|---|
| Active | X (will be set to ´1´ by reset) | X | Always |
| Inactive | 1 | Asynchron (Motorola or Intel) | If GCM5 or GCM6 are written and their values N or M change |
| | | SPI or SCI | If pinstrapping values change |
| | 0 | Asynchron (Motorola or Intel) | Never |
| | | SPI or SCI | If pinstrapping values change |
| | 0 -> 1 or 1 -> 0 | Asynchron (Motorola or Intel) | If actual values of N or M in GCM5 or GCM6 are different to internal settings of the “clocking fixed mode” |
| | | SPI or SCI | If pinstrap values are different to internal settings of the “clocking fixed mode”; That is not allowed! |

## 3.6 Line Coding and Framer Interface Modes

An overview of the coding at the line interface and the Modes at the framer interface is given in **Table 13**.

**Table 13 Line Coding and Framer Interface Modes**

| Line Code, Framer IF Mode | Register Bits | | Signals at Pins | | | |
|---|---|---|---|---|---|---|
| | FMR0.RC, LIM3.DRR | FMR0.XC, LIM3.DRX | RDON (RPC) | RDO | XDI | XDIN (XPB) |
| AMI, single rail | 10<br>0 | 10<br>0 | Pos and neg | AMI error | Pos, via encoder | Neg, via encoder |
| AMI, dual rail | 10<br>1 | 10<br>1 | Pos | Neg | Pos, encoder bypass | Neg, encoder bypass |
| HDB3/B8ZS, single rail | 11<br>0 | 11<br>0 | Decoded data | Violation | Via encoder | (HDB3/B8ZS coding) |
| HDB3/B8ZS, dual rail | 11<br>1 | 11<br>1 | Pos | Neg | Via encoder | (HDB3/B8ZS coding) |
| NRZ, single rail | 00<br>0 | 00<br>0 | Pos | ´0´ | NRZ, via encoder | Frame marker |
| NRZ, dual rail | 00<br>1 | 00<br>1 | Pos | Neg | NRZ | Frame marker |
| CMI, single rail | 01<br>0 | 01<br>0 | Decoded data | Violation | Via encoder | (CMI coding) |
| CMI, dual rail | 01<br>1 | 01<br>1 | Pos | Neg | Via encoder | (CMI coding) |

**Table 13 Line Coding and Framer Interface Modes** (cont'd)

| Line Code, Framer IF Mode | Register Bits | | Signals at Pins | | | |
|---|---|---|---|---|---|---|
| | FMR0.RC, LIM3.DRR | FMR0.XC, LIM3.DRX | RDON (RPC) | RDO | XDI | XDIN (XPB) |
| | 0 -> 1 or 1 -> 0 | Asynchron (Motorola or Intel) | If actual values of N or M in GCM5 or GCM6 are different to internal settings of the "clocking fixed mode" | | | |
| | | SPI or SCI | If pinstrap values are different to internal settings of the "clocking fixed mode"; That is not allowed! | | | |

### 3.6.1 Bipolar Violation Detection

If the register bit **BFR**.BPV is set to ´0´ and after execution of the sequence described below, Bipolar Violations (BPV) consisting on single ´1´ pulses (separated from the previous ´1´ pulse by at least one ´0´ pulse) or on two consecutive ´1´ pulses are detected correctly and thus counted by the bipolar violation counter. Bipolar Violations (BPV) consisting on more than two consecutive ´1´ pulses are not detected correctly and thus not counted by the bipolar violation counter.

Compatibel to the QuadFALC V2.1, Bipolar Violations (BPV) are not detected correctly and thus not counted by the bipolar violation counter, if **BFR**.BPV is set to ´1´ (default after reset).

If the second of two consecutively received Alternate Mark Inversion (AMI) pulses is a BPV (second pulse has the same polarity as the first pulse) and **BFR**.BPV is set to ´1´, the receiver converts the second AMI pulse to a logic zero. This conversion will cause a bit error and will mask detection and counting of the BPV. In contrast, any BPV separated from the previous ´1´ pulse by at least one ´0´ pulse is detected, counted, and recorded correctly

This BPV conversion is not expected to cause any system level problems. BPV counts, bit errors counts, and CRC counts may be slightly inaccurate, depending on the BPV rate. Note that the special B8ZS and HDB3 substitution do not contain consecutive BPV pulses so the conversion described above will not occur when receiving these patterns

The behaviour of the Bipolar Violation Detection is illustrated in **Figure 21**.

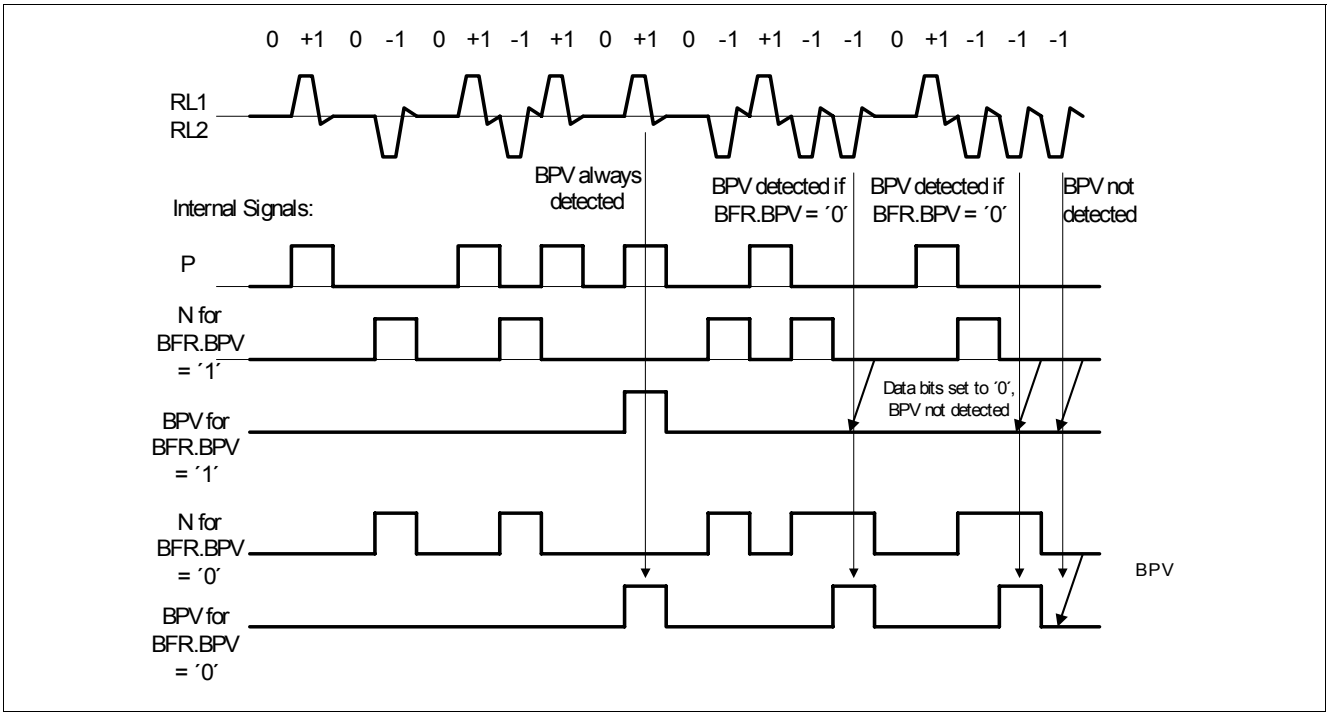



**Figure 21 Behaviour of Bipolar Violation Detection**

Independent from the setting of **BFR**.BPV all BPVs will be detected

- In patterns with alternate ´1´ and ´0´ (50 % ´1´ density)
- In all fixed patterns with no consecutive ´1´ (less than 50 % ´1´ density)

For **BFR**.BPV = ´1´ and execution of the sequence described below, variable or fixed patterns with at least two consecutive ´1´ pulses will show reduced BPVs. Reduction of BPVs depends on densitiy of ´1´ pulses. As ´1´ pulse density increases, BPV rate decrease until the limiting case of “all-one”. In framed “all-one” pattern no BPVs will be detected, except a BPV following a frameing bit that is ´0´.

For **BFR**.BPV = ´0´ variable or fixed patterns with at maximum two consecutive ´1´ pulses will show no reduced BPVs.

### Sequence

If the register bit **BFR**.BPV is set to ´0´, additionally the global registers **REGFP** and **REGFD** must be written with the following sequence to configure the best performance of the Bipolar Violation detection for all four channels:

- Write ´$2C_H$´ into REGFP
- Write ´$FF_H$´ into REGFD
- Write ´$AC_H$´ into REGFP
- Write ´$2B_H$´ into REGFP
- Write ´$00_H$´ into REGFD
- Write ´$AB_H$´ into REGFP
- Write ´$2A_H$´ into REGFP
- Write ´$FF_H$´ into REGFD
- Write ´$AA_H$´ into REGFP
- Write ´$29_H$´ into REGFP
- Write ´$FF_H$´ into REGFD
- Write ´$A9_H$´ into REGFP
- Write ´$28_H$´ into REGFP
- Write ´$00_H$´ into REGFD
- Write ´$A8_H$´ into REGFP
- Write ´$27_H$´ into REGFP
- Write ´$FF_H$´ into REGFD

- Write ´A7$_H$´ into REGFP
- Write ´00$_H$´ into REGFP

Note that the configuration of the Bipolar Violation detection by these sequence is reset by a receive reset (**CMDR**.RRES = ´1´)

## 3.7 Receive Path

An overview about the receive path of one channel of the QuadLIU™ is given in **Figure 22**.

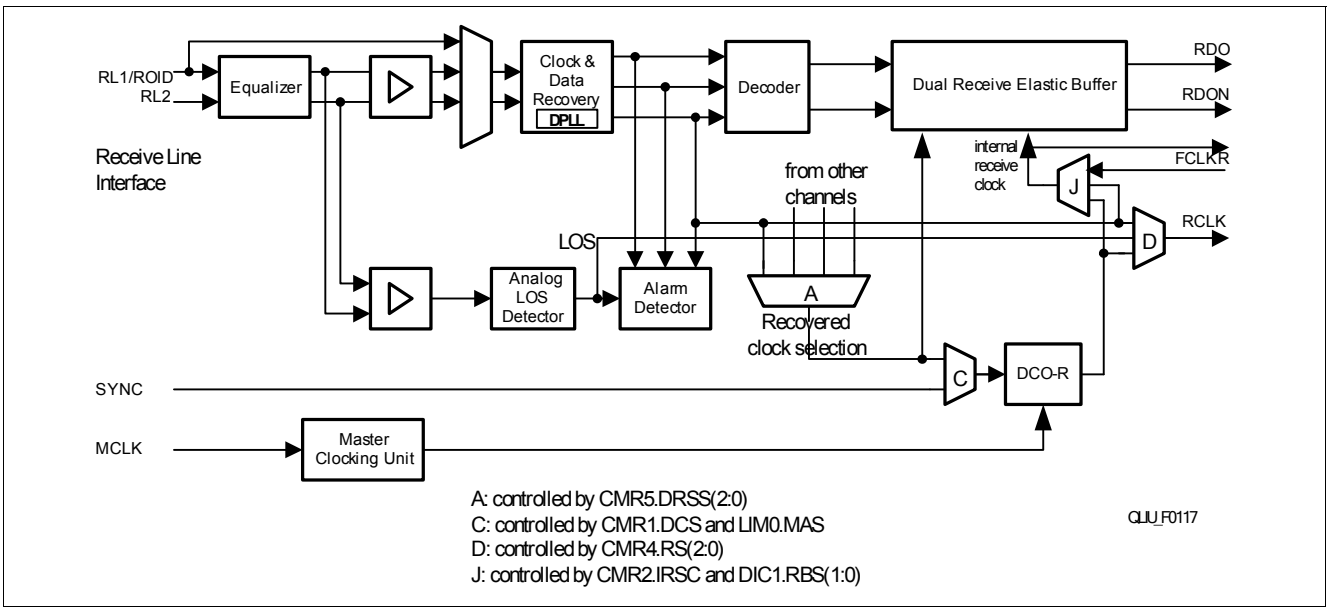



**Figure 22 Receive System of one Channel**

The recovered clock selection of **Figure 22** (multiplexer “A”) is shown in more detail in **Figure 23**.

The multiplexer “C” in **Figure 22** selects the mode of the receive jitter attenuator, see chapter **Chapter 3.7.8**.

The multiplexer “D” in **Figure 22** selects if the receive clock RCLK of a channel is sourced by the recovered route clock or by the DCO-R (see above). The appropriate control register bits are CMR4.RS(2:0) (**CMR4**). These register bits selects also different DCO-R output frequencies.

The sources of the receive clock output pins of the QuadLIU™ (RCLK(4:1)), can be selected out of the receive clocks of the channels:

The source of each of the four receive clock pins of the QuadLIU™ (RCLK(4:1)) can be independently selected out of each of the four receive clocks of the channels by programming the registers bits GPC(2:6).RS(2:0) (**GPC2**), see cross connection “B” in **Figure 23**.

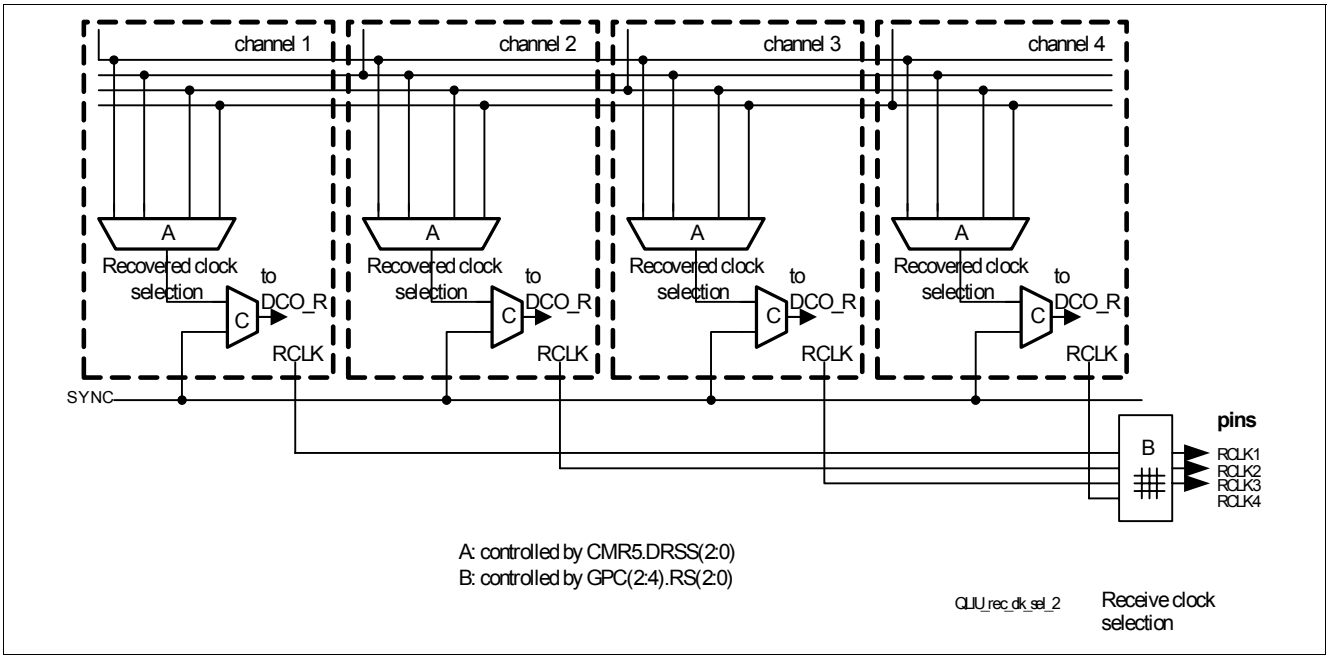



**Figure 23 Recovered and Receive Clock Selection**

### 3.7.1 Receive Line Interface

For data input, two different data types are supported:

- Ternary coded signals received at pins RL1 and RL2 from 0 dB downto -43 dB for E1 or downto -36 dB for T1/J1 ternary interface. The ternary interface is selected if LIM1.DRS is cleared.
- Unipolar data (CMI code) on pin ROID received from an optical interface. The optical interface is selected if LIM1.DRS is set and MR0.RC(1:0) = ´$01_b$´.

### 3.7.2 Receive Line Coding

In E1 applications, HDB3 line code and AMI coding is provided for the data received from the ternary interface. In T1/J1 mode, B8ZS and AMI code is supported. Selection of the receive line code is done with register bits MR0.RC(1:0) (**MR0**). In case of the optical interface the CMI Code (1T2B) with HDB3 or AMI postprocessing is provided. If CMI code is selected the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. The HDB3 code is used along with double violation detection or extended code violation detection (selectable by MR0.EXZE)). In AMI code all code violations are detected. The detected errors increment the code violation counter (16 bits length).

The signal at the ternary interface is received at both ends of a transformer.

An overview of the receive line coding is given in **Table 13**.

### 3.7.3 Receive Line Interface

Each of the QuadLIU™ receivers includes an integrated switchable resistor $R_{TERM}$ = 300 Ω .

Only for P/PG-LBGA-160-1 package it also includes an integrated analog switch, see **Figure 24**. In this case the connectors RLAS2(1:4) must not be connected to VSSX. This allows the device to support 100 Ω T1, 110 Ω J1, 120 Ω E1 and 75 Ω E1 applications with a single bill of materials (so called “generic” modes).

The 300 Ω switch is controlled by the registerbit LIM0.RTRS (**LIM0**). The multi purpose analog switch is controlled by LIM2.MPAS. So a simple software controlling of both switches is possible, independent from one another.

To enable switching of the separate analog switches of all four ports in general the register bits GPC(3:6).ENMPAS must be all set to ´1´. This is an additional protection to avoid closing of the analog switches if its connectors RLAS2(1:4) are connected to VSSX in fully QuadLIU™ Version 1.2 hardware compatible

applications. **Closing of the separate analog switches if its connectors RLAS2(1:4) are connected to VSSX the device might get demaged.**

It is also possible to control both switches by using a combination of both hardware and software using one (but not more) of the receive Multi Function Ports as a Receive Line Termination (RLT) input.

It is proposed that the Multi Function Port RPB be used for the RLT input, if this is the case then the PC2.RPC2(3:0) register bits must be programed to ´$1000_b$´, see **Table 34**.

If RLT is configured at one of the Multi Function Ports, the $R_{TERM}$ = 300 Ω switch is controlled by the logical function (LIM0.RTRS == RLT) & LIM2.MPAS and the analog switch is controlled by the logical function LIM0.RTRS == RLT, were "==" means logical equivalence.

This enables a simple redundancy application using only one common board signal for switching between two channels. While one channel terminates the receive line with an impedance matched to the line impedance $Z_0$, the other channel is in high impedance mode (both switches are óff´).

**Table 14** shows the controlling of the switches (if GPC(3:6).ENMPAS = ´$1111_b$´).

**Table 14 Controlling of the Receive Interface Switches**

| 300 Ohm Switch | Analog Switch | RLT is not Configured | | RLT is Configured | |
|---|---|---|---|---|---|
| | | LIM0.RTRS | LIM2.MPAS | LIM0.RTRS == RLT | LIM2.MPAS |
| off | off | 0 | 0 | 0 | X |
| off | on | 0 | 1 | 1 | 0 |
| on | off | 1 | 0 | Not applicable[1)] | |
| on | on | 1 | 1 | 1 | 1 |

1) Because makes no sense for redundancy applications

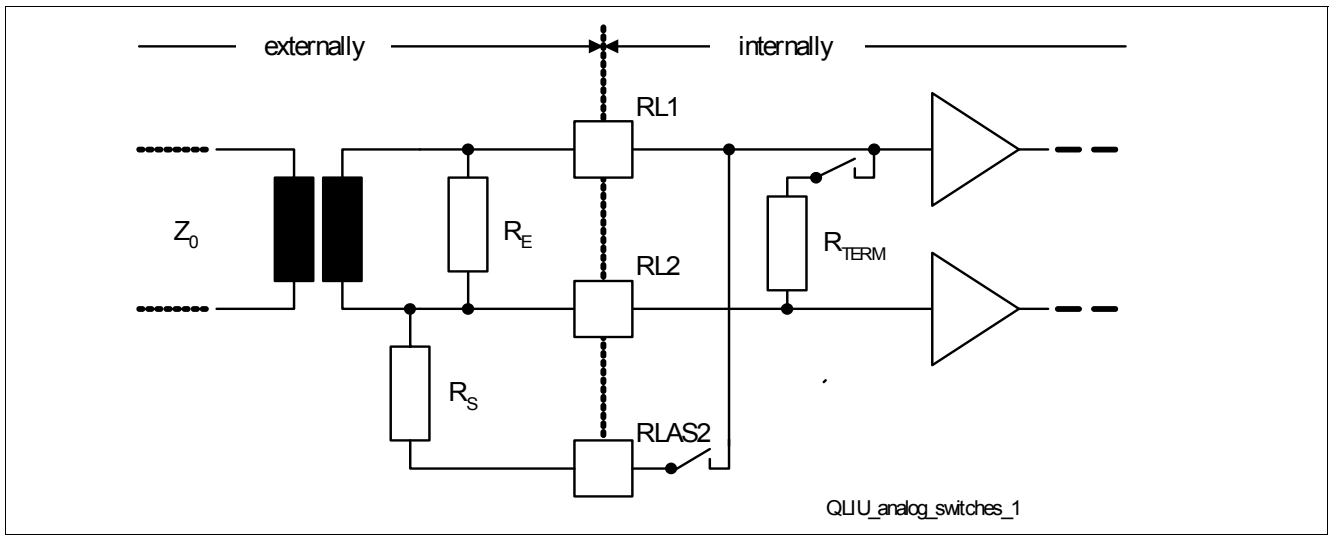



**Figure 24 General Receiver Configuration with Integrated Resistor and Analog Switches for Receive Impedance Matching**

This type of control offers very flexible receiver configurations which are described in the next chapters:

### 3.7.3.1 "Generic" Receiver Interface

A "generic" receiver configuration, using the same resistor $R_E$ = 100 Ω for all applications with different line impedances $Z_0$, is shown in **Table 15**.

**Table 15 Generic Receiver Configuration Example**

| Line Impedance $Z_0$ | External Resistor $R_E$ | External Resistors $R_{S1}$ and $R_{S2}$ | 300 Ohm Switch | Analog Switch |
|---|---|---|---|---|
| 120 Ω | 100 Ω (for common E1/T1/J1 applications) | ---- | off | not used |
| 100 Ω | | | off | |
| 75Ω | | | on | |

This example uses the 300 Ω switch to switch between 100 Ω and 75 Ω termination resistance for the different line impedances, the analog switch is not used.

### 3.7.3.2 Receive Line Monitoring Mode (RLM)

For short-haul monitoring applications, the receive equalizer can be switched into receive line monitoring mode (RLM) by setting of the register bit LIM0.RLM. One channel is used as a short-haul receiver while the other is used as a short-haul monitor, see **Figure 25**. In this mode the receiver sensitivity of the monitor is increased to detect an incoming signal of -20 dB resistive attenuation.

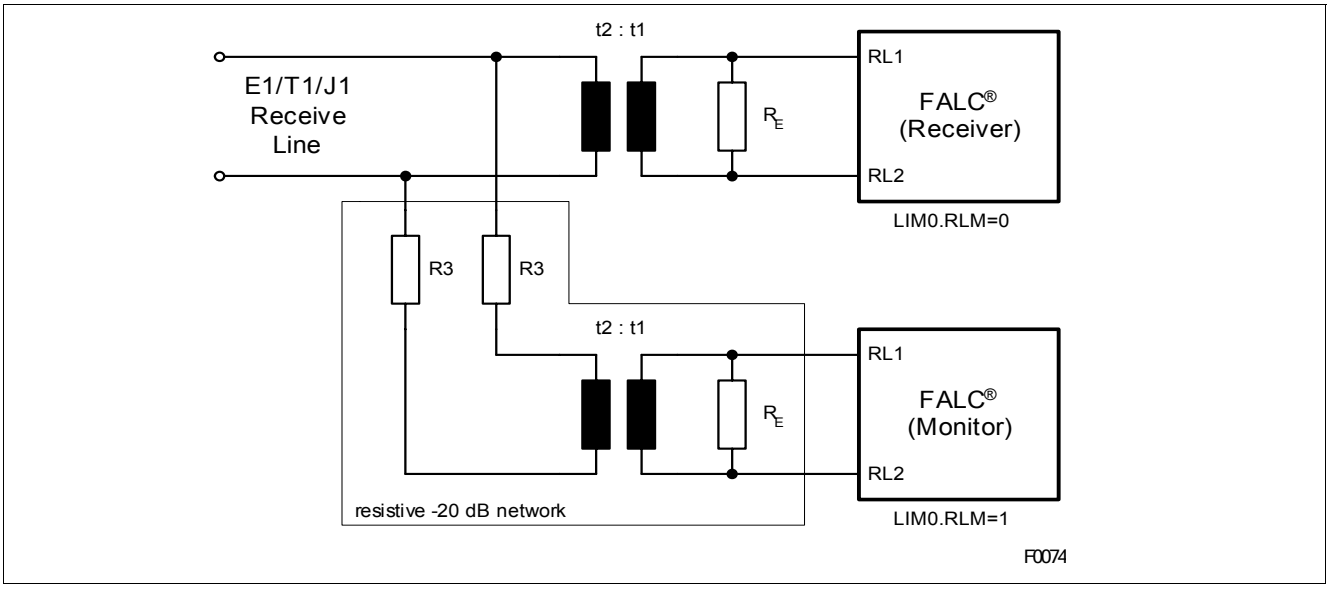



**Figure 25 Principle of Receive Line Monitoring RLM (shown for one line)**

### 3.7.3.3 Monitoring Application using RLM

A monitoring application using the receive line monitoring mode is shown in **Figure 26**. Both, the 300 Ω switch and the separate analog switch are always óff´, so that in P/PG-LBGA-160-1 package the pins RLAS2 can be connected to VSSX and HW compatibility to the QuadLIU™ V2.1 is fullfiled.

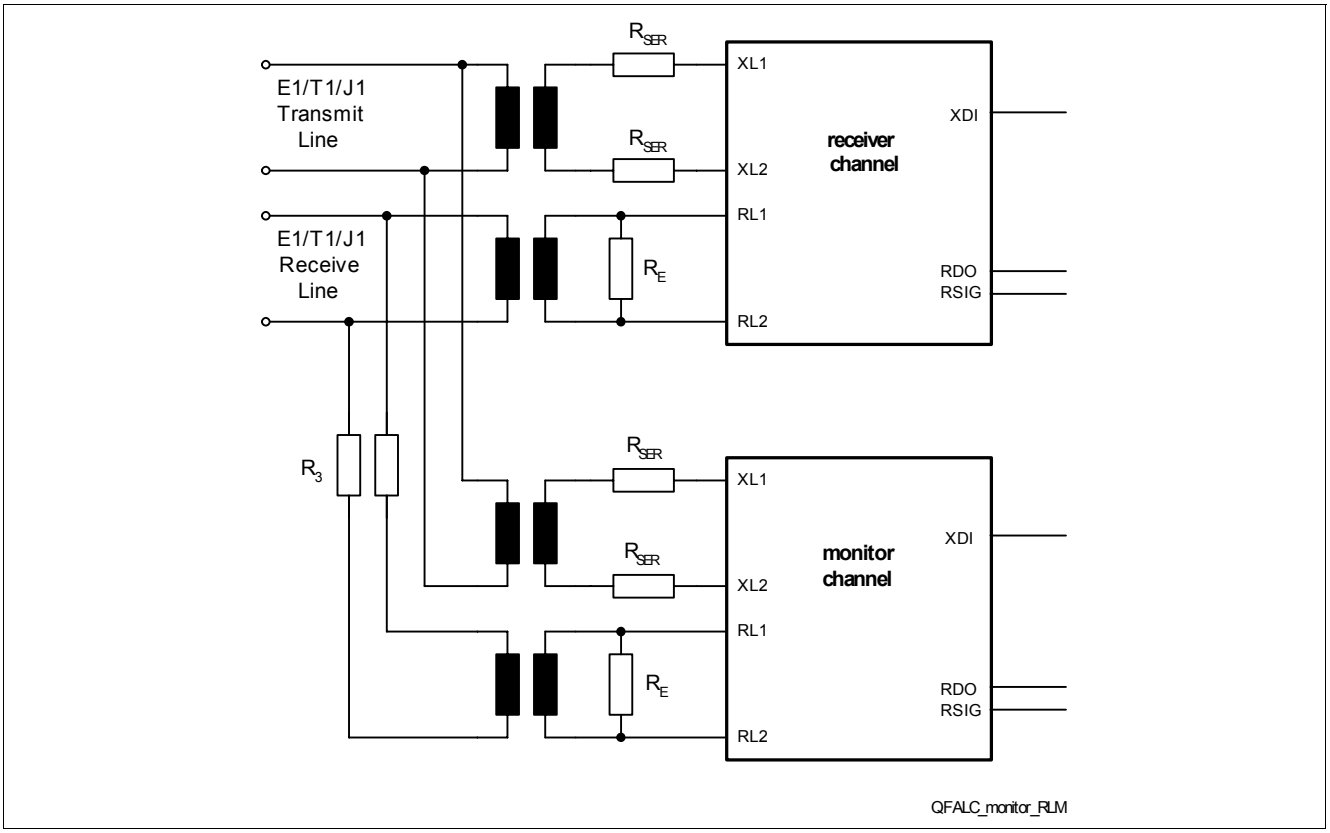



**Figure 26 Monitoring Application using RLM (shown for one line)**

The required resistor and transformer values are given in **Table 16**.

**Table 16 External Component Recommendations for Monitoring Applications using RLM**

| Parameters of external components[1)] | Line Impedance $Z_0$ | | Line Impedance $Z_0$ | |
|---|---|---|---|---|
| | E1 | | T1 | J1 |
| | **75 Ohm** | **120 Ohm** | **100 Ohm** | **110 Ohm** |
| $R_E$ (±1 %) | 75 Ω | 120 Ω | 100 Ω | 110 Ω |
| $R_3$ (±1 %) | 330 Ω | 510 Ω | 430 Ω | 470 Ω |
| $R_{SER}$ | See **Chapter 3.9.1** | | | |
| $t_2 : t_1$ | 1 :1 | 1 :1 | 1 : 1 | 1 : 1 |

1) This includes all parasitic effects caused by circuit board design.

### 3.7.3.4 Redundancy Application using RLM

In general for redundancy applications (“protection switching”) one channel is active while the other is in stand-by mode.

Switching between active and stand-by mode can be done by software and by hardware.

Software controlled switching can be done on the line side in transmit direction by using the register bit XPM2.XLT.

Combined hardware and software controlled switching can be done on the line side in transmit direction by a hardware signal if a Multi Function Port is configured as tristate input XLT. It is proposed that the Multi Function Port XPA be used for XLT or $\overline{XLT}$ input respectively, if this is the case then the PC1.XPC1(3:0) register bits must be programed, see **Table 34**. For one channel the Multi Function Port XPA must be programmed as low active (PC1.XPC1 = ´$1110_b$´) and for the other channel as high active (PC1.XPC1 = ´$1000_b$´), so that no external inverter

is necessary. So switching between both channels on line side is possible using only one signal as it is shown in **Figure 27**.

If XLT or $\overline{\text{XLT}}$ is configured, the value of the register bit XPM2.XLT and the value of XLT are logically ored to control the transmit line side. (That means if XPA is configured as low active then the line side is in tristate mode for

tristate = XPM2.XLT or not($\overline{\text{XPA}}$).

Because the register bit XPM2.XLT and the Multi Function Port XPA exist individually for every channel, switching on the line side in transmit direction can be done between channels of different or of the same QuadLIU™ device.

This enables a simple application using only one common board signal for switching between two channels were both transmit channels are working in parallel (see **Figure 27**). While one of them is driving the line, the other one is switched into transmit line tristate mode.

The receive system interface pins RDO, RSIG, SCLKR and RFM can be set by software into tristate mode constantly using the register bit SIC3.RRTRI. In this mode “tristate” means high impedance against $V_{DD}$ and $V_{SS}$: No internal pull up or pull down resistor is present.

Combined hardware and software controlling of the tristate mode can be done by a hardware signal if a Multi Function Port is configured as RTDMT input . It is proposed that the Multi Function Port RPA be used for RTDMT, if this is the case then the PC1.RPC1(3:0) register bits must be programed, see **Table 34**. If RTDMT is configured the value of the register bit SIC3.RRTRI and the value of RTDMT are logically exored.

This enables a simple application using only one common board signal for switching between two channels. While one of them is driving the system receive interface, the other one is switched into tristate mode.

An overview about the tristate configurations of RDO, RSIG, SCLKR and RFM is given in **Table 17**.

**Table 17 Tristate Configurations for the RDO, RSIG, SCLKR and RFM Pins**

| SIC3.RRTRI / SIC3.RRTRI exor RTDMT if RTDMT is selected on Multi Function Port | SIC3.RTRI | Pins RDO and RSIG | Pins SCLKR and RFM |
|---|---|---|---|
| 1 | X | Constant tristate (without pull up and pull down resistor) | Constant tristate (without pull up and pull down resistor) |
| 0 | 0 | Never tristate | Never tristate |
| 0 | 1 | Tristate during inactive channel phases (with pull up resistor | Never tristate |

Switching between both channels can be done on the system side in the receive direction by using the register bit SIC3.RRTRI and with or without selection of the Multi Function Port as RTDMT. If the RTDMT function is selected, the values of RTDMT and SIC3.RRTRI are logically exored. If in one channel SIC3.RRTRI is set, RTDMT is active low because of the logical exor, and if in the other channel SIC3.RRTRI is cleared, RTDMT is active low because of the logical exor. So switching between both channels on the system side in the receive direction is possible using only one board signal.

For application using RLM for protection switching the XLT, $\overline{\text{XLT}}$ and RTDMT Multi Function Ports operate in conjunction with the SIC3.RRTRI bits. Switching between channels can be done together on the system and the line side with only one common board signal, connected to XPA (XLT, $\overline{\text{XLT}}$) and RPA (RTDMT), as shown in **Figure 27** and **Table 17**: If this signal has low level channel 1 is active and channel 2 is in stand-by, if it has high level channel 1 is in stand-by and channel 2 is active.

Different line impedances require different resistor values as shown in **Table 16**. Both switches are always off so that LIM0.RTRS and GPC1.MPAS must be always ´0´.

If both channels are configured identically and supplied with the same system data and clocks, the transmit path can be switched from one channel to the other without causing a synchronization loss at the remote end.

**Table 18 Configuration for Redundancy Application using RLM, switching with only one board signal**

| Configuration | Register Bits | Channel 1 (active/stand-by) | Channel 2 (stand-by/active) |
|---|---|---|---|
| XLT, $\overline{XLT}$ | PC1.XPC1(3:0) | 1000 | 1110 |
| RTDMT | PC1.RPC1(3:0) | 1101 | 1101 |
| Receive system interface | SIC3.RRTRI | 0 | 1 |
| RLM mode | LIM0.RLM | 0 | 1 |
| Analog switch (always off) | LIM2.MPAS | 0 | 0 |
| 300 Ω switch (always off) | LIM0.RTRSS | 0 | 0 |

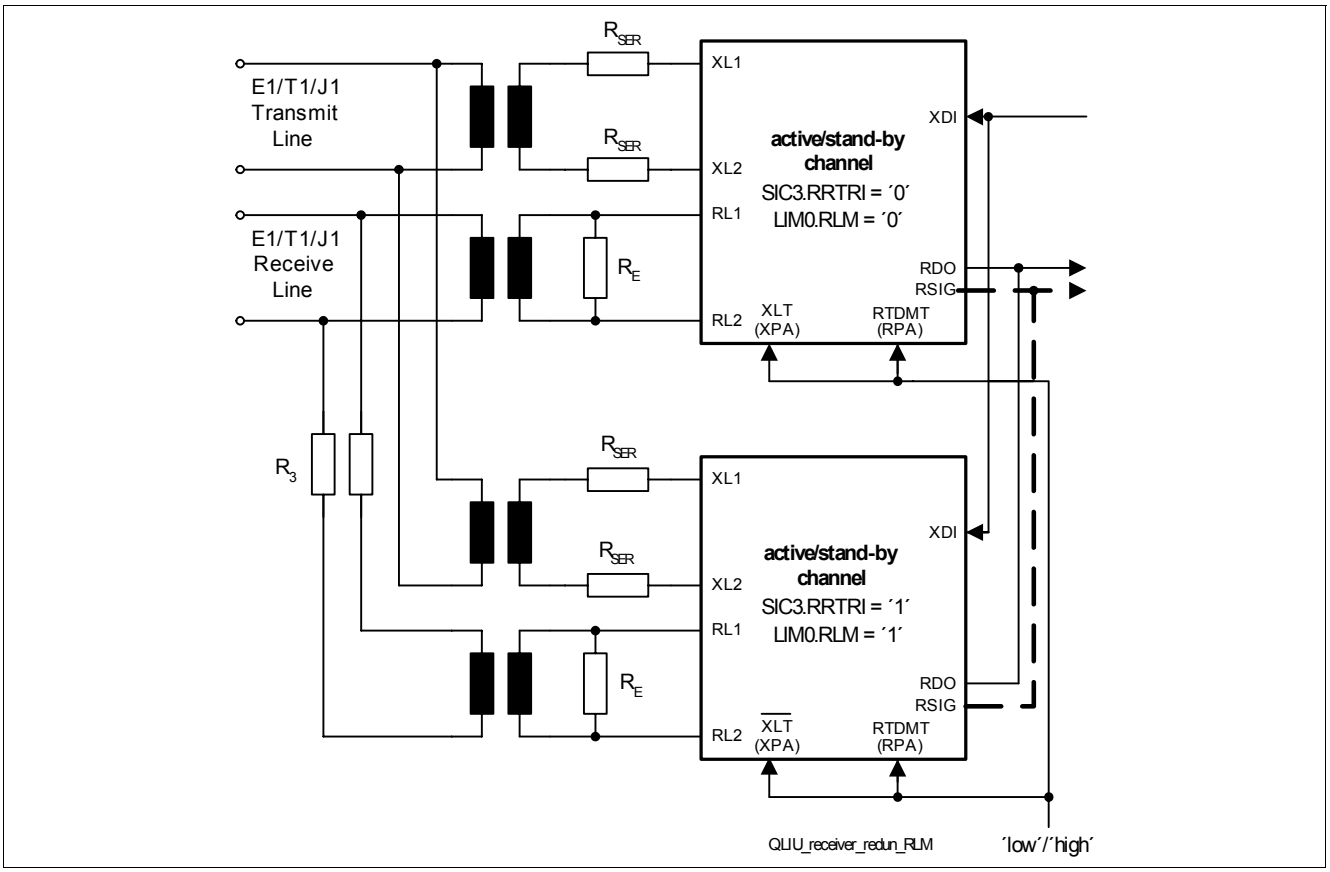



**Figure 27 Redundancy Application using RLM (shown for one line)**

### 3.7.3.5 General Redundancy Applications

Using the integrated analog switch of the QuadLIU™ general redundancy applications are possible were no additional resistive network is necessary. Therefore, unlike in the redundancy application using RLM, long haul redundancy applications are possible as there are no serial resistors in the receive path.

For these applications all of the hardware control functions described in **Chapter 3.7.3.4** are used in the same way. Additionally the hardware control function of the receive interface switches is used: By configuring one of the Multi Function Ports in both of the two channels to RLT, the receive interfaces of these channels can be connected on one receive line as shown in **Figure 28**.

If RLT is configured at the Multi Function Port RPB (proposed) by programming of the register bits PC2.RPC2(3:0) the configuration for the redundancy mode application is listed in **Table 19**.

The analog switch is connected at the resistor $R_S$.

Switching between active and stand-by modes can be achieved by a single common board signal which is connected at the RLT, XLT and RTDMT inputs of both channels . In this application both receive channels are working in parallel for redundancy purpose. While one of them builds an interface with a receive termination resistance matched to the line impedance $Z_0$ , the other one is switched into high impedance mode.

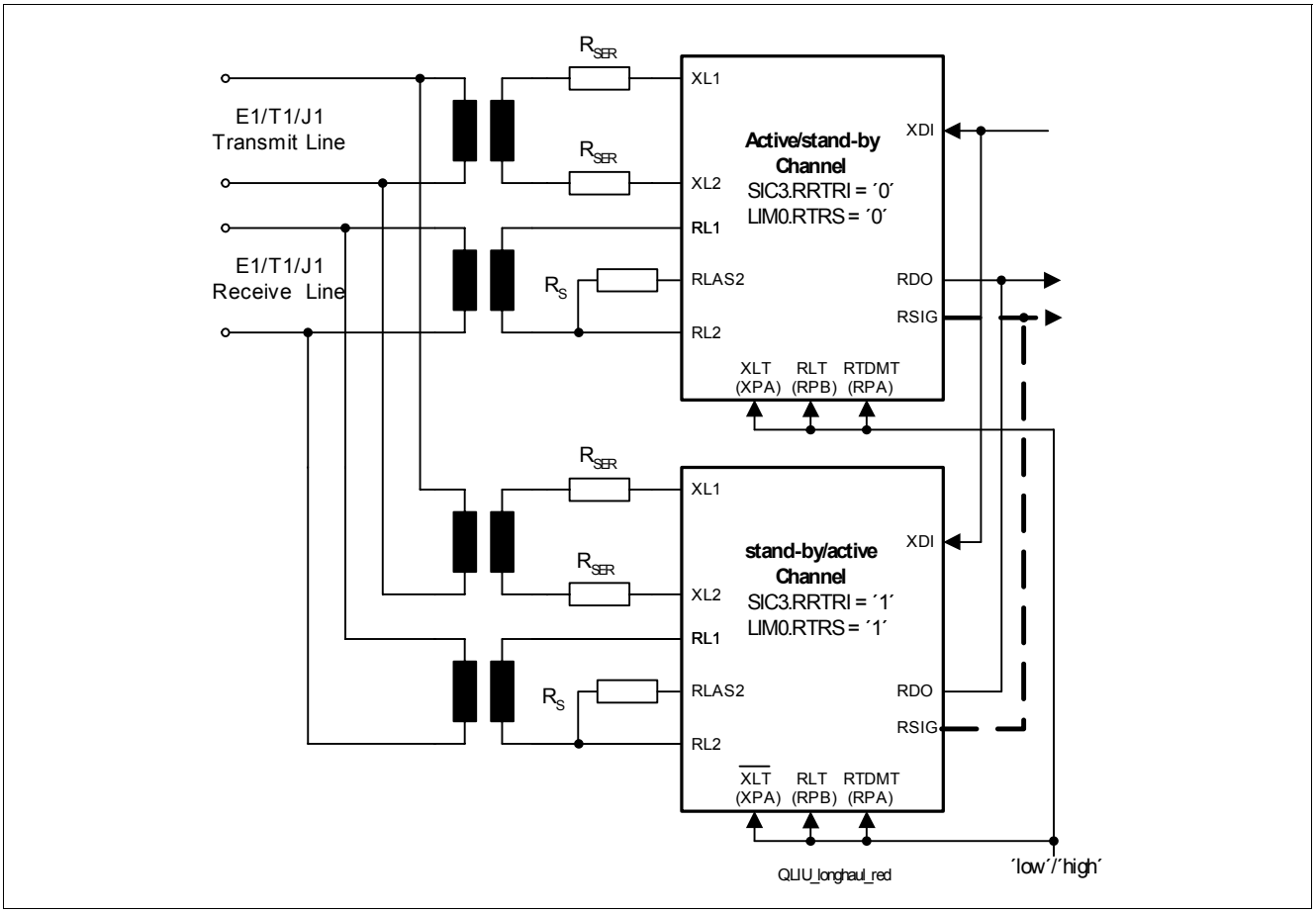



**Figure 28 General Redundancy Application (shown for one line)**

**Table 19 General (proposed) Configuration for Redundancy Applications, Switching with only one Board Signal**

| Configuration | Register Bits | Channel 1 (active/stand-by) | Channel 2 (stand-by/active) |
|---|---|---|---|
| XLT, $\overline{XLT}$ | PC1.XPC1(3:0) | 1000 | 1110 |
| RTDMT | PC1.RPC1(3:0) | 1101 | 1101 |
| RLT | PC2.RPC2(3:0) | 1000 | 1000 |
| Receive system interface | SIC3.RRTRI | 0 | 1 |
| Receive line interface | LIM0.RTRS | 0 | 1 |
| RLM mode | LIM0.RLM | 0 | 0 |

Two types of general redundancy applications like shown in **Figure 28** can be configured:

- A first application were the values of the external resistors $R_S$ and $R_{SER}$ are dependend on the line impedance $Z_0$.
- A so called “generic” redundancy application were the values of the external resistors $R_S$ and $R_{SER}$ are fix for different line impedances $Z_0$.

For both applications the general configuration shown in **Table 19** is used.

In the first (“non-generic”) application only the analog switch is used. These switch is ´on´ in the active and ´off´ in the stand-by channel. The 300 Ω switch is unused (always ´off´, register bit LIM2.MPAS of both channels is always ´0´). Also the transmit interface works in a non-generic mode (see **Chapter 3.9.1**): The register bit PC6.TSRE of both channels is always ´0´. The configuration (additional to that of **Table 19**) is shown in **Table 20**:

**Table 20 Configuration for “non-generic” Redundancy Applications, Switching with only one Board Signal**

| Line Impedance $Z_0$ [Ohm] | $R_S$ [Ohm] | $R_{SER}$ [Ohm] | LIM2.MPAS | PC6.TSRE |
|---|---|---|---|---|
| 120 | 95 | 5.5 or 0, see **Table 28** | 0 | 0 |
| 110 | | | | |
| 100 | | | | |
| 75 | 70 | | | |

In the generic redundancy application different line impedances $Z_0$ can be used without changing the board. Additionally to the the analog switch the 300 Ω switch is used to match the termination resistance to the different line impedances $Z_0$ (register bit LIM2.MPAS of both channels). In the active channel this switch is ´on´ if the line impedance is 75 Ω and ´off´ otherwise. In the stand-by channel this switch is always óff´, see **Table 22**.

Also the transmit interface works in a generic mode (see **Chapter 3.9.1**) using the register bit PC6.TSRE of both channels.

The configuration (additional to that of **Table 19**) is shown in **Table 21**:

**Table 21 Configuration for “generic” Redundancy Applications, Switching with only one Board Signal**

| Line Impedance $Z_0$ [Ohm] | $R_S$ [Ohm] | $R_{SER}$ [Ohm] | LIM2.MPAS | PC6.TSRE |
|---|---|---|---|---|
| 120 | 95 | 0 | 0 | See **Table 28** |
| 110 | | | | |
| 100 | | | | |
| 75 | | | 1 | |

**Table 22** illustrates the switching in the receive path used in the “generic” redundancy application:

**Table 22 Switching in “Generic” Redundancy Application**

| Channel | 300 Ohm Switch | Analog Switch |
|---|---|---|
| Active channel | Off, if $Z_0$ is 120 Ω,110 Ω or 100 Ω (GPC1.MPAS = ´0´)<br>On, if $Z_0$ is 75 Ω (LIM2.MPAS = ´1´) | On |
| Stand-by channel | Off | Off |

## 3.7.4 Loss-of-Signal Detection

There are different definitions for detecting Loss-Of-Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The QuadLIU™ covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable by using register GCR.SCI.

- Detection: An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS = ´0´) (**LIM1**). The receive signal level Q is programmable by three control bits LIM1.RIL(2:0) see **Table 56**. The number N can be set by an 8-bit register (PCD). The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, i.e. the time which has to suspend until the alarm has to be detected. The programmable range is 16 to 4096 pulse

periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS is detected.

- Recovery: In general the recovery procedure starts after detecting a logical one (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL(2:0)) of the nominal pulse. The value in the 8-bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm.

If a loss-of-signal condition is detected in long-haul mode, the data stream can optionally be cleared automatically to avoid bit errors before LOS is indicated. The Selection is done by LIM1.CLOS = ´1´.

### 3.7.5 Receive Equalization Network

The QuadLIU™ automatically recovers the signals received on pins RL1 and RL2 in a range of up to -43 dB for E1 or -36 dB for T1/J1. The maximum reachable length with a 22 AWG twisted pair cable is about 1500 m for E1 and about 2000m (~6560 ft) for T1. The integrated receive equalization network recovers signals with up to -43 dB for E1 or -36 dB for T1/J1 of cable attenuation automatically. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak-detected and sliced to produce the digital data stream. The slicing level is software selectable in four steps (45%, 50%, 55%, 67%), see **Table 56**. For typical E1 applications, a level of 50% is used. The received data is then forwarded to the clock & data recovery unit.

### 3.7.6 Receive Line Attenuation Indication

Status register RES reports the current receive line attenuation

- For E1 in a range from 0 to -43 dB in 25 steps of approximately 1.7 dB each.
- For T1/J1 in a range from 0 to -36 dB in 25 steps of approximately 1.4 dB each.

The least significant 5-bits of this register indicate the cable attenuation in dB. These 5-bits are only valid in combination with the most significant two bits (RES.EV(1:0) = ´$01_b$´).

### 3.7.7 Receive Clock and Data Recovery

The analog received signal on pins RL1 and RL2 is equalized and then peak-detected to produce a digital signal. The digital received signal on pins RDIP and RDIN is directly forwarded to the clock & data recovery. The so called DPLL (digital PLL) of the receive clock & data recovery extracts the route clock from the data stream received at the RL1/2 or ROID lines. The clock & data recovery converts the data stream into a dual-rail, unipolar bit stream. The clock and data recovery uses an internally generated high frequency clock out of the master clocking unit based on MCLK.

The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI.

### 3.7.8 Receive Jitter Attenuator

The receive jitter attenuator is based on the DCO-R (digital clock oscillator, receive) in the receive path. Jitter attenuation of the received data is done in the dual receive elastic buffer. The working clock is an internally generated high frequency clock based on the clock provided on pin MCLK. The jitter attenuator meets the E1 requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13 and the T1 requirements of AT&T PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824.

The internal PLL circuitry DCO-R generates a "jitter-free" output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock. The receive jitter attenuator can be synchronized either on the extracted receive clock RCLK or on a 2.048 MHz/8 kHz or 1.544 MHz/8 kHz clock provided on pin SYNC (8 kHz in master mode only). The jitter attenuated DCO-R output clock can be output on pin RCLK and FCLKR. Optionally an 8 kHz clock is provided on pin SEC/FSC.

For jitter attenuation the received data is written into the receive elastic buffer with the recovered clock sourced by the clock & data recovery and are read out with the de-jittered clock sourced by DCO-R.

If the receive elastic buffer is read out directly with the recovered receive clock, no jitter attenuation is performed.

If the receive elastic buffer is read out with the receive framer clock FCLKR, the receive elastic buffer performs a clock adoption from the recovered receive clock to FCLKR.

The DCO-R circuitry attenuates the incoming jittered clock starting at its corner frequency with 20 dB per decade fall-off. Wander with a jitter frequency below the corner frequency is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

The corner frequency of the DCO-R can be configured in a wide range, see **Table 23** and **Figure 29**. The jitter attenuator PLL in the transmit path, so called as DCO-X, is equivalent to the DCO-R so that the principle for its configuring is the same.

**Table 23 Overview DCO-R (DCO-X) Programming**

| CMR6.DCOCOMPN | CMR2.ECFAR (CMR2.ECFAX) | LIM2.SCF (CMR6.SCFX) | CMR3.CFAR(3:0) (CMR3.CFAX(3:0)) | CMR4.IAR(3:0) (CMR5.IAX(4:0)) | Corner-frequencies of DCO-R (DCO-X) E1 / T1 |
|---|---|---|---|---|---|
| X | 0 | 0 | Not used | Not used | 2 Hz / 6 Hz |
| X | 0 | 1 | Not used | Not used | 0.2 Hz / 0.6 Hz |
| 0 | 1 | X | $7_H$´<br>´$4_H$´ | Not used | 0.2 Hz / 0.6 Hz<br>2 Hz / 6 Hz |
| 1 | 1 | X | ´$0_H$´ ...´$F_H$´ , used as proportional parameter<br><br>´$9_H$´<br>´$8_H$´<br>´$6_H$´<br>´$4_H$´<br>´$3_H$´<br>´$2_H$´<br>´$1_H$´ | ´$00_H$´ ...´$1F_H$´ used as integral parameter<br><br>´$19_H$´<br>´$13_H$´<br>´$12_H$´<br>´$0F_H$´<br>´$0C_H$´<br>´$0A_H$<br>´$08_H$´ | Range 0.2 Hz ... 100 Hz<br><br>0.2 Hz<br>0.6 Hz<br>2 Hz<br>6 Hz<br>25 Hz<br>50 Hz<br>100 Hz |

After reset the corner frequencies are 2 Hz in E1 and 6 Hz in T1/J1 mode and can be switched to 0.2 Hz in E1 mode or 0.6 Hz n T1 mode by setting the register bit LIM2.SCF for the DCO-R or the register bit CMR5.SCFX for the DCO-X respectively. A logical table builds the integral (I) and proportional (P) parameter for the PI filter of the DCO-R or DCO-X, see **Figure 29**.

If the register bits CMR2.ECFAR or CMR2.ECFAX are set for the DCO-R or the DCO-X respectively, the corner frequencies can be configured in a range between 2 Hz and 0.2 Hz using the register bits CMR3.CFAR(3:0) or CMR3.CFAX(3:0) respectively, see **CMR3**, **CMR4** and **CMR5**. A logical table builds the integral and proportional parameter for the PI filter of the DCO-R or DCO-X out of the settings in CMR3.CFAR(3:0) or CMR3.CFAX(3:0) respectively.

If additionally to CMR2.ECFAR or CMR2.ECFAX the bit CMR6.DCOCOMPN (**CMR6**) is set, which is valid for the DCO-R and the DCO-X, the corner frequencies and attenuation factors can be programmed in a wide range using the register bits CMR3.CFAR(3:0) and CMR4.IAR(4:0) for the DCO-R and CMR3.CFAX(3:0) and CMR5.IAX(4:0) for the DCO-X. The settings in CMR3.CFAR(3:0)/CFAX(3:0) build the proportional parameter, the settings in CMR4.IAR(4:0) and CMR5.IAX(4:0) build the integral parameter for the PI filters, independent from another.

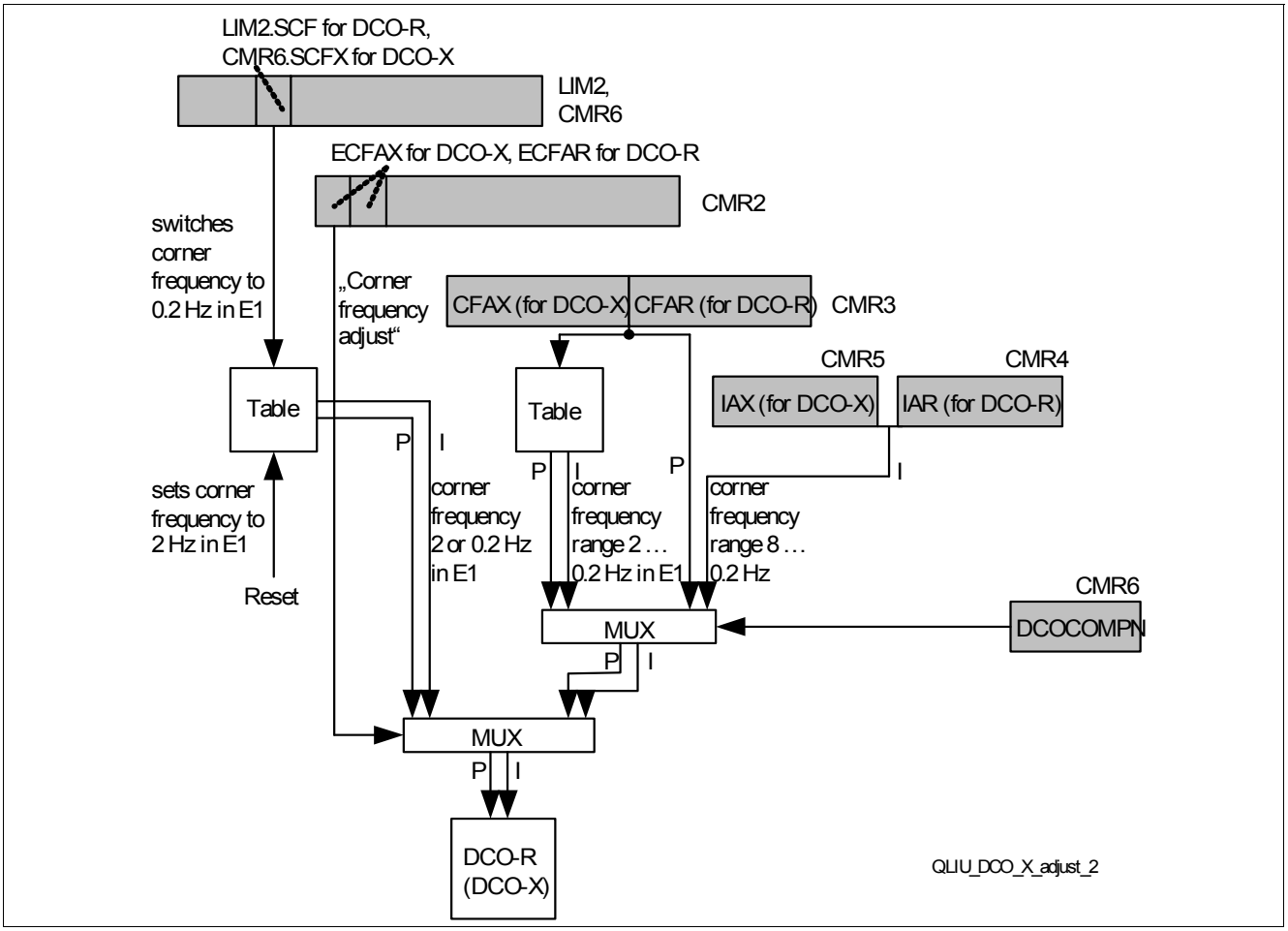



**Figure 29 Principle of Configuring the DCO-R and DCO-X Corner Frequencies**

The DCO-R reference clock is watched: If one, two or three clock periods of the 2.048 MHz (1.544 MHz in T1/J1 mode) clock at pin SYNC or RCLKI (in single rail digital line interface mode) are missing the DCO-R regulates it´s output frequency. If four or more clock periods are missing

- The DCO-R circuitry is automatically centered to the nominal bit rate if the center function of DCO-R is enabled by CMR2.DCF = ´0´.
- The actual DCO-R output frequency is “frozen” if the center function of DCO-R is disabled by CMR2.DCF = ´1´.

The receive jitter attenuator works in two different modes, selected by the multiplexer “C” in **Figure 22**:

- Slave mode: In slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss of signal (LOS) the DCO-R switches automatically to Master mode. The frequency at the pin SYNC must be 2.048 MHz (1.544 MHz). If bit CMR1.DCS is set automatic switching from the recovered route clock to SYNC is disabled.
- Master mode: In master mode (LIM0.MAS = ´1´) the DCO-R is in free running mode if no clock is supplied on pin SYNC. If an external clock on the SYNC input is applied, the DCO-R synchronizes to this input. The external frequency can be 2.048 MHz (1.544 MHz) for IPC.SSYF = ´0´ or 8.0 kHz for IPC.SSYF = ´1´.

The following table **Table 24** shows this modes with the corresponding synchronization sources.

**Table 24 Clocking Modes of DCO-R**

| Mode | Internal LOS Active | SYNC Input | System Clocks generated by DCO-R |
|---|---|---|---|
| Master | Independent | Fixed to $V_{DD}$ | DCO-R centered, if CMR2.DCF = ´0´. (CMR2.DCF should not be set), see also **CMR2** |
| Master | Independent | 2.048 MHz (E1) or 1.544 MHz (T1) | Synchronized to SYNC input (external 2.048 MHz or 1.544 MHz, IPC.SSYF = ´0´), see also **IPC** |
| Master | Independent | 8.0 kHz | Synchronized to SYNC input (external 8.0 kHz, IPC.SSYF = ´1´, CMR2.DCF = ´0´) |
| Slave | No | Fixed to $V_{DD}$ | Synchronized to recovered line clock |
| Slave | No | 2.048 MHz (E1) or 1.544 MHz (T1) | Synchronized to recovered line clock |
| Slave | Yes | Fixed to $V_{DD}$ | CMR1.DCS = ´0´: DCO-R is centered, if CMR2.DCF = ´0´. (CMR2.DCF should not be set) |
| | | | CMR1.DCS = ´1´: Synchronized on recovered line clock |
| Slave | Yes | 2.048 MHz | CMR1.DCS = ´0´: Synchronized to SYNC input (external 2.048 MHz or 1.544 MHz) |
| | | | CMR1.DCS = ´1´: Synchronized on recovered line clock |

The receive clock output RCLK of every channel can be switched between 2 sources, see multiplexer “D” in **Figure 22**:

- If the DCO-R is the source of RCLK the following frequencies are possible: 1.544, 3.088, 6.176, and 12.352 in T1/J1 mode and 2.048, 4.096, 8.192, and 16.384 MHz in E1 mode. Controlling of the frequency is done by the register bits CMR4.RS(1:0).
- If the recovered clock out (of the clock and data recovery) is the source of RCLK (see multiplexer “D” in **Figure 22**), only 2.048 MHz (1.544 MHz) is possible as output frequency.

### 3.7.8.1 Receive Jitter Attenuation Performance

For E1 the jitter attenuator meets the jitter transfer requirements of the ITU-T I.431 and G.735 to 739 (refer to **Figure 30**)

For T1/J1 the jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431 and G.703 (refer to **Figure 31**).

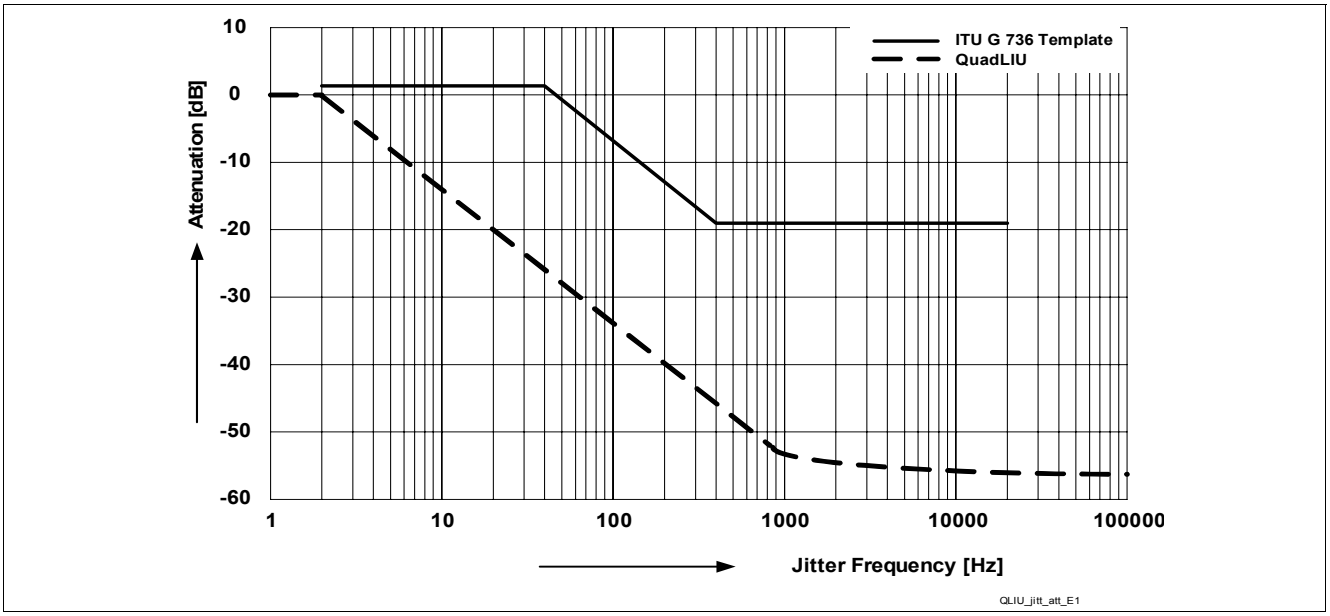



**Figure 30 Jitter Attenuation Performance (E1)**

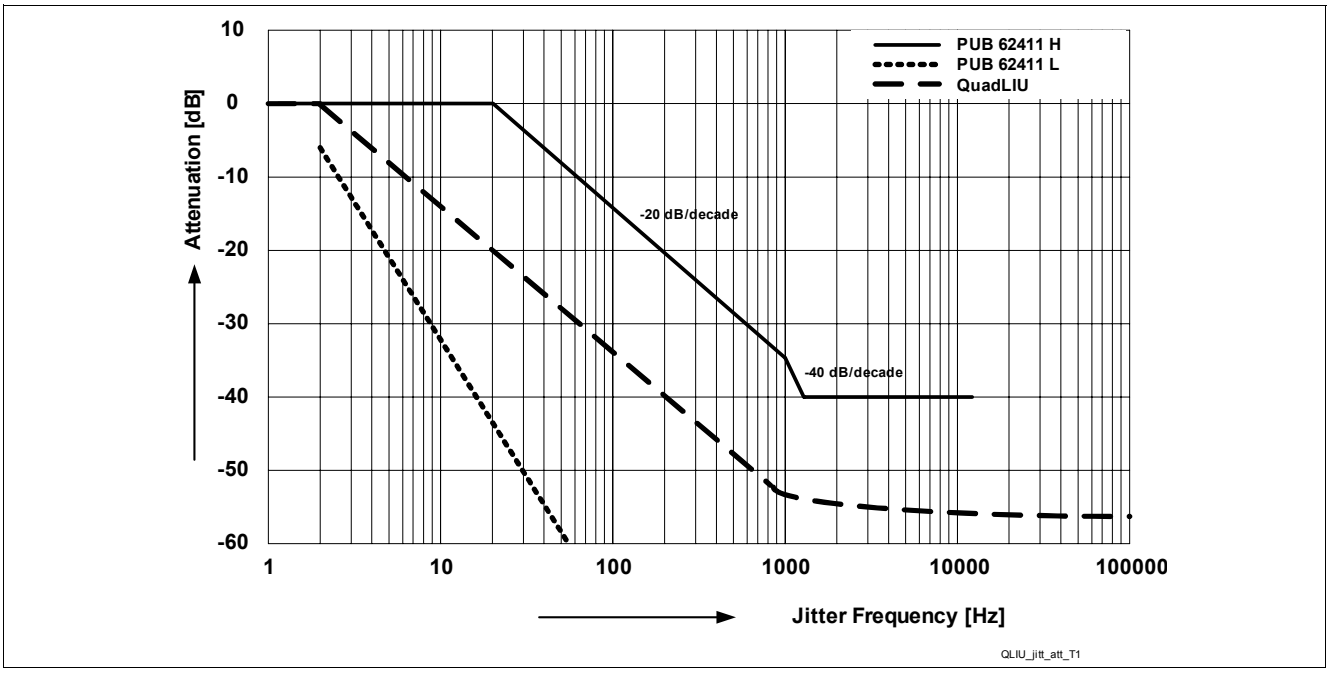



**Figure 31 Jitter Attenuation Performance (T1/J1)**

Also the requirements of ETSI TBR12/13 are satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the DCO-R circuitry starts jitter attenuation at about 2 Hz.

### 3.7.8.2 Jitter Tolerance (E1)

The QuadLIU™ receiver's tolerance to input jitter complies with ITU for CEPT applications.

**Figure 32** and **Figure 33** shows the curves of different input jitter specifications stated below as well as the QuadLIU™ performance.

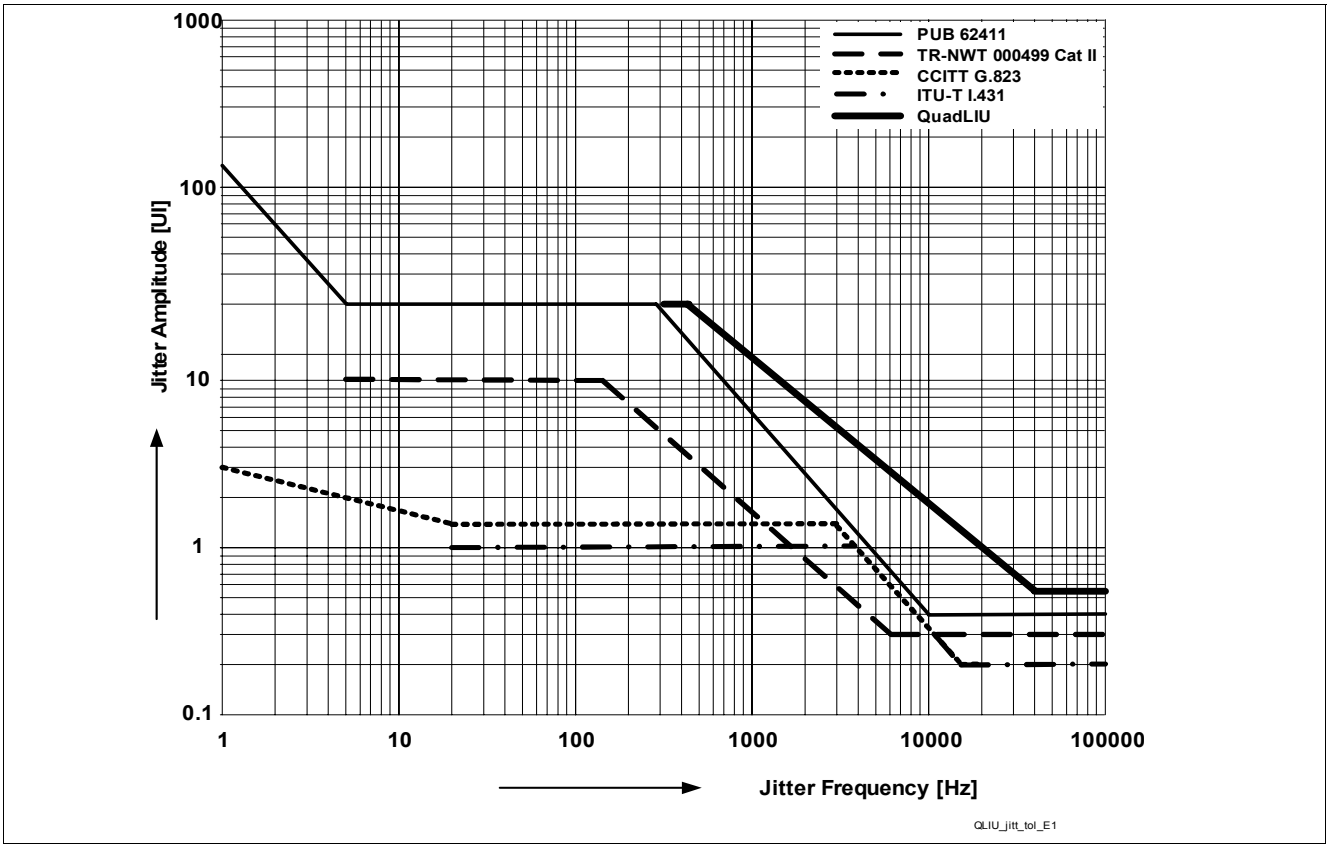



**Figure 32 Jitter Tolerance (E1)**

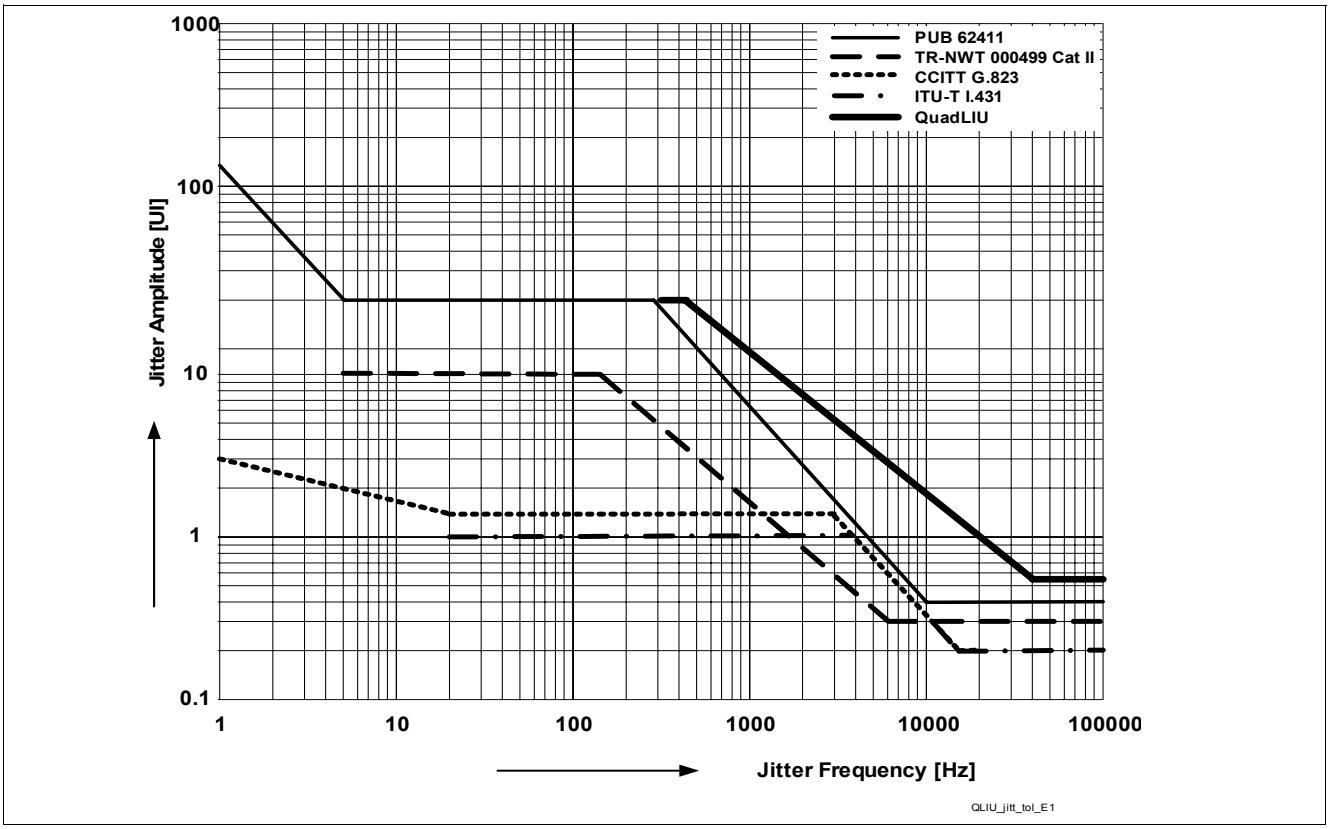



**Figure 33 Jitter Tolerance (T1/J1)**

### 3.7.8.3 Output Jitter

In the absence of any input jitter the QuadLIU™ generates the intrinsic output jitter, which is specified in the**Table 25** below.

**Table 25 Output Jitter**

| Specification | Measurement Filter Bandwidth | | Intrinsic Output Jitter (UI peak to peak) |
|---|---|---|---|
| | Lower Cutoff | Upper Cutoff | |
| ITU-T I.431 | 20 Hz | 100 kHz | < 0.015 |
| | 700 Hz | 100 kHz | < 0.015 |
| ETSI TBR 12 | 40 Hz | 100 kHz | < 0.11 |
| PUB 62411 | 10 Hz | 8 kHz | < 0.015 |
| | 8 Hz | 40 kHz | < 0.015 |
| | 10 Hz | 40 kHz | < 0.015 |
| | Broadband | | < 0.02 |

### 3.7.8.4 Output Wander

**Figure 34** shows 2 curves for the output wander. For both, setting of the register bits of GCM1 to GCM8 is identical to **Table 49**.

Curve 1 gives the default output wander were no additional programming of bits of registers **GPC6**, **REGFP**, **REGFD** and **WCON** is necessary as described below. The corner frequency of the DCO-R is 2 Hz (see **Table 23**).

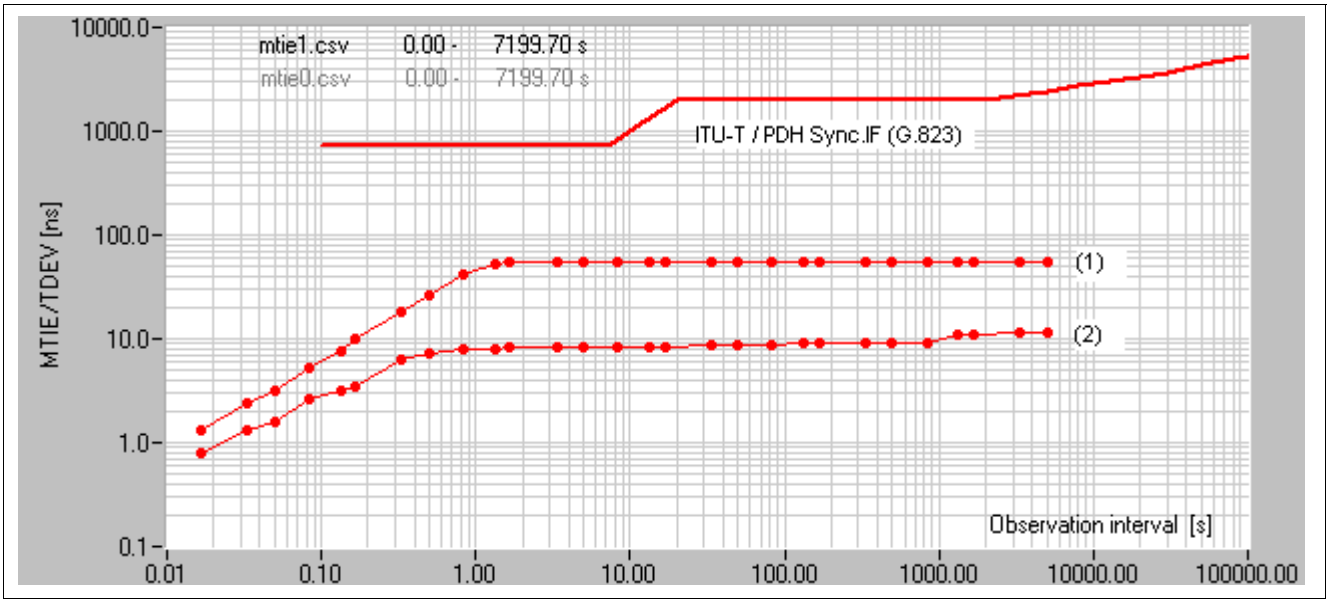



**Figure 34 Output Wander**

For further improvement of the output wander (curve 2), the following programming of register bits must be done:

- **GPC6**. WAND_IMP = ´1´
- **WCON**.WAND = ´$03_H$´

After that, the global registers **REGFP** and **REGFD** must be written with the following sequence to improve the output wander for both channels:

- Write ´$30_H$´ into REGFP
- Write ´$AA_H$´ into REGFD
- Write ´$B0_H$´ into REGFP
- Write ´$31_H$´ into REGFP

- Write ´$00_H$´ into REGFD
- Write ´$B1_H$´ into REGFP
- Write ´$32_H$´ into REGFP
- Write ´$AA_H$´ into REGFD
- Write ´$B2_H$´ into REGFP
- Write ´$33_H$´ into REGFP
- Write ´$00_H$´ into REGFD
- Write ´$B3_H$´ into REGFP

Note that these wander configuration is reset by a receive reset (**CMDR**.RRES = ´1´)

Using this programming and 2 Hz for the corner frequency of the DCO-R, the output wander is given by curve 2.

### 3.7.9 Dual Receive Elastic Buffer

For jitter attenuation the received data is written into the receive elastic buffer with the recovered clock sourced by the clock & data recovery and are read out with the de-jittered clock sourced by DCO-R, see **Figure 22**.

If the receive elastic buffer is read out directly with the recovered receive clock, no jitter attenuation is performed.

If the receive elastic buffer is read out with the receive framer clock FCLKR of the framer interface (FCLKR is input), the receive elastic buffer performs a clock adoption from the recovered receive clock to FCLKR.

The receive elastic buffer can buffer two data streams so that dual rail mode is possible at the receive framer interface (RDOP/RDON). In case of single rail mode on the receive framer interface, the bipolar violation signal BPV is buffered in the same way as the single rail signal and is supported at multi function pin RDON.

The size of the elastic buffer can be configured independently for the receive and transmit direction. Programming of the receive buffer size is done by DIC1.RBS(1:0), of the transmit buffer size by DIC1.XBS(1:0) see **Table 26**:

**Table 26 Receive (Transmit) Elastic Buffer Modes**

| DIC1.RBS(1:0) | (DIC1.XBS(1:0)) | Mode | Frame buffer size (bits) | Maximum of wander (UI = 648 ns) | Average delay after performing a slip | Slip Performance |
|---|---|---|---|---|---|---|
| 00 | 10 | E1 | 512 | 190 | 256 | Yes |
| | | T1/J1 | 396 | 140 | 193 | |
| 01 | 01 | E1 | 256 | 100 | 128 | |
| | | T1/J1 | 193 | 74 | 96 | |
| 10 | 11 (short buffer mode) | E1 | 96 | 38 | 48 | |
| | | T1/J1 | | | | |
| 11 | 00 | E1 | Bypass of the receive (transmit) elastic buffer | | | No |
| | | T1/J1 | Bypass of the receive (transmit) elastic buffer | | | |

The functions are:

- Clock adoption between framer receive clock (FCLKR input) and internally generated route clock (recovered line clock), see **Chapter 3.7.8**.
- Compensation of input wander and jitter.
- Reporting and controlling of slips

In “one frame” or short buffer mode the delay through the receive buffer is reduced to an average delay of 128 or 46 bits. In bypass mode the time slot assigner is disabled. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

**Figure 35** gives an idea of operation of the dual receive elastic buffer: A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive

backplane interface. I.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

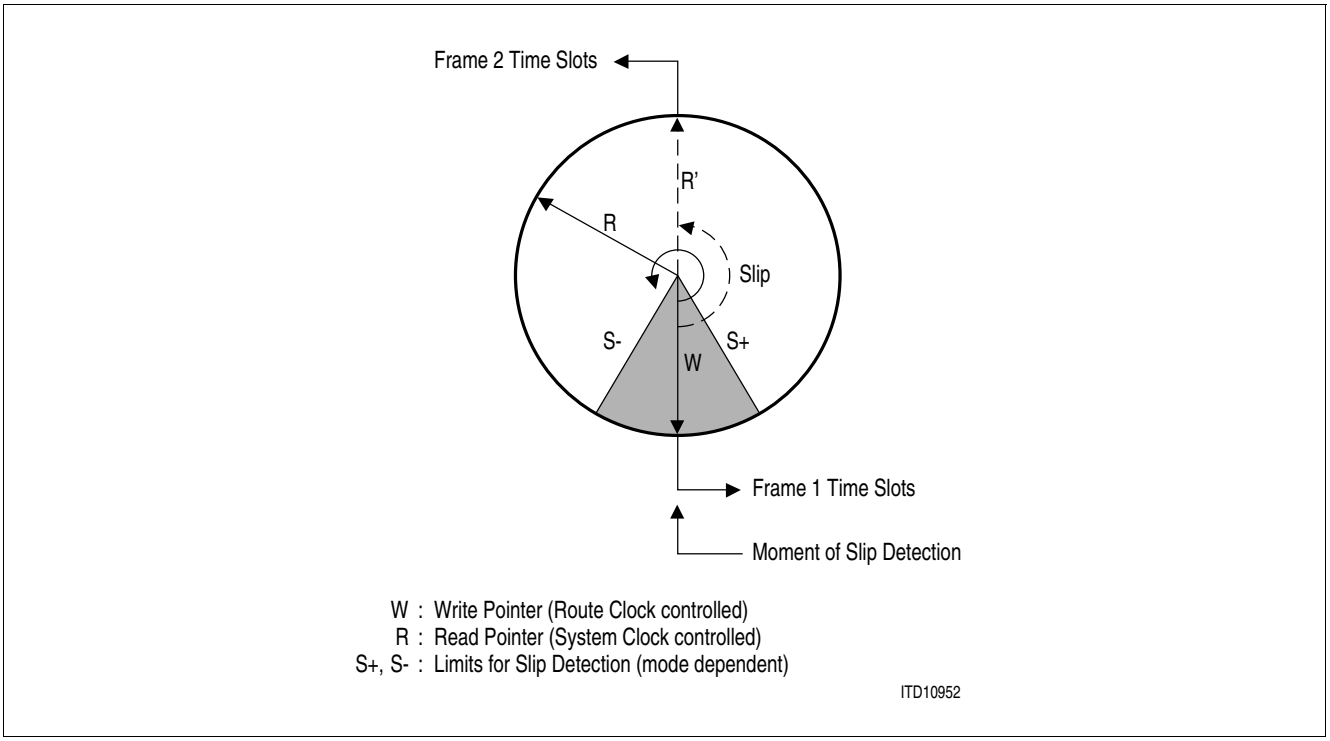



**Figure 35 The Receive Elastic Buffer as Circularly Organized Memory**

## 3.8 Additional Receiver Functions

### 3.8.1 Error Monitoring and Alarm Handling

The following error monitoring and alarm handling is supported by the QuadLIU™:

- Loss-Of-Signal: Detection and recovery is flagged by bit LSR0.LOS and ISR2.LOS.
- Transmit Line Shorted: Detection and release is flagged by bit LSR1.XLS and ISR1.XLSC
- Transmit Ones-Density: Detection and release is flagged by bit LSR1.XLO and ISR1.XLSC

**Table 27 Summary of Alarm Detection and Release**

| Alarm | Detection Condition | Clear Condition |
|---|---|---|
| Loss-Of-Signal (LOS) | No transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods. Programmable receive input signal threshold | Programmable number of ones (1 to 256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold. |
| Transmit Line Short (XLS) | More than 3 pulse periods with highly increased transmit line current on XL1/2 | Transmit line current limiter inactive, see also **Chapter 3.9.7** |
| Transmit Ones-Density (XLO) | 32 consecutive zeros in the transmit data stream on XL1/2 | Cleared with each transmitted pulse |

### 3.8.2 Automatic Modes

The following automatic modes are performed by the QuadLIU™:

- Automatic clock source switching (see also: In slave mode (LIM0.MAS = ´0´) the DCO-R synchronizes to the recovered route clock. In case of loss-of-signal (LOS) the DCO-R switches to Master mode automatically. If bit CMR1.DCS is set, automatic switching from the recovered route clock to SYNC is disabled. See also **Table 24**.
- Automatic transmit clock switching, see **Chapter 3.9.3**.
- Automatic local and remote loop switching based on In-Band loop codes, see **Chapter 3.11.2**.

### 3.8.3 Error Counter

The QuadLIU™ offers two error counters where each of them has a length of 16 bit:

- Code Violation Counter, status registers CVCL and CVCH
- PRBS error counter, status registers BECL and BECH

The error counters are buffered. Buffer updating is done in two modes:

- One-second accumulation
- On demand by handshake with writing to the DEC register

In the one-second mode an internal/external one-second timer updates these buffers and resets the counter to accumulate the error events in the next one-second period. The error counter cannot overflow. Error events occurring during an error counter reset are not lost.

### 3.8.4 One-Second Timer

A one-second timer interrupt can be generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one-second timer signal is output on port SEC/FSC if configured by GPC1.CSFP(1:0) (**GPC1**). Optionally synchronization to an external second timer is possible which has to be provided on pin SEC/FSC. Selecting the external second timer is done with GCR.SES.

## 3.9 Transmit Path

The transmit path of the QuadLIU™ is shown in **Figure 36**.

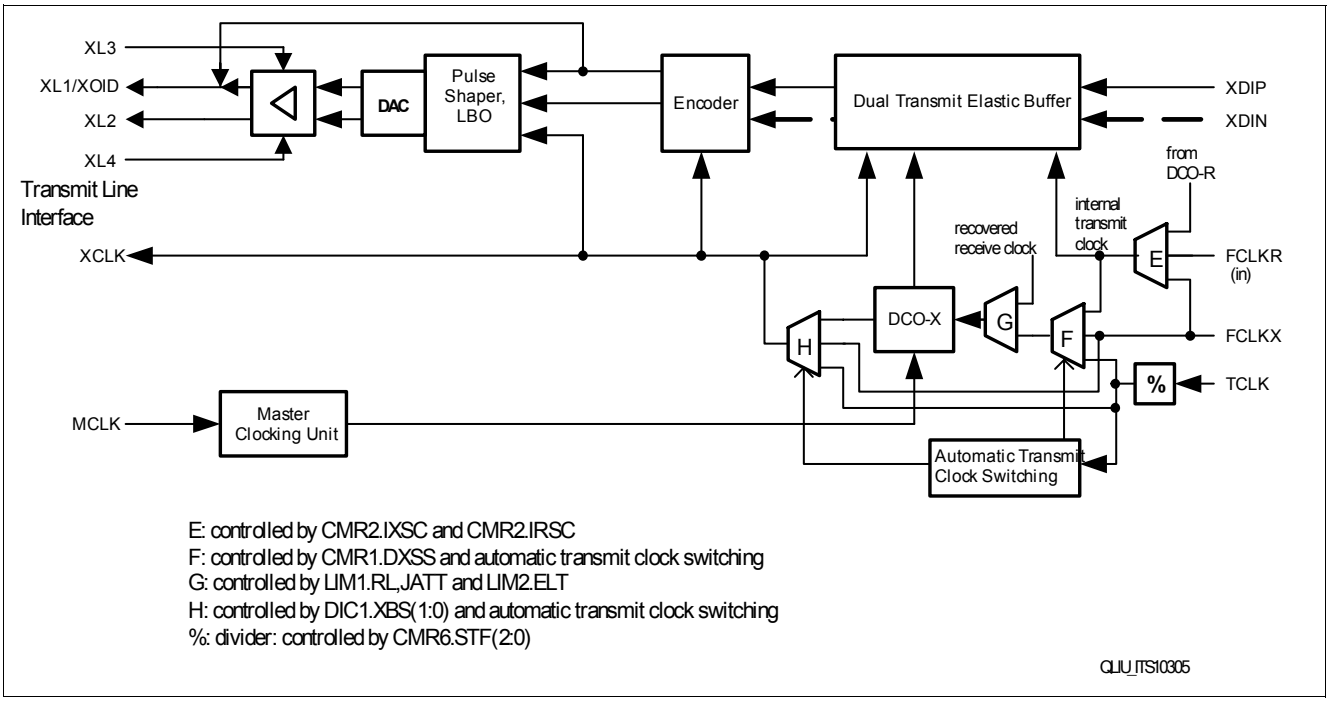



**Figure 36 Transmit System of one Channel**

The serial transmit bit stream (single rail or dual rail) is processed by the transmitter which has the following functions:

- AIS generation (blue alarm)
- Generation of In-band loop-up/-down code

### 3.9.1 Transmit Line Interface

The transmit line interface includes two integrated serial resistors $R_{TX}$ as shown in **Figure 37**. Two application modes are possible:

- For non-generic applications the external serial resistance $R_{SER}$ is dependent on the operation mode (E1/T1/J1) as shown in **Table 28**. The additional register bit PC6.TSRE is not used, $R_{TX}$ is always 2 Ω
- For generic E1/T1/J1 applications with optimized return loss the transmit output resistance $R_{TX}$ is configured by the register bit PC6.TSRE: The operation mode (E1/T1/J1) is selected by software without the need for external hardware changes: Here the external resistor $R_{SER}$ is always 0 Ω, see **Table 28**.

In E1 mode the value of $R_{SER}$ in **Table 28** is valid for both characteristic line impedances $Z_0$ = 120 Ω and $Z_0$ = 75 Ω.

Note that shorts between XL1 and XL2 cannot be detected, because the short circuit current is lower than 120 mA. This way a short between XL1 and XL2 will not harm the device

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided on pin XDI and the digital transmitter.

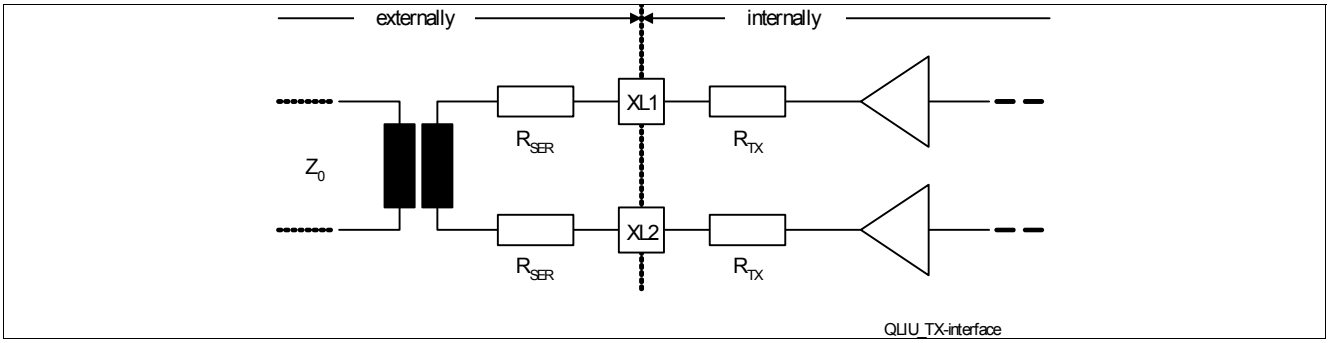



**Figure 37 Transmit Line Interface**

**Table 28 Recommended Transmitter Configuration Values**

| $R_{SER}$ (Ohm), accuracy +/- 1 % | Application Mode | PC6.TSRE | XL3, XL4 | Operation Mode |
|---|---|---|---|---|
| 2[1)] | Generic | 1 | Connected to $R_{SER}$ and Xformer junction | E1 |
| 2 | | 0 | | T1/J1 |
| 7.5 | Non generic | 0 | Left open | E1 |
| 2 | | 0 | Left open | T1/J1 |

1) The values in this column refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

Similar to the receive line interface two different data types are supported:

- Ternary Signal: Single-rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding is provided.
- Unipolar data on port XOID is transmitted in CMI code with or without (DIC3.CMI) preprocessed by B8ZS coding or HDB3 precoding (MR3.CMI) to a fiber-optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (1544 kHz) and with a programmable polarity. Selection is done by MR0.XC1 = ´0´ and LIM1.DRS = ´1´.

An overview of the transmit line coding is given in **Table 13**.

### 3.9.2 Transmit Clock TCLK

The transmit clock input TCLK (multi function port) of the QuadLIU™ can be configured for 1.544, 3.088, 6.176, 12.352 and 24.704 MHz input frequency in T1/J1 mode and 2.048, 4.096, 8.192, 16.384 and 32.768 MHz input frequency in E1 mode. Frequency selection is done by the register bits CMR6.STF(2:0) (**CMR6**). See divider “%” in **Figure 36**.

### 3.9.3 Automatic Transmit Clock Switching

The transmit clock output XCLK can be derived from TCLK

- Directly. In this case the TCLK frequency must be 32.768 MHz in E1 or 24.704 MHz in T1/J1 mode. or
- With using the DCO-X, were the DCO-X reference is TCLK.

If TCLK fails, the transmit clock output XCLK will also fail. To avoid this, a so called automatic transmit clock switching can be enabled by setting the register bit CMR6.ATCS (**CMR6**). Then FCLKX will be used instead of TCLK if TCLK is lost. The transmit elastic buffer must be active. Automatically switching between TCLK and FCLKX is done in the following both cases:

- If the TCLK input is used directly as source for the transmit clock XCLK, the output of the DCO-X is not used. The DCO-X reference clock is FCLKX. If loss of TCLK is detected, the transmit clock XCLK will be switched automatically (if CMR6.ATCS = ´1´) to the DCO-X output which is synchronous to FCLKX (see multiplexer “H” in **Figure 36**). If XCLK was switched to the DCO-X output and TCLK becomes active, switching of XCLK (back)

to TCLK is automatically performed if CMR6.ATCS = ´1´. All switchings of XCLK between TCLK and the DCO-X output are shown in the interrupt status bit ISR7.XCLKSS0 which is masked by IMR7.XCLKSS0. These kinds of switching cannot be done in general without causing phase jumps in the transmit clock XCLK. Additionally after loss of TCLK the transmit clock XCLK is also lost during the “detection time” for loss of TCLK and the transmit pulses are disturbed. If CMR6.ATCS is cleared, TCLK is used (again) as source for the transmit clock XCLK, independent if TCLK is lost or not. The interrupt status bit ISR7.XCLKSS0 will be set also.

- If the transmit clock XCLK is sourced by the DCO-X output and the DCO-X reference clock is TCLK, the DCO-X reference will be switched automatically (if CMR6.ATCS = ´1´) to FCLKX (see multiplexer “F” in **Figure 36**) after a loss of TCLK was detected. If the DCO-X reference was switched to FCLKX and TCLK becomes active, switching of the reference (back) to TCLK is automatically performed if CMR6.ATCS = ´1´. All switchings of the reference between TCLK and FCLKX are shown in the interrupt status bit ISR7.XCLKSS1 which is masked by IMR7.XCLKSS1. For these kinds of automatically switching, the transmit clock XCLK fulfills the jitter-, wander- and frequency deviation- requirements as specified for E1/T1 after the clock source of the DCO-X was changed. If CMR6.ATCS is cleared, TCLK is used (again) as reference for the DCO-X, independent if TCLK is lost or not. The interrupt status bit ISR7.XCLKSS1 will be set also.

The status register bits CLKSTAT.TCLKLOS and CLKSTAT.FCLKXLOS (**CLKSTAT**) show if the appropriate clock is actual lost or not, so together with ISR7.XCLKSS1 and ISR7.XCLKSS0 the complete information regarding the current status of the transmit clock system is provided.

### 3.9.4 Transmit Jitter Attenuator

The transmit jitter attenuator is based on the so called DCO-X (digital clock oscillator, transmit) in the transmit path. Jitter attenuation of the transmit data is done in the transmit elastic buffer, see **Figure 36**. The DCO-X circuitry generates a "jitter-free" transmit clock and meets the E1 requirements of ITU-T I.431, G. 736 to 739, G.823 and ETSI TBR12/13 and the T1 requirements of AT&T PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824. The DCO-X circuitry works internally with the same high frequency clock as the DCO-R. It synchronizes either to the working clock of the transmit system interface (internal transmit clock) or the clock provided on multi function pin TCLK or the receive clock RCLK (remote loop/loop-timed). The DCO-X attenuates the incoming jitter starting at its corner frequency with 20 dB per decade fall-off. With the jitter attenuated clock, which is directly depending on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (512/386 bit) or from the JATT buffer (512/386 bit, remote loop), see **Figure 38**. Wander with a jitter frequency below the corner frequency is passed transparently.

The dual transmit elastic buffer can buffer two data streams so that dual rail mode is possible at the transmit framer interface (XDIP/XDIN).

The DCO-X is equivalent to the DCO-R so that the principle for its configuring is the same, see **Figure 29** and **CMR3**, **CMR4** and **CMR5**.

The DCO-X reference clock is monitored: If one, two or three clock periods of the 2.048 MHz (1.544 MHz in T1/J1 mode) clock at FCLKX are missing the DCO-X regulates it´s output frequency. If four or more clock periods are missing

- The DCO-X circuitry is automatically centered to the nominal frequency of 2.048 MHz (1.544 MHz in T1/J1) if the center function of DCO-X is enabled by CMR2.DCOXC = ´1´.
- The actual DCO-X output frequency is “frozen” if the center function of DCO-R is disabled by CMR2.DCOXC = ´0´.

The jitter attenuated clock is output on pin XCLK if the transmit jitter attenuator is enabled, see multiplexer “H” in **Figure 36**.

The transmit jitter attenuator can be disabled. In that case data is read from the transmit elastic buffer with the clock sourced on pin TCLK, see multiplexer “H” in **Figure 36**. Synchronization between FCLKX and TCLK has to be done externally.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized on RCLK, see **Figure 38** and multiplexers “G” and “F” in **Figure 36**. In this configuration the transmit elastic buffer has to be enabled.

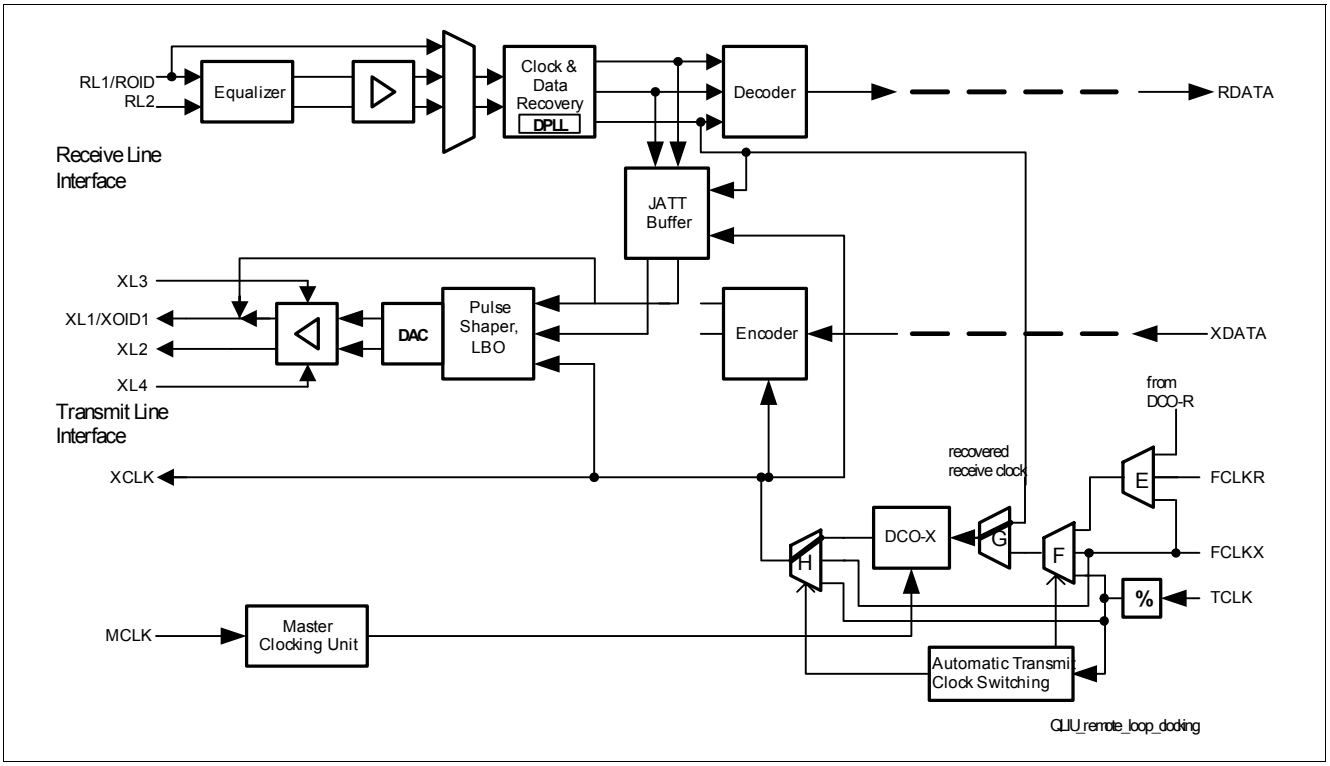



**Figure 38 Clocking and Data in Remote Loop Configuration**

### 3.9.5 Dual Transmit Elastic Buffer

The received single rail bit stream from pin XDI or dual rail bit stream from the pins XDIP and XDIN are optionally stored in the transmit elastic buffer, see **Figure 36**. The tansmit elastic buffer is organized as the receive elastic buffer. The functions are also equal to the receive side. Programming of the dual transmit buffer size is done by DIC1.XBS(1:0) in the same way as programming of the dual receive buffer size by DIC1.RBS(1:0), see **Table 26**:

The functions of the transmit buffer are:

- Clock adoption between framer transmit clock (FCLKX) and internally generated transmit route clock, see **Chapter 3.9.4**.
- Compensation of input wander and jitter.
- Reporting and controlling of slips

Writing of received data from XDIP/XDIN is controlled by the internal transmit clock. Selection of FCLKX or FCLKR is possible, see multiplexer “E” in **Figure 36**. (If the DCO-R output is selected, the DCO_R output is also output at FCLKR.)

Reading of stored data is controlled by the clock generated either by the DCO-X circuitry or the externally generated TCLK. With the de-jittered clock data is read from the dual transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR4.XSP and ISR4.XSN. If the transmit buffer is bypassed data is directly transferred to the transmitter.

### 3.9.6 Programmable Pulse Shaper and Line Build-Out

The transmitter includes a programmable pulse shaper to generate transmit pulse masks according to:

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), see **Figure 64** and **Figure 40** for measurement configuration were $R_{load}$ = 100 Ω
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length) see **Figure 63**; ITU-T G703 11/2001, figure 20 (for DCIM mode), see **Figure 39** for measurement configuration were $R_{load}$ = 120 Ω or $R_{load}$ = 75 Ω

The transmit pulse shape ($U_{PULSE}$) is programmed either

- By the registers XMP(2:0) compatible to the QuadLIU™, see **Table 29** and **Table 30**, if the register bit XPM2.XPDIS is cleared, see **XPM2**
- Or by the registers TXP(16:1), see **TXP1**, if the register bit XPM2.XPDIS is set, see **Table 31** and **Table 32**. For more details see chapter “Operational Description”

To reduce the crosstalk on the received signals in long haul applications the QuadLIU™ offers the ability to place a transmit attenuator (Line Build-Out, LBO) in the data path. This is used only in T1 mode. LBO attenuation is selectable with the values 0, -7.5, -15 or -22.5 dB (register bits **LIM2**.LBO(2:1)). ANSI T1. 403 defines only 0 to -15 dB.

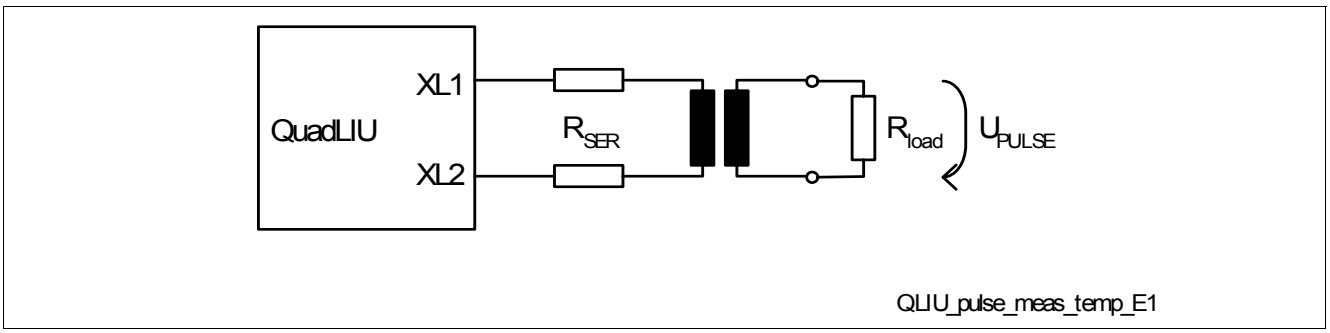



**Figure 39 Measurement Configuration for E1 Transmit Pulse Template**

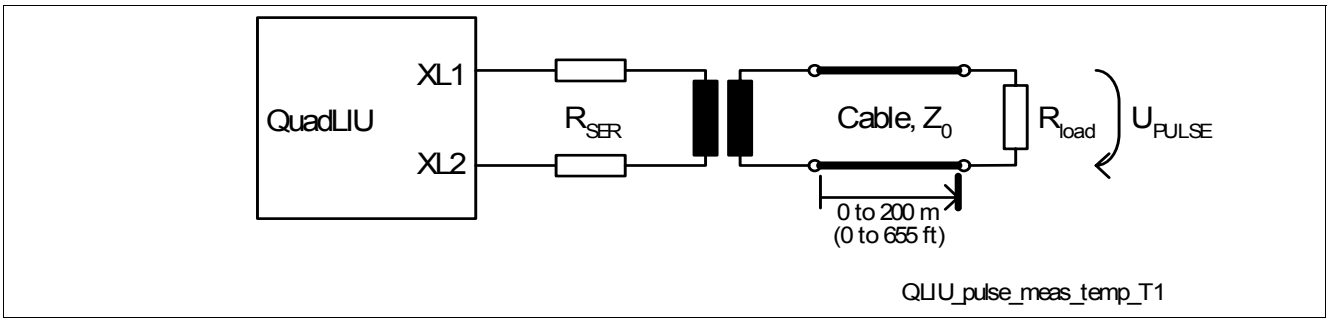



**Figure 40 Measurement Configuration for T1/J1 Transmit Pulse Template**

### 3.9.6.1 QuadFALC™ V2.1 Compatible Programming with XPM(2:0) Registers

After reset XPM2.XPDIS is zero so that programming with XPM(2:0) is selected. The default setting after reset for the registers XMP(2:0) generates the E1 pulse shape, see **Table 30**, but with an unreduced amplitude. No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming like described in **Table 29** is necessary.

If LBO attenuation is selected, the programming of XPM(2:0) will be ignored. Instead the pulse shape programming is handled internally: The generated pulse shape before LBO filtering is the same as for T1 0 to 40 m.

The given values are optimized for transformer ratio: 1 : 2.4 and cable type AWG24 using transmitter configurations listed in **Table 28** and shown in **Figure 37**. The measurement configurations of **Figure 39** with $R_{load}$ = 120 Ω and **Figure 40** with $R_{load}$ = 100 Ω are used.

**Table 29 Recommended Pulse Shaper Programming for T1/J1 with Registers XPM(2:0) (Compatible to QuadFALC V2.1 )**

| LBO | Range | Range | XPM0 | XPM1 | XPM2 |
|---|---|---|---|---|---|
| (dB) | (m) | (ft) | Hexadecimal | | |
| 0 | 0 to 40 | 0 to 133 | D7 | 22 | 11 |
| 0 | 40 to 81 | 133 to 266 | FA | 26 | 11 |
| 0 | 81 to 122 | 266 to 399 | 3D | 37 | 11 |
| 0 | 122 to 162 | 399 to 533 | 5F | 3F | 11 |

**Table 29 Recommended Pulse Shaper Programming for T1/J1 with Registers XPM(2:0) (Compatible to QuadFALC V2.1** (cont'd)**)**

| LBO | Range | Range | XPM0 | XPM1 | XPM2 |
|---|---|---|---|---|---|
| 0 | 162 to 200 | 533 to 655 | 3F | CB | 11 |
| 7.5 | --- | | Are not taken into account: pulse shape generation is handled internally. | | |
| 15 | --- | | | | |
| 22.5 | --- | | | | |

**Table 30 Recommended Pulse Shaper Programming for E1 with Registers XPM(2:0) (Compatible to QuadFALC V2.1)**

| $R_{SER}$ | $Z_0$ | Transmit Line Interface Mode | XPM0 | XPM1 | XPM2 |
|---|---|---|---|---|---|
| (Ω) | (Ω) | | Hexadecimal | | |
| 7.5[1)] | 120 | Non generic | 9C | 03 | 00 |
| 7.5 | 75 | Non generic | 8D | 03 | 00 |
| --- | Reset values | | 7B | 03 | 40 |
| 7.5 | DCIM Mode | Non generic | EF | BD | 07 |

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

### 3.9.6.2 Programming with TXP(16:1) Registers

By setting of register bit XPM2.XPDIS the pulse shape will be configured by the registers TXP(16:1) (TXP1). Every of these registers define the amplitude value of one sampling point in the symbol. A symbol is formed by 16 sampling points.

The default setting after reset for the registers TXP(16:1) generates also the E1 pulse shape (0m), but with an unreduced amplitude. (TXP(9:16) = ´$00_H$´; TXP(1:8) = ´$38_H$´= $56_D$´) No reset value for T1 mode exists. So after switching into T1 mode, an explicit new programming like Table 31 is necessary.

The pulse shape configuration will be done also by the registers TXP(16:1) if a LBO attenuation is selected. The pulse shape is then determined by both, the values of TXP(16:1) and the LBO filtering.

The given values in Table 31 and Table 32 are optimized for transformer ratio: 1 : 2.4; cable: AWG24 and configurations listed in Table 28 and shown in Figure 37.

**Table 31 Recommended Pulse Shaper Programming for T1 with Registers TXP(16:1)**

| LBO | Range | Range | TXP Values, Decimal | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (dB) | (m) | (ft) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| 0 | 0 to 40 | 0 to 133 | 46 | 46 | 46 | 44 | 44 | 44 | 44 | 44 | 16 | -17 | -14 | -14 | -4 | -4 | -4 | -4 |
| 0 | 40 to 81 | 133 to 266 | 48 | 50 | 48 | 46 | 46 | 44 | 44 | 44 | 16 | -17 | -14 | -14 | -4 | -4 | -4 | -4 |
| 0 | 81 to 122 | 266 to 399 | 48 | 50 | 46 | 44 | 44 | 44 | 44 | 44 | 16 | -25 | -17 | -14 | -4 | -4 | -4 | -4 |
| 0 | 81 to 122 | 266 to 399 | 56 | 58 | 54 | 52 | 48 | 48 | 48 | 48 | 16 | -25 | -17 | -14 | -4 | -4 | -4 | -4 |
| 0 | 122 to 162 | 399 to 533 | 63 | 63 | 58 | 56 | 52 | 52 | 51 | 51 | 16 | -34 | -32 | -17 | -4 | -4 | -4 | -4 |
| 7.5 | -- | -- | 46 | 46 | 46 | 44 | 44 | 44 | 44 | 44 | 16 | -17 | -14 | -14 | -4 | -4 | -4 | -4 |
| 155 | -- | -- | 46 | 46 | 46 | 44 | 44 | 44 | 44 | 44 | 16 | -17 | -14 | -14 | -4 | -4 | -4 | -4 |
| 22.5 | -- | -- | 46 | 46 | 46 | 44 | 44 | 44 | 44 | 44 | 16 | -17 | -14 | -14 | -4 | -4 | -4 | -4 |

**Table 32 Recommended Pulse Shaper Programming for E1 with registers TXP(16:1)**

| $R_{SER}$ | $Z_0$ | Transmit Line Interface Mode | TXP values, decimal | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (Ω) | (Ω) | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| 2[1)] | 120 | Generic | 42 | 40 | 40 | 40 | 40 | 40 | 40 | 42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7.5 | 120 | Non generic | 63 | 57 | 57 | 57 | 57 | 57 | 57 | 57 | -4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 75 | Generic | 42 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7.5 | 75 | Non generic | 60 | 58 | 58 | 58 | 58 | 58 | 58 | 58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -- | Reset values | | 56 | 56 | 56 | 56 | 56 | 56 | 56 | 56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | DCIM Mode | Generic | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | -20 | -20 | -20 | -20 | -20 | -20 | -20 | -20 |
| 7.5 | DCIM mode | Non generic | 28 | 28 | 28 | 28 | 28 | 28 | 28 | 28 | -28 | -28 | -28 | -28 | -28 | -28 | -28 | -28 |

1) The values in this row refers to an ideal application without any parasitics. Any other parasitic resistances have to be taken into account when calculating the final value of the output serial resistors.

## 3.9.7 Transmit Line Monitor

The transmit line monitor (see principle in **Figure 41**) compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly increased transmit line current (more than 120 mA for at least 3 consecutive pulses sourced by VDDX) and protects the device from damage by setting the transmit line driver XL1/2 into high-impedance state automatically (if enabled by XPM2.DAXLT = ´0´, see **XPM2**). The current limiter checks the actual current value of XL1/2 and if the transmit line current drops below the detection limit the high-impedance state is cleared.

Two conditions are detected by the monitor:

- Transmit line ones density (more than 31 consecutive zeros) indicated by LSR1.XLO (**LSR1**).
- Transmit line high current indicated by LSR1.XLS.

In both cases a transmit line monitor status change interrupt is provided.

Shorts between XL1 or XL2 and $V_{DD}$, $V_{DDC}$ or $V_{DDP}$ are not detected.

Note that shorts between XL1 and XL2 cannot be detected. This way a short between XL1 and XL2 will not harm the device.

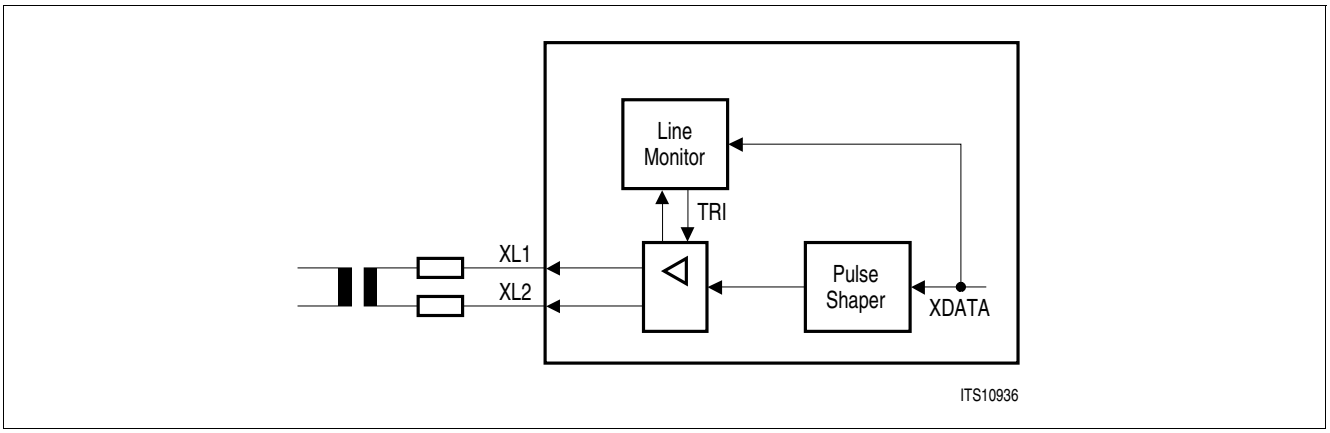



**Figure 41 Transmit Line Monitor Configuration**

## 3.10 Framer Interface

The framer interface of the QuadLIU™ is shown in **Figure 42**.

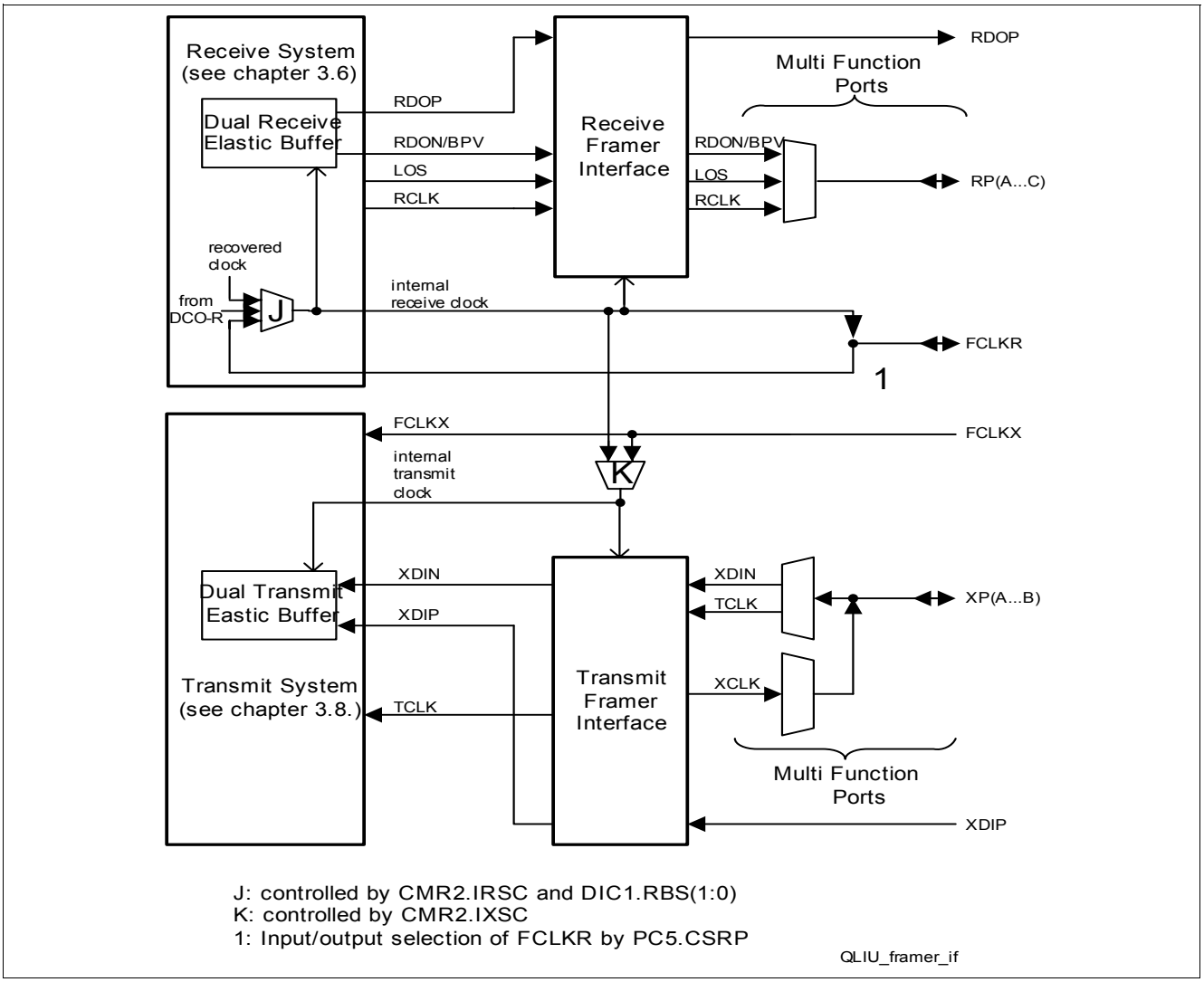



**Figure 42 Framer Interface (shown for one channel)**

Configuring of the framer interface consists on

- Configuration of the interface mode (single/dual rail)
- Configuration of the multi function ports, see **Chapter 3.12**

Selection of dual or single rail mode can be done in receive and transmit direction independent from each other.

In single rail mode of the receive direction (LIM3.DRR = ´0´, **LIM3**), the unipolar data is supported at RDOP and the bipolar violation (BPV) is supported at the receive multifunction pins. Therefore one of the three receive multifunction pins must be configured to RDON/BPV output (for example PC3.RPX3(3:0) = ´$1110_b$´), see**Table 34**, if BPV output is used exernally.

If dual rail mode is selected in receive direction by setting of register bit LIM3.DRR, the positive rail of the data is supported at RDOP and the negative rail of the data or is supported at the receive multi function pins. Therefore one of the three receive multifunction pins must be configured to RDON/BPV output, see**Table 34**.

Clocking of RDOP and RDON/BPV is done with the rising or falling edge of the internal receive clock, selected by DIC3.RESR. The internal receive clock can be sourced either

- By the receive clock RCLK of the receive system (CMR2.IRSC = ´1´, **CMR2**). To support the framer with these clock FCLKR output pin function must be selected by PC5.CSRP = ´1´ (**PC5**). or

- By the FCLKR input pin. In that case FCLKR input pin function must be selected by PC5.CSRP = ´0´ to use the receiver clock from the framer.

In single rail mode of the transmit direction (LIM3.DRX = ´0´, **LIM3**), the input for the unipolar data of the framer is XDIP.

If dual rail mode is selected in transmit direction by setting of register bit LIM3.DRX, the input for the positive rail of the data is XDIP and the input for the negative rail of the data is the multi function port XDIN. Therefore one of the both transmit multifunction ports must be configured to XDIN (for example PC1.XPX1(3:0) = ´$1101_b$´), see**Table 34**.

Clocking (sampling) of XDIP and XDIN is done with the rising or falling edge of the internal transmit clock, selected by DIC3.RESX. The internal transmit clock can be sourced either

- By the internal receive clock of the receive system (CMR2.IXSC = ´1´). To support the framer with these clock FCLKR output pin function must be selected by PC5.CSRP = ´1´. or
- By the FCLKX input pin (CMR2.IXSC = ´0´). In that case FCLKX is supported by the framer.

## 3.11 Test Functions

The following chapters describe the different test function of the QuadLIU™.

### 3.11.1 Pseudo-Random Binary Sequence Generation and Monitor

All bits of all slots in a E1T1/J1 frame are used for PRBS.

The QuadLIU™ has the ability to generate and monitor pseudo-random binary sequences (PRBS). The generated PRBS pattern is transmitted to the remote end on pins XL1/2 and can be inverted optionally. Generating and monitoring of PRBS pattern is done according to ITU-T O.150 and ITU-T O.151.

The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non-inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter BEC (**BECL**). Synchronization is reached within 400 ms with a probability of 99.9% at a bit error rate of up to $10^{-1}$.

The PRBS pattern (polynomials) can be selected to be 211-1, 215-1, 220-1or 223-1 by the register bits TPC0.PRP(1:0) and LCR1.LLBP (**LCR1**), see **Table 33**. For definition of this polynomials see the Standards ITU-T O.150, O.151. and TR62441. The polynomials 211-1 and 223-1 can be selected only if TPC0.PRM unequal ´00b´.

Transmission of PRBS pattern is enabled by register bit LCR1.XPRBS. With the register bit LCR1.FLLB switching between not inverted and inverted transmit pattern can be done.

The receive monitoring of PRBS patterns is enabled by register bit LCR1.EPRM. In general, depending on bit LCR1.EPRM the source of the interrupt status bit ISR1.LLBSC changed, see register description. The type of detected PRBS pattern in the receiver is shown in the status register bits PRBSSTA.PRS. Every change of the bits PRS in PRBSSTA sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if the mode “alarm simulation” is active.

The detection of all_zero or all_ones pattern is done over 12, 16, 21 or 24 consecutive bits, depending on the selected PRBS polynomial (211-1, 215-1, 220-1or 223-1 respectively). The detection of all_zero or all_ones is independent on LCR1.FLLB.

The distinction between all-ones and all-zeros pattern is possible by combination of.

- The information about the first reached PRBS status after the PRBS monitor was enabled (“PRBS pattern detected” or “inverted PRBS pattern detected”) with
- The status information “all-zero pattern detected” or “all-ones pattern detected”

If an “all-one” or an “all-zero” pattern is detected by the PRBS monitor, the interrupt status bit ISR1.LLBSC is set not only once, but is set permanent. To avoid that the LLBSC interrupt is issued permanent and the HOST micro controller would permanent be occupied, the following proceeding is recommended:

After reading of the interrupt status bit ISR1.LLBSC , the appropriate interrupt routine should set the interrupt mask bits IMR1.LLBSC to ´1´, after an “all-one” or an “all-zero” pattern was indicated, to avoid permanent interrupts issued by the QuadLIU™. The PRBS status register bits PRBSSTA.PRS should be polled to detect changes in

the pattern, for example once per second, using the ISR3.SEC interrupt. In case PRBSSTA.PRS(2:1) is unequal ´$11_B$´, the interrupt mask bits should be cleared to return to normal operation.

Because every bit error in the PRBS sequence increments the bit error counter BEC, no special status information like “PRBS detected with errors” is given here.

**Table 33 Supported PRBS Polynomials**

| TPC0.PRP(1:0) | TPC0.PRM | LCR1.LLBP | Kind of Polynomial | Comment |
|---|---|---|---|---|
| 00 | 01 or 11 | X | $2^{11}$ -1 | |
| 01 | 01 or 11 | X | $2^{15}$ -1 | |
| 10 | 01 or 11 | X | $2^{20}$ -1 | |
| 11 | 01 or 11 | X | $2^{23}$ -1 | |
| XX | 00 | 0 | $2^{15}$ -1 | SW compatible to QuadLIU |
| XX | 00 | 1 | $2^{20}$ -1 | |

## 3.11.2 In-Band Loop Generation, Detection and Loop Switching

Detection and generation of In-band Loop code is supported by the QuadLIU™ on the line side and on the framer side independent from another. On the framer side it is only supported in single rail mode.

The QuadLIU™ generates and detects unframed In-band codes where the complete data stream is used by the In-band signaling information.The so called loop-up code (for loop activation) and loop-down code (for loop deactivation) are recognized.

The maximum allowed bit error rate within the loop codes can be up to $10^{-2}$ for proper detection of the loop codes. One “In-band loop sequence” consists of a bit sequence of 51200 consecutive bits. The In-band loop code detection is based on the examination of such “In-band loop sequences”.

The following In-band loop code functionality is performed by the QuadLIU™:

- The necessary reception time of In-band loop codes until an automatic loop switching is performed is configured for the system side by the register bits INBLDTR.INBLDT(1:0) (**INBLDTR**). Configuring for the line side is done by INBLDTR.INBLDR(1:0). If for example INBLDTR.INBLDR(1:0) = ´$00_b$´ a time of 16 “In-band loop sequences” (16 x 51200 bits) is selected for the line side.
- The interrupt status register bits ISR6.(3:0) reflects the type of detected In-band loop code. Masking can be done by IMR6(3:0). The status bits are set after one “In-band loop sequence” is detected (no dependency on INBLDTR).
- Transmission of In-Band loop codes is enabled by programming MR3.XLD/XLU in E1 mode or MR5.XLD/XLU in T1/J1 mode. Transmission of codes is done by the QuadLIU™ lasting for at least 5 seconds.
- The QuadLIU™ also offers the ability to generate and detect flexible In-band loop-up and loop-down patterns (LCR1.LLBP = ´1´) (**LCR1**). Programming of these patterns is done in registers LCR2 and LCR3 (**LCR2**). The pattern length is individually programmable in length from 2 to 8 bits by LCR1.LAC(1:0) and LCR1.LDC(1:0). A shorter pattern can be inplemented by configuring a repeating pattern in the LCR2 and LCR3.
- Automatic loop switching (activation and deactivation, for remote loop, see **Chapter 3.11.3** and local loop, see **Chapter 3.11.4**) based on In-band Loop codes can be done. Two kinds of line loop back (LLB) codes are defined in ANSI-T1.403, 1999 in chapter 9.4.1.1 and 9.4.1.2. respectively. Automatic loop switching must be enabled through configuration register bits ALS.SILS for the In-Band Loop codes coming from the system side and ALS.LILS for the In-Band Loop codes coming from the line side respectively. Masking of ISR6.(3:0) for interrupt can be done by register bits IMR6.(3:0). The interrupt status register bits ISR6.(3:0) (**ISR6**) will be set to ´1´ if an appropriate In-Band code were detected, independent if automatic loop switching is enabled. (Because the controller knows if automatic loop switching is enabled, it knows if a loop is activated or not.) Code detection status only for the line side is displayed in E1 mode in status register bits LSR2.LLBDD / LLBAD and in T1/J1 mode in LSR1.LLBDD / LLBAD.

Only unframed In-Band loop code can be generated and detected.

Automatic loop switching is logically OR´d with the appropriate loop switching by register bits.

If a remote loop is activated by an automatic loop switching the register bit LIM0.JATT controls also if the jitter attenuator is active or not, see also **Figure 38**.

If ALS.LILS is set (**ALS**), the remote loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the line side and if the local loop is not activated by LIM0.LL = ´1´. The remote loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the line side. (But if the remote loop is additionally activated by LIM0.RL = ´1´ the remote loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

If ALS.SILS is set, the local loop is activated after an activation In-Band loop code (see ANSI T1 404, chapter 9.4.1.1.) was detected from the system side. The local loop is deactivated after a deactivation In-Band loop code (see ANSI T1 404, chapter 9.4.1.2.) was detected from the system side. (But if the local loop is additionally activated by LIM0.LL = ´1´ the local loop is still active, because automatic loop switching is logically OR´d with the appropriate loop switching by register bits.).

ALS.SILS and ALS.LILS both must not be set to ´1´ simultaneous.

If ALS.SILS or ALS.LILS are set after an In-Band loop code was detected, no automatic loop switching is performed.

If ALS.LILS is cleared, an automatic activated remote loop is deactivated.

If ALS.SILS is cleared, an automatic activated local loop is deactivated.

The kind of detected In-Band loop codes is shown in the interrupt status register bits ISR6.(3:0).

To avoid deadlocks in the QuadLIU™ an activation of the remote loop is not possible by In-band loop codes if the local loop (see **Chapter 3.11.4**) is closed (LIM0.LL is set).

### 3.11.3 Remote Loop

In the remote loop-back mode the clock and data recovered from the line inputs RL1/2 or ROID are routed back to the line outputs XL1/2 or XOID through the analog or digital transmitter, see **Figure 43** and **Figure 38**. As in normal mode they are also sent to the framer interface. The remote loop-back mode is activated by

- Control bit LIM1.RL or
- After detection of the appropriate In-band loop code, if enabled by ALS.LILS and if LIM0.LL = ´0´ (**LIM0**) (to avoid deadlocks), see **Chapter 3.11.2**.

Received data can be looped with or without the jitter attenuator (JATT buffer) dependent on LIM1.JATT (**LIM1**).

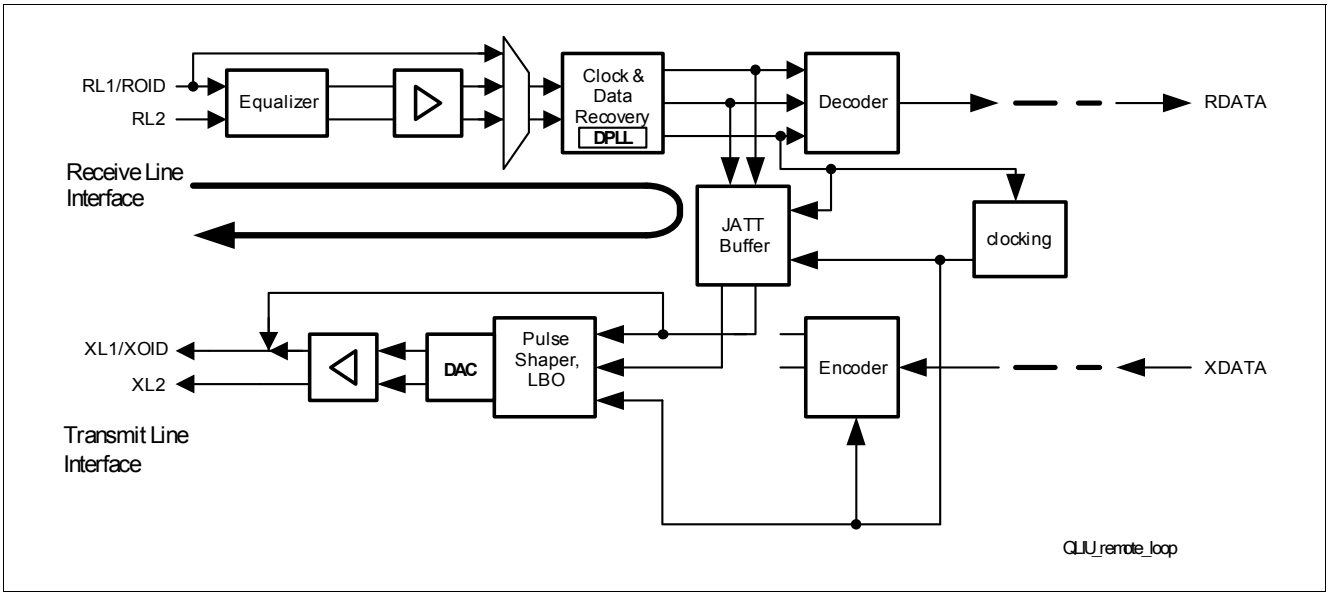



**Figure 43 Remote Loop**

### 3.11.4 Local Loop

The local loop-back is activated by

- The control bit LIM0.LL (**LIM0**).
- After detection of the appropriate In-band loop code, if enabled by ALS.SILS, see **Chapter 3.11.2**.

The local loop-back mode disconnects the receive lines RL1/2 or ROID from the receiver. Instead of the signals coming from the line the data provided by the framer interface is routed through the analog receiver back to the framer interface. However, the bit stream is transmitted undisturbed on the line at XL1/2. However, an AIS to the distant end can be enabled by setting MR1.XAIS = ´1´ without influencing the data looped back to the framer interface.

The signal codes for transmitter and receiver have to be identical.

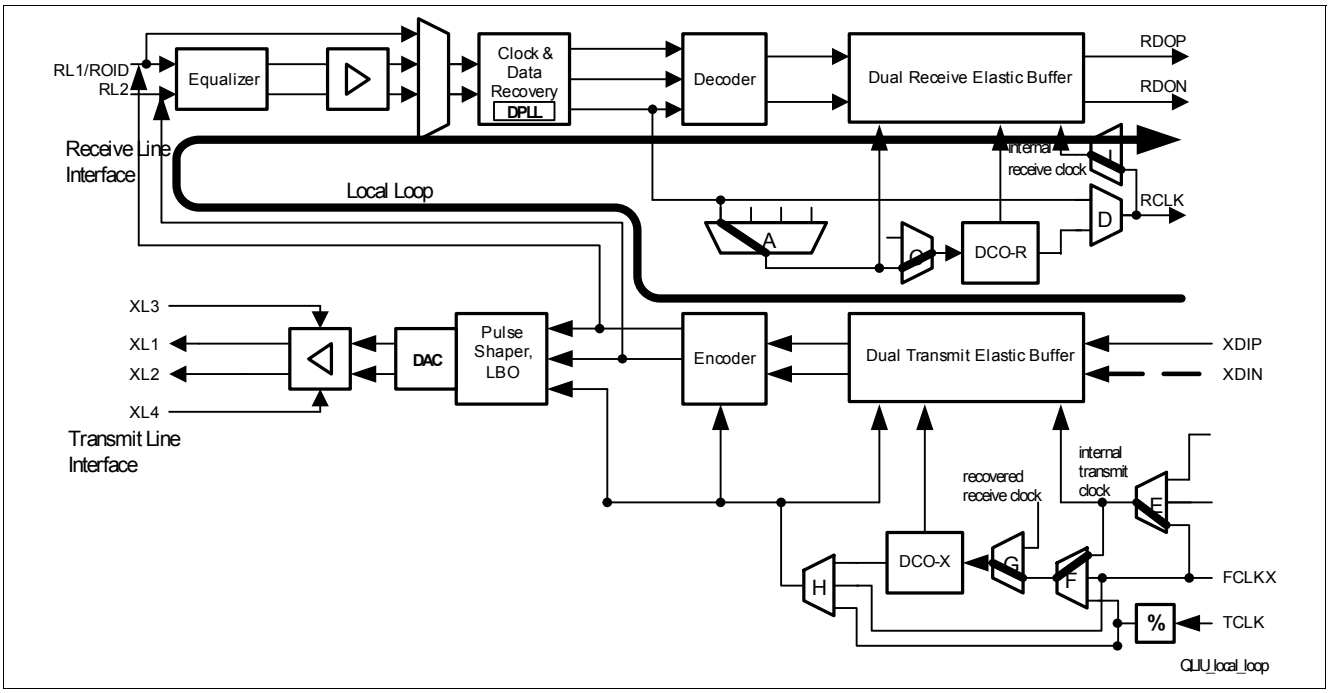



**Figure 44 Local Loop**

### 3.11.5 Payload Loop-Back

The payload loop-back is activated by setting MR2.PLB (**MR2**).

During activated payload loop-back the data stream is looped from the receiver section back to transmitter section. The looped data passes the complete receiver including the wander and jitter compensation in the receive elastic buffer and is output on pin RDO. Instead of the data an AIS signal (MR2.SAIS) can be sent to the framer interface.

If the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with FCLKR instead of FCLKX. All the received data is processed normally.

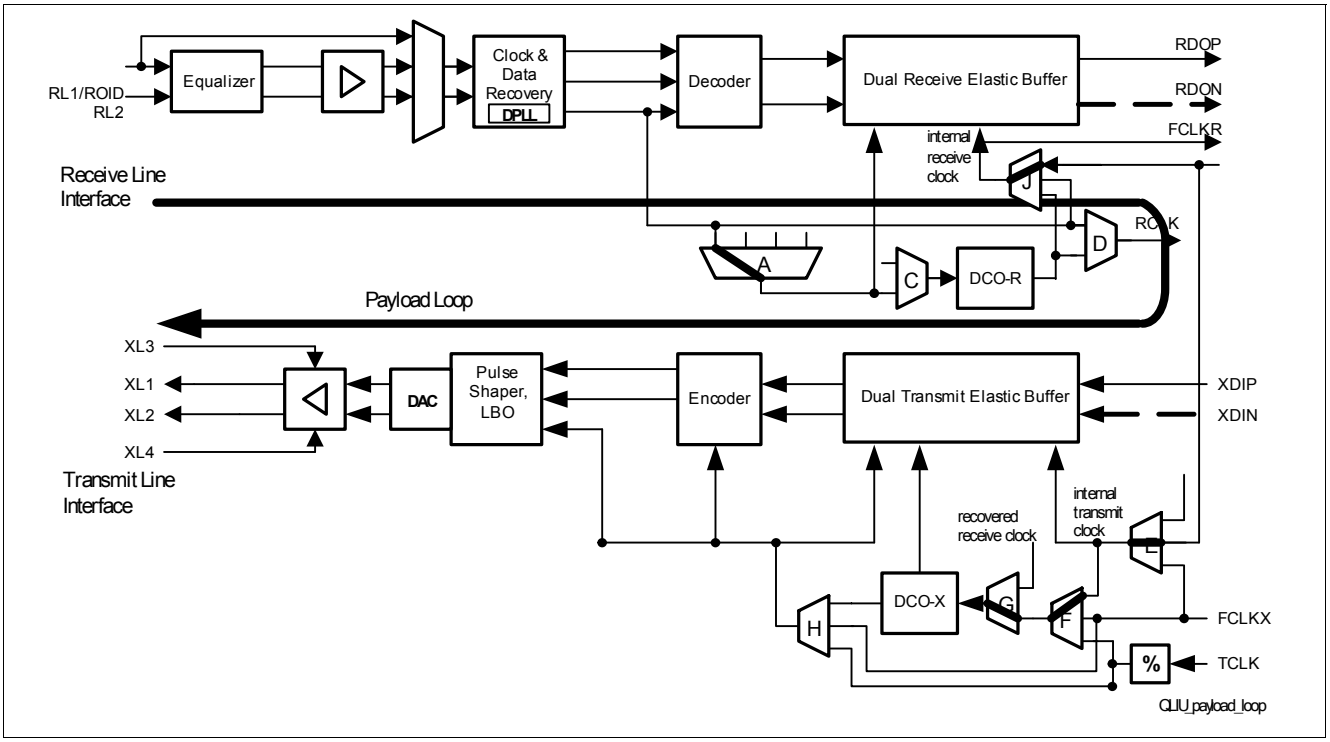



**Figure 45 Payload Loop**

### 3.11.6 Alarm Simulation

Alarm simulation does not affect the normal operation of the device. However, possible *real* alarm conditions are not reported to the micro controller or to the remote end when the device is in the alarm simulation mode.

The alarm simulation and setting of the appropriate status bists is initiated by setting the bit MR0.SIM. For details (differences between E1 and T1/J1 mode) see description in **MR0**. The following alarms are simulated:

- Loss-Of-Signal (LOS)
- Alarm Indication Signal (AIS)
- Code violation counter (HDB3 Code)

Error counting and indication occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status registers and error counters are automatically cleared on read.

## 3.12 Multi Function Ports

Several signals are available on the multi function ports, see **Table 34** and **PC1**. After reset, no function is selected (´$0000_b$´).

Four multi function ports (MFP) for RX - so called as RPA, RPB, RPC, RPC - and four MFPs for TX - XPA to XPD - are implemented for every channel. The port levels are reflected in the appropriate bits of the register MFPI, see **MFPI**D

The functions of RPA, RPB, RPC and RPC are configured by PC1.RPC1(3:0) , PC2.RPC2(3:0), PC3.RPC2(3:0) and PC4.RPC3(3:0) respectively. The functions of XPA to XPD are configured by PC1.XPC1(3:0) to PC4.XPC2(3:0) respectively.

The actual logical state of the 8 multifunction ports can be read out using the register MFPI. This function together with static output signal options in **Table 34** offers general purpose I/O functionality on unused multi function port pins.

If a port is configured as GPOH or GPOL the port level is set fix to high or low-level respectively.

Each of the input functions may only be selected once in a channel except for the GPI functionality. No input function must be selected twice or more.

**Table 34 Multi Function Port Selection**

| Selection | RFP Signal | Available on port | RFP Function | XFP Signal | Available on port | XFP Function |
|---|---|---|---|---|---|---|
| 0000 | Reserved | | Reserved | Reserved | | Reserved |
| 0001 | Reserved | | Reserved | Reserved | | Reserved |
| 0010 | Reserved | | Reserved | Reserved | | Reserved |
| 0011 | Reserved | | Reserved | TCLK | A, B, C, D | Transmit clock input |
| 0100 | Reserved | | Reserved | Reserved | | Reserved |
| 0101 | Reserved | | Reserved | Reserved | | Reserved |
| 0110 | Reserved | | Reserved | Reserved | | Reserved |
| 0111 | Reserved | | Reserved | XCLK | A, B, C, D | Transmit clock output |
| 1000 | RLT | A, B, C, D | Receive line termination; logically OR´d with LIM0.RTRS | XLT | A, B, C, D | Transmit line tristate control, high active |
| 1001 | GPI | A, B, C, D | General purpose input | GPI | A, B, C, D | General purpose input |
| 1010 | GPOH | A, B, C, D | General purpose output high | GPOH | A, B, C, D | General purpose output high |
| 1011 | GPOL | A, B, C, D | General purpose output low | GPOL | A, B, C, D | General purpose output low |
| 1100 | LOS | A, B, C, D | Loss of signal indication output | Reserved | A, B, C, D | Reserved |
| 1101 | RTDMT | A, B, C, D | Receive framer interface tristate for pins RDOP and RCLK; logically OR´d with DIC3.RRTRI | XDIN | A, B, C, D | Transmit data negative input |
| 1110 | RDON | A, B, C, D | Receive data negative output or bipolar violation output | $\overline{\text{XLT}}$ | A, B, C, D | Transmit line tristate control, low active |
| 1111 | RCLK | A, B, C, D | RCLK output | Reserved | | Reserved |

# 4 Register Description

To maintain easy readability this chapter is divided into separate control register and status register sections.

The higher address part of all global registers is ´$00_H$´, that of the port (channel) specific ones include the channel number 0 to 3 and is marked in the following tables with ´$xx_H$´. So ´$xx_H$´ has the values ´$00_H$´ up to ´$03_H$´.

*Note: "RES" in the register schematics means reserved, not reset. If these bits are written then the value must be ´0´.*

*Note: In all bit fields used in the register schematics and also in the table descriptions the most significant bit is the left one and the least significant bit is the right one. Sometimes in the text a bit field with the name "bitfieldname" is denoted as <bitfieldname>(MSB:LSB). For example: In register GPC2 the bit field FSS consists on MDS(2:0).*

## 4.1 Detailed Control Register Description

**Table 35 Registers Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| IPC | Interrupt Port Configuration | $0008_H$ | 121 |
| GCR | Global Configuration Register | $0046_H$ | 158 |
| GPC1 | Global Port Configuration 1 | $0085_H$ | 164 |
| GPC2 | Global Port Configuration Register 2 | $008A_H$ | 166 |
| GCM1 | Global Clock Mode Register 1 | $0092_H$ | 167 |
| GCM2 | Global Clock Mode Register 2 | $0093_H$ | 168 |
| GCM3 | Global Clock Mode Register 3 | $0094_H$ | 170 |
| GCM4 | Global Clock Mode Register 4 | $0095_H$ | 171 |
| GCM5 | Global Clock Mode Register 5 | $0096_H$ | 172 |
| GCM6 | Global Clock Mode Register 6 | $0097_H$ | 173 |
| GCM7 | Global Clock Mode Register 7 | $0098_H$ | 175 |
| GCM8 | Global Clock Mode Register 7 | $0099_H$ | 176 |
| GIMR | Global Interrupt Mask Register | $00A7_H$ | 177 |
| REGFP | Register Field Pointer | $00BB_H$ | 179 |
| REGFD | Register Field Data | $00BC_H$ | 180 |
| GPC3 | Global Port Configuration Register 3 | $00D3_H$ | 183 |
| GPC4 | Global Port Configuration Register 4 | $00D4_H$ | 184 |
| GPC5 | Global Port Configuration Register 5 | $00D5_H$ | 185 |
| GPC6 | Global Port Configuration Register 6 | $00D6_H$ | 186 |
| INBLDTR | In-Band Loop Detection Time Register | $00D7_H$ | 187 |
| CMDR | Command Register | $xx02_H$ | 120 |
| IMR1 | Interrupt Mask Register 1 | $xx15_H$ | 122 |
| IMR2 | Interrupt Mask Register 2 | $xx16_H$ | 122 |
| IMR3 | Interrupt Mask Register 3 | $xx17_H$ | 122 |
| IMR4 | Interrupt Mask Register 4 | $xx18_H$ | 122 |
| IMR6 | Interrupt Mask Register 6 | $xx1A_H$ | 122 |

**Table 35 Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| MR0 | Mode Register 0 | $xx1C_H$ | 124 |
| MR1 | Mode Register 1 | $xx1D_H$ | 126 |
| MR2 | Mode Register 2 | $xx1E_H$ | 127 |
| LOOP | Loop-Back Register | $xx1F_H$ | 128 |
| MR4 | Mode Register 4 | $xx20_H$ | 129 |
| MR5 | Framer Mode Register 5 | $xx21_H$ | 130 |
| RC0 | Receive Control 0 | $xx24_H$ | 131 |
| XPM0 | Transmit Pulse Mask0 | $xx26_H$ | 132 |
| XPM1 | Transmit Pulse Mask1 | $xx27_H$ | 133 |
| XPM2 | Transmit Pulse Mask2 | $xx28_H$ | 134 |
| CCB1 | Clear Channel Register 1 | $xx2F_H$ | 135 |
| CCB2 | Clear Channel Register 2 | $xx30_H$ | 135 |
| MR3 | Mode Register 3 | $xx31_H$ | 136 |
| CCB3 | Clear Channel Register 3 | $xx31_H$ | 135 |
| LIM0 | Line Interface Mode 0 | $xx36_H$ | 137 |
| LIM1 | Line Interface Mode 1 | $xx37_H$ | 139 |
| PCD | Pulse Count Detection Register | $xx38_H$ | 140 |
| PCR | Pulse Count Recovery | $xx39_H$ | 141 |
| LIM2 | Line Interface Mode 2 | $xx3A_H$ | 142 |
| LCR1 | Loop Code Register 1 | $xx3B_H$ | 143 |
| LCR2 | Loop Code Register 2 | $xx3C_H$ | 145 |
| LCR3 | Loop Code Register 3 | $xx3D_H$ | 146 |
| DIC1 | Digital Interface Control 1 | $xx3E_H$ | 147 |
| DIC2 | Digital Interface Control 2 | $xx3F_H$ | 148 |
| DIC3 | Digital Interface Control 3 | $xx40_H$ | 149 |
| CMR4 | Clock Mode Register 4 | $xx41_H$ | 151 |
| CMR5 | Clock Mode Register 5 | $xx42_H$ | 152 |
| CMR6 | Clock Mode Register 6 | $xx43_H$ | 153 |
| CMR1 | Clock Mode Register 1 | $xx44_H$ | 155 |
| CMR2 | Clock Mode Register 2 | $xx45_H$ | 156 |
| CMR3 | Clock Mode Register 3 | $xx48_H$ | 159 |
| PC1 | Port Configuration 1 | $xx80_H$ | 160 |
| PC2 | Port Configuration Register 2 | $xx81_H$ | 162 |
| PC3 | Port Configuration Register 3 | $xx82_H$ | 162 |
| PC4 | Port Configuration Register 4 | $xx83_H$ | 162 |
| PC5 | Port Configuration 5 | $xx84_H$ | 163 |
| PC6 | Port Configuration 6 | $xx86_H$ | 165 |
| TPC0 | Test Pattern Control Register 0 | $xxA8_H$ | 178 |
| BFR | Bugfix Register | $xxBD_H$ | 181 |
| TXP1 | TX Pulse Template Register 1 | $xxC1_H$ | 182 |
| TXP2 | TX Pulse Template Register 2 | $xxC2_H$ | 182 |

**Table 35 Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| TXP3 | TX Pulse Template Register 3 | $xxC3_H$ | 182 |
| TXP4 | TX Pulse Template Register 4 | $xxC4_H$ | 182 |
| TXP5 | TX Pulse Template Register 5 | $xxC5_H$ | 182 |
| TXP6 | TX Pulse Template Register 6 | $xxC6_H$ | 182 |
| TXP7 | TX Pulse Template Register 7 | $xxC7_H$ | 182 |
| TXP8 | TX Pulse Template Register 8 | $xxC8_H$ | 182 |
| TXP9 | TX Pulse Template Register 9 | $xxC9_H$ | 182 |
| TXP10 | TX Pulse Template Register 10 | $xxCA_H$ | 182 |
| TXP11 | TX Pulse Template Register 11 | $xxCB_H$ | 182 |
| TXP12 | TX Pulse Template Register 12 | $xxCC_H$ | 182 |
| TXP13 | TX Pulse Template Register 13 | $xxCD_H$ | 182 |
| TXP14 | TX Pulse Template Register 14 | $xxCE_H$ | 182 |
| TXP15 | TX Pulse Template Register 15 | $xxCF_H$ | 182 |
| TXP16 | TX Pulse Template Register 16 | $xxD0_H$ | 182 |
| ALS | Automatic Loop Switching Register | $xxD9_H$ | 188 |
| IMR7 | Interrupt Mask Register 7 | $xxDF_H$ | 122 |
| LIM3 | LIU Mode Register 3 | $xxE2_H$ | 189 |
| WCON | Wander Configuration Register | $xxE8_H$ | 190 |

The register is addressed wordwise.

**Table 36 Registers Access Types**

| Mode | Symbol | Description Hardware (HW) | Description Software (SW) |
|---|---|---|---|
| **Basic Access Types** | | | |
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read/write virtual | rwv | Physically, there is no new register in the generated register file. The real readable and writable register resides in the attached hardware. | Register is read and writable by SW (same as rw type register) |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior |
| read only | ro | Same as r type register | Same as r type register |
| read virtual | rv | Physically, there is no new register in the generated register file. The real readable register resides in the attached hardware. | Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior (same as r type register) |
| write | w | Register is written by software and affects hardware behavior with every write by software. | Register is writable by SW. When read, the register does not return the value that has been written previously, but some constant value instead. |
| write virtual | wv | Physically, there is no new register in the generated register file. The real writable register resides in the attached hardware. | Register is writable by SW (same as w type register) |
| read/write hardware affected | rwh | Register can be modified by hardware and software at the same time. A priority scheme decides, how the value changes with simultaneous writes by hardware and software. | Register can be modified by HW and SW, but the priority SW versus HW has to be specified.<br>SW can read the register. |
| **Special Access Types** | | | |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |

**Table 36 Registers Access Types** (cont'd)

| Mode | Symbol | Description Hardware (HW) | Description Software (SW) |
|---|---|---|---|
| Interrupt enable register | ien | Enables the interrupt source for interrupt generation | SW can read and write this register |
| latch_on_reset | lor | rw register, value is latched after first clock cycle after reset | Register is read and writable by SW |
| Read/write self clearing | rwsc | Register is used as input for the HW, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW. |

## 4.1.1 Control Registers

### Command Register

| CMDR | Offset | Reset Value |
|---|---|---|
| Command Register | $xx02_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | **RRES** | Res | **XRES** | Res | | | |
| | w | | w | | | | |

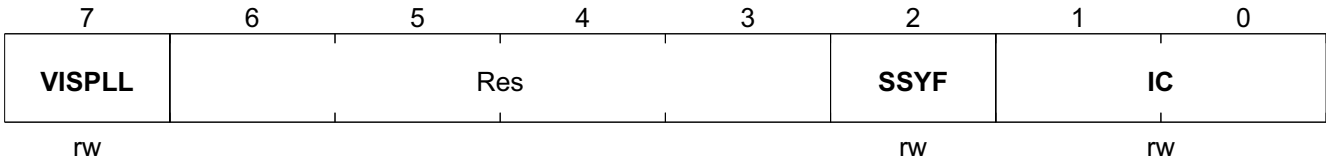
| Field | Bits | Type | Description |
|---|---|---|---|
| RRES | 6 | w | **Receiver Reset**<br>The receive line interface except the clock and data recovery unit (DPLL) is reset. However the contents of the control registers is not deleted.<br>A receiver reset should be made after switching from power down to power up (GCR.PD = ´1´ -> ´0´). |
| XRES | 4 | w | **Transmitter Reset**<br>The transmit framer and transmit line interface excluding the system clock generator and the pulse shaper are reset. However the contents of the control registers is not deleted. |

**Interrupt Port Configuration**

See **Chapter 3.5.3** and **Table 10**.

*Note: Unused bits have to be cleared.*

| IPC | Offset | Reset Value |
|---|---|---|
| **Interrupt Port Configuration** | **$0008_H$** | **$00_H$** |



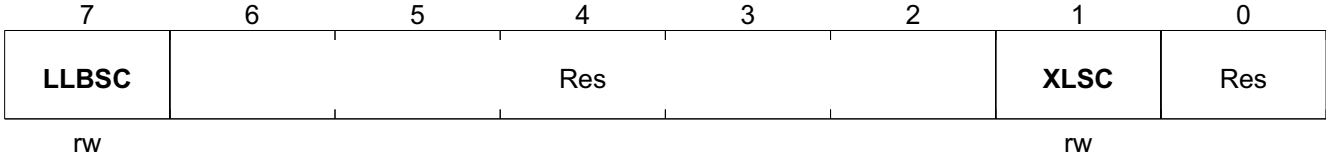

| Field | Bits | Type | Description |
|---|---|---|---|
| VISPLL | 7 | rw | **Masked PLL Interrupts Visible**<br>See also **Chapter 3.5.3**<br>$0_B$ Masked interrupt status bits PLLLC and PLLIC are not visible in register GIS2.<br>$1_B$ Masked interrupt status bits PLLLC and PLLIC are visible in GIS2, but they are not visible in registers GIS. |
| SSYF | 2 | rw | **Select SYNC Frequency**<br>Only applicable in master mode (LIM0.MAS = ´1´) and bit CMR2.DCF is cleared, see also Table 9.<br>$0_B$ Reference clock on port SYNC is 2.048 MHz<br>$1_B$ Reference clock on port SYNC is 8 kHz |
| IC | 1:0 | rw | **Interrupt Port Configuration**<br>These bits define the function of the interrupt output pin INT.<br>$X0_B$ Open drain output<br>$01_B$ Push/pull output, active low<br>$11_B$ Push/pull output, active high |

### Interrupt Mask Register 1

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined by register IPC). A “1” in a bit position of IMR(1:4), IMR(6:7) sets the mask active for the interrupt status in ISR(1:4), ISR(6:7). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are- not displayed in the interrupt status register if bit GCR.VIS is cleared- displayed in the interrupt status register if bit GCR.VIS is set, see **Chapter 3.5.3**.

*Note: After reset, all interrupts are disabled.*

| IMR1 | Offset | Reset Value |
|---|---|---|
| **Interrupt Mask Register 1** | **$xx15_H$** | **$FF_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| LLBSC | 7 | rw | **Interrupt Mask Bit LLBSC**<br>Each interrupt source can generate an interrupt signal on port INT. Characteristics of the output stage are defined by register IPC. A ´1´ in a bit position of IMR(7:0) sets the mask active for the interrupt status in the registers ISR. Mask interrupt statuses neither generate a signal on INT, not are they visible in register GIS. Moreover they are not displayed in the interrupt status register if bit GCR.VIS is cleared; they are displayed in the interrupt status register if bit GCR.VIS is set.<br>The bit IMR1.LLBSC is only valid in E1 mode. For T1/J1 mode the equivalent bit is in IMR3.LLBSC. |
| XLSC | 1 | rw | **Interrupt Mask Bit XLSC** |

The other Interrupt Mask Registers have the same description.

The Offset Addresses are listed in **IMRn Overview**, for bit names and layout refer to **Interrupt Mask Registers**.

**Table 37 IMRn Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| IMR2 | Interrupt Mask Register 2 | $xx16_H$ | |
| IMR3 | Interrupt Mask Register 3 | $xx17_H$ | |
| IMR4 | Interrupt Mask Register 4 | $xx18_H$ | |
| IMR6 | Interrupt Mask Register 6 | $xx1A_H$ | |
| IMR7 | Interrupt Mask Register 7 | $xxDF_H$ | |

**Table 38 Interrupt Mask Registers**

| bit number | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IMR1 | LLBSC (E1 only) | | | | | | XLSC | |

**Table 38 Interrupt Mask Registers** (cont'd)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| IMR2 | | | | | AIS | LOS | | |
| IMR3 | | SEC | | | LLBSC (T1/J1 only) | LTC | RSN | RSP |
| IMR4 | XSP | XSN | | | | | | |
| IMR6 | | | | | | | LILSU | LILSD |
| IMR7 | | | | XCLKSS1 | XCLKSS0 | | | |

## Mode Register 0

| MR0 | Offset | Reset Value |
|---|---|---|
| Mode Register 0 | xx1C$_H$ | 00$_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| XC | | RC | | EXZE | ALM | Res | SIM |
| rw | | rw | | rw | rw | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| XC | 7:6 | rw | **Transmit Code**<br>Serial line code for the transmitter, independent of the receiver. After changing XC(1:0), a transmitter software reset is required (CMDR.XRES = 1). See **Chapter 3.9.1**.<br>$00_B$ reserved<br>$01_B$ CMI (1T2B+HDB3), (optical interface)<br>$10_B$ AMI (ternary or digital dual-rail interface)<br>$11_B$ HDB3 Code in E1 or B8ZS code in T1/J1 mode (ternary or digital dual-rail interface) |
| RC | 5:4 | rw | **Receive Code**<br>Serial line code for the receiver, independent of the transmitter. After changing RC(1:0), a receiver software reset is required (CMDR.RRES = ´1´). See **Chapter 3.7.2**.<br>$00_B$ reserved<br>$01_B$ CMI (1T2B+HDB3), (optical interface)<br>$10_B$ AMI (ternary or digital dual-rail interface)<br>$11_B$ HDB3 Code in E1 or B8ZS code in T1/J1 mode (ternary or digital dual-rail interface) |
| EXZE | 3 | rw | **Extended HDB3 Error Detection, E1 only**<br>Selects error detection mode in E1 mode. In T1/J1 mode this bit is reserved.<br>$0_B$ Only double violations are detected.<br>$1_B$ Extended code violation detection: 0000 strings are detected additionally. Incrementing of the code violation counter CVC is done after receiving four zeros. Errors are indicated by LSR1.EXZD = ´1´. |

| Field | Bits | Type | Description |
|---|---|---|---|
| ALM | 2 | rw | **Alarm Mode, E1 only**<br>Selects the AIS alarm detection mode in E1 mode. In T1/J1 mode this bit is reserved.<br>$0_B$ The AIS alarm is detected according to ETS300233. Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a loss of frame alignment is indicated. Recovery: The alarm is cleared if 3 or more zeros within 512 bits are detected or the FAS word is found.<br>$1_B$ The AIS alarm is detected according to ITU-T G.775 Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros in each doubleframe period of two consecutive doubleframe periods (1024 bits). Recovery: The alarm is cleared if 3 or more zeros are detected within two consecutive doubleframe periods. |
| SIM | 0 | rw | **Alarm Simulation, in E1 mode**<br>SIM has to be held stable at high or low level for at least one receive clock period before changing it again.<br>$0_B$ Normal operation.<br>$1_B$ Initiates internal error simulation of AIS, loss-of-signal and code violations.<br>**Alarm Simulation, in T1/J1 mode**<br>Setting/resetting of SIM initiates internal error simulation of AIS (blue alarm), loss-of-signal (red alarm) and code violations. The error counter CVC is incremented.The selection of simulated alarms is done by the error simulation counter: LSR2.ESC(2:0) which is incremented with each setting of bit SIM. For complete checking of the alarm indications eight simulation steps are necessary (LSR2.ESC(2:0) = ´0´ after a complete simulation).<br>SIM has to be held stable at high or low level for at least one receive clock period before changing it again. |

## Mode Register 1

| MR1 | Offset | Reset Value |
|---|---|---|
| Mode Register 1 | $xx1D_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | **PMOD** | Res | | | **XAIS** |
| | | | rw | | | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PMOD | 4 | rw | **PCM Mode**<br>This bit decides between E1 and T1/J1 mode. Switching from E1 to T1 or vice versa the device needs up to 20 µs to settle up to the internal clocking.<br>$0_B$ PCM 30 or E1 mode.<br>$1_B$ PCM 24 or T1/J1 mode . |
| XAIS | 0 | rw | **Transmit AIS Towards Remote End**<br>Sends AIS on ports XL1, XL2, XOID towards the remote end. The outgoing data stream which can be looped back through the local loop to the system interface is not affected. |

## Mode Register 2

| MR2 | Offset | Reset Value |
|---|---|---|
| Mode Register 2 | $xx1E_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | **RTM** | **DAIS** | Res | **PLB** | Res | |
| | | rw | rw | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RTM | 5 | rw | **Receive Transparent Mode, E1 only**<br>For E1 mode this bit must be set to ´1´ for proper operation.<br>$0_B$ reserved<br>$1_B$ |
| DAIS | 4 | rw | **Disable AIS to Framer Interface**<br>This bit must be set to ´1´ for proper operation.<br>$0_B$ AIS is automatically inserted into the data stream to RDO if QuadLIU™ is in asynchronous state.<br>$1_B$ Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit MR2.SAIS. |
| PLB | 2 | rw | **Payload Loop-Back**<br>See **Chapter 3.11.5**.<br>$0_B$ Normal operation. Payload loop is disabled.<br>$1_B$ The payload loop-back loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, $\overline{SYPX}$ and XMFS is ignored. |

## Loop-Back Register

| LOOP | Offset | Reset Value |
|---|---|---|
| Loop-Back Register | $xx1F_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | **RTM** | Res | | | | | |
| | rw | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RTM | 6 | rw | **Receive Transparent Mode, T1 only**<br>For T1/J1 mode this bit must be set to ´1´ for proper operation.<br>$0_B$ reserved<br>$1_B$ |

## Mode Register 4

| MR4 | Offset | Reset Value |
|---|---|---|
| Mode Register 4 | $xx20_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | **TM** | Res | | | | | |
| | rw | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| TM | 6 | rw | **Transparent Mode, T1 only**<br>For T1/J1 mode this bit must be set to ´1´ for proper operation.<br>$0_B$ reserved<br>$1_B$ |

## Mode Register 5

| MR5 | Offset | Reset Value |
|---|---|---|
| Framer Mode Register 5 | $xx21_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | **XLD_TT0** | **XLU** | Res | **XTM** | Res | |
| | | rw | rw | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| XLD_TT0 | 5 | rw | **XLD, Transmit Line Loop-Back (LLB) Down Code, T1/J1 only**<br>The equivalent bit in E1 mode is MR3.XLD.<br>$0_B$ Normal operation.<br>$1_B$ A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down code is overwritten by the framing/DL/CRC bits optionally.<br>**TT0, Transmit Transparent Mode, E1 only**<br>For proper operation this bit must be set to ´1´ in E1 mode. |
| XLU | 4 | rw | **Transmit LLB Up Code, T1/J1 only**<br>This bit is not valid in E1 mode. The equivalent bit in E1 mode is MR3.XLU.<br>$0_B$ Normal operation.<br>$1_B$ A one in this bit position causes the transmitter to replace normal transmit data with the LLB up (activate) code continuously until this bit is reset. The LLB up code is optionally overwritten by the framing/DL/CRC bits. For proper operation bit MR5.XLD must be cleared. |
| XTM | 2 | rw | **Transmit Transparent Mode**<br>For proper operation this bit must be set to ´1´. |

## Receive Control 0

| RC0 | Offset | Reset Value |
|---|---|---|
| Receive Control 0 | $xx24_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | | **RDIS** | Res | | |
| | | | | rw | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RDIS | 3 | rw | **Receive Data Input Sense**<br>Configures the input polarity of the digital receive inputs.<br>$0_B$ in dual rail mode RDI, RDIN are active low, in DCIM mode ROID is active high.<br>$1_B$ in dual rail mode RDI, RDIN are active high, in DCIM mode ROID is active low. |

### Transmit Pulse Mask 0

See **Chapter 3.9.6.1** and **Chapter 3.9.6.2**. The transmit pulse shape which is defined in ITU-T G.703 is output on pins XL1 and XL2. The level of the pulse shape can be programmed by registers XPM(2:0) if XPM2.XPDIS is set to ´0´ to create a custom waveform. If XPM2.XPDIS is set to ´1´, the custom waveform can be programed by the registers TXP(16:1) and the register bits of XPM(2:0) are unused with exception of the bits XPM2.XLT, XPM2.DAXLT and XPM2.XPDIS. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes if XPM2.XPDIS is set to ´0´. In each sub pulse shape a programmed 5-bit value defines the level of the analog voltage on pins XL1/2. Together four 5-bit values have to be programmed to form one complete transmit pulse shape. The four 5-bit values are sent in the following sequence:

XP04 to 00: First pulse shape level

XP14 to 10: Second pulse shape level

XP24 to 20: Third pulse shape level

XP34 to 30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV. Recommended values for standard applications are given in Table 22 and Table 23.

Note that in the special cases were the LBO pulse masks are performed in T1 mode, the programming of the pulse masks is done internally, independent on the settings in XPM(2:0).

| XPM0 | Offset | Reset Value |
|---|---|---|
| Transmit Pulse Mask0 | $xx26_H$ | $7B_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **XP12** | **XP11** | **XP10** | **XP04** | **XP03** | **XP02** | **XP01** | **XP00** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| XP12 | 7 | rw | **Bit 2 of second pulse shape level** |
| XP11 | 6 | rw | **Bit 1 of second pulse shape level** |
| XP10 | 5 | rw | **Bit 0 (LSB) of second pulse shape level** |
| XP04 | 4 | rw | **Bit 4 (MSB) of first pulse shape level** |
| XP03 | 3 | rw | **Bit 3 of first pulse shape level** |
| XP02 | 2 | rw | **Bit 2 of first pulse shape level** |
| XP01 | 1 | rw | **Bit 1 of first pulse shape level** |
| XP00 | 0 | rw | **Bit 0 (LSB) of first pulse shape level** |

**Transmit Pulse Mask 1**

For description see **Transmit Pulse Mask 0**

| XPM1 | Offset | Reset Value |
|---|---|---|
| Transmit Pulse Mask1 | $xx27_H$ | $03_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **XP30** | **XP24** | **XP23** | **XP22** | **XP21** | **XP20** | **XP14** | **XP13** |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| XP30 | 7 | rw | **Bit 0 (LSB) of fourth pulse shape level** |
| XP24 | 6 | rw | **Bit 4 (MSB) of third pulse shape level** |
| XP23 | 5 | rw | **Bit 3 of third pulse shape level** |
| XP22 | 4 | rw | **Bit 2 of third pulse shape level** |
| XP21 | 3 | rw | **Bit 1of third pulse shape level** |
| XP20 | 2 | rw | **Bit 0 (LSB) of third pulse shape level** |
| XP14 | 1 | rw | **Bit 4 (MSB) of second pulse shape level** |
| XP13 | 0 | rw | **Bit 3 of second pulse shape level** |

### Transmit Pulse Mask 2

For description see **Transmit Pulse Mask 0**

| XPM2 | Offset | Reset Value |
|---|---|---|
| Transmit Pulse Mask2 | $xx28_H$ | $40_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **0** | **XLT** | **DAXLT** | **XPDIS** | **XP34** | **XP33** | **XP32** | **XP31** |
| r | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| 0 | 7 | r | **Always ´0´** |
| XLT | 6 | rw | **Transmit Line Tristate**<br>See also **Chapter 3.9.1**.<br>$0_B$ Normal operation<br>$1_B$ Transmit line XL1 and XL2 are switched into high-impedance state. If this bit is set the transmit line monitor status information is frozen (default value after hardware reset). |
| DAXLT | 5 | rw | **Disable Automatic Tristating of XL1/2**<br>See **Chapter 3.9.7**.<br>$0_B$ Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high-impedance state.<br>$1_B$ If a short is detected on XL1/2 pins automatic setting these pins into a high-impedance (by the XL-monitor) state is disabled. |
| XPDIS | 4 | rw | **Disable XPM Values**<br>See **Chapter 3.9.6**.<br>$0_B$ XP values from registers XPM(2:0) are used for pulse shaping.<br>$1_B$ TXP values from registers TXP(16:1) are used for pulse shaping. |
| XP34 | 3 | rw | **Bit 4 (MSB) of second pulse shape level**<br>See **Chapter 3.9.6.1**. |
| XP33 | 2 | rw | **Bit 3 of fourth pulse shape level** |
| XP32 | 1 | rw | **Bit 2 of fourth pulse shape level** |
| XP31 | 0 | rw | **Bit 1 of fourth pulse shape level** |

### Clear Channel Register 1

The registers CCB(1:3) are only valid in T1/J1 mode.

| CCB1 | Offset | Reset Value |
|---|---|---|
| Clear Channel Register 1 | $xx2F_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | CH8 |
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| CH1 | 7 | rw | **Channel Selection Bits**<br>If AMI code is selected, all bits must be set to ´1´ for proper operation.<br>$0_B$ Normal operation. Bit robbing information and zero code suppression (ZCS, B7 stuffing) can change contents of the selected speech/data channel if assigned modes are enabled by bits MR5.EIBR and MR0.XC(1:0).<br>$1_B$ Clear channel mode. Contents of selected speech/data channel are not overwritten by internal or external bit robbing and ZCS information. Transmission of channel assigned signaling and control of pulse-density is applied by the user. |
| CH2 | 6 | | |
| CH3 | 5 | | |
| CH4 | 4 | | |
| CH5 | 3 | | |
| CH6 | 2 | | |
| CH7 | 1 | | |
| CH8 | 0 | | |

Registers CCB2 and CCB3 have the same description.

The Offset Addresses are listed in **CCBn Overview**, for layout and bit names refer to **Clear Channel Registers**

**Table 39 CCBn Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| CCB2 | Clear Channel Register 2 | $xx30_H$ | |
| CCB3 | Clear Channel Register 3 | $xx31_H$ | |

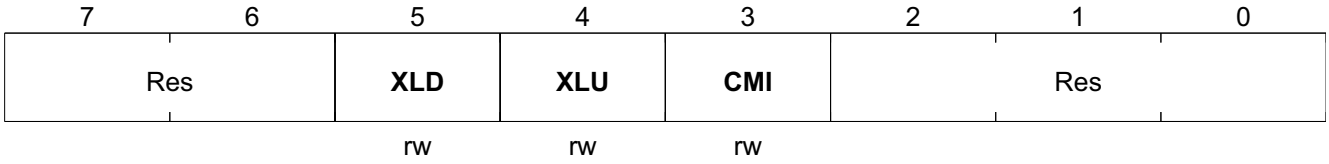
**Table 40 Clear Channel Registers**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CCB1 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | CH8 |
| CCB2 | CH9 | CH10 | CH11 | CH12 | CH13 | CH14 | CH15 | CH16 |
| CCB3 | CH17 | CH18 | CH19 | CH20 | CH21 | CH22 | CH23 | CH24 |

### Mode Register 3

Only valid in E1 mode.

| MR3 | Offset | Reset Value |
|---|---|---|
| Mode Register 3 | $xx31_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| XLD | 5 | rw | **Transmit LLB Down Code, E1 only**<br>This bit is not valid in T1/J1 mode. In T1/J1 mode the bis MR5.XLD is used instead.<br>$0_B$ Normal operation.<br>$1_B$ A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) Code continuously until this bit is reset. The LLB down Code is optionally overwritten by the time slot 0 depending on bit LCR1.FLLB. |
| XLU | 4 | rw | **Transmit LLB UP Code, E1 only**<br>This bit is not valid in T1/J1 mode. In T1/J1 mode the bit MR5.XLU is used instead.<br>$0_B$ Normal operation.<br>$1_B$ A one in this bit position causes the transmitter to replace normal transmit data with the LLB UP Code continuously until this bit is reset. The LLB UP Code is overwritten by the time slot 0 depending on bit LCR1.FLLB. For proper operation bit MR3.XLD must be cleared. |
| CMI | 3 | rw | **Select CMI Precoding, E1 only**<br>This bit is not valid in T1/J1 mode. In T1/J1 mode the similar bit for B8ZS precoding is DIC3.CMI.<br>In E1 mode only valid if CMI code (MR0.XC(1:0) = ´$01_b$´) is selected. This bit defines the CMI precoding and influences transmit and receive data.<br>*Note: Before local loop is selected, HDB3 precoding has to be disabled.*<br>$0_B$ CMI with HDB3 precoding<br>$1_B$ CMI without HDB3 precoding |

## Line Interface Mode 0

| LIM0 | Offset | Reset Value |
|---|---|---|
| Line Interface Mode 0 | $xx36_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **XFB** | **XDOS** | **RTRS** | **DCIM** | Res | **RLM** | **LL** | **MAS** |
| rw | rw | rw | rw | | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| XFB | 7 | rw | **Transmit Full Bauded Mode**<br>Only applicable for dual-rail mode (bit LIM1.DRS = ´1´).<br>*Note: If CMI coding is selected (MR0.XC(1:0) = ´$01_b$´) this bit has to be cleared.*<br>$0_B$ Output signals XDO/XDON are half bauded.<br>$1_B$ Output signals XDO/XDON are full bauded. |
| XDOS | 6 | rw | **Transmit Data Out Sense**<br>*Note: If CMI coding is selected (MR0.XC(1:0) = ´$01_b$´) this bit has to be cleared. The transmit frame marker XFM is independent of this bit.*<br>$0_B$ Output signals XDO/XDON are active low. Output XOID is active high (normal operation).<br>$1_B$ Output signals XDO/XDON are active high. Output XOID is active low. |
| RTRS | 5 | rw | **Receive Termination Resistance Selection**<br>This bit controls switching of the internal 300 Ω resistance at the receive line interface, see also **Chapter 3.7.3**.<br>*Note: If the RLT functionality is selected at one of the multi function ports, the 300 Ω resistance is switched off, independend from RTRS and the level at RLT. If RLT functionality is not configured at one of the multi function ports, the 300 Ω switch is controlled only by RTRS.*<br>$0_B$ 300 Ω resistance is switched off.<br>$1_B$ 300 Ω resistance is switched on. |
| DCIM | 4 | rw | **Digital Clock Interface Mode**<br>*Note: DCO-X must be used in DCIM mode (CMR1.DXJA = ´0´).*<br>$0_B$ normal operation.<br>$1_B$ enables the digital Clock Interface Mode (synchronization interface mode) according to ITU-T G.703, Section 13.<br>A 2048/1544 kHz clock is expected on RL1/2. On XL1/2 a 2048/1544 kHz output clock is driven. The transmit clock signal on XL1/2 is derived from the clock supplied on FCLKX (CMR1.DXSS = ´0´). |

| Field | Bits | Type | Description |
|---|---|---|---|
| RLM | 2 | rw | **Receive Line Monitoring**<br>See **Chapter 3.7.3.2**.<br>$0_B$ Normal receiver mode<br>$1_B$ Receiver mode for receive line monitoring; the receiver sensitivity is increased to detect resistively attenuated signals of -20 dB (short-haul mode only) |
| LL | 1 | rw | **Local Loop**<br>See **Chapter 3.11.4**.<br>$0_B$ Normal operation<br>$1_B$ Local loop active. The local loop back mode disconnects the receive lines RL1/RL2 or ROID from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbed on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver. |
| MAS | 0 | rw | **Master Mode**<br>See also **Table 24**.<br>$0_B$ Slave mode<br>$1_B$ Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized to the clock (2.048 MHz or 8 kHz, see IPC.SSYF) supplied by SYNC. If this pin is connected to VSS or VDD (or left open and pulled up to VDD internally) the DCO-R circuitry is centered and no receive jitter attenuation is performed (only if 2.048 MHz clock is selected by resetting bit IPC.SSYF). The generated clocks are stable. |

## Line Interface Mode 1

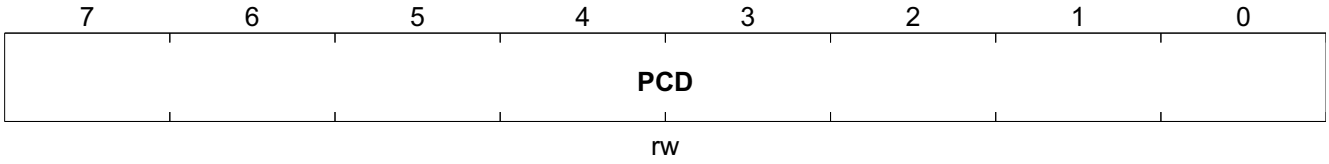
| LIM1 | Offset | Reset Value |
|---|---|---|
| Line Interface Mode 1 | $xx37_H$ | $80_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **CLOS** | **RIL2** | **RIL1** | **RIL0** | Res | **JATT** | **RL** | **DRS** |
| rw | rw | rw | rw | | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| CLOS | 7 | rw | **Clear Data in Case of LOS**<br>$0_B$ Normal receiver mode, receive data stream is transferred normally in long-haul mode<br>$1_B$ received data is cleared (driven to low level), as soon as LOS is detected |
| RIL2 | 6 | rw | **Receive Input Threshold**<br>Only valid if analog line interface is selected (LIM1.DRS = ´0´).“No signal” is declared if the voltage between pins RL1 and RL2 drops below the limits programmed by bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register.<br>See DC characteristics for detail. |
| RIL1 | 5 | rw | |
| RIL0 | 4 | rw | |
| JATT | 2 | rw | **Transmit Jitter Attenuator**<br>*Note: JATT is only used to define the jitter attenuation during remote loop operation. Remote loop operation can be set by LIM1.RL Jitter attenuation during normal operation is not affected by JATT.*<br>$0_B$ Transmit jitter attenuator is disabled for remote Loop. Transmit data bypasses the remote loop jitter attenuator buffer.<br>$1_B$ Jitter attenuator is active for remote loop. Received data from pins RL1/2 or ROID is sent "jitter-free" on ports XL1/2 or XOID. The de-jittered clock is generated by the DCO-X circuitry. |
| RL | 1 | rw | **Remote Loop**<br>*Note: RL is logically OR´d with automatic loop switching by BOM messages.*<br>$0_B$ Normal operation.<br>$1_B$ Remote Loop active. |
| DRS | 0 | rw | **Dual-Rail Select**<br>$0_B$ The ternary interface is selected. Ports RL1/2 and XL1/2 become analog in/outputs.<br>$1_B$ The digital dual-rail interface is selected. Received data is latched on ports RDIP/RDIN while transmit data is output on pins XDOP/XDON. |

## Pulse Count Detection Register

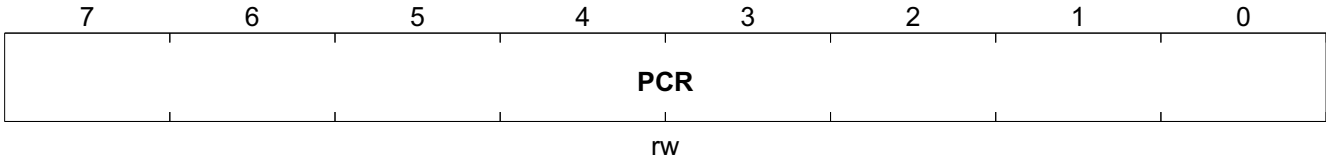
| PCD | Offset | Reset Value |
|---|---|---|
| Pulse Count Detection Register | $xx38_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| PCD | 7:0 | rw | **Pulse Count Detection**<br>A LOS alarm is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable by the PCD register and can be calculated as follows: T = 16 x (N+1); with 0 ≤ N ≤ 255.The maximum time is: 256 x 16 x 488 ns = 2 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK. |

## Pulse Count Recovery

| PCR | Offset | Reset Value |
|---|---|---|
| Pulse Count Recovery | $xx39_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| PCR | 7:0 | rw | **Pulse Count Recovery**<br>A LOS alarm is cleared if a pulse-density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable by the PCR register and can be calculated as follows: M = N+1; with $0 \leq N \leq 255$.The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared to the contents of PCR register. If the pulse number is higher or equal to the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval. |

## Line Interface Mode 2

| LIM2 | Offset | Reset Value |
|---|---|---|
| Line Interface Mode 2 | xx3A$_H$ | 20$_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | SLT1 | SLT0 | SCF | ELT | MPAS | Res |
| | | rw | rw | rw | rw | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| SLT1 | 5 | rw | **Receive Slicer Threshold** |
| SLT0 | 4 | rw | $00_B$ The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 55% of the peak amplitude.<br>$01_B$ The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 67% of the peak amplitude (recommended in some T1/J1 applications).<br>$10_B$ The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 50% of the peak amplitude (default, recommended in E1 mode).<br>$11_B$ The receive slicer generates a mark (digital one) if the voltage at RL1/2 exceeds 45% of the peak amplitude. |
| SCF | 3 | rw | **Select Corner Frequency of DCO-R**<br>Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.2 Hz. See **Chapter 3.7.8**.<br>*Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time before the frequencies are synchronized.* |
| ELT | 2 | rw | **Enable Loop-Timed**<br>$0_B$ Normal operation<br>$1_B$ Transmit clock is generated from the clock supplied by MCLK which is synchronized to the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. For correct operation of loop timed the remote loop (bit LIM1.RL = ´0´) must be inactive and bit CMR1.DXSS must be cleared. |
| MPAS | 1 | rw | **Multi Purpose Analog Switch**<br>Controls the multi purpose analog switch at receive line interface if GPC(3:6).ENMPAS are all set to ´1´ . If RLT is not configured at any multi function port, only MPAS controls the switch. If RLT is configured at one of the multi function ports see **Table 14** for contrrolling.<br>$0_B$ multi purpose analog switch is óff´.<br>$1_B$ multi purpose analog switch is on´. |

## Loop Code Register 1

| LCR1 | Offset | Reset Value |
|---|---|---|
| Loop Code Register 1 | $xx3B_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EPRM | XPRBS | LDC | | LAC | | FLLB | LLBP |
| rw | rw | rw | | rw | | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| EPRM | 7 | rw | **Enable Pseudo-Random Binary Sequence Monitor**<br>See **Chapter 3.11.1**.<br>$0_B$ Pseudo-Random Binary Sequence (PRBS) monitor is disabled.<br>$1_B$ PRBS is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit LSR2.LLBAD. |
| XPRBS | 6 | rw | **Transmit Pseudo-Random Binary Sequence**<br>A one in this bit position enables transmission of a pseudo-random binary sequence to the remote end. Depending on bit LLBP the PRBS is generated according to $2^{15}$ -1 or $2^{20}$ -1 with a maximum-14-zero restriction (ITU-T O. 151). See **Chapter 3.11.1**. |
| LDC | 5:4 | rw | **Length Deactivate (Down) Code**<br>These bits defines the length of the LLB deactivate code which is programmable in register LCR2.<br>$00_B$ Length: 5 bit<br>$01_B$ Length: 6 bit, 2 bit, 3 bit<br>$10_B$ Length: 7 bit<br>$11_B$ Length: 8 bit, 2 bit, 4bit |
| LAC | 3:2 | rw | **Length Activate (Up) Code**<br>These bits defines the length of the LLB activate code which is programmable in register LCR3.<br>$00_B$ Length: 5 bit<br>$01_B$ Length: 6 bit, 2 bit, 3 bit<br>$10_B$ Length: 7 bit<br>$11_B$ Length: 8 bit, 2 bit, 4 bit |
| FLLB | 1 | rw | **Framed Line Loop-Back/Invert PRBS**<br>Depending on bit LCR1.XPRBS this bit enables different functions:<br>LCR1.XPRBS = ´0´: **Table 41**.<br>*Note: Invert PRBS LCR1.XPRBS = ´1´: see **Table 42*** |
| LLBP | 0 | rw | **Line Loop-Back Pattern**<br>See **Chapter 3.11.2**<br>LCR1.XPRBS = ´0´: see **Table 43**<br>LCR1.XPRBS = ´1´ or LCR1.EPRM = ´1´: see **Table 44** |

**Table 41 FLLB Constant Values (Case 1)**

| Name and Description | Value |
|---|---|
| **Framed Line Loop-Back/Invert PRBS**<br>The line loop-back code is transmitted including framing bits. LLB code overwrites the FS/DL-bits. | $0_B$ |
| **Framed Line Loop-Back/Invert PRBS**<br>The line loop-back code is transmitted unframed. LLB code does not overwrite the FS/DL-bits. | $1_B$ |

**Table 42 FLLB Constant Values (Case 2)**

| Name and Description | Value |
|---|---|
| **Framed Line Loop-Back/Invert PRBS**<br>The generated PRBS is transmitted not inverted. | $0_B$ |
| **Framed Line Loop-Back/Invert PRBS**<br>The PRBS is transmitted inverted. | $1_B$ |

**Table 43 LLBP Constant Values (Case 1)**

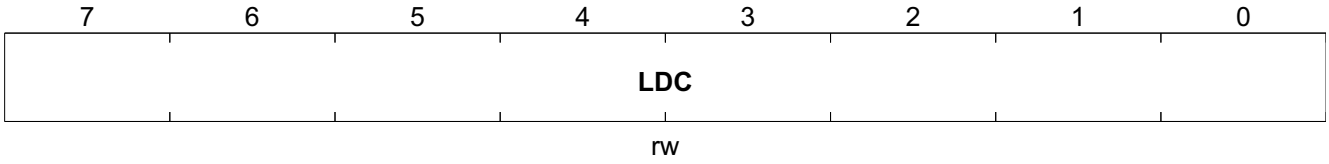
| Name and Description | Value |
|---|---|
| **Line Loop-Back Pattern**<br>Fixed line loop-back code according to ANSI T1. 403. | $0_B$ |
| **Line Loop-Back Pattern**<br>Enable user-programmable line loop-back code by register LCR2/3. | $1_B$ |

**Table 44 LLBP Constant Values (Case 2)**

| Name and Description | Value |
|---|---|
| **Line Loop-Back Pattern**<br>$2^{15}$ -1 | $0_B$ |
| **Line Loop-Back Pattern**<br>$2^{20}$ -1 | $1_B$ |

## Loop Code Register 2

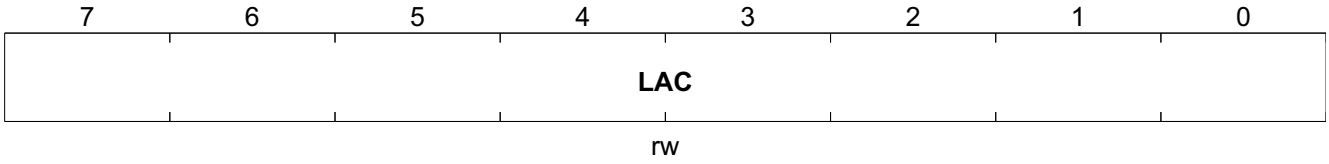
| LCR2 | Offset | Reset Value |
|---|---|---|
| Loop Code Register 2 | $xx3C_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| LDC | 7:0 | rw | **Line Loop-Back Deactivate Code**<br>If enabled by bit MR3.XLD = ´1´ in E1 or MR5.XLD = ´1´ in T1/J1 mode the LLB deactivate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared. If LCR2 is changed while the previous deactivate code has been detected and is still received, bit LSR2.LLBDD in E1 or LSR1.LLBDD in T1/J1 mode will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´). |

## Loop Code Register 3

| LCR3 | Offset | Reset Value |
|---|---|---|
| Loop Code Register 3 | $xx3D_H$ | $00_H$ |

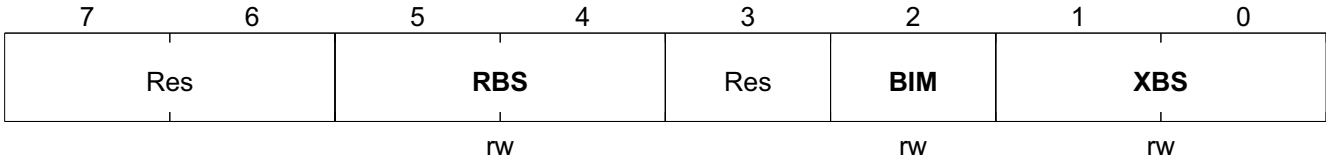



| Field | Bits | Type | Description |
|---|---|---|---|
| LAC | 7:0 | rw | **Line Loop-Back Activate Code**<br>If enabled by bit MR3.XLD = ´1´ in E1 or MR5.XLD = ´1´ in T1/J1 mode the LLB activate code automatically repeats until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. For correct operations bit LCR1.XPRBS has to cleared.If LCR3 is changed while the previous activate code has been detected and is still received, bit LSR2.LLBAD in E1 or LSR1.LLBAD in T1/J1 mode will stay active until the incoming signal changes or a receiver reset is initiated (CMDR.RRES = ´1´). |

**Digital Interface Control 1**

See **Chapter 3.7.9**.

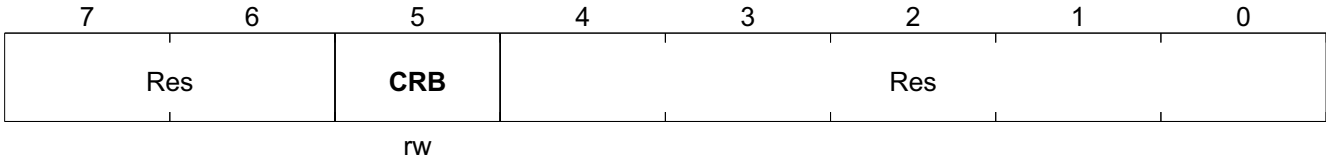
| DIC1 | Offset | Reset Value |
|---|---|---|
| **Digital Interface Control 1** | **xx3E$_H$** | **00$_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| RBS | 5:4 | rw | **Receive Buffer Size**<br>See **Table 26**.<br>$00_B$ Buffer size: 2 frames<br>$01_B$ Buffer size: 1 frame<br>$10_B$ Buffer size: 96 bits<br>$11_B$ bypass of receive elastic store |
| BIM | 2 | rw | **Bit Interleaved Mode**<br>$0_B$ Byte interleaved mode<br>$1_B$ Bit interleaved mode |
| XBS | 1:0 | rw | **Transmit Buffer Size**<br>See **Table 26**.<br>$00_B$ Bypass of transmit elastic store<br>$01_B$ Buffer size: 1 frame<br>$10_B$ Buffer size: 2 frames<br>$11_B$ Buffer size: 96 bits |

## Digital Interface Control 2

| DIC2 | Offset | Reset Value |
|---|---|---|
| Digital Interface Control 2 | $xx3F_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| CRB | 5 | rw | **Center Receive Elastic Buffer**<br>Only applicable if the time slot assigner is disabled (PC(3:1).RPC(3:0) = ´$0001_b$´), no external or internal synchronous pulse receive is generated. A transition from low to high forces a receive slip and the read- pointer of the receive elastic buffer is centered. The delay through the buffer is set to one half of the current buffer size. It should be hold high for at least two 2.048 MHz periods before it is cleared. |

## Digital Interface Control 3

| DIC3 | Offset | Reset Value |
|---|---|---|
| Digital Interface Control 3 | $xx40_H$ | $00_H$ |

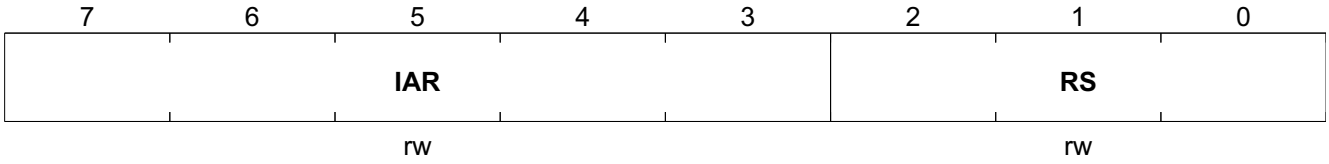
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **CMI** | **RRTRI** | **RTRI** | **FSCT** | **RESX** | **RESR** | Res | |
| rw | rw | rw | rw | rw | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| CMI | 7 | rw | **Select CMI Precoding (T1 only)**<br>Only valid if CMI code (MR0.XC(1:0) = ´$01_b$´) is selected. This bit defines the CMI precoding and influences transmit and receive data.<br>*Note: Before local loop is closed, B8ZS precoding has to be switched off.*<br>$0_B$ CMI with B8ZS precoding<br>$1_B$ CMI without B8ZS precoding |
| RRTRI | 6 | rw | **RDO Tristate Mode**<br>See **Chapter 3.7.3.4**<br>*Note: RRTRI is logically exored with RTDMT multi function port, if this function is selected. RTDMT exor RRTRI sets additionally RCLK into tristate.*<br>$00_B$ normal operation (RDOP is switched to low level during inactive channel/bit phases).<br>$01_B$ RDO is switched into tristate mode during inactive channel/bit phases.<br>$10_B$ RDO is tristate constantly (and also RCLK).<br>$11_B$ RDO is tristate constantly (and also RCLK). |
| RTRI | 5 | | |
| FSCT | 4 | rw | **FSC Tristate Mode**<br>$0_B$ normal operation of FSC pin.<br>$1_B$ FSC is switched into tristate mode. |
| RESX | 3 | rw | **Rising Edge Synchronous Transmit**<br>Depending on this bit all transmit framer interface data are clocked (outputs) or sampled (inputs) with the selected active edge of the selected framer transmit clock.<br>Only valid if CMR2.IXSC = ´0´:<br>*Note: CMR2.IXSC = ´1´: value of RESX bit has no impact on the selected edge of the system interface clock but value of $\overline{RESR}$ bit is used as RESX. Example: If RESR = ´0´, the rising edge of system interface clock is the selected one for sampling data on XDI and vice versa.*<br>$0_B$ Clocked or sampled with the first falling edge of the selected framer interface transmit clock.<br>$1_B$ Clocked or sampled the first rising edge of the selected framer interface transmit clock. |

| Field | Bits | Type | Description |
|---|---|---|---|
| RESR | 2 | rw | **Rising Edge Synchronous Receive**<br>Depending on this bit all receive framer interface data are clocked (outputs) or sampled (inputs) with the selected active edge.<br>$0_B$ Clocked or sampled with the first falling edge of the selected framer interface receive clock.<br>$1_B$ Clocked or sampled with the first rising edge of the selected framer interface receive clock. |

## Clock Mode Register 4

| CMR4 | Offset | Reset Value |
|---|---|---|
| Clock Mode Register 4 | $xx41_H$ | $00_H$ |

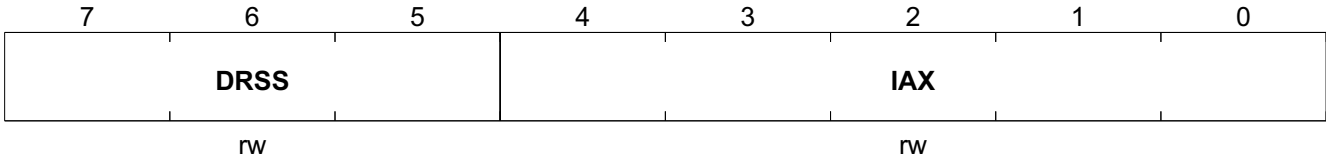



| Field | Bits | Type | Description |
|---|---|---|---|
| IAR | 7:3 | rw | **Integral Parameter Selection**<br>(Corner frequency and attenuation selection) for the DCO-R<br>Only valid if CMR6.DCOCOMPN = ´1´and CMR2.ECFAR = ´1´, see Chapter 3.7.8. |
| RS | 2:0 | rw | **Receive Clock (RCLK) Frequency Selection**<br>See also Chapter 3.7.<br>$000_B$ clock recovered from the line through the DPLL drives RCLK.<br>$001_B$ clock recovered from the line through the DPLL drives RCLK. logically OR´d with the incoming LOS signal.<br>$010_B$ 2.048 MHz, dejitered, sourced by DCO-R.<br>$011_B$ 4.096 MHz, dejitered, sourced by DCO-R.<br>$100_B$ 8.192 MHz, dejitered, sourced by DCO-R.<br>$101_B$ 16.384 MHz, dejitered, sourced by DCO-R.<br>$110_B$ 2.048 MHz logically OR´d with LOS.<br>$111_B$ 16.384 MHz logically OR´d with LOS. |

## Clock Mode Register 5

*Note: The reset value depends on the channel, so that for the DCO-R the current channel is selected by the bits DRSS (for example for channel 3 the reset value is ´40´$_H$).*

| CMR5 | Offset | Reset Value |
|---|---|---|
| Clock Mode Register 5 | $xx42_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| DRSS | 7:5 | rw | **DCO-R Channel Selection**<br>See **Chapter 3.7**.<br>$000_B$ receive reference clock generated by the DPLL of channel 1.<br>$001_B$ receive reference clock generated by the DPLL of channel 2.<br>$010_B$ receive reference clock generated by the DPLL of channel 3.<br>$011_B$ receive reference clock generated by the DPLL of channel 4.<br>$1xx_B$ reserved. |
| IAX | 4:0 | rw | **Integral Parameter Selection**<br>(Corner frequency and attenuation selection) for the DCO-X<br>Only valid if CMR6.DCOCOMPN = ´1´ and CMR2.ECFAX = ´1´, see **Chapter 3.7.8**. |

## Clock Mode Register 6

| CMR6 | Offset | Reset Value |
|---|---|---|
| Clock Mode Register 6 | $xx43_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DCOCOMPN | SRESR | SRESX | STF | | | SCFX | ATCS |
| rw | rw | rw | rw | | | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| DCOCOMPN | 7 | rw | **Compatibility Programming of DCO-R/DCO-X Disable**<br>Only applicable if CMR2.ECFAR/ECFAX is set. See Chapter 3.7.8, Table 23.<br>$0_B$ programming of corner frequencies of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0) /CFAX(3:0), compatible to the QuadLIU. Register bits CMR5.IAX(4:0)/CMR4.IAR(4:0) are not valid.<br>$1_B$ programming of corner frequencies and attenuation factors of DCO-R/DCO-X is done with registers CMR3.CFAR (3:0)/CFAX(3:0) and CMR4.IAR(4:0)/CMR5.IAX(4:0) in the range 0.2 ... 20 Hz. |
| SRESR | 6 | rw | **Soft Reset of DCO-R**<br>By setting this bit a soft reset of the DCO-R will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-R lock functionality, this bit must be cleared subsequently. See Chapter 3.7.8.<br>$0_B$ DCO-R enabled (normal lock functionality).<br>$1_B$ soft reset of DCO-R, no lock functionality. |
| SRESX | 5 | rw | **Soft Reset of DCO-X**<br>By setting this bit a soft reset of the DCO-X will be performed: The initial phase error is set to zero and the loop filter is cleared. To enable the DCO-X lock functionality, this bit must be cleared subsequently. See Chapter 3.7.8.<br>$0_B$ DCO-X enabled (normal lock functionality).<br>$1_B$ soft reset of DCO-X, no lock functionality. |
| STF | 4:2 | rw | **Transmit Clock (TCLK) Frequency Selection**<br>See Chapter 3.9.2. Note that frequencies are not in ascent ordering.<br>$000_B$ 2.048 MHz.<br>$001_B$ 8.192 MHz.<br>$010_B$ 4.096 MHz.<br>$011_B$ 16.384 MHz.<br>$100_B$ 32.768 MHz.<br>$101_B$ reserved.<br>$110_B$ reserved.<br>$111_B$ reserved. |

| Field | Bits | Type | Description |
|---|---|---|---|
| SCFX | 1 | rw | **Select Corner Frequency of DCO-X**<br>Only applicable if CMR2.EXFAX = ´0´. See **Chapter 3.7.8** and **Chapter 3.9.4**.<br>$0_B$ corner frequency of DCO-X is 2 Hz.<br>$1_B$ corner frequency of DCO-X is 0.2 Hz. |
| ATCS | 0 | rw | **Automatic Transmit Clock Switching**<br>See **Chapter 3.9.3**. If TCLK is lost, automatically switching to FCLKX can be performed.<br>*Note: Kind of used transmit clock source is shown in status register XCLKS.*<br>$0_B$ automatic clock switching is disabled.<br>$1_B$ automatic clock switching is enabled. |

## Clock Mode Register 1

| CMR1 | Offset | Reset Value |
|---|---|---|
| Clock Mode Register 1 | $xx44_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | | **DCS** | Res | **DXJA** | **DXSS** |
| | | | | rw | | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| DCS | 3 | rw | **Disable Clock-Switching**<br>In Slave mode (LIM0.MAS = ´0´) the DCO-R is synchronized on the recovered route clock. In case of loss-of-signal LOS the DCO-R switches automatically to the clock sourced by port SYNC.<br>$0_B$ automatic switching from RCLK to SYNC is enabled<br>$1_B$ automatic switching from RCLK to SYNC is disabled |
| DXJA | 1 | rw | **Disable Internal Transmit Jitter Attenuation**<br>Setting this bit disables the transmit jitter attenuation. Reading the data out of the transmit elastic buffer and transmitting on XL1/2 (XDOP/N/XOID) is done with the clock provided on pin TCLK. In transmit elastic buffer bypass mode the transmit clock is taken from FCLKX, independent of this bit. |
| DXSS | 0 | rw | **DCO-X Synchronization Clock Source**<br>$0_B$ The DCO-X circuitry synchronizes to the internal reference clock which is sourced by FCLKX/R or RCLK. Since there are many reference clock opportunities the following internal prioritizing in descending order from left to right is realized: LIM1.RL > CMR1.DXSS > LIM2.ELT > current working clock of transmit system interface. If one of these bits is set the corresponding reference clock is taken.<br>$1_B$ DCO-X synchronizes to an external reference clock provided on multi function port XPA or XPB pin function TCLK, if no remote loop is active. TCLK is selected by PC(2:1).XPC(3:0) = ´0011B´. |

## Clock Mode Register 2

| CMR2 | Offset | Reset Value |
|---|---|---|
| Clock Mode Register 2 | $xx45_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **ECFAX** | **ECFAR** | **DCOXC** | **DCF** | **IRSP** | **IRSC** | Res | **IXSC** |
| rw | rw | rw | rw | rw | rw | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| ECFAX | 7 | rw | **Enable Corner Frequency Adjustment for DCO-X**<br>See **Chapter 3.7.8**.<br>*Note: DCO-X must be activated.*<br>$0_B$ adjustment is disabled (only 2 Hz and 0.2 Hz are possible).<br>$1_B$ adjustment is enabled as programmed in CMR3.CFAX(3:0) and CMR4.IAX(4:0). |
| ECFAR | 6 | rw | **Enable Corner Frequency Adjustment for DCO-R**<br>See **Chapter 3.7.8**.<br>*Note: DCO-R must be activated.*<br>$0_B$ adjustment is disabled (only 2 Hz and 0.2 Hz are possible).<br>$1_B$ adjustment is enabled as programmed in CMR3.CFAR(3:0) and CMR5.IAR(4:0). |
| DCOXC | 5 | rw | **DCO-X Center-Frequency Enable**<br>See **Chapter 3.7.8**<br>$0_B$ The center function of the DCO-X circuitry is disabled.<br>$1_B$ The center function of the DCO-X circuitry is enabled. DCO-X centers to 2.048 MHz related to the master clock reference (MCLK), if reference clock (e.g. FCLKX) is missing. |
| DCF | 4 | rw | **DCO-R Center- Frequency Disabled**<br>See also **Table 24**.<br>$0_B$ The DCO-R circuitry is frequency centered in master mode if no 2.048 MHz reference clock on pin SYNC is provided or in slave mode if a loss-of-signal occurs in combination with no 2.048 MHz clock on pin SYNC or a gapped clock is provided on pin RCLKI and this clock is inactive or stopped.<br>$1_B$ The center function of the DCO-R circuitry is disabled. The generated clock (DCO-R) is frequency frozen in that moment when no clock is available on pin SYNC or pin RCLKI. The DCO-R circuitry starts synchronization as soon as a clock appears on pins SYNC or RCLKI. |

| Field | Bits | Type | Description |
|---|---|---|---|
| IRSP | 3 | rw | **Internal Receive System Frame Sync Pulse**<br>*Note: Recommendation: This bit should be set to ´1´.*<br>$0_B$ The frame sync pulse is derived from RDOP output signal internally (free running).<br>$1_B$ The frame sync pulse for the receive system interface is internally sourced by the DCO-R circuitry. This internally generated frame sync signal can be output (active low) on multifunction ports RP(A to D) (RPC(3:0) = ´$0001_H$´). |
| IRSC | 2 | rw | **Internal Receive Digital (Framer) Clock**<br>$0_B$ The working clock for the receive framer interface is sourced by FCLKR or in receive elastic buffer bypass mode from the corresponding extracted receive clock RCLK.<br>$1_B$ The working clock for the receive framer interface is sourced internally by DCO-R or in bypass mode by the extracted receive clock. FCLKR is ignored. |
| IXSC | 0 | rw | **Internal Transmit Digital (Framer) Clock**<br>$0_B$ The working clock for the transmit framer interface is sourced by FCLKX.<br>$1_B$ The working clock for the transmit framer interface is sourced internally by the working clock of the receive framer interface. FCLKX is ignored. |

## Global Configuration Register

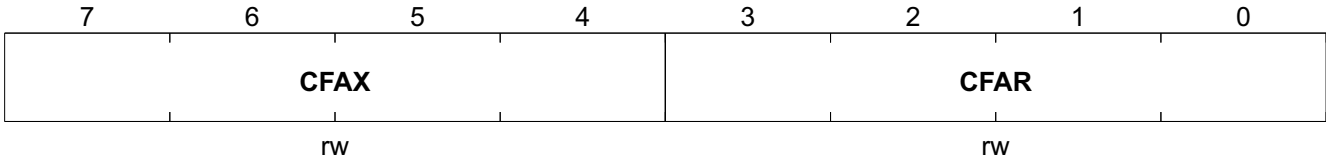
| GCR | Offset | Reset Value |
|---|---|---|
| Global Configuration Register | $0046_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **VIS** | **SCI** | Res | | | | | **PD** |
| rw | rw | | | | | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| VIS | 7 | rw | **Masked Interrupts Visible**<br>See also **Chapter 3.5.3**<br>$0_B$ Masked interrupt status bits are not visible in registers ISR(7:0).<br>$1_B$ Masked interrupt status bits are visible in ISR(7:0), but they are not visible in register GIS. |
| SCI | 6 | rw | **Status Change Interrupt**<br>$0_B$ Interrupts are generated either on activation or deactivation of the internal interrupt source.<br>$1_B$ The following interrupts are activated both on activation and deactivation of the internal interrupt source: ISR2.LOS, ISR2.AIS, ISR3.LMFA16. |
| PD | 0 | rw | **Power Down**<br>Switches between power-up and power-down mode. After switching from power down to power up a receiver reset should be made by setting of CMDR.RRES.<br>$0_B$ Power up<br>$1_B$ Power down: All outputs are driven inactive; multifunction ports are driven high by the weak internal pull-up device. |

## Clock Mode Register 3

| CMR3 | Offset | Reset Value |
|---|---|---|
| Clock Mode Register 3 | $xx48_H$ | $00_H$ |

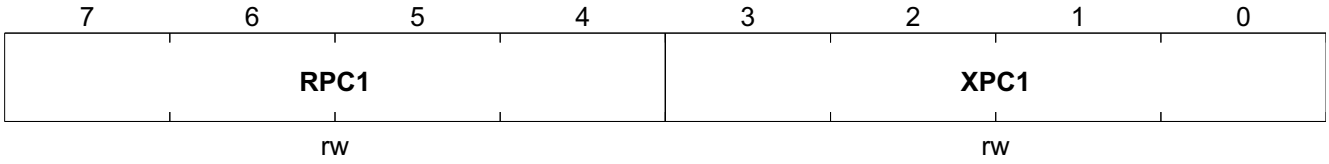



| Field | Bits | Type | Description |
|---|---|---|---|
| CFAX | 7:4 | rw | **Corner Frequency Adjustment for DCO-X**<br>see **Chapter 3.7.8**.<br>*Note: DCO-X must be activated and CMR2.ECFAX must be set (adjustment must be enabled).* |
| CFAR | 3:0 | rw | **Corner Frequency Adjustment for DCO-R**<br>See **Chapter 3.7.8**.<br>*Note: DCO-R must be activated and CMR2.ECFAR must be set (adjustment must be enabled).* |

**Port Configuration 1**

See **Chapter 3.12**.

| PC1 | Offset | Reset Value |
|---|---|---|
| **Port Configuration 1** | **xx80$_H$** | **00$_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| RPC1 | 7:4 | rw | **Receive Multifunction Port Configuration**<br>See **Chapter 3.12**. The multifunction ports RP(A to D) are bidirectional. After Reset the ports RPA and RPB are reserved, the port RPC is configured as RCLK output. With the selection of the pin function the In/Output configuration is also achieved. Register PC1 configures port RPA, while PC2 configures port RPB, PC3 configures port RPC and PC4 configures port RPD.<br>See **RPC1 Constant Values** |
| XPC1 | 3:0 | rw | **Transmit Multifunction Port Configuration**<br>See **Chapter 3.12**. The multifunction ports XP(A to D) are bidirectional. After Reset these ports are configured as inputs. With the selection of the pin function the In/Output configuration is also achieved. Each of the three different input functions (TCLK, XLT and $\overline{\text{XLT}}$) may only be selected once. No input function must be selected twice or more. Register PC1 configures port XPA, PC2 configures port XPB, PC3 configures port XPC and PC4 the port XPD.<br>See **XPC1 Constant Values** |

**Table 45 RPC1 Constant Values**

| Name and Description | Value |
|---|---|
| **Reserved** | $0000_B$ |
| **Reserved** | $0001_B$ |
| **Reserved** | $0010_B$ |
| **Reserved** | $0011_B$ |
| **Reserved** | $0100_B$ |
| **Reserved** | $0101_B$ |
| **Reserved** | $0110_B$ |
| **Reserved** | $0111_B$ |
| **RLT: Receive line termination (input)**<br>“Hardware” switching of receive line termination, see **Chapter 3.7.3** and **LIM0**. | $1000_B$ |
| **GPI: general purpose input**<br>Value of this input is stored in register MFPI. | $1001_B$ |

**Table 45 RPC1 Constant Values** (cont'd)

| Name and Description | Value |
|---|---|
| **GPOH: General purpose output, high level**<br>Pin is set fixed to high level | $1010_B$ |
| **GPOL: General purpose output, low level**<br>Pin is set fixed to low level | $1011_B$ |
| **LOS: Loss of signal**<br>Loss of signal indication output | $1100_B$ |
| **RTDMT: Receive TDM tristate (input)**<br>Receive TDM i/f tristate (RDOP, RCLK). | $1101_B$ |
| **RDON: Receive data out negative**<br>Negative receive data out in dual rail mode or bipolar violation out in LIU single rail mode | $1110_B$ |
| **RCLK: RCLK output** | $1111_B$ |

**Table 46 XPC1 Constant Values**

| Name and Description | Value |
|---|---|
| **Reserved** | $0000_B$ |
| **Reserved** | $0001_B$ |
| **Reserved** | $0010_B$ |
| **TCLK: Transmit Clock (Input)**<br>A 2.048/8.192 MHz clock has to be sourced by the system if the internal generated transmit clock (DCO-X) is not used. Optionally this input is used as a synchronization clock for the DCO-X circuitry with a frequency of 2.048 MHz. | $0011_B$ |
| **Reserved** | $0100_B$ |
| **Reserved** | $0101_B$ |
| **Reserved** | $0110_B$ |
| **XCLK: Transmit Line Clock (Output)**<br>Frequency: 2.048 MHz | $0111_B$ |
| **XLT: Transmit Line Tristate control input, high active**<br>With a high level on this port the transmit lines XL1/2 or XDOP/N are set directly into tristate. This pin function is logically OR´d with register XPM2.XLT. See **Chapter 3.9.1**. | $1000_B$ |
| **GPI: General Purpose Input, low level**<br>Value of this input is stored in register MFPI. | $1001_B$ |
| **GPOH: General Purpose Output, high level**<br>Pin is set fixed to high level | $1010_B$ |
| **GPOL: General Purpose Output, low level**<br>Pin is set fixed to low level | $1011_B$ |
| **Reserved** | $1100_B$ |
| **XDIN: Transmit Data In Negative**<br>Negative transmit data in for dual rail mode | $1101_B$ |
| **XLT: Transmit Line Tristate control input, low active**<br>See XLT | $1110_B$ |
| **Reserved** | $1111_B$ |

Only one of the ports RPA, RPB, RPC or RPD must be configured as RTDMT.

Only one of the ports XPA, XPB, XPC or XPD must be configured as XLT or $\overline{\text{XLT}}$.

The registers PC1, PC2 and PC4 have the reset values ´$00_H$´, PC3 has the reset value ´$F0_H$´.
The Offset Addresses are listed in **PCn Overview**, for bit names refer to **Port Configuration Registers**.

**Table 47 PCn Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| PC2 | Port Configuration Register 2 | $xx81_H$ | |
| PC3 | Port Configuration Register 3 | $xx82_H$ | |
| PC4 | Port Configuration Register 4 | $xx83_H$ | |

**Table 48 Port Configuration Registers**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PC1 | RPC13 | RPC12 | RPC11 | RPC10 | XPC13 | XPC12 | XPC11 | XPC10 |
| PC2 | RPC23 | RPC22 | RPC21 | RPC20 | XPC23 | XPC22 | XPC21 | XPC20 |
| PC3 | RPC33 | RPC32 | RPC31 | RPC30 | XPC33 | XPC32 | XPC31 | XPC30 |
| PC4 | RPC43 | RPC42 | RPC41 | RPC40 | XPC43 | XPC42 | XPC41 | XPC40 |

## Port Configuration 5

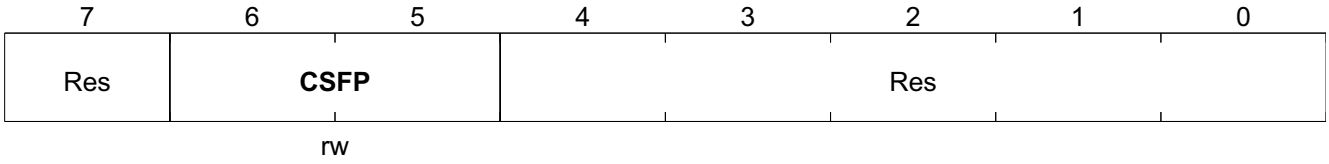
| PC5 | Offset | Reset Value |
|---|---|---|
| Port Configuration 5 | $xx84_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **PHDSX** | **PHDSR** | Res | | | **0** | **CSRP** | **CRP** |
| rw | rw | | | | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| PHDSX | 7 | rw | **Phase Decoder Switch for DCO-X**<br>See formulas in **GCM6**.<br>$0_B$ switch phase decoder by 1/3<br>$1_B$ switch phase decoder by 1/6 |
| PHDSR | 6 | rw | **Phase Decoder Switch for DCO-R**<br>See formulas in **GCM6**.<br>$0_B$ switch phase decoder by 1/3<br>$1_B$ switch phase decoder by 1/6 |
| 0 | 2 | rw | **Fixed 0** |
| CSRP | 1 | rw | **Configure FCLKR Port**<br>$0_B$ FCLKR: Input<br>$1_B$ FCLKR: Output |
| CRP | 0 | rw | **Configure RCLK Port**<br>$0_B$ RCLK: Input<br>$1_B$ RCLK: Output |

## Global Port Configuration 1

| GPC1 | Offset | Reset Value |
|---|---|---|
| Global Port Configuration 1 | $0085_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| CSFP | 6:5 | rw | **Configure SEC/FSC Port**<br>The FSC pulse is generated if the DCO-R circuitry of the selected channel is active (CMR2.IRSC = ´1´ or CMR1.RS(1:0) = ´$10_b$´ or ´$11_b$´), see **Chapter 3.8.4**<br>$00_B$ SEC: Input, active high<br>$01_B$ SEC: Output, active high<br>$10_B$ FSC: Output, active high<br>$11_B$ FSC: Output, active low |

## Port Configuration 6

| PC6 | Offset | Reset Value |
|---|---|---|
| Port Configuration 6 | $xx86_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | **TSRE** | Res | | | | | |
| | rw | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| TSRE | 6 | rw | **Transmit Serial Resistor Enable**<br>$0_B$ Internal serial resistors are disabled.<br>$1_B$ Internal serial resistors are enabled. |

## Global Port Configuration Register 2

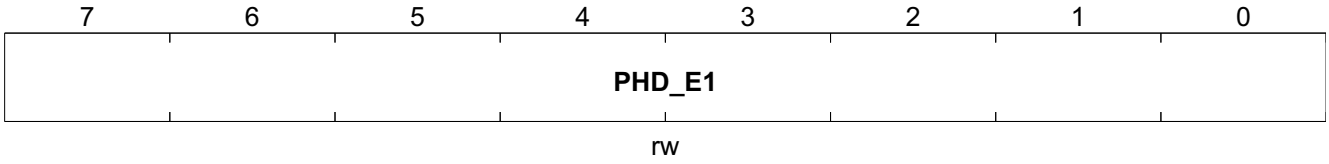
| GPC2 | Offset | Reset Value |
|---|---|---|
| Global Port Configuration Register 2 | $008A_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | FSS | | | Res | R1S | | |
| | rw | | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| FSS | 6:4 | rw | **FSC Source Selection**<br>See **Chapter 3.8.4**.<br>$000_B$ FSC sourced by channel 1.<br>$001_B$ FSC sourced by channel 2.<br>$010_B$ FSC sourced by channel 3.<br>$011_B$ FSC sourced by channel 4.<br>$1xx_B$ reserved. |
| R1S | 2:0 | rw | **RCLK1 Source Selection**<br>See **Chapter 3.7**.<br>$000_B$ RCLK1 sourced by channel 1.<br>$001_B$ RCLK1 sourced by channel 2.<br>$010_B$ RCLK1 sourced by channel 3.<br>$011_B$ RCLK1 sourced by channel 4.<br>$1xx_B$ reserved. |

## Global Clock Mode Register 1

| GCM1 | Offset | Reset Value |
|---|---|---|
| Global Clock Mode Register 1 | $0092_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| PHD_E1 | 7:0 | rw | **Frequency Adjust for E1 lower 8 bits, for highest 4 bits see GCM2)**<br>For details see calculation formulas in register **GCM6** and **Table 49**. |

## Global Clock Mode Register 2

| GCM2 | Offset | Reset Value |
|---|---|---|
| Global Clock Mode Register 2 | $0093_H$ | $10_H$ |

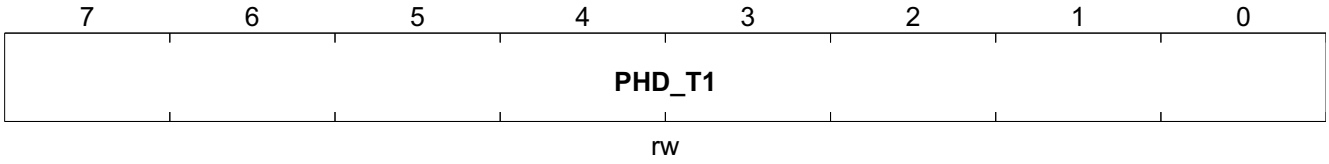
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PHSDEM | PHSDIR | PHSDS | VFREQ_EN | PHD_E1 | | | |
| rw | rw | rw | rw | rw | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| PHSDEM | 7 | rw | **RX Phase Decoder Demand**<br>$0_B$ default operation<br>$1_B$ see formulas in **GCM6**. |
| PHSDIR | 6 | rw | **RX Phase Decoder Direction**<br>$0_B$ default operation<br>$1_B$ see formulas in **GCM6**. |
| PHSDS | 5 | rw | **RX Phase Decoder Switch**<br>$0_B$ default operation<br>$1_B$ see formulas in **GCM6**. |
| VFREQ_EN | 4 | rw | **Variable Frequency Enable**<br>If “fixed mode” mode is selected the clock frequency at the pin MCLK must be 2.048 for E1 or 1.544 MHz for T1/J1 respectively. The setting of the whole clock mode is done automatically: Register bits of GCM1, GCM2.PHSDEM, PHDIR, PHSDS, PHD_E1 and GCM3 to GCM8 are unused. If “fixed mode” mode is selected and the SPI- or SCI-interface is used as controller interface, the pinstrapping values at D(15:5) are also not used. See also **Chapter 3.5.5**.<br>*Note: If “fixed mode “ is enabled all of the four ports must work in the same mode, either in T1 or in E1 mode. A switching between E1 and T1 modes causes a reset of the whole clock system. If “fixed mode“ is disabled a switching between E1 and T1 mode (which can be done in this case individually for every port) causes not a reset of the whole clock system.*<br>$0_B$ Fixed clock frequency of 2.048 (E1) or 1.544 MHz (T1/J1)<br>$1_B$ Variable master clock frequency (normal operation, operation after reset) |

| Field | Bits | Type | Description |
|---|---|---|---|
| PHD_E1 | 3:0 | rw | **Frequency Adjust for E1**<br>(highest 4 bits, for lower 8 bits see GCM1)<br>The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6** and **Table 49**.<br>$100000000000_B$ -2048<br>$\cdots_B$<br>$000000000000_B$ 0<br>$\cdots_B$<br>$011111111111_B$ +2047 |

## Global Clock Mode Register 3

| GCM3 | Offset | Reset Value |
|---|---|---|
| Global Clock Mode Register 3 | $0094_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| PHD_T1 | 7:0 | rw | **Frequency Adjust for T1**<br>(lower 8 bits, for highest 4 bits see GCM4)<br>The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6** and **Table 49**.<br>$100000000000_B$ -2048<br>…B<br>$000000000000_B$ 0<br>…B<br>$011111111111_B$ +2047 |

## Global Clock Mode Register 4

| GCM4 | Offset | Reset Value |
|---|---|---|
| Global Clock Mode Register 4 | $0095_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DVM_T1 | | | Res | PHD_T1 | | | |
| rw | | | | rw | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| DVM_T1 | 7:5 | rw | **Divider Mode for T1**<br>This bits can be write and read to be software compatible to QuadLIU, but has no influence on the clock system |
| PHD_T1 | 3:0 | rw | **Frequency Adjust for T1**<br>(highest 4 bits, for lower 8 bits see GCM3)<br>The 12 bit frequency adjust value is in the decimal range of -2048 to +2047. Negative values are represented in 2s-complement format. For details see calculation formulas in register **GCM6** and **Table 49**.<br>$100000000000_B$ -2048<br>…B<br>$000000000000_B$ 0<br>…B<br>$011111111111_B$ +2047 |

## Global Clock Mode Register 5

*Note: Write operations to GCM5 and GCM6 initiate a PLL reset if the asynchronous interface is selected (IM(1:0) = ´0x´) and if the "flexible master clocking mode" is selected (GCM2.VFREQ_EN = ´1´), see* ***Chapter 3.5.5****.*

| GCM5 | Offset | Reset Value |
|---|---|---|
| **Global Clock Mode Register 5** | **$0096_H$** | **$00_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **MCLK_LOW** | Res | | **PLL_M** | | | | |
| rw | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| MCLK_LOW | 7 | rw | **Master Clock Range Low**<br>This bit can be write and read to be software compatible to QuadLIU, but has no influence on the clock system. |
| PLL_M | 4:0 | rw | **PLL Dividing Factor M**<br>For details see calculation formulas in register **GCM6** and **Table 49**.<br>$00001_B$ 1<br>…B<br>$11111_B$ 31 |

## Global Clock Mode Register 6

*Note: Write operations to GCM5 and GCM6 initiate a PLL reset if the asynchronous interface is selected (IM(1:0) = ´0x´) and if the "flexible master clocking mode" is selected (GCM2.VFREQ_EN = ´1´), see* ***Chapter 3.5.5.1****.*

| GCM6 | Offset | Reset Value |
|---|---|---|
| **Global Clock Mode Register 6** | **$0097_H$** | **$00_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | **PLL_N** | | | | |
| | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| PLL_N | 4:0 | rw | **PLL Dividing Factor N**<br>For details see calculation formulas below and **Table 49**.<br>$000001_B$ 1<br>…B<br>$111111_B$ 63 |

**Flexible Clock Mode Settings:**

If "flexible master clock mode" is used (VFREQ_EN = ´1´), the according register settings can be calculated as follows (a windows-based program for automatic calculation is available, see **Chapter 8.3**. For some of the standard frequencies see the table below.

**1.** The master clock MCLK must be in the following frequency range:

1.02 MHz ≤ $f_{MCLK}$ ≤ 20 MHz

**2.** Generally the PLL of the master clocking unit includes an input divider with a dividing factor PLL_M +1 and a feedback divider with a dividing factor 4 x (PLL_N +1). So it generates a clock $f_{PLL}$ of about

$f_{PLL}$ = $f_{MCLK}$ x 4 x (PLL_N +1) / (PLL_M +1).

**3.** The selection of PLL_N and PLL_M must be done in the following way:

The PLL frequency $f_{PLL}$ must be in the following range:

200 MHz ≤ $f_{PLL}$ ≤ 300 MHz.

The combinations of the values PLL_M and PLL_M must fulfill the equations:

2 MHz ≤ $f_{MCLK}$ / (PLL_M +1) ≤ 6 MHz , if PLL_N is in the range 25 to 63.

5 MHz ≤ $f_{MCLK}$ / (PLL_M +1) ≤ 15 MHz , if PLL_N is in the range 1 to 24.

**4.** In E1 mode, the selection of PHSN_E1 and PHSX_E1 must be done in such a manner that the frequency for the receiver $f_{RX\_E1}$ has nearly the value 16 x $f_{DATA\_E1}$ x (1 + 100ppm) = 32.7713 MHz:

$f_{RX\_E1}$ = $f_{PLL}$ / {PHSN_E1 + (PHSX_E1 / 6)}.

In T1/J1 mode, the selection of PHSN_T1 and PHSX_T1 must be done in such a manner that the frequency for the receiver $f_{RX\_T1}$ has nearly the value 16 x $f_{DATA\_T1}$ x (1 + 100ppm) = 24.706 MHz:

$f_{RX\_T1}$ = $f_{PLL}$ / {PHSN_T1 + (PHSX_T1 / 6)}.

GCM2.PHSDEM, GCM2.PHSDIR, GCM2.PHSDS, PC5.PHDSX and PC5.PHDSR must be left to ´0´

**5.** To bring the “characteristic E1 frequency” $f_{outE1}$ exact to 16 x $f_{DATA\_E1}$ = 32.7680 MHz a correction value PHD_E1 is necessary:

PHD_E1 = round **(**12288 x { [PHSN_E1 + (PHSX_E1 / 6)] - [$f_{pll}$ / (16 x $f_{DATA\_E1}$)] }**)**.

To bring the “characteristic T1 frequency” $f_{outT1}$ exact to 16 x $f_{DATA\_T1}$ = 24.704 MHz a correction value PHD_T1 is necessary:

PHD_T1 = round **(**12288 x { [PHSN_T1 + (PHSX_T1 / 6)] - [$f_{pll}$ / (16 x $f_{DATA\_T1}$)] }**)**.

Example: $f_{MCLK}$ = 2.048 MHz

PLL_N = 33; PLL_M = 0 : $f_{PLL}$ = 278.528 MHz

PHSN_E1 = 8; PHSN_E1 = 2: $f_{RX\_E1}$ = 33.42 MHz

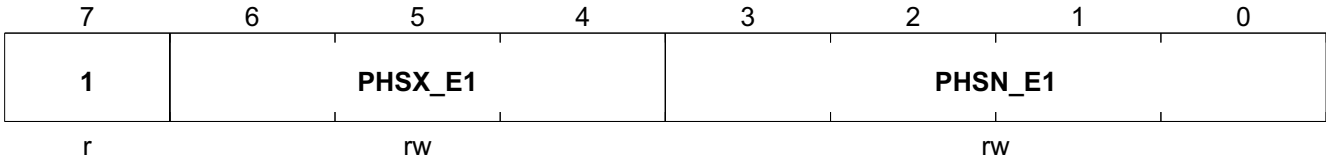
PHD_E1 = -2048: $f_{outE1}$ = 32.768 MHz

**Table 49 Clock Mode Register Settings for E1 or T1/J1**

| fMCLK [MHz] | GCM1 | GCM2 | GCM3 | GCM4 | GCM5 | GCM6 | GCM7 | GCM8 |
|---|---|---|---|---|---|---|---|---|
| 1.5440 | $00_H$ | $15_H$ | $00_H$ | $08_H$ | $00_H$ | $3F_H$ | $9C_H$ | $DF_H$ |
| 2.0480 | $00_H$ | $18_H$ | $FB_H$ | $0B_H$ | $00_H$ | $2F_H$ | $DB_H$ | $DF_H$ |
| 8.1920 | $00_H$ | $18_H$ | $FB_H$ | $0B_H$ | $00_H$ | $0B_H$ | $DB_H$ | $DF_H$ |
| 16.3840 | $00_H$ | $18_H$ | $FB_H$ | $0B_H$ | $01_H$ | $0B_H$ | $DB_H$ | $DF_H$ |

## Global Clock Mode Register 7

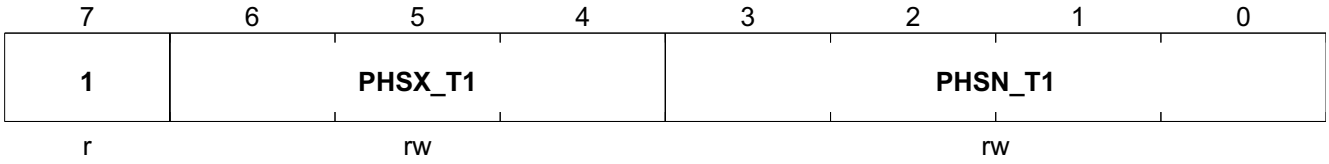
| GCM7 | Offset | Reset Value |
|---|---|---|
| Global Clock Mode Register 7 | $0098_H$ | $80_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| 1 | 7 | r | **Fixed ´1´** |
| PHSX_E1 | 6:4 | rw | **Frequency Adjustment value E1**<br>For details see calculation formulas in register **GCM6** and **Table 49**.<br>$000_B$ 0<br>…B<br>$101_B$ 5 |
| PHSN_E1 | 3:0 | rw | **Frequency Adjustment value E1**<br>For details see calculation formulas in register **GCM6** and **Table 49**.<br>$0001_B$ 1<br>…B<br>$1111_B$ 15 |

## Global Clock Mode Register 7

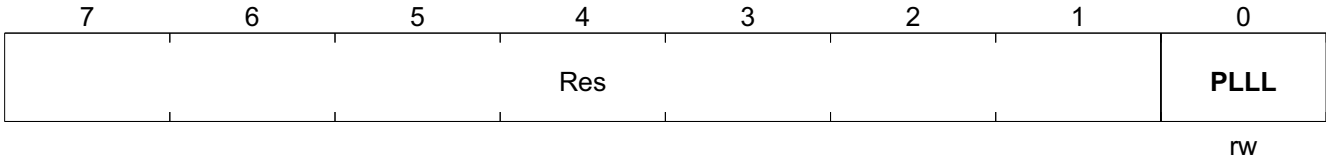
| GCM8 | Offset | Reset Value |
|---|---|---|
| Global Clock Mode Register 7 | $0099_H$ | $80_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| 1 | 7 | r | **Fixed ´1´** |
| PHSX_T1 | 6:4 | rw | **Frequency Adjustment Value T1**<br>For details see calculation formulas in register **GCM6** and **Table 49**.<br>$000_B$ 0<br>…B<br>$101_B$ 5 |
| PHSN_T1 | 3:0 | rw | **Frequency Adjustment Value T1**<br>For details see calculation formulas in register **GCM6** and **Table 49**.<br>$0001_B$ 1<br>…B<br>$1111_B$ 15 |

## Global Interrupt Mask Register

| GIMR | Offset | Reset Value |
|---|---|---|
| Global Interrupt Mask Register | $00A7_H$ | $FF_H$ |

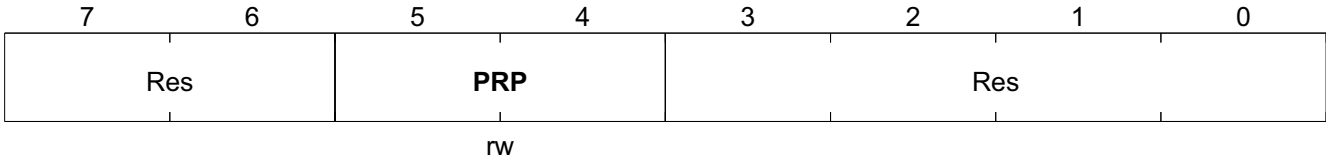



| Field | Bits | Type | Description |
|---|---|---|---|
| PLLL | 0 | rw | **PLL Locked Interrupt Mask**<br>$0_B$ GIS2.PLLLC is enabled.<br>$1_B$ GIS2.PLLLC is disabled. |

**Test Pattern Control Register 0**

See **Chapter 3.11.1**.

| TPC0 | Offset | Reset Value |
|---|---|---|
| **Test Pattern Control Register 0** | **xxA8$_H$** | **00$_H$** |

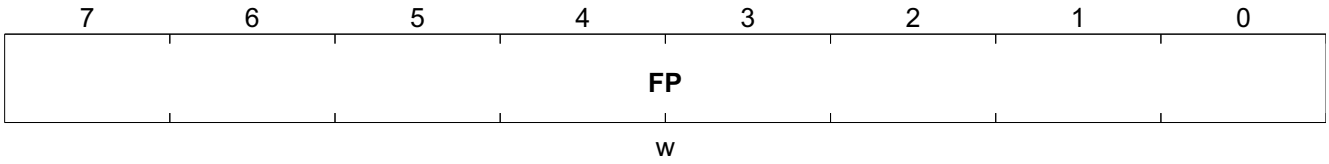



| Field | Bits | Type | Description |
|---|---|---|---|
| PRP | 5:4 | rw | **PRBS Pattern Selection**<br>$00_B$ PRBS11 pattern.<br>$01_B$ PRBS15 pattern.<br>$10_B$ PRBS20 pattern.<br>$11_B$ PRBS23 pattern. |

### Register Field Pointer

This register is used to set a pointer (address) onto the internal register field. After a pointer is set, data can be written into one register of the register field (that register with the address **REGFP**.FP) by writing data into the register **REGFD**. The registers **REGFP** and **REGFD** must be used only as described in **Chapter 3.6.1** and **Chapter 3.7.8.4**. Note that all registers of the register field are reset by a receive reset (**CMDR**.RRES = ´1´).

| REGFP | Offset | Reset Value |
|---|---|---|
| Register Field Pointer | $00BB_H$ | $00_H$ |

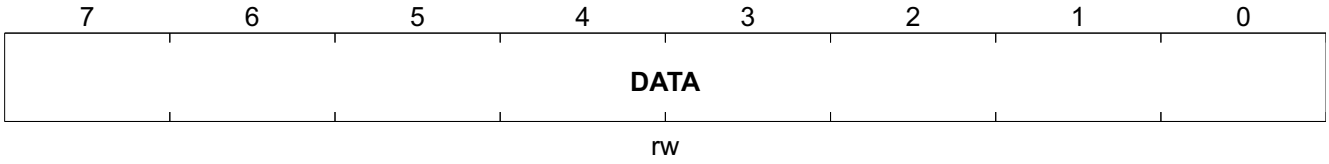



| Field | Bits | Type | Description |
|---|---|---|---|
| FP | 7:0 | w | **Field Pointer**<br>This bitfield is a pointer onto one rtegister in the internal registerfield. |

### Register Field Data

See **REGFP** and **Chapter 3.6.1**. for further description.

| REGFD | Offset | Reset Value |
|---|---|---|
| Register Field Data | $00BC_H$ | $00_H$ |

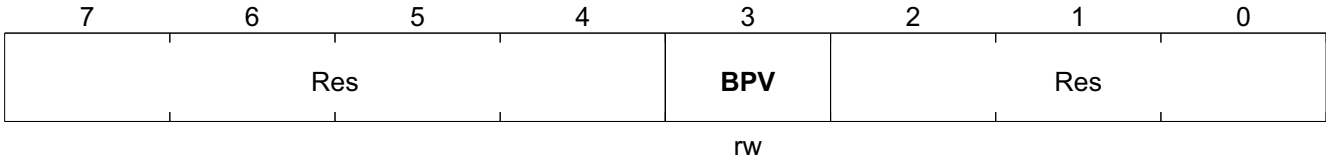



| Field | Bits | Type | Description |
|---|---|---|---|
| DATA | 7:0 | rw | **Data**<br>Data of one register of the internal register field, pointed with the pointer FP. |

## Bugfix Register

See **Chapter 3.5.1**.

| BFR | Offset | Reset Value |
|---|---|---|
| **Bugfix Register** | **xxBD$_H$** | **08$_H$** |

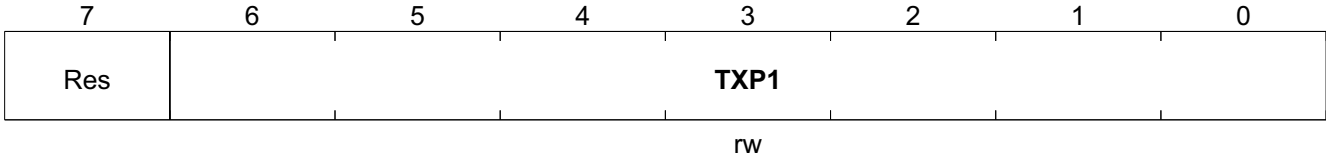



| Field | Bits | Type | Description |
|---|---|---|---|
| BPV | 3 | rw | **Bipolar Violation Detection**<br>This bit selects the kind of Bipolar Violation Detection.<br>$0_B$ Improved Bipolar Violation Detection: Bipolar Violations (BPV) consisting on single ´1´ pulses or on two consecutive ´1´ pulses are detected.<br>$1_B$ Same behaviour of Bipolar Violation Detection as in the QuadLIU™ V2.1. |

### TX Pulse Template Register 1

See **Chapter 3.9.6.1** and **Chapter 3.9.6.2**. This register contains the transmit amplitude of the 1st 1/16 of the transmit pulse. The contents of this register is ignored unless bit XPM2.XPDIS is set. By default, the values programmed in XPM0 to XPM2 are used to control the transmit pulse template.

| TXP1 | Offset | Reset Value |
|---|---|---|
| **TX Pulse Template Register 1** | **xxC1$_H$** | **00$_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| TXP1 | 6:0 | rw | **Transmit Pulse Amplitude**<br>Two´s Complement number of pulse amplitude. |

Registers TXP1to TXP16 have the same description and layout. Every register TXPn defines the amplitude of the part n of 16 of the transmit pulse. An overview is given is the next table.

Note that the reset values of the registers TXP1 to TXP8 are ´38$_H$´, that of the registers TXP9 to TXP16 are ´00$_H$´.

**Table 50 TXP Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| TXP2 | TX Pulse Template Register 2 | xxC2$_H$ | |
| TXP3 | TX Pulse Template Register 3 | xxC3$_H$ | |
| TXP4 | TX Pulse Template Register 4 | xxC4$_H$ | |
| TXP5 | TX Pulse Template Register 5 | xxC5$_H$ | |
| TXP6 | TX Pulse Template Register 6 | xxC6$_H$ | |
| TXP7 | TX Pulse Template Register 7 | xxC7$_H$ | |
| TXP8 | TX Pulse Template Register 8 | xxC8$_H$ | |
| TXP9 | TX Pulse Template Register 9 | xxC9$_H$ | |
| TXP10 | TX Pulse Template Register 10 | xxCA$_H$ | |
| TXP11 | TX Pulse Template Register 11 | xxCB$_H$ | |
| TXP12 | TX Pulse Template Register 12 | xxCC$_H$ | |
| TXP13 | TX Pulse Template Register 13 | xxCD$_H$ | |
| TXP14 | TX Pulse Template Register 14 | xxCE$_H$ | |
| TXP15 | TX Pulse Template Register 15 | xxCF$_H$ | |
| TXP16 | TX Pulse Template Register 16 | xxD0$_H$ | |

## Global Port Configuration Register 3

See **Chapter 3.7**.

| GPC3 | Offset | Reset Value |
|---|---|---|
| Global Port Configuration Register 3 | $00D3_H$ | $21_H$ |

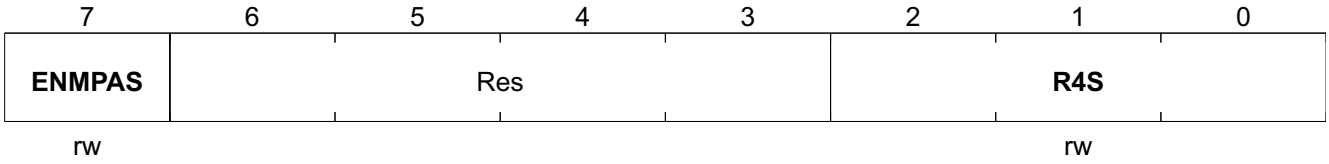
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **ENMPAS** | **R3S** | | | Res | **R2S** | | |
| rw | rw | | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| ENMPAS | 7 | rw | **Enable Multi Purpose Analog Switches**<br>GPC(3:6).ENMPAS must be set all to ´1´ to enable in general the switching of the separate analog switches of all ports.<br>$0_B$ switching to ón´ of the separate analog switches of all ports is disabled.<br>$1_B$ switching to ón´ of the separate analog switches of all ports is enabled (together with GPC(4:6).MPAS). |
| R3S | 6:4 | rw | **RCLK3 Source Selection**<br>$000_B$ RCLK3 sourced by channel 1.<br>$001_B$ RCLK3 sourced by channel 2.<br>$010_B$ RCLK3 sourced by channel 3.<br>$011_B$ RCLK3 sourced by channel 4.<br>$1xx_B$ reserved. |
| R2S | 2:0 | rw | **RCLK2 Source Selection**<br>$000_B$ RCLK2 sourced by channel 1.<br>$001_B$ RCLK2 sourced by channel 2.<br>$010_B$ RCLK2 sourced by channel 3.<br>$011_B$ RCLK2 sourced by channel 4.<br>$1xx_B$ reserved. |

## Global Port Configuration Register 4

See **Chapter 3.7**.

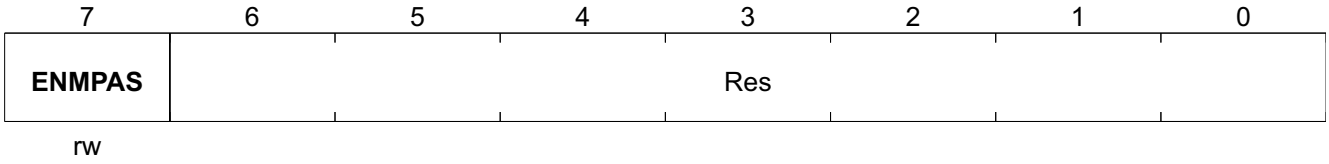
| GPC4 | Offset | Reset Value |
|---|---|---|
| **Global Port Configuration Register 4** | **$00D4_H$** | **$03_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| ENMPAS | 7 | rw | **Enable Multi Purpose Analog Switches**<br>GPC(3:6).ENMPAS must be set all to ´1´ to enable in general the switching of the separate analog switches of all ports.<br>$0_B$ switching to ón´ of the separate analog switches of all ports is disabled.<br>$1_B$ switching to ón´ of the separate analog switches of all ports is enabled (together with GPC(3,5,6).MPAS). |
| R4S | 2:0 | rw | **RCLK4 Source Selection**<br>$000_B$ RCLK4 sourced by channel 1.<br>$001_B$ RCLK4 sourced by channel 2.<br>$010_B$ RCLK4 sourced by channel 3.<br>$011_B$ RCLK4 sourced by channel 4.<br>$1xx_B$ reserved. |

## Global Port Configuration Register 5

| GPC5 | Offset | Reset Value |
|---|---|---|
| Global Port Configuration Register 5 | $00D5_H$ | $65_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| ENMPAS | 7 | rw | **Enable Multi Purpose Analog Switches**<br>GPC(3:6).ENMPAS must be set all to ´1´ to enable in general the switching of the separate analog switches of all ports.<br>$0_B$ switching to ón´ of the separate analog switches of all ports is disabled.<br>$1_B$ switching to ón´ of the separate analog switches of all ports is enabled (together with GPC(3,4,6).MPAS). |

## Global Port Configuration Register 6

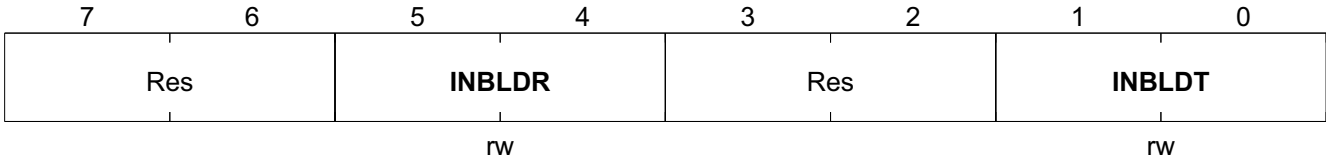
| GPC6 | Offset | Reset Value |
|---|---|---|
| Global Port Configuration Register 6 | $00D6_H$ | $07_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **ENMPAS** | Res | **COMP_DIS** | Res | | | | |
| rw | | rw | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| ENMPAS | 7 | rw | **Enable Multi Purpose Analog Switches**<br>GPC(3:6).ENMPAS must be set all to ´1´ to enable in general the switching of the separate analog switches of all ports.<br>$0_B$ switching to ón´ of the separate analog switches of all ports is disabled.<br>$1_B$ switching to ón´ of the separate analog switches of all ports is enabled (together with GPC(3:5).MPAS). |
| COMP_DIS | 5 | rw | **Compatibility Mode Disable**<br>Setting of this bit disables the compatibility mode. See**Chapter 3.2**.<br>$0_B$ “Compatibility mode”: The QuadLIU™ is fully software compatibel to the version 2.1.<br>$1_B$ “Generic mode”: The QuadLIU™ is not fully software compatibel to the version 2.1 and additional clock configuration features are available. |

## In-Band Loop Detection Time Register

| INBLDTR | Offset | Reset Value |
|---|---|---|
| In-Band Loop Detection Time Register | $00D7_H$ | $00_H$ |

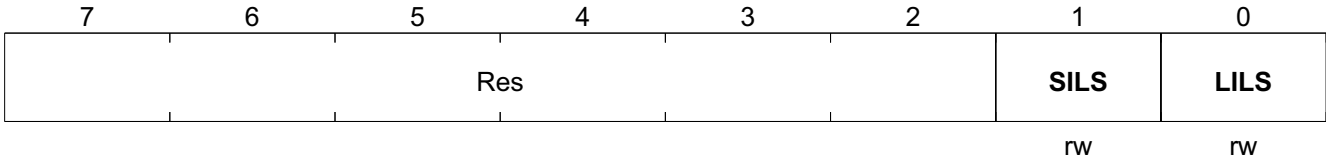



| Field | Bits | Type | Description |
|---|---|---|---|
| INBLDR | 5:4 | rw | **In-Band Loop Detection Time for Line Side**<br>See **Chapter 3.11.2**.<br>$00_B$ at least 16 consecutive in-band loop pattern must be valid for detection and to perform automatic loop switching.<br>$01_B$ at least 32 consecutive in-band loop pattern must be valid for detection and to perform automatic loop switching.<br>$10_B$ in-band loop pattern must be valid for at least 4 seconds for detection and to perform automatic loop switching.<br>$11_B$ in-band loop pattern must be valid for at least 5 seconds for detection and to perform automatic loop switching. |
| INBLDT | 1:0 | rw | **In-Band Loop Detection Time for Framer Side**<br>See **Chapter 3.11.2**<br>$00_B$ at least 16 consecutive “In-band loop sequences” must be valid to perform automatic loop switching.<br>$01_B$ at least 32 consecutive “In-band loop sequences” must be valid to perform automatic loop switching.<br>$10_B$ “In-band loop sequences” must be valid for at least 4 seconds to perform automatic loop switching.<br>$11_B$ “In-band loop sequences” must be valid for at least 5 seconds to perform automatic loop switching. |

### Automatic Loop Switching Register

Enabling of automatic loop switching by In-band loop codes, see **Chapter 3.11.2**, is performed by this register.

| ALS | Offset | Reset Value |
|---|---|---|
| **Automatic Loop Switching Register** | **xxD9$_H$** | **00$_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| SILS | 1 | rw | **Framer (System) In-Band Loop Switching (Local Loop)**<br>This bit controls if automatic switching of the local loop will be done by In-Band loop codes from the framer side, see **Chapter 3.11.2**. The necessary receiption time of In-band loop codes until an automatic loop switching is performed is configured by INBLDTR.INBLDT(1:0).<br>*Note: This feature is not described in E1/T1/J1 standards. Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.*<br>$0_B$ automatic switching of local loop (“on framer side”) is disabled (default).<br>$1_B$ automatic switching of local loop (“on framer side”) by In-band loop codes detected from the framer side is enabled. |
| LILS | 0 | rw | **Line In-Band Loop Switching (Remote Loop)**<br>This bit controls if automatic switching of the remote loop will be done by In-Band loop codes from the line side, see **Chapter 3.11.2**.<br>*Note: Generation of an interrupt when loop up or down code is detected can be selected by demasking (register IMR6). Setting both, SILS and LILS to ´1´ is forbidden.*<br>$0_B$ automatic switching of remote loop (“on line side”) is disabled (default).<br>$1_B$ automatic switching of remote loop (“on line side”) by In-band loop codes detected from the line side is enabled if local loop is not activated by LIM0.LL = ´1´. |

## LIU Mode Register 3

| LIM3 | Offset | Reset Value |
|---|---|---|
| LIU Mode Register 3 | $xxE2_H$ | $00_H$ |

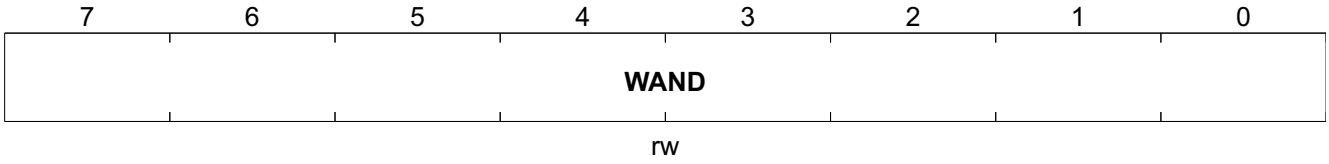
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | | | | DRR | DRX |
| | | | | | | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| DRR | 1 | rw | **Dual-Rail mode on digital side, receive direction**<br>$0_B$ single rail mode on framer receive side.<br>$1_B$ dual rail mode on framer receive side. |
| DRX | 0 | rw | **Dual-Rail mode on digital side, transmit direction**<br>$0_B$ single rail mode on framer transmit side.<br>$1_B$ dual rail mode on framer transmit side. |

### Wander Configuration Register

This register is only valid if register bit **GPC6**.WAN_IMP is set. See **Chapter 3.6.1**. for further description.

| WCON | Offset | Reset Value |
|---|---|---|
| **Wander Configuration Register** | **xxE8$_H$** | **00$_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| WAND | 7:0 | rw | **Wander Improovement**<br>This bitfield configures the internal PLLs for output wander improvement if register bit **GPC6**.WAN_IMP is set.The value must be set to ´03$_H$´. |

## 4.2 Detailed Status Register Description

**Table 51 Registers Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| VSTR | Version Status Register | $004A_H$ | 195 |
| CIS | Channel Interrupt Status Register | $006F_H$ | 212 |
| GIS2 | Global Interrupt Status 2 | $00AD_H$ | 215 |
| DSTR | Device Status Register | $00E7_H$ | 218 |
| RBD | Receive Buffer Delay | $xx49_H$ | 194 |
| RES | Receive Equalizer Status | $xx4B_H$ | 196 |
| LSR0 | Line Status Register 0 | $xx4C_H$ | 197 |
| LSR1 | Line Status Register 1 | $xx4D_H$ | 198 |
| LSR3 | Line Status Register 3 | $xx4E_H$ | 200 |
| LSR2 | Line Status Register 2 | $xx4F_H$ | 202 |
| CVCL | Code Violation Counter Lower Byte | $xx52_H$ | 203 |
| CVCH | Code Violation Counter Higher Byte | $xx53_H$ | 204 |
| BECL | PRBS Bit Error Counter Lower Bytes | $xx58_H$ | 205 |
| BECH | PRBS Bit Error Counter Higher Bytes | $xx59_H$ | 206 |
| ISR1 | Interrupt Status Register 1 | $xx69_H$ | 207 |
| ISR2 | Interrupt Status Register 2 | $xx6A_H$ | 208 |
| ISR3 | Interrupt Status Register 3 | $xx6B_H$ | 209 |
| ISR4 | Interrupt Status Register 4 | $xx6C_H$ | 210 |
| GIS | Global Interrupt Status Register | $xx6E_H$ | 211 |
| MFPI | Multi Function Port Input Register | $xxAB_H$ | 213 |
| ISR6 | Interrupt Status Register 6 | $xxAC_H$ | 214 |
| ISR7 | Interrupt Status Register 7 | $xxD8_H$ | 216 |
| PRBSSTA | PRBS Status Register | $xxDA_H$ | 217 |
| CLKSTAT | Clock Status Register | $xxFE_H$ | 219 |

The register is addressed wordwise.

**Table 52 Registers Access Types**

| Mode | Symbol | Description Hardware (HW) | Description Software (SW) |
|---|---|---|---|
| **Basic Access Types** | | | |
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read/write virtual | rwv | Physically, there is no new register in the generated register file. The real readable and writable register resides in the attached hardware. | Register is read and writable by SW (same as rw type register) |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior |
| read only | ro | Same as r type register | Same as r type register |
| read virtual | rv | Physically, there is no new register in the generated register file. The real readable register resides in the attached hardware. | Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior (same as r type register) |
| write | w | Register is written by software and affects hardware behavior with every write by software. | Register is writable by SW. When read, the register does not return the value that has been written previously, but some constant value instead. |
| write virtual | wv | Physically, there is no new register in the generated register file. The real writable register resides in the attached hardware. | Register is writable by SW (same as w type register) |
| read/write hardware affected | rwh | Register can be modified by hardware and software at the same time. A priority scheme decides, how the value changes with simultaneous writes by hardware and software. | Register can be modified by HW and SW, but the priority SW versus HW has to be specified.<br>SW can read the register. |
| **Special Access Types** | | | |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |

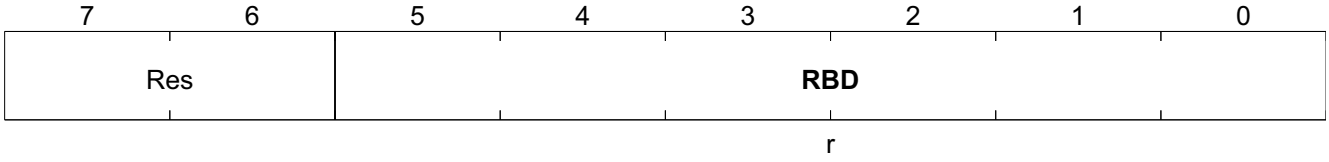
**Table 52 Registers Access Types** (cont'd)

| Mode | Symbol | Description Hardware (HW) | Description Software (SW) |
|---|---|---|---|
| Interrupt enable register | ien | Enables the interrupt source for interrupt generation | SW can read and write this register |
| latch_on_reset | lor | rw register, value is latched after first clock cycle after reset | Register is read and writable by SW |
| Read/write self clearing | rwsc | Register is used as input for the HW, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW. |

## 4.2.1 Status Registers

**Receive Buffer Delay**

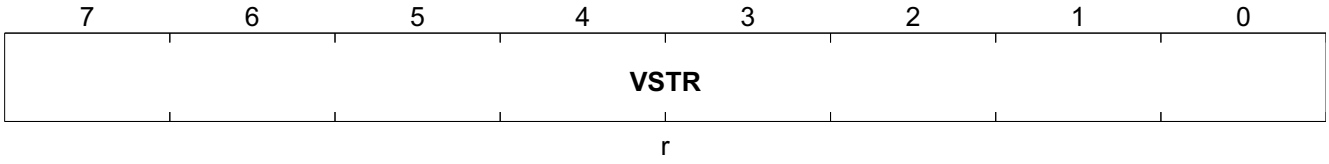
| RBD | Offset | Reset Value |
|---|---|---|
| **Receive Buffer Delay** | **xx49$_H$** | **00$_H$** |




| Field | Bits | Type | Description |
|---|---|---|---|
| RBD | 5:0 | r | **Receive Elastic Buffer Delay**<br>These bits informs the user about the current delay (in time slots) through the receive elastic buffer. The delay is updated every 512 or 256 bits (DIC1.RBS(1:0)). Before reading this register the user has to set bit DEC.DRBD in order to halt the current value of this register. After reading RBD updating of this register is enabled. Not valid if the receive buffer is bypassed.<br>$000000_B$ Delay < 1 time slot<br>…$_B$<br>$111111_B$ Delay > 63 time slot |

## Version Status Register

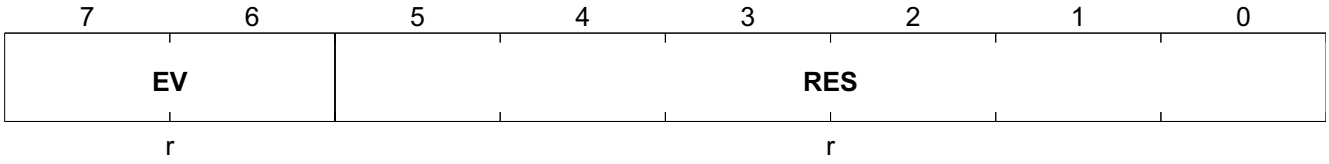
| VSTR | Offset | Reset Value |
|---|---|---|
| Version Status Register | $004A_H$ | H |




| Field | Bits | Type | Description |
|---|---|---|---|
| VSTR | 7:0 | r | **Version Number of Chip**<br>Status information depends on the setting of GPC6.COMP_DIS:<br>$00000101_B$ for COMP_DIS = ´0´<br>$00100000_B$ for COMP_DIS = ´1´ |

## Receive Equalizer Status

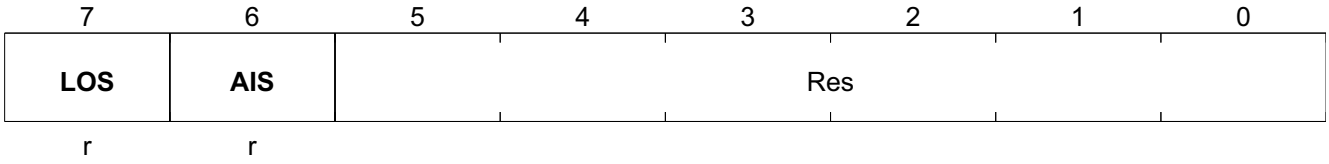
| RES | Offset | Reset Value |
|---|---|---|
| Receive Equalizer Status | $xx4B_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| EV | 7:6 | r | **Equalizer Status Valid**<br>These bits informs the user about the current state of the receive equalization network.<br>$00_B$ Equalizer status not valid, still adapting<br>$01_B$ Equalizer status valid<br>$10_B$ Equalizer status not valid<br>$11_B$ Equalizer status valid but high noise floor |
| RES | 5:0 | r | **Receive Equalizer Status**<br>The current line attenuation status in steps of about 1.7 dB for E1 and 1.4 dB for T1/J1 mode are displayed in these bits. Only valid if bits EV(1:0) = ´$01_b$´. Accuracy: ± 2 digits, based on temperature influence and noise amplitude variations.<br>$00000_B$ Minimum attenuation: 0 dB<br>…B<br>$11001_B$ Maximum attenuation: -43 dB (E1), -36 dB (T1/J1) |

## Line Status Register 0

| LSR0 | Offset | Reset Value |
|---|---|---|
| Line Status Register 0 | xx4C$_H$ | 00$_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| LOS | 7 | r | **Loss-of-Signal**<br>• Detection: This bit is set when the incoming signal has “no transitions” (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by register PCD. Total account of consecutive pulses: 16 ≤ T ≤ 4096. Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL(2:0).<br>• Recovery: Analog interface: The bit is reset in short-haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval. In long-haul mode additionally bit RES.6 must be set for at least 250 µs. Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval. With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. The bit is also set during alarm simulation and reset, if MR0.SIM is cleared and no alarm condition exists. |
| AIS | 6 | r | **Alarm Indication Signal**<br>The function of this bit is determined by MR0.ALM.<br>• MR0.ALM = ´0´: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 ms and the QuadLIU™ is in asynchronous state (LSR0.LFA = ´1´). The bit is reset when no alarm condition is detected (according to ETSI standard).<br>• MR0.ALM = ´1´: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame period (512 bits). This bit is cleared when each of two consecutive doubleframe periods contain three or more zeros or when the frame alignment signal FAS has been found. (ITU-T G.775)<br>The bit is also set during alarm simulation and reset if MR0.SIM is cleared and no alarm condition exists.With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set. |

## Line Status Register 1

| LSR1 | Offset | Reset Value |
|---|---|---|
| Line Status Register 1 | $xx4D_H$ | $xx_H$ |

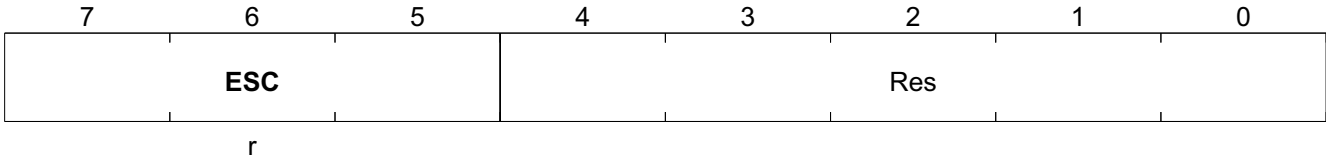
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **EXZD** | **PDEN** | Res | **LLBDD** | **LLBAD** | Res | **XLS** | **XLO** |
| r | r | | r | r | | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| EXZD | 7 | r | **Excessive Zeros Detected**<br>Significant only, if excessive zero detection has been enabled (MR0.EXZE = ´1´). Set after detection of more than 3 (HDB3 code) or 15 (AMI code) contiguous zeros in the received data stream.This bit is cleared on read. |
| PDEN | 6 | r | **Pulse-Density Violation Detected**<br>The pulse-density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 14 consecutive zeros are detected. With the violation of the pulse-density this bit is set and remains active until the pulse-density requirement is fulfilled for 23 consecutive "1"-pulses. Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN. |
| LLBDD | 4 | r | **Line Loop-Back Deactivation Signal Detected, only valid in T1 mode**<br>In E1 mode the equivalent bit is LSR2.LLBDD.<br>This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than $10^{-2}$. The bit remains set as long as the bit error rate does not exceed $10^{-2}$. If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.Any change of this bit causes an LLBSC interrupt. |
| LLBAD | 3 | r | **Line Loop-Back Activation Signal Detected, only valid in T1 mode**<br>In E1 mode the equivalent bit is LSR2.LLBAD.<br>Depending on bit LCR1.EPRM the source of this status bit changed.<br>• LCR1.EPRM = ´0´: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than $10^{-2}$. The bit remains set as long as the bit error rate does not exceed $10^{-2}$. If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation. Any change of this bit causes an LLBSC interrupt.<br>• LCR1.EPRM = ´1´: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of up to $10^{-3}$. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo-random binary sequence. |

| Field | Bits | Type | Description |
|---|---|---|---|
| XLS | 1 | r | **Transmit Line Short**<br>See **Chapter 3.9.7**. Significant only if the ternary line interface is selected by LIM1.DRS = ´0´.<br>$0_B$ Normal operation. No short is detected.<br>$1_B$ The XL1 and XL2 are shortened for at least 3 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high-impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high-impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen. |
| XLO | 0 | r | **Transmit Line Open**<br>See also **Chapter 3.9.7**.<br>$0_B$ Normal operation<br>$1_B$ This bit is set if at least 32 consecutive zeros were sent on pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen. |

## Line Status Register 3

| LSR3 | Offset | Reset Value |
|---|---|---|
| Line Status Register 3 | $xx4E_H$ | $xx_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| ESC | 7:5 | r | **Error Simulation Counter, T1 only**<br>This three-bit counter is incremented by setting bit MR0.SIM. The state of the counter determines the function to be tested. For complete checking of the alarm indications, eight simulation steps are necessary (LSR3.ESC = ´$000_b$´ after a complete simulation). |

**Table 53 Alarm Simulation States**

| Tested Alarms ESC(2:0) = | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| LFA | | | x | | | | x | |
| LMFA | | | x | | | | x | |
| RRA (bit2 = 0) | | x | | | | | | |
| RRA (S-bit frame 12) | | | x | | | | | |
| RRA (DL-pattern) | | | | | | | x | |
| LOS[1)] | | x | x | | | x | | |
| EBC[2)] (F12,F72) | | | x | | | | (x) | |
| EBC[2)] (only ESF) | | x | x | | | x | (x) | |
| AIS[1)] | | x | x | | | x | x | |
| FEC[2)] | | | x | | | | (x) | |
| CVC | | x | x | | | x | | |
| CEC (only ESF) | | x | x | | | x | x | |
| RSP | | x | | | | | | |
| RSN | | | | | | x | | |
| XSP | | x | | | | | | |
| XSN | | | | | | x | | |
| BEC[1)] | | x | x | | | x | | |
| COEC | | | x | | | | x | |

1) Only active during FMR0.SIM = 1

2) FEC is counting +2 while EBC is counting +1 if the framer is in synchronous state; if asynchronous in state 2 but synchronous in state 6, counters are incremented during state 6

Some of these alarm indications are simulated only if the QuadLIU™ is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset automatically and clearing of the error counters and interrupt status registers ISR(7:0) should be done. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations might occur at later steps. Control bit FMR0.SIM has to be held stable at high or low level for at least one receive clock period before changing it again.

## Line Status Register 2

| LSR2 | Offset | Reset Value |
|---|---|---|
| Line Status Register 2 | $xx4F_H$ | $xx_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | LLBDD | LLBAD | Res | | |
| | | | r | r | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| LLBDD | 4 | r | **Line Loop-Back Deactivation Signal Detected**<br>Only valid in E1 mode<br>In T1/J1 mode the equivalent bit is LSR1.LLBDD.<br>This bit is set in case of the LLB deactivate signal is detected and then received over a period of more than 25 ms with a bit error rate less than $10^{-2}$. The bit remains set as long as the bit error rate does not exceed $10^{-2}$.<br>If framing is aligned, the time slot 0 is not taken into account for the error rate calculation.Any change of this bit causes an LLBSC interrupt. |
| LLBAD | 3 | r | **Line Loop-Back Activation Signal Detected**<br>Only valid in E1 mode<br>In T1/J1 mode the equivalent bit is LSR1.LLBAD.<br>Depending on bit LCR1.EPRM the source of this status bit changed.<br>• LCR1.EPRM = ´0´: This bit is set in case of the LLB activate signal is detected and then received over a period of more than 25 ms with a bit error rate less than $10^{-2}$. The bit remains set as long as the bit error rate does not exceed $10^{-2}$. If framing is aligned, the time slot 0 is not taken into account for the error rate calculation. Any change of this bit causes an LLBSC interrupt.<br>• LCR1.EPRM = ´1´: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a bit error rate of $10^{-1}$. A data stream containing all zeros or all ones with/without framing bits is also a valid pseudo-random binary sequence. |

## Code Violation Counter Lower Byte

| CVCL | Offset | Reset Value |
|---|---|---|
| Code Violation Counter Lower Byte | $xx52_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CV7 | CV6 | CV5 | CV4 | CV3 | CV2 | CV1 | CV0 |
| r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| CV7 | 7 | r | **Code Violations**<br>If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit MR0.EXTD. If simple AMI coding is enabled (MR0.RC(1:0) = ´$01_b$´) all bipolar violations are counted. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit MR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. |
| CV6 | 6 | r | |
| CV5 | 5 | r | |
| CV4 | 4 | r | |
| CV3 | 3 | r | |
| CV2 | 2 | r | |
| CV1 | 1 | r | |
| CV0 | 0 | r | |

## Code Violation Counter Higher Byte

| CVCH | Offset | Reset Value |
|---|---|---|
| Code Violation Counter Higher Byte | $xx53_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **CV15** | **CV14** | **CV13** | **CV12** | **CV11** | **CV10** | **CV9** | **CV8** |
| r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| CV15 | 7 | r | **Code Violations**<br>If the HDB3 or the CMI code with HDB3-precoding is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit MR0.EXTD. If simple AMI coding is enabled (MR0.RC(1:0) = ´$01_b$´) all bipolar violations are counted. The error counter does not roll over.During alarm simulation, the counter is incremented every four bits received up to its saturation. Clearing and updating the counter is done according to bit MR1.ECM. If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. |
| CV14 | 6 | r | |
| CV13 | 5 | r | |
| CV12 | 4 | r | |
| CV11 | 3 | r | |
| CV10 | 2 | r | |
| CV9 | 1 | r | |
| CV8 | 0 | r | |

## PRBS Bit Error Counter Lower Bytes

| BECL | Offset | Reset Value |
|---|---|---|
| PRBS Bit Error Counter Lower Bytes | $xx58_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BEC7 | BEC6 | BEC5 | BEC4 | BEC3 | BEC2 | BEC1 | BEC0 |
| r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| BEC7 | 7 | r | **PRBS Bit Error Counter**<br>If the PRBS monitor is enabled by LCR1.EPRM = ´1´ this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state LSR1.LLBAD = ´1´.<br>The error counter does not roll over.During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit MR1.ECM.If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset.<br>Bit DEC.DBEC is automatically reset with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. |
| BEC6 | 6 | r | |
| BEC5 | 5 | r | |
| BEC4 | 4 | r | |
| BEC3 | 3 | r | |
| BEC2 | 2 | r | |
| BEC1 | 1 | r | |
| BEC0 | 0 | r | |

## PRBS Bit Error Counter Higher Bytes

| BECH | Offset | Reset Value |
|---|---|---|
| PRBS Bit Error Counter Higher Bytes | $xx59_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **BEC15** | **BEC14** | **BEC13** | **BEC12** | **BEC11** | **BEC10** | **BEC9** | **BEC8** |
| r | r | r | r | r | r | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| BEC15 | 7 | r | **PRBS Bit Error Counter**<br>If the PRBS monitor is enabled by LCR1.EPRM = ´1´ this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state LSR1.LLBAD = ´1´.<br>The error counter does not roll over.During alarm simulation, the counter is incremented continuously with every second received bit. Clearing and updating the counter is done according to bit MR1.ECM.If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset.<br>Bit DEC.DBEC is automatically reset with reading the error counter high byte. If MR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second. |
| BEC14 | 6 | r | |
| BEC13 | 5 | r | |
| BEC12 | 4 | r | |
| BEC11 | 3 | r | |
| BEC10 | 2 | r | |
| BEC9 | 1 | r | |
| BEC8 | 0 | r | |

### Interrupt Status Register 1

All bits are reset when ISR1 is read. If bit GCR.VIS is set, interrupt statuses in ISR1 are flagged although they are masked by register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

| ISR1 | Offset | Reset Value |
|---|---|---|
| **Interrupt Status Register 1** | **xx69$_H$** | **00$_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **LLBSC** | Res | | | | | **XLSC** | Res |
| rsc | | | | | | rsc | |

| Field | Bits | Type | Description |
|---|---|---|---|
| LLBSC | 7 | rsc | **Line Loop-Back Status Change, E1 only**<br>In T1/J1 mode this bit is not valid and ISR3.LLBSC is used instead. Depending on bit LCR1.EPRM the source of this interrupt status changed:<br>• LCR1.EPRM = 0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively, is detected over a period of 25 ms with a bit error rate less than $10^{-2}$. The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds $10^{-2}$. The actual detection status can be read from the LSR2.LLBAD / LSR2.LLBDD in E1 or LSR1.LLBAD / LSR1.LLBDD in T1/J1 mode, respectively.<br>• PRBS Status Change LCR1.EPRM = ´1´: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in LSR2.LLBAD (E1) or LSR1.LLBAD (T1/J1). |
| XLSC | 1 | rsc | **Transmit Line Status Change**<br>XLSC is set with the rising edge of the bit LSR1.XLO or with any change of bit LSR1.XLS.<br>The actual status of the transmit line monitor can be read from the LSR1.XLS and LSR1.XLO. |

### Interrupt Status Register 2

All bits are reset when ISR2 is read. If bit GCR.VIS is set, interrupt statuses in ISR2 are flagged although they are masked by register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS. See **Chapter 3.5.3**

| ISR2 | Offset | Reset Value |
|---|---|---|
| **Interrupt Status Register 2** | **xx6A$_H$** | **00$_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | | **AIS** | **LOS** | Res | |
| | | | | r | r | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| AIS | 3 | r | **Alarm Indication Signal (Blue Alarm)**<br>This bit is set when an alarm indication signal is detected and bit LSR0.AIS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of LSR0.AIS.It is set during alarm simulation. |
| LOS | 2 | r | **Loss-of-Signal (Red Alarm)**<br>This bit is set when a loss-of-signal alarm is detected in the received data stream and LSR0.LOS is set. If GCR.SCI is set high this interrupt status bit is activated with every change of state of LSR0.LOS. It is set during alarm simulation. |

### Interrupt Status Register 3

All bits are reset when ISR3 is read. If bit GCR.VIS is set, interrupt statuses in ISR3 are flagged although they are masked by register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

| ISR3 | Offset | Reset Value |
|---|---|---|
| Interrupt Status Register 3 | $xx6B_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | **SEC** | Res | | **LLBSC** | Res | **RSN** | **RSP** |
| | rsc | | | rsc | | rsc | rcs |

| Field | Bits | Type | Description |
|---|---|---|---|
| SEC | 6 | rsc | **Second Timer**<br>The internal one-second timer has expired. The timer is derived from clock RCLK or external pin SEC/FSC. |
| LLBSC | 3 | rsc | **Line Loop-Back Status Change, T1/J1 only**<br>In E1 mode this bit is not valid and ISR1.LLBSC is used instead. Depending on bit LCR1.EPRM the source of this interrupt status changed:<br>• LCR1.EPRM = 0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively, is detected over a period of 25 ms with a bit error rate less than $10^{-2}$. The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds $10^{-2}$. The actual detection status can be read from the LSR2.LLBAD / LSR2.LLBDD in E1 or LSR1.LLBAD / LSR1.LLBDD in T1/J1 mode, respectively.<br>• PRBS Status Change LCR1.EPRM = ´1´: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in LSR2.LLBAD (E1) or LSR1.LLBAD (T1/J1). |
| RSN | 1 | rsc | **Receive Slip Negative**<br>The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is skipped. It is set during alarm simulation. See **Chapter 3.7.9**. |
| RSP | 0 | rcs | **Receive Slip Positive**<br>The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 2.048 MHz. A frame is repeated. It is set during alarm simulation. See **Chapter 3.7.9**. |

### Interrupt Status Register 4

All bits are reset when ISR4 is read. If bit GCR.VIS is set, interrupt statuses in ISR4 are flagged although they are masked by register IMR4. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

| ISR4 | Offset | Reset Value |
|---|---|---|
| **Interrupt Status Register 4** | **xx6C$_H$** | **00$_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **XSP** | **XSN** | Res | | | | | |
| rsc | rsc | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| XSP | 7 | rsc | **Transmit Slip Positive**<br>The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is repeated. After a slip has performed writing of register XC1 is not necessary. |
| XSN | 6 | rsc | **Transmit Slip Negative**<br>The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 2.048 MHz. A frame is skipped. After a slip has performed writing of register XC1 is not necessary. |

### Global Interrupt Status Register

This status register points to pending interrupts sourced by ISR(1:4) and ISR(6:7), see **Chapter 3.5.3**.

| GIS | Offset | Reset Value |
|---|---|---|
| **Global Interrupt Status Register** | **xx6E$_H$** | **00$_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **ISR7** | **ISR6** | **ISR5** | **ISR4** | **ISR3** | **ISR2** | **ISR1** | **ISR0** |
| rsc | rsc | rsc | rsc | rsc | rsc | rsc | rsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| ISR7 | 7 | rsc | **Interrupt Status Register 7 Pointer**<br>$0_B$ no interrupt is pending in ISR6.<br>$1_B$ at least one interrupt is pending in ISR6. |
| ISR6 | 6 | rsc | **Interrupt Status Register 6 Pointer**<br>$0_B$ no interrupt is pending in ISR6.<br>$1_B$ at least one interrupt is pending in ISR6. |
| ISR5 | 5 | rsc | **Interrupt Status Register 5 Pointer**<br>Always ´0´, because no ISR5 exists |
| ISR4 | 4 | rsc | **Interrupt Status Register 4 Pointer**<br>$0_B$ no interrupt is pending in ISR4.<br>$1_B$ at least one interrupt is pending in ISR4. |
| ISR3 | 3 | rsc | **Interrupt Status Register 3 Pointer**<br>$0_B$ no interrupt is pending in ISR3.<br>$1_B$ at least one interrupt is pending in ISR3. |
| ISR2 | 2 | rsc | **Interrupt Status Register 2Pointer**<br>$0_B$ no interrupt is pending in ISR2.<br>$1_B$ at least one interrupt is pending in ISR2. |
| ISR1 | 1 | rsc | **Interrupt Status Register 1 Pointer**<br>$0_B$ no interrupt is pending in ISR1.<br>$1_B$ at least one interrupt is pending in ISR1. |
| ISR0 | 0 | rsc | **Interrupt Status Register 0 Pointer**<br>Always ´0´, because no ISR0 exists. |

### Channel Interrupt Status Register

This status register points to pending interrupts of channels 1to 4, see **Chapter 3.5.3**.

| CIS | Offset | Reset Value |
|---|---|---|
| **Channel Interrupt Status Register** | **$006F_H$** | **$00_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **PLLL** | Res | | | **GIS4** | **GIS3** | **GIS2** | **GIS1** |
| rsc | | | | rsc | rsc | rsc | rsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| PLLL | 7 | rsc | **PLL Lock Status**<br>This bit shows the lock status of the internal PLL.<br>*Note: PLLL has the same value as PLLLS in register GIS2 (which is used for GPC6.COMP_DIS = $1_B$).*<br>$0_B$ PLL is unlocked.<br>$1_B$ PLL is locked. |
| GIS4 | 3 | rsc | **Global Interrupt Status of Channel 4**<br>$0_B$ no interrupt is pending on channel 4.<br>$1_B$ at least one interrupt is pending on channel 4, read GIS of channel 4 for more information. |
| GIS3 | 2 | rsc | **Global Interrupt Status of Channel 3**<br>$0_B$ no interrupt is pending on channel 3.<br>$1_B$ at least one interrupt is pending on channel 3, read GIS of channel 3 for more information. |
| GIS2 | 1 | rsc | **Global Interrupt Status of Channel 2**<br>$0_B$ no interrupt is pending on channel 2.<br>$1_B$ at least one interrupt is pending on channel 2, read GIS of channel 2 for more information. |
| GIS1 | 0 | rsc | **Global Interrupt Status of Channel 1**<br>$0_B$ no interrupt is pending on channel 1.<br>$1_B$ at least one interrupt is pending on channel 1, read GIS of channel 1 for more information. |

### Multi Function Port Input Register

This register always reflects the state of the multi function ports, see **Chapter 3.12**. If used as an input, the according port should be switched to general purpose input mode. If not, the programmed output signal can be monitored through this register (see registers PC1 to PC3).

| MFPI | Offset | Reset Value |
|---|---|---|
| **Multi Function Port Input Register** | **xxAB$_H$** | **xx$_H$** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | **RPC** | **RPB** | **RPA** | Res | | **XPB** | **XPA** |
| | r | r | r | | | r | r |

| Field | Bits | Type | Description |
|---|---|---|---|
| RPC | 6 | r | **RPC Input Level**<br>$0_B$ Low level on pin RPC.<br>$1_B$ High level on pin RPC. |
| RPB | 5 | r | **RPB Input Level**<br>$0_B$ Low level on pin RPB.<br>$1_B$ High level on pin RPB. |
| RPA | 4 | r | **RPA Input Level**<br>$0_B$ Low level on pin RPA.<br>$1_B$ High level on pin RPA. |
| XPB | 1 | r | **XPB Input Level**<br>$0_B$ Low level on pin XPB.<br>$1_B$ High level on pin XPB. |
| XPA | 0 | r | **XPA Input Level**<br>$0_B$ Low level on pin XPA.<br>$1_B$ High level on pin XPA. |

## Interrupt Status Register 6

| ISR6 | Offset | Reset Value |
|---|---|---|
| Interrupt Status Register 6 | $xxAC_H$ | $00_H$ |

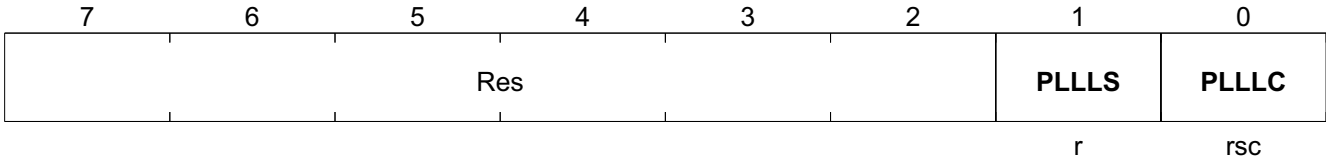
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | | SILSU | SILSD | LILSU | LILSD |
| | | | | rsc | rsc | rsc | rsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| SILSU | 3 | rsc | **Framer (System) In-Band Loop Switching Up detected**<br>See **Chapter 3.11.2**.<br>System loop up code detected and payload loop is switched on if ALS.SILS is set. |
| SILSD | 2 | rsc | **Framer (System) In-Band Loop Switching Down detected**<br>See **Chapter 3.11.2**.<br>System loop down code detected and payload loop is switched off if ALS.SILS is set. |
| LILSU | 1 | rsc | **Line In-Band Loop Switching Up Interrupt**<br>See **Chapter 3.11.2**.<br>$0_B$ no line loop up code detected.<br>$1_B$ line loop up code detected and line loop is switched on if ALS.LILS is set. |
| LILSD | 0 | rsc | **Line In-Band Loop Switching Down Interrupt**<br>See **Chapter 3.11.2**.<br>$0_B$ no line loop down code detected.<br>$1_B$ line loop down code detected and line loop is switched off if ALS.LILS is set. |

### Global Interrupt Status 2

Interrupt status register for the PLL of the master clocking unit.

| GIS2 | Offset | Reset Value |
|---|---|---|
| Global Interrupt Status 2 | $00AD_H$ | $00_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| PLLLS | 1 | r | **PLL Locked Status Information**<br>*Note: PLLLS is only a status bit, not an interrupt status bit, so type is r and not rsc. This bit is valid independent on value of COMP. For COMP = ´0´ this bit must be used instead of bit 7 of register CIS which has then the function GIS8.*<br>$0_B$ PLL is unlocked.<br>$1_B$ PLL is locked |
| PLLLC | 0 | rsc | **PLL Locked Status Change**<br>$0_B$ no change of PLL lock status since last read of this register.<br>$1_B$ PLL lock status has changed since last read. Status information is available in bit PLLLS. |

### Interrupt Status Register 7

All bits are reset when ISR7 is read. If bit GCR.VIS is set, interrupt statuses in ISR7 are flagged although they are masked by register IMR7. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS, see **Chapter 3.5.3**.

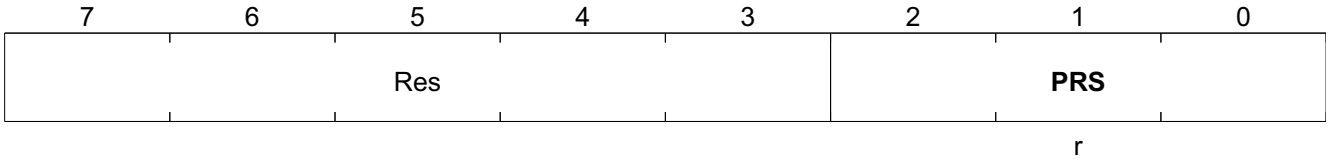
| ISR7 | Offset | Reset Value |
|---|---|---|
| Interrupt Status Register 7 | $xxD8_H$ | $00_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | XCLKSS1 | XCLKSS0 | Res | | |
| | | | rsc | rsc | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| XCLKSS1 | 4 | rsc | **XCLK Source Switched 1**<br>See **Chapter 3.9.3**. Shows if an automatically switching of the DCO-X reference between TCLK and FCLKX was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in **CLKSTAT**.TCLKLOS.<br>$0_B$ DCO-X reference not switched.<br>$1_B$ DCO-X reference has switched between TCLK and FCLKX. The XCLK is always sourced by the DCO-X output. |
| XCLKSS0 | 3 | rsc | **XCLK Source Switched 0**<br>See **Chapter 3.9.3**. Shows if an automatically switching of the XCLK source between TCLK and DCO-X output was performed. If automatically switching is not enabled (CMR6.ATCS = ´0´), this bit is always ´0´. Note that the status of TCLK is shown independent on CMR6.ATC in **CLKSTAT**.TCLKLOS.<br>$0_B$ XCLK source not switched.<br>$1_B$ XCLK source has switched automatically from TCLK to DCO-X output in case of TCLK loss or automatically switched back from DCO-X output to TCLK in case that TCLK is active again. The DCO-X is always sourced by FCLKX. |

## PRBS Status Register

| PRBSSTA | Offset | Reset Value |
|---|---|---|
| PRBS Status Register | $xxDA_H$ | $0x_H$ |

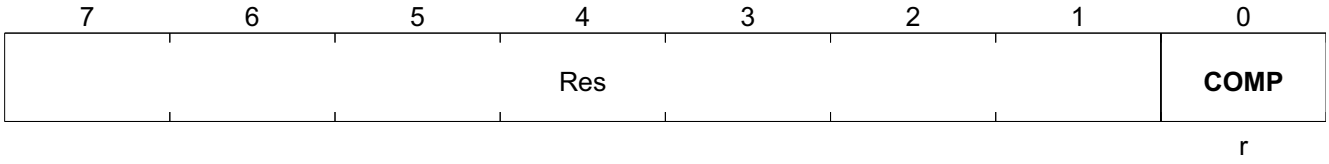



| Field | Bits | Type | Description |
|---|---|---|---|
| PRS | 2:0 | r | **PRBS Status Information**<br>*Note: Every change of the bits PRS sets the interrupt bit ISR1.LLBSC if register bit LCR1.EPRM is set. No pattern is also detected if signal "alarm simulation" is active. Detection of all_zero or all_ones is done over 12, 16, 21 or 24 consecutive bits, dependent on the choosed PRBS polynomial (11, 15, 20 or 23). Because every bit error in the PRBS increments the bit error counter BEC, no special status information like "PRBS detected with errors" is given here*<br>$000_B$ no pattern detected.<br>$001_B$ reserved.<br>$010_B$ PRBS pattern detected.<br>$011_B$ inverted PRBS pattern detected.<br>$100_B$ reserved.<br>$101_B$ reserved.<br>$110_B$ all-zero pattern detected.<br>$111_B$ all-ones pattern detected. |

## Device Status Register

.

| DSTR | Offset | Reset Value |
|---|---|---|
| Device Status Register | $00E7_H$ | $0x_H$ |




| Field | Bits | Type | Description |
|---|---|---|---|
| COMP | 0 | r | **COMPatibility Status**<br>$0_B$ GPC6.COMP_DIS = ´1´, generic mode is selected.<br>$1_B$ GPC6.COMP_DIS = ´0´, QuadFALC® v2.1 compatibility mode is selected. |

### Clock Status Register

The bits show the current status of the input clocks TCLK and FCLKX.

| CLKSTAT | Offset | Reset Value |
|---|---|---|
| Clock Status Register | $xxFE_H$ | $xx_H$ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Res | | | TCLKLOS | FCLKXLOS | Res | | |
| | | | r | r | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| TCLKLOS | 4 | r | **Loss of TCLK**<br>Status of TCLK.<br>*Note: See **Chapter 3.9.3** for more detail.*<br>$0_B$ TCLK is active.<br>$1_B$ TCLK is lossed. |
| FCLKXLOS | 3 | r | **Loss of FCLKX**<br>Status of FCLKX.<br>*Note: See **Chapter 3.9.3** for more detail.*<br>$0_B$ FCLKX is active.<br>$1_B$ FCLKX is lossed. |

# 5 Package Outlines

**Figure 46** shows the Ball Grid Array Packages.

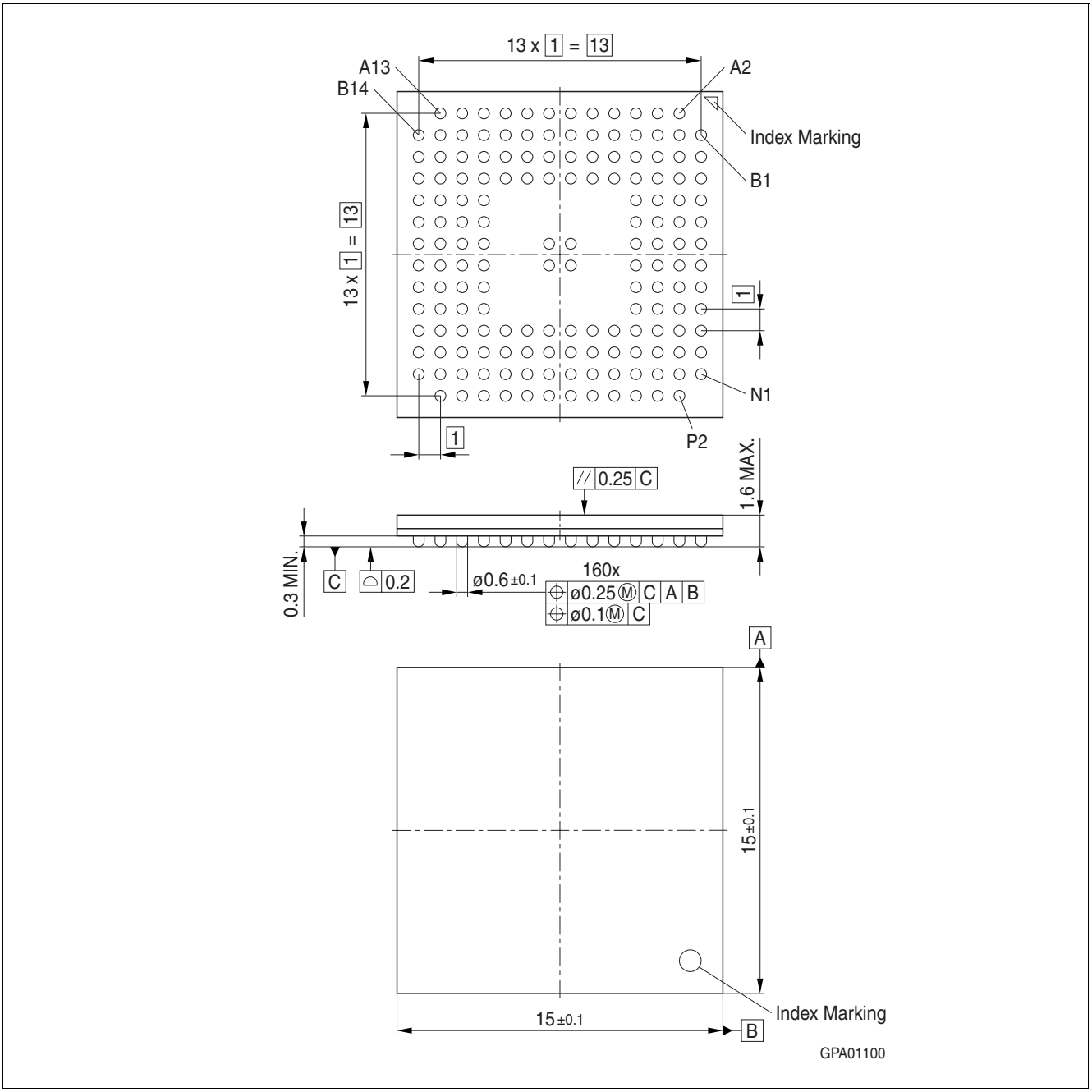



**Figure 46 P/PG-LBGA-160-1** (Plastic Green Low Profile Ball Grid Array Package)

Dimensions in mm.

Figure 47 shows the Flat Thin Pack package.

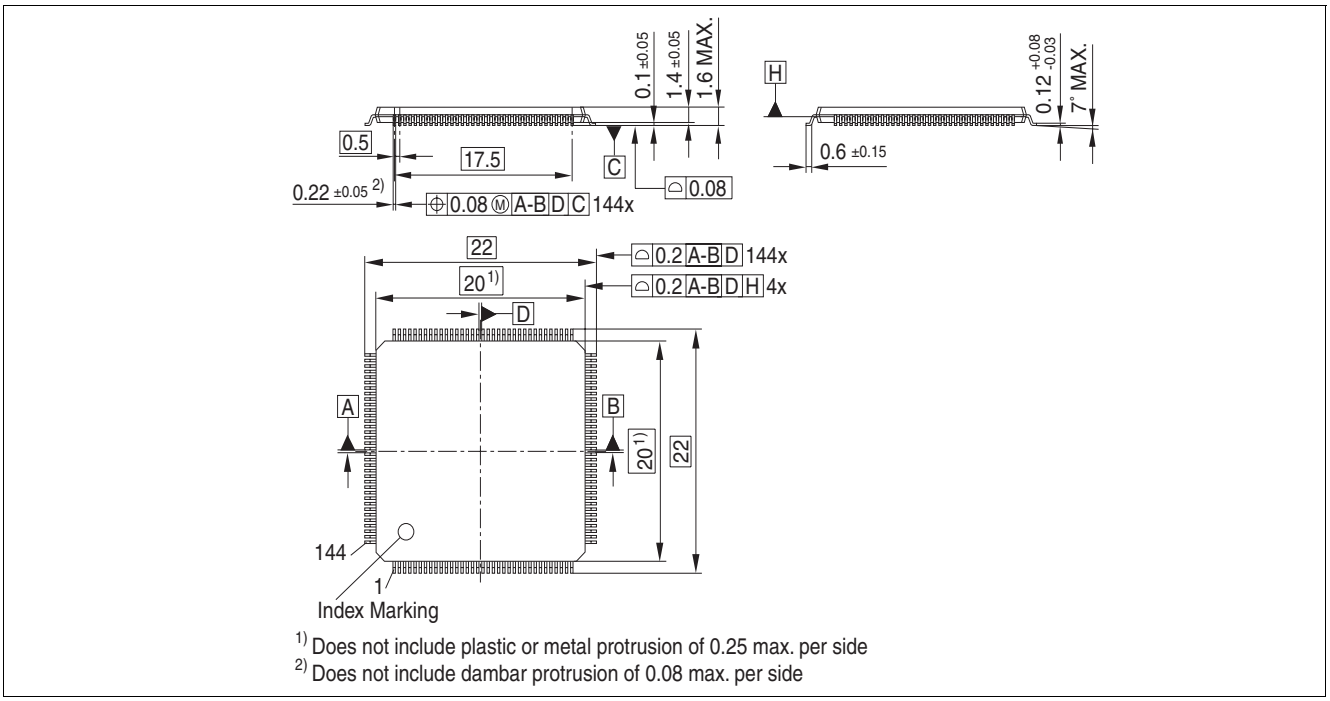



**Figure 47 PG-TQFP-144-17** (Plastic Thin Quad Flat Package)

Dimensions in mm

# 6 Electrical Characteristics

In Table 54 the absolute maximum ratings of the QuadLIU™ are listed.

**Table 54 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Ambient temperature under bias | $T_A$ | -40 | – | 85 | °C | – |
| Storage temperature | $T_{stg}$ | -65 | – | 125 | °C | – |
| Moisture Level 3 temperature | $T_{ML3}$ | – | – | 225 | °C | According to IPS J-STD 020 |
| | | | | 245 | °C | According to Infineon internal standard |
| IC supply voltage (pads, digital) | $V_{DD}$ | -0.5 | 3.3 | 4.5 | V | – |
| IC supply voltage (core, digital) | $V_{DDC}$ | -0.5 | 1.8 | 2.4 | V | – |
| IC supply voltage receive (analog) | $V_{DDR}$ | -0.4 | – | 4.5 | V | – |
| IC supply voltage transmit (analog) | $V_{DDX}$ | -0.4 | – | 4.5 | V | – |
| Receiver input signal with respect to ground | $V_{RLmax}$ | -0.8 | – | 4.5 | V | RL1, RL2 |
| Voltage on any pin with respect to ground | $V_{max}$ | -0.4 | – | 4.5 | V | Except RL1, RL2 |
| ESD robustness[1] HBM: 1.5 kΩ, 100 pF | $V_{ESD,HBM}$ | – | – | 2000 | V | – |
| ESD robustness[2] CDM | $V_{ESD,CDM}$ | – | – | 500 | | – |

1) According to JEDEC standard JESD22-A114.

2) According to ESD Association Standard DS5.3.1 - 1999

***Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.***
***Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.***

***Attention: To avoid demage of the QuadLIU™ during power up, use the following sequence for biasing:***

- Core voltage
- Pad voltage not before core voltage
- Signal voltage not before Pad voltage

If this sequence does not meet your requirements make sure that

- The inverse current per signal pad is lower than 10 mA
- The current per supply domain is lower than 100 mA

Table 55 defines the maximum values of voltages and temperature which may be applied to guarantee proper operation of the QuadLIU™.

**Table 55 Operating Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Ambient temperature | $T_A$ | -40 | – | 85 | °C | – |
| Supply voltage digital pads | $V_{DD}$ | 3.13 | 3.30 | 3.46 | V | 3.3 V ± 5 % 1) |
| Supply voltage digital core | $V_{DDC}$ | 1.62 | 1.80 | 1.98 | V | 1.8 V ±10 % 2) |
| Supply voltage analog receiver | $V_{DDR}$ | 3.13 | 3.30 | 3.46 | V | 3.3 V ±5 % 3) |
| Supply voltage analog transmitter | $V_{DDX}$ | 3.13 | 3.30 | 3.46 | V | 3.3 V ±5 % 4) |
| Analog input voltages | $V_{RL}$ | 0 | – | $V_{DDR}$ +0.3 | V | RL1, RL2 |
| Digital input voltages | $V_{ID}$ | -0.4 | – | 3.46 | V | $V_{DD}$ = 3.3 V ±5 % |
| Ground | $V_{SS}$ $V_{SSR}$ $V_{SSX}$ | 0 | – | 0 | V | – |

1) Voltage ripple on analog supply less than 50 mV
2) Voltage ripple on analog supply less than 50 mV
3) Voltage ripple on analog supply less than 50 mV
4) Voltage ripple on analog supply less than 50 mV

*Note: In the operating range, the functions given in the circuit description are fulfilled.*
*$V_{DD}$, $V_{DDR}$ and $V_{DDX}$ have to be connected to the same voltage level,*
*$V_{SS}$, $V_{SSR}$ and $V_{SSX}$ have to be connected to ground level.*

**Table 56 DC Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input low voltage | $V_{IL}$ | -0.4 | – | 0.8 | V | 1) |
| Input high voltage | $V_{IH}$ | 2.0 | – | 3.46 | V | 1) |
| Output low voltage | $V_{OL}$ | $V_{SS}$ | – | 0.45 | V | $I_{OL}$ = +2 mA 2) |
| Output high voltage | $V_{OH}$ | 2.4 | – | $V_{DD}$ | V | $I_{OH}$ = -2 mA 2) |

**Table 56 DC Characteristics** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Medium power supply current at 3.3 V supply (analog line interface mode) | $I_{DD33E1}$ | – | – | 230 | mA | E1 application [3] LIM1.DRS = ´0´, All-one´s pattern; 16 MHz at system interface; VSEL = 0 |
| | $I_{DD33E1}$ | – | – | 200 | | E1 application [4] LIM1.DRS = ´0´, PRBS pattern; 2 MHz at system interface; VSEL = 0 |
| | $I_{DD33T1}$ | – | – | 215 | | T1 application[5] LIM1.DRS = ´0´, all-one´s pattern; 12 MHz at system interface; VSEL = 0 |
| | $I_{DD33T1}$ | – | – | 190 | | T1 application [6] LIM1.DRS = ´0´, PRBS pattern; 1.5 MHz at system interface; VSEL = 0 |
| Medium power supply current at 1.8 V supply (digital line interface mode) | $I_{DD18E1}$ | – | – | 220 | mA | E1 application [7] LIM1.DRS = ´1´, all-one´s pattern; 16 MHz at system interface; VSEL = 0 |
| Medium power supply current at 3.3 V supply (digital line interface mode) | $I_{DD33T1}$ | – | – | 20 | mA | |
| Input leakage current | $I_{IL11}$ | – | – | 1 | µA | $V_{IN} = V_{DD}$ [8]; all except RDO |
| Input leakage current | $I_{IL12}$ | – | – | 1 | µA | $V_{IN} = V_{SS}$ [6]; all except RDO |
| Input pullup current | $I_{IP}$ | 2 | – | 15 | µA | $V_{IN} = V_{SS}$ |
| Output leakage current | $I_{OZ1}$ | – | – | 1 | µA | $V_{OUT}$ = tristate[1] $V_{SS} < V_{meas} < V_{DD}$ measured against $V_{DD}$ and $V_{SS}$; all except XL1/2 |
| Transmitter leakage current | $I_{TL}$ | – | – | 30 | µA | XL1/2 = $V_{DDX}$; XPM2.XLT = ´1´ |
| | | – | – | 30 | | XL1/2 = $V_{SSX}$; XPM2.XLT = ´1´ |
| Transmitter output impedance | $R_X$ | – | – | 3 | Ω | Applies to XL1and XL2[9] |
| Transmitter output current | $I_X$ | – | – | 105 | mA | XL1, XL2 |
| Differential peak voltage of a mark (between XL1 and XL2) | $V_X$ | – | – | 2.15 | V | – |
| Receiver peak voltage of a mark (at RL1 or RL2) | $V_{RL12}$ | -0.45 | – | 3.8 | V | RL1, RL2 |
| | | -0.75 | – | 4.1 | | RZ signals; must only be applied during T1 pulse over/undershoot according to ANSI T1.403-1999 |
| Receiver differential peak voltage of a mark (between RL1 and RL2) | $V_{RL12}$ | – | – | 4.0 | V | RL1, RL2 |
| | | | | 4.63 | V | RZ signals; must only be applied during T1 pulse over/undershoot according to ANSI T1.403-1999 |
| Receiver input impedance | $Z_R$ | – | 50 | – | kΩ | [9] |

**Table 56 DC Characteristics** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Receiver internal termination resistor | $R_{TERM}$ | 255 | 300 | 345 | Ω | Internal termination enabled |
| Multi Purpose Analog Switch | $R_{DSON}$ | 2.7 | – | 7.1 | Ω | – |
| | $R_{DSOFF}$ | 100 | – | – | kΩ | – |
| | $R_{DSONDC}$ | – | – | 2 | mA | @ 125 °C |
| | $R_{DSON}$ | – | – | 25 | mA | @ 50% duty cycle |
| Receiver sensitivity | $S_{RSH}$ | 0 | – | 10 | dB | RL1, RL2 LIM0.EQON = ´0´ (short-haul) |
| Receiver sensitivity | $S_{RLH}$ | -43 | – | 0 | dB | RL1, RL2 LIM0.EQON = ´1´ (E1, long-haul) |
| | | -36 | – | 0 | | RL1, RL2 LIM0.EQON = ´1´ (T1/J1, long-haul) |
| Receiver input threshold | $V_{RTH}$ | – | 45 | – | % | LIM2.SLT(1:0) = ´$11_b$´ 9) |
| | | – | 50 | – | | LIM2.SLT(1:0) = ´$10_b$´ 9) default setting |
| | | – | 55 | – | | LIM2.SLT(1:0) = ´$00_b$´ 9) |
| | | – | 67 | – | | LIM2.SLT(1:0) = ´$01_b$´ 9) |
| Loss-Of-signal (LOS) detection limit | $V_{LOS}$ | 1560 | – | 1710 | mV | RIL(2:0) = ´$000_b$´ 9) |
| | | 790 | – | 960 | | RIL(2:0) = ´$001_b$´ 9) |
| | | 430 | – | 500 | | RIL(2:0) = ´$010_b$´10) |
| | | 220 | – | 260 | | RIL(2:0) = ´$011_b$´ 9) |
| | | 125 | – | 130 | | RIL(2:0) = ´$100_b$´ 9) |
| | | 65 | – | 70 | | RIL(2:0) = ´$101_b$´ 9) |
| | | 35 | – | 40 | | RIL(2:0) = ´$110_b$´ 9) |
| | | 10 | – | 15 | | RIL(2:0) = ´$111_b$´ 9) |

1) Applies to all input pins except analog pins RLx
2) Applies to all output pins except pins XLx
3) Wiring conditions and external circuit configuration according to **Figure 67** and **Table 72**.
4) Wiring conditions and external circuit configuration according to **Figure 67** and **Table 72**.
5) Wiring conditions and external circuit configuration according to **Figure 67** and **Table 73**.
6) Wiring conditions and external circuit configuration according to **Figure 67** and **Table 72**.
7) Wiring conditions and external circuit configuration according to **Figure 67** and **Table 72**.
8) Pin leakage is measured in a test mode with all internal pullups disabled. RDO pins are not tristatable, no leakage is measured.
9) Parameter not tested in production
10) Value measured in production to fulfil ITU-T G.775

*Note: Typical characteristics specify mean values expected over the production spread. If not specified otherwise, typical characteristics apply at $T_A$ = 25 °C and 3.3 V supply voltage.*

## 6.1 AC Characteristics

### 6.1.1 Master Clock Timing

**Figure 48** shows the timing and **Table 57** the appropriate timing parameter values of the master clock at the pin MCLK. The accuracy is required to fulfill the jitter requirements, see **Chapter 3.7.8.1** and **Chapter 3.9.4**.

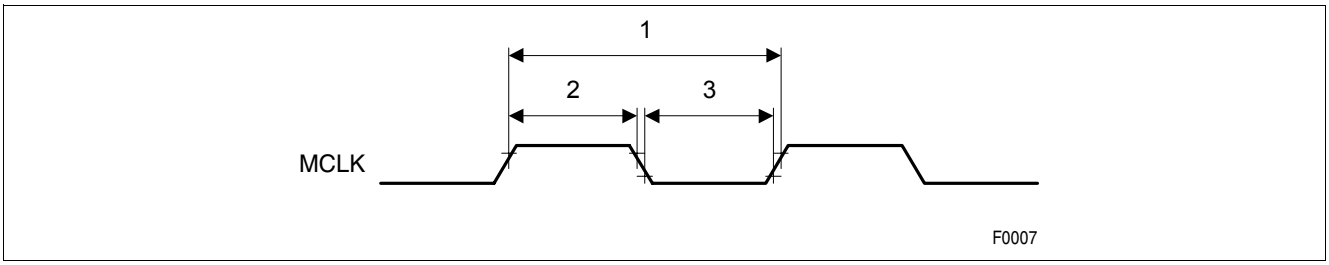



**Figure 48 MCLK Timing**

**Table 57 MCLK Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period of MCLK | 1 | – | 488 | – | ns | E1, fixed mode |
| | | – | 648 | – | | T1/J1, fixed mode |
| | | 50 | – | 980.4 | | E1/T1/J1, flexible mode |
| High phase of MCLK | 2 | 40 | – | – | % | – |
| Low phase of MCLK | 3 | 40 | – | – | % | – |
| Clock accuracy | – | 32[1)] | – | 28[2)] | ppm | – |

1) If clock divider programming fits without rounding

2) If clock divider programming requires rounding

### 6.1.2 JTAG Boundary Scan Interface

**Figure 49** shows the timing and **Table 58** the appropriate timing parameter values at the JTAG pins to perform a boundary scan test of the QuadLIU™, see **Chapter 3.5.4**.

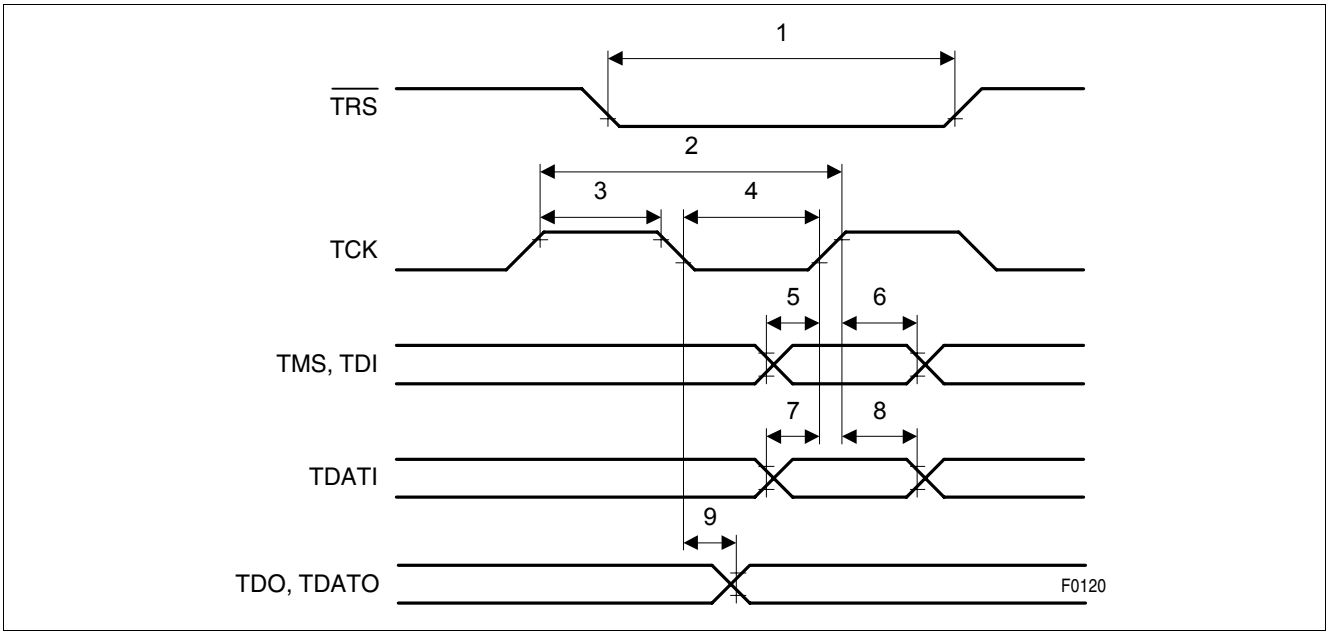



**Figure 49 JTAG Boundary Scan Timing**

**Table 58 JTAG Boundary Scan Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $\overline{TRS}$ reset active low time | 1 | 200 | – | – | ns | – |
| TCK period | 2 | 250 | – | – | ns | – |
| TCK high time | 3 | 80 | – | – | ns | – |
| TCK low time | 4 | 80 | – | – | ns | – |
| TMS, TDI setup time | 5 | 40 | – | – | ns | – |
| TMS, TDI hold time | 6 | 40 | – | – | ns | – |
| TDATI setup time | 7 | 40 | – | – | ns | – |
| TDATI hold time | 8 | 40 | – | – | ns | – |
| TDO, TDATO output delay | 9 | – | – | 100 | ns | – |

### 6.1.3 Reset

**Figure 50** shows the timing and **Table 59** the appropriate timing parameter value at the pin $\overline{RES}$ to perform a reset of the QuadLIU™.

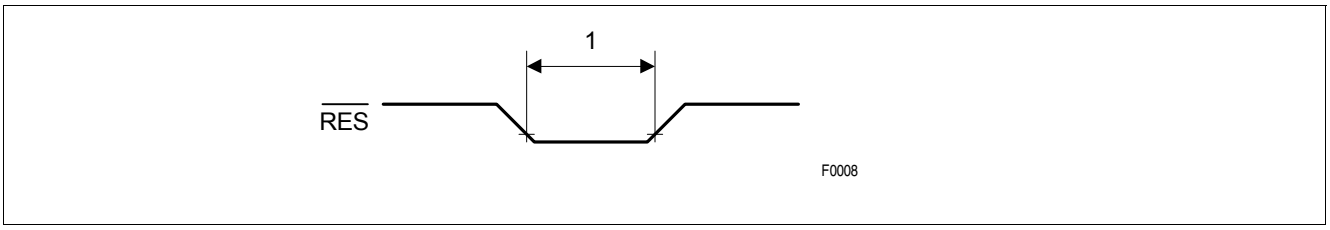



**Figure 50 Reset Timing**

**Table 59 Reset Timing Parameter Value**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $\overline{RES}$ pulse width low | 1 | 10[1)] | – | – | µs | – |

1) While MCLK is running

### 6.1.4 Asynchronous Microprocessor Interface

#### 6.1.4.1 Intel Bus Interface Mode

**Figure 51** to **Figure 54** show the timing of the SCI Interface and **Table 60** the appropriate timing parameter values.

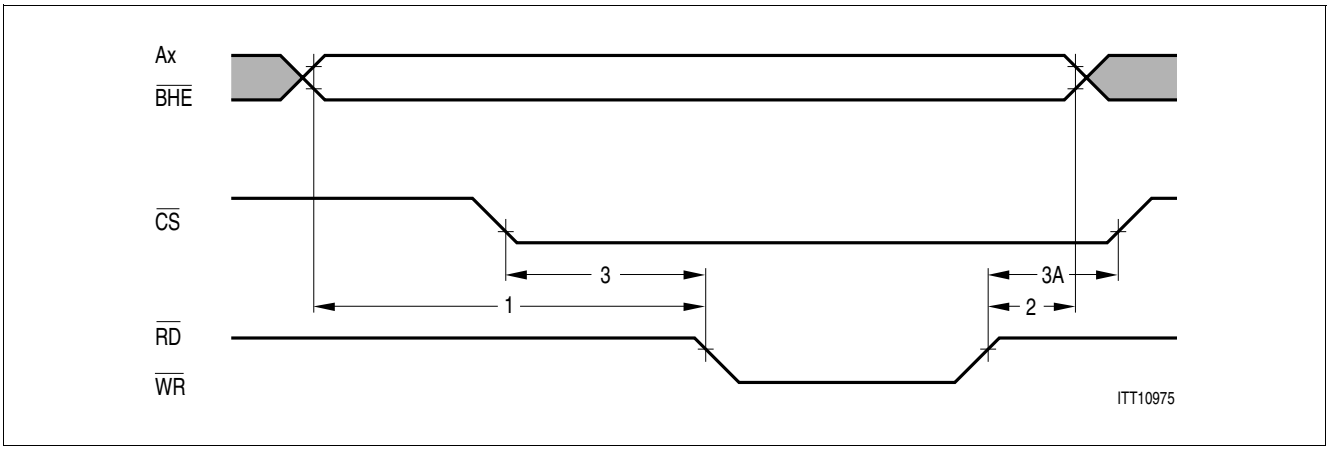



**Figure 51 Intel Non-Multiplexed Address Timing**

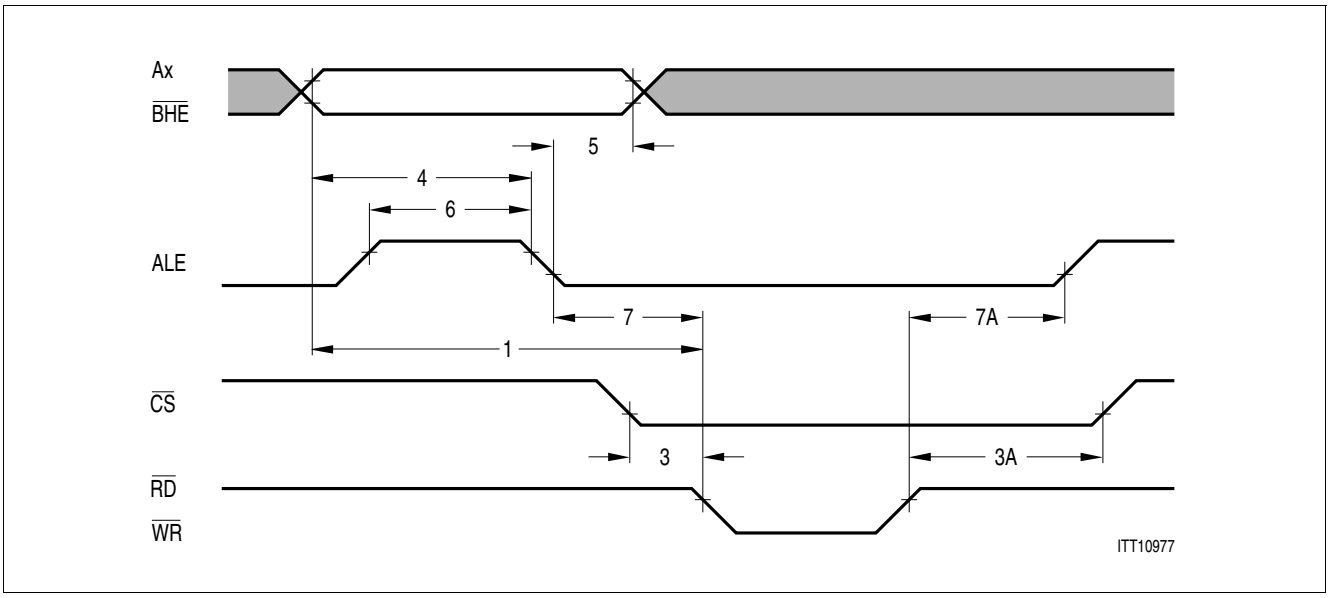



**Figure 52 Intel Multiplexed Address Timing**

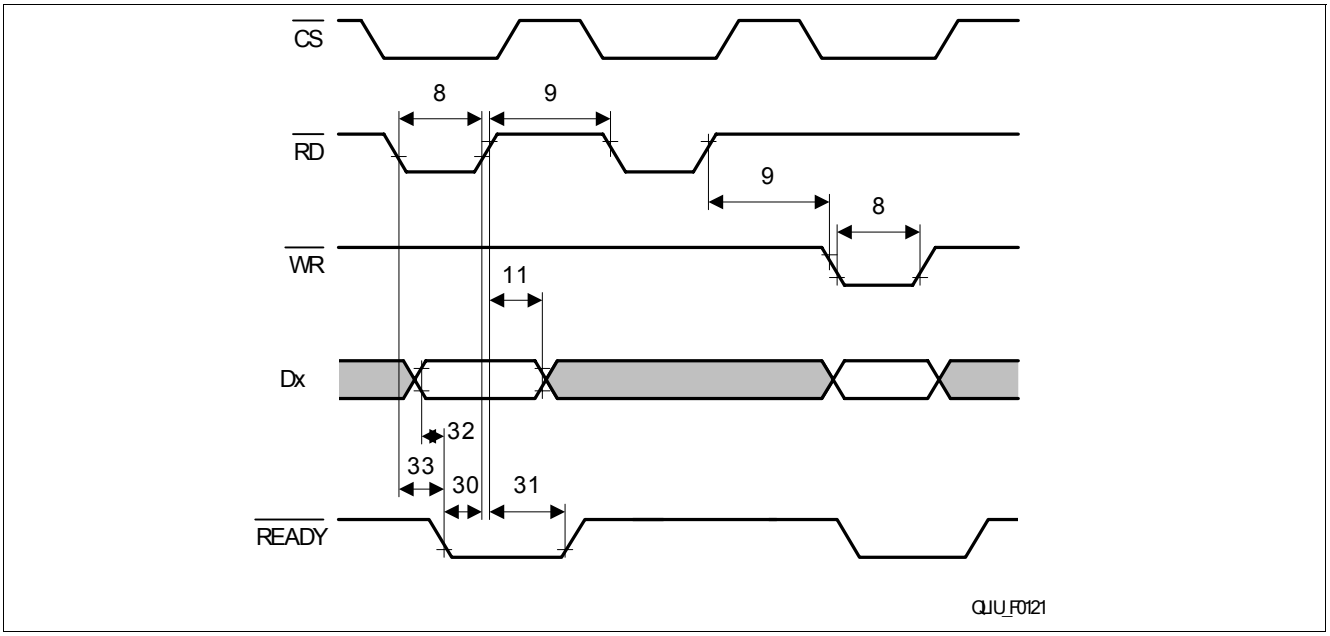



**Figure 53 Intel Read Cycle Timing**

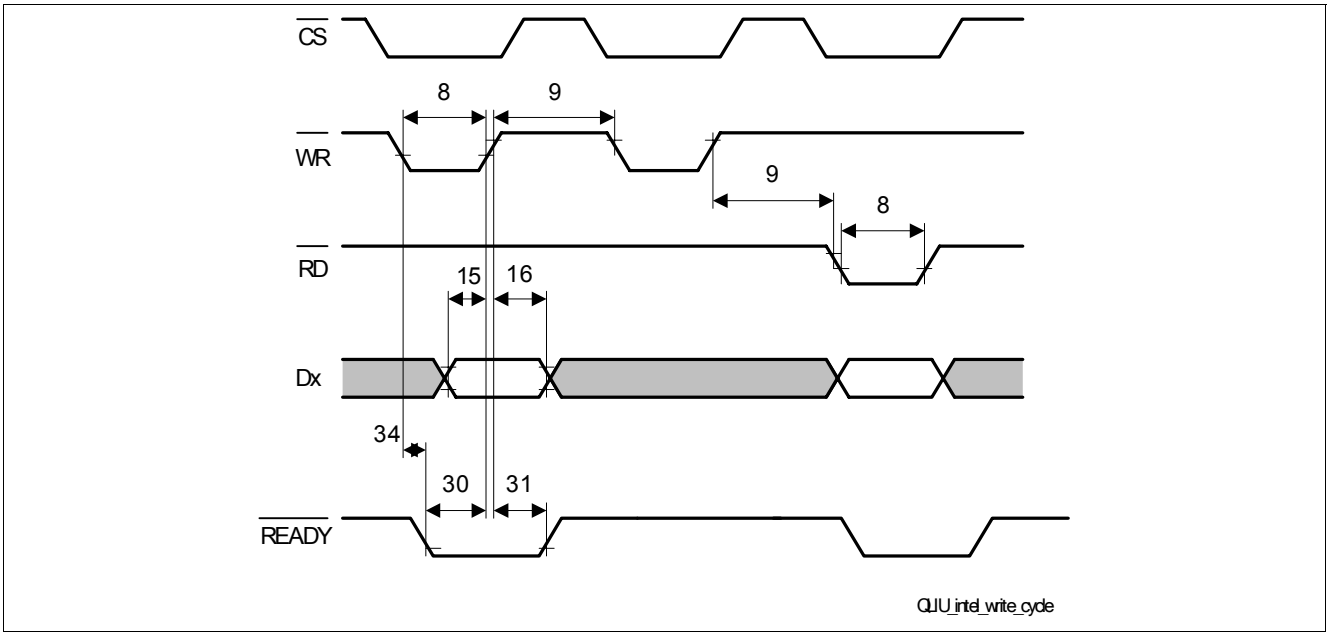



**Figure 54 Intel Write Cycle Timing**

**Table 60 Intel Bus Interface Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Address, $\overline{BHE}$ setup time | 1 | 5 | – | – | ns | – |
| Address, $\overline{BHE}$ hold time | 2 | 0 | – | – | ns | – |
| $\overline{CS}$ setup time | 3 | 0 | – | – | ns | – |
| $\overline{CS}$ hold time | 3A | 0 | – | – | ns | – |
| Address, $\overline{BHE}$ stable before ALE inactive | 4 | 25 | – | – | ns | – |
| Address, $\overline{BHE}$ hold after ALE inactive | 5 | 10 | – | – | ns | – |

**Table 60 Intel Bus Interface Timing Parameter Values** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ALE pulse width | 6 | 30 | – | – | ns | – |
| ALE setup time before $\overline{RD}$ or $\overline{WR}$ | 7 | 0 | – | – | ns | – |
| ALE hold time after $\overline{RD}$ or $\overline{WR}$ | 7A | 30[1)] | – | – | ns | – |
| $\overline{RD}$, $\overline{WR}$ pulse width | 8 | 80 | – | – | ns | – |
| RD, WR control interval | 9 | 70[2)] | – | – | ns | – |
| Data hold after $\overline{RD}$ inactive | 11 | 10 | – | 30 | ns | – |
| Data stable before $\overline{WR}$ inactive | 15 | 30 | – | – | ns | – |
| Data hold after $\overline{WR}$ inactive | 16 | 10 | – | – | ns | – |
| $\overline{RD}$ or $\overline{WR}$ delay after $\overline{READY}$ | 30 | – | – | 50 | ns | – |
| $\overline{READY}$ hold time after $\overline{RD}$ or $\overline{WR}$ | 31 | 5 | – | – | ns | – |
| Data stable before $\overline{READY}$ | 32 | – | – | 100 | ns | – |
| $\overline{RD}$ to $\overline{READY}$ delay | 33 | – | – | 100 | ns | – |
| $\overline{WR}$ to $\overline{READY}$ delay | 34 | – | – | 100 | ns | – |

1) Not tested in production

2) Not tested in production

### 6.1.4.2 Motorola Bus Interface Mode

**Figure 55** and **Figure 56** show the timing of the SCI Interface and **Table 61** the appropriate timing parameter values.

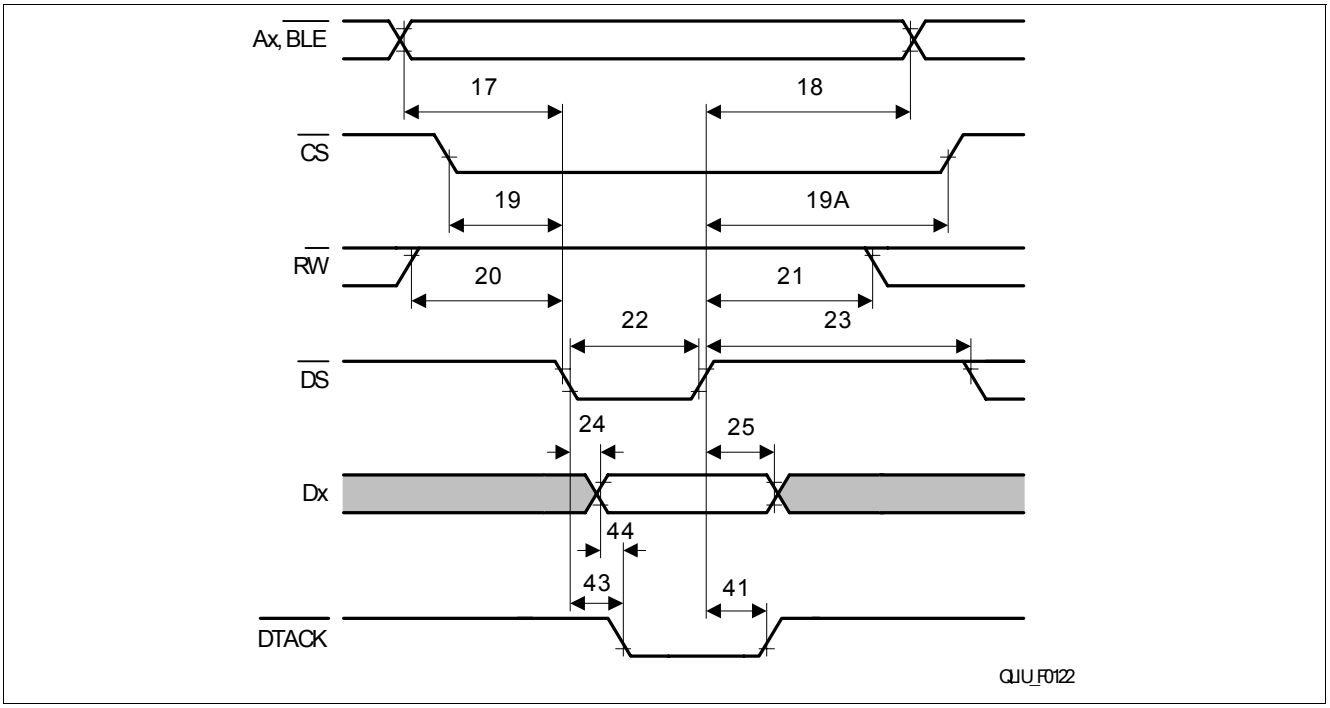



**Figure 55 Motorola Read Cycle Timing**

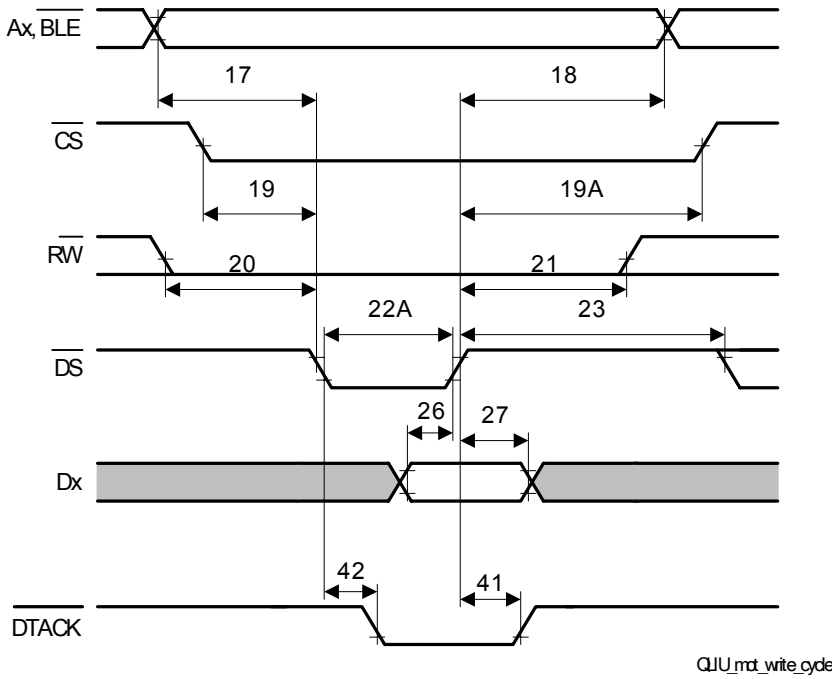



**Figure 56 Motorola Write Cycle Timing**

**Table 61 Motorola Bus Interface Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Address, $\overline{BLE}$ setup time before $\overline{DS}$ active | 17 | 15 | – | – | ns | – |
| Address, $\overline{BLE}$ hold after $\overline{DS}$ inactive | 18 | 0 | – | – | ns | – |
| $\overline{CS}$ active before $\overline{DS}$ active | 19 | 0 | – | – | ns | – |
| $\overline{CS}$ hold after $\overline{DS}$ inactive | 19A | 0 | – | – | ns | – |
| R$\overline{W}$ stable before $\overline{DS}$ active | 20 | 10 | – | – | ns | – |
| R$\overline{W}$ hold after $\overline{DS}$ inactive | 21 | 0 | – | – | ns | – |
| $\overline{DS}$ pulse width (read access) | 22 | 80 | – | – | ns | – |
| $\overline{DS}$ pulse width (write access) | 22A | 100 | – | – | ns | – |
| $\overline{DS}$ control interval | 23 | 70[1)] | – | – | ns | – |
| Data valid after $\overline{DS}$ active (read access) | 24 | – | – | 75[2)] | ns | – |
| Data hold after $\overline{DS}$ inactive (read access) | 25 | – | – | 30 | ns | – |
| Data stable before $\overline{DS}$ inactive (write access) | 26 | 30 | – | – | ns | – |
| Data hold after $\overline{DS}$ inactive (write access) | 27 | 10 | – | – | ns | – |
| $\overline{DTACK}$ hold time after $\overline{DS}$ inactive | 41 | 10 | – | – | ns | – |
| $\overline{DS}$ to $\overline{DTACK}$ delay for write | 42 | – | – | 100 | ns | – |
| $\overline{DS}$ to $\overline{DTACK}$ delay for read | 43 | – | – | 100 | ns | – |
| Data strobe before $\overline{DTACK}$ | 44 | 0 | – | – | ns | – |

1) Not tested in production

2) Not tested in production

### 6.1.4.3 SCI Interface

**Figure 57** shows the timing of the SCI Interface and **Table 62** the appropriate timing parameter values.

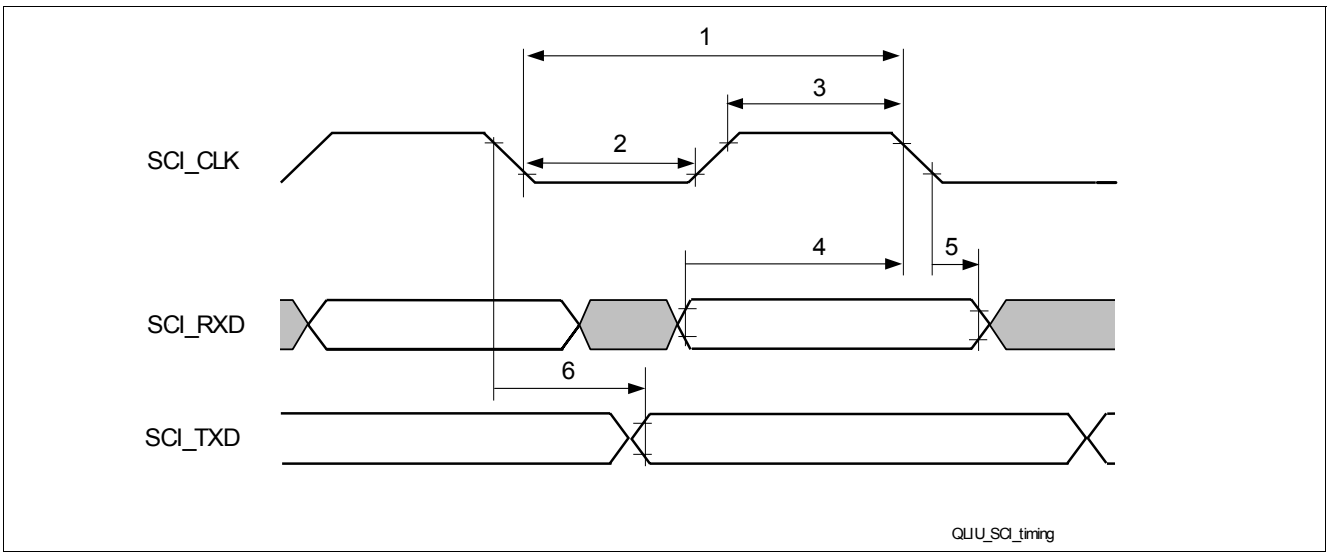



**Figure 57 SCI Interface Timing**

**Table 62 SCI Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCI_CLK cycle time in full duplex mode | 1 | 170 | – | – | ns | – |
| SCI_CLK cycle time in half duplex mode | 1 | 500 | – | – | ns | – |
| SCI_CLK clock low time | 2 | 76.5[1)] | – | – | ns | – |
| SCI_CLK clock high time | 3 | 76.5[2)] | – | – | ns | – |
| SCI_RXD setup time before SCI_CLK | 4 | 0 | – | – | ns | – |
| SCI_RXD hold time after SCI_CLK | 5 | 0 | – | – | ns | – |
| SCI_TXD delay time after SCI_CLK | 6 | – | – | 30 | ns | – |

1) Not tested in production

2) Not tested in production

### 6.1.4.4 SPI Interface

Figure 58 shows the timing of the SCI Interface and Table 63 the appropriate timing parameter values.

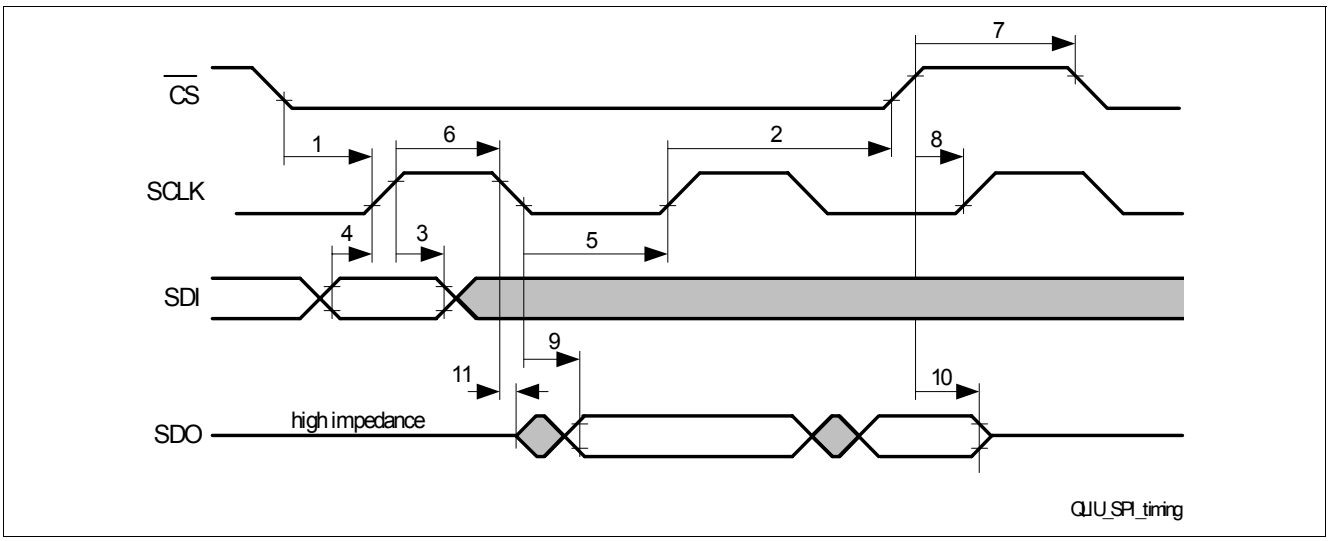



**Figure 58 SPI Interface Timing**

**Table 63 SPI Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLK frequency | – | – | – | 100 | MHz | – |
| $\overline{CS}$ setup time before SCLK | 1 | 40 | – | – | ns | – |
| $\overline{CS}$ hold time after SCLK | 2 | 40 | – | – | ns | – |
| SDI hold time after SCLK | 3 | 40 | – | – | ns | – |
| SDI setup time before SCLK | 4 | 40 | – | – | ns | – |
| SCLK low time | 5 | 45[1)] | – | – | ns | – |
| SCLK high time | 6 | 45[2)] | – | – | ns | – |
| $\overline{CS}$ high time | 7 | 100 | – | – | ns | – |
| Clock disable time before SCLK | 8 | 50 | – | – | ns | – |
| SDO output stable after SCLK | 9 | – | – | 40 | ns | – |
| SDO output hold after $\overline{CS}$ disable | 10 | – | – | 40 | ns | – |
| SDO output high impedance after SCLK | 11 | 0 | – | – | ns | – |

1) Not tested in production

2) Not tested in production

## 6.1.5 Digital Interface (Framer Interface)

Figure 59, Figure 60, Figure 61 and Figure 62 show the timing and Table 65, Table 66, Table 67 the appropriate timing parameter values at the digital interface of the QuadLIU™.

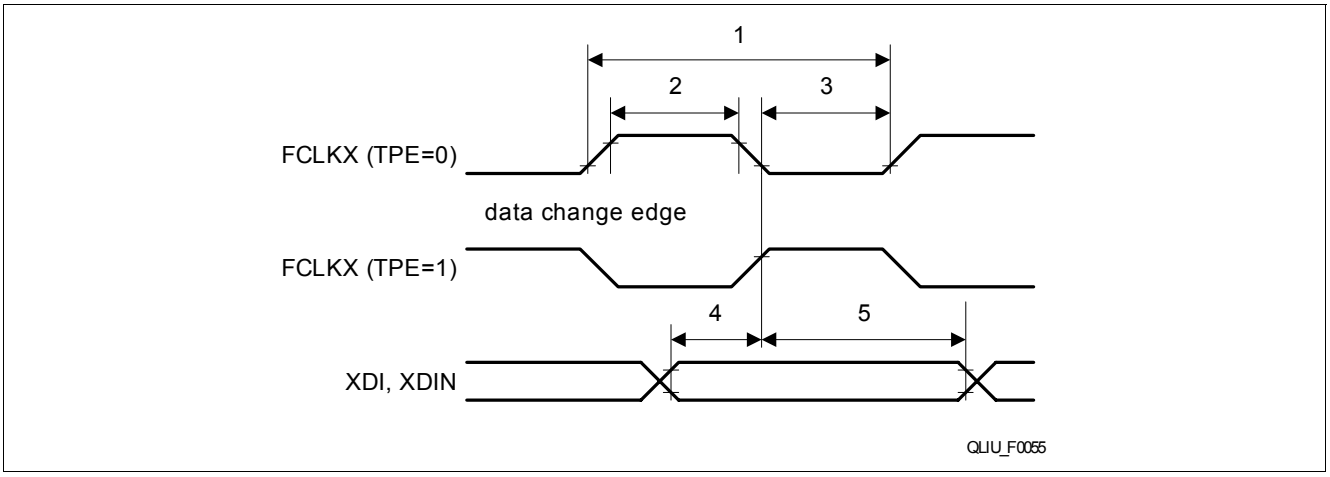



**Figure 59 FCLKX Output Timing**

**Table 64 FCLKX Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLKX clock period E1 | 1 | – | 488 | – | ns | – |
| FCLKX clock period T1/J1 | 1 | – | 648 | – | ns | – |
| FCLKX high | 2 | 40 | – | – | % | – |
| FCLKX low | 3 | 40 | – | – | % | – |
| XDI, XDIN setup time | 4 | 20 | – | – | ns | – |
| XDI, XDIN hold time | 5 | 20 | – | – | ns | – |

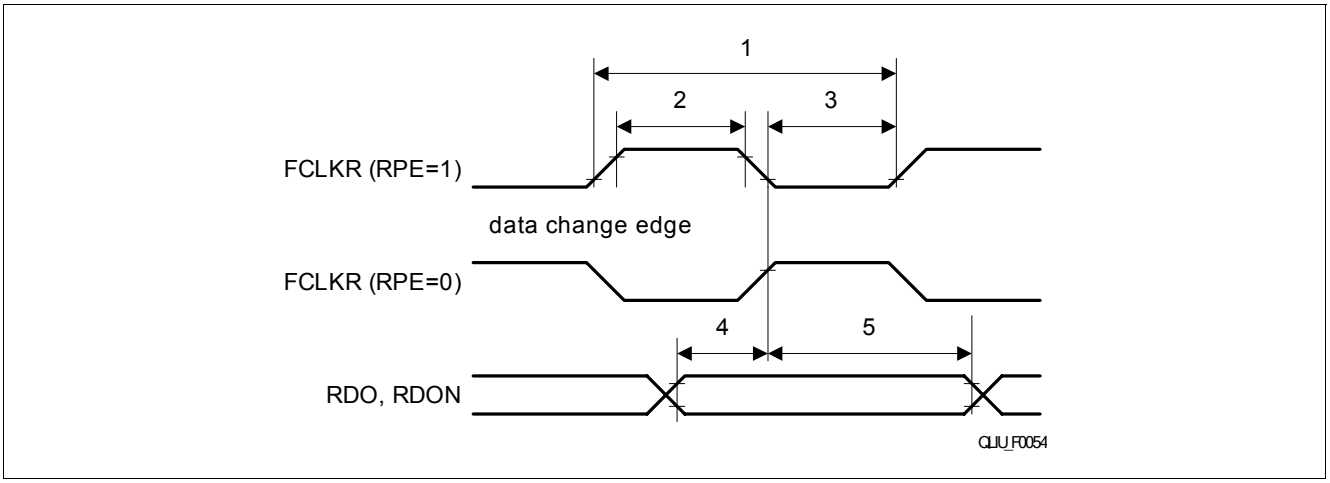



**Figure 60 FCLKR Output Timing**

**Table 65 FCLKR Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLKR clock period E1 | 1 | – | 488 | – | ns | – |
| FCLKR clock period T1/J1 | 1 | – | 648 | – | ns | – |
| FCLKR high | 2 | 40 | – | – | % | – |
| FCLKR low | 3 | 40 | – | – | % | – |
| RDO, RDON setup time | 4 | -10 | – | – | ns | – |
| RDO, RDON hold time | 5 | 200 | – | – | ns | – |

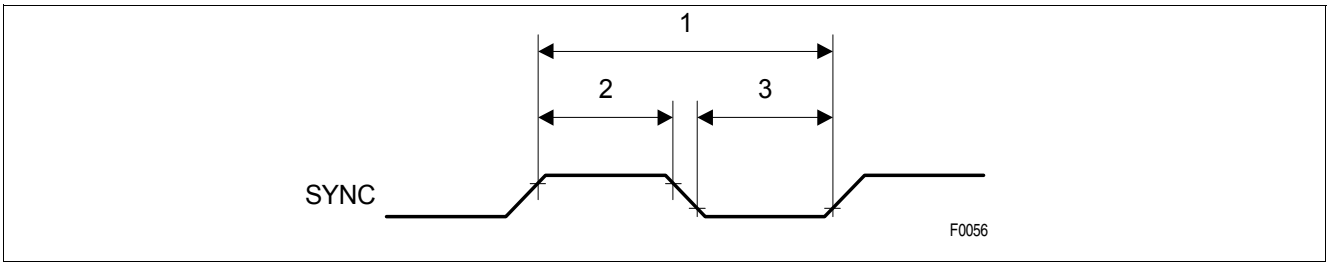



**Figure 61 SYNC Timing**

**Table 66 SYNC Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SYNC period 2.048 MHz | 1 | – | 488 | – | ns | – |
| SYNC period 1.544 MHz | 1 | – | 648 | – | ns | – |
| SYNC period 8 kHz | 1 | – | 125 | – | ns | – |
| SYNC low time | 2 | 20 | – | – | % | – |
| SYNC high time | 3 | 20 | – | – | % | – |

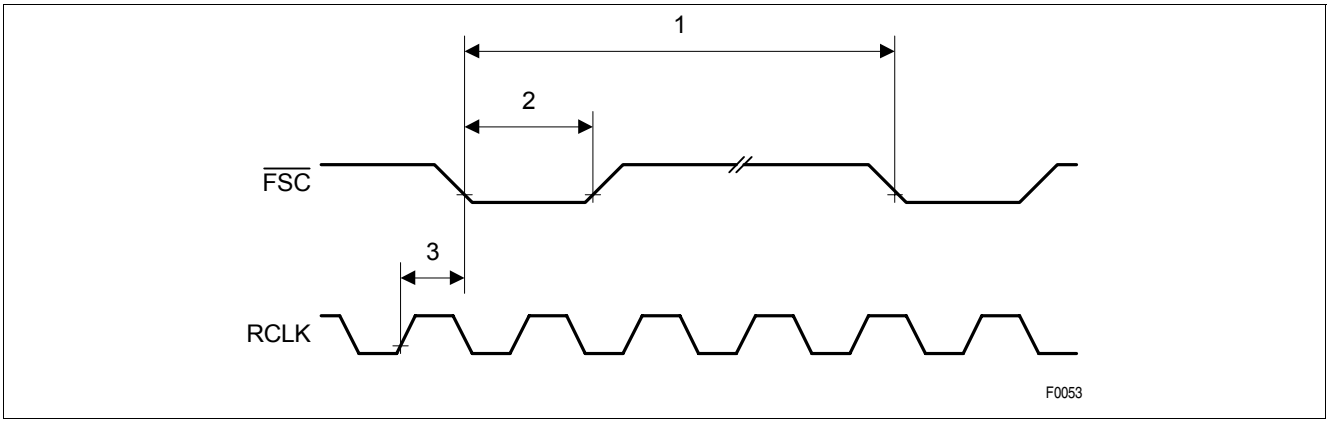



**Figure 62 FSC Timing**

**Table 67 FSC Timing Parameter Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FSC period | 1 | – | 125 | – | µs | – |
| FSC low time E1 | 2 | – | 488 | – | ns | – |
| FSC low time T1/J1 | 2 | – | 648 | – | ns | – |
| RCLK to FSC delay E1 | 3 | – | – | 370 | ns | – |
| RCLK to FSC delay T1/J1 | 3 | – | – | 280 | ns | – |

### 6.1.6 Pulse Templates - Transmitter

The transmitter includes a programmable pulse shaper to generate transmit pulse masks according to:

- For T1: FCC68; ANSI T1. 403 1999, figure 4; ITU-T G703 11/2001, figure 10 (for different cable lengths), see **Figure 64**. For measurement configuration were $R_{load}$ = 100 Ω see **Figure 40**.
- For E1: ITU-T G703 11/2001, figure 15 (for 0 m cable length), see **Figure 63**; ITU-T G703 11/2001, figure 20 (for DCIM mode). For measurement configuration were $R_{load}$ = 120 Ω or $R_{load}$ = 75 Ω see **Figure 39**.

The transmit pulse form is programmed either

- By the registers XMP(2:0) compatible to the QuadLIU®, see **Table 29** and **Table 30**, if the register bit XPM2.XPDIS is cleared
- Or by the registers TXP(16:1), if the register bit XPM2.XPDIS is set, see **Table 31** and **Table 32**.

#### 6.1.6.1 Pulse Template E1

With the given values in **Table 30** or **Table 32**, for transformer ratio: 1 : 2.4, cable type AWG24 and with $R_{load}$ = 120 Ω the pulse mask according to ITU-T G703 11/2001, see **Figure 63**, is fulfilled.

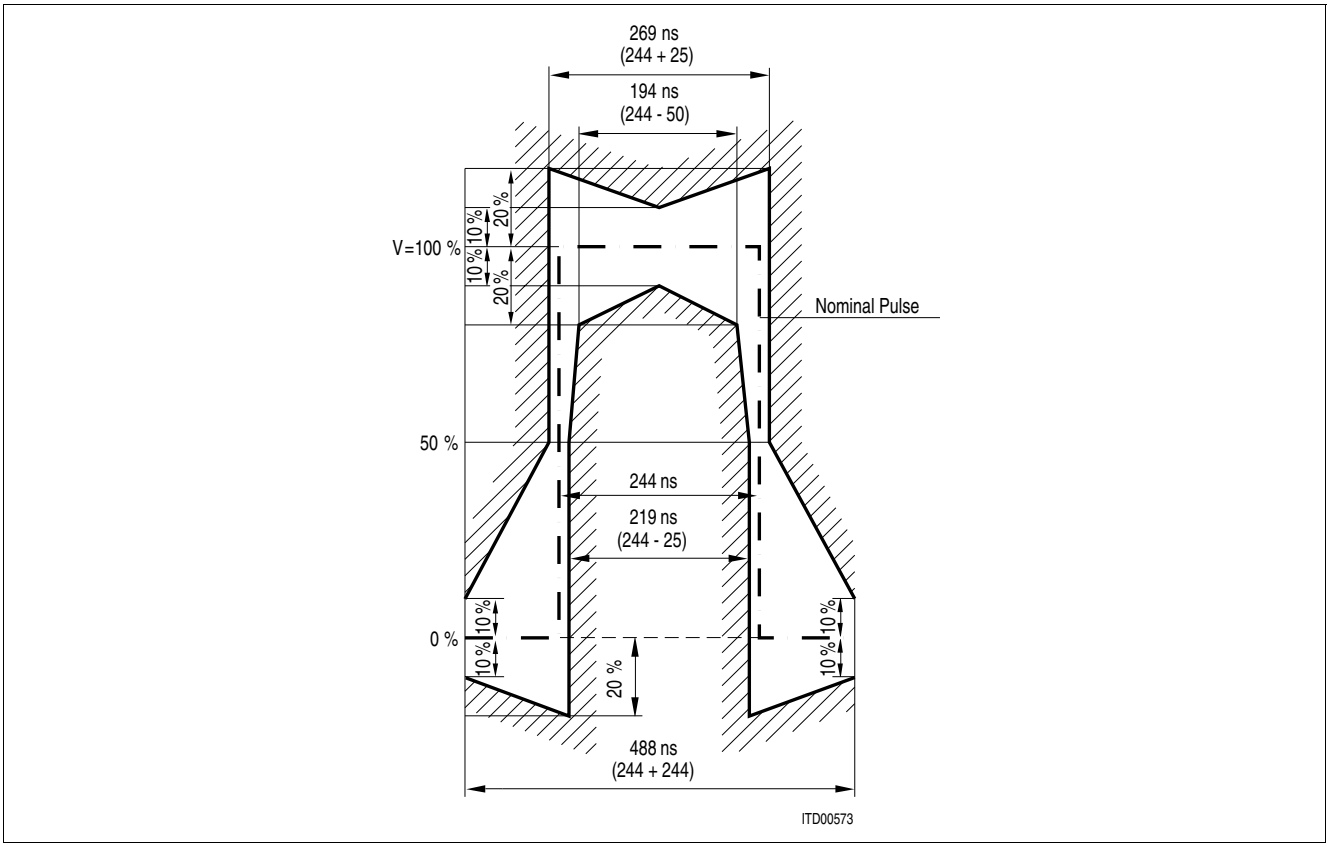



**Figure 63 E1 Pulse Shape at Transmitter Output**

### 6.1.6.2 Pulse Template T1

With the given values in **Table 29** or **Table 31**, for transformer ratio: 1 : 2.4, cable type AWG24 and with $R_{load}$ = 100 Ω the pulse mask according to ITU-T G703 11/2001, figure 10, see **Figure 64**, is fulfilled.

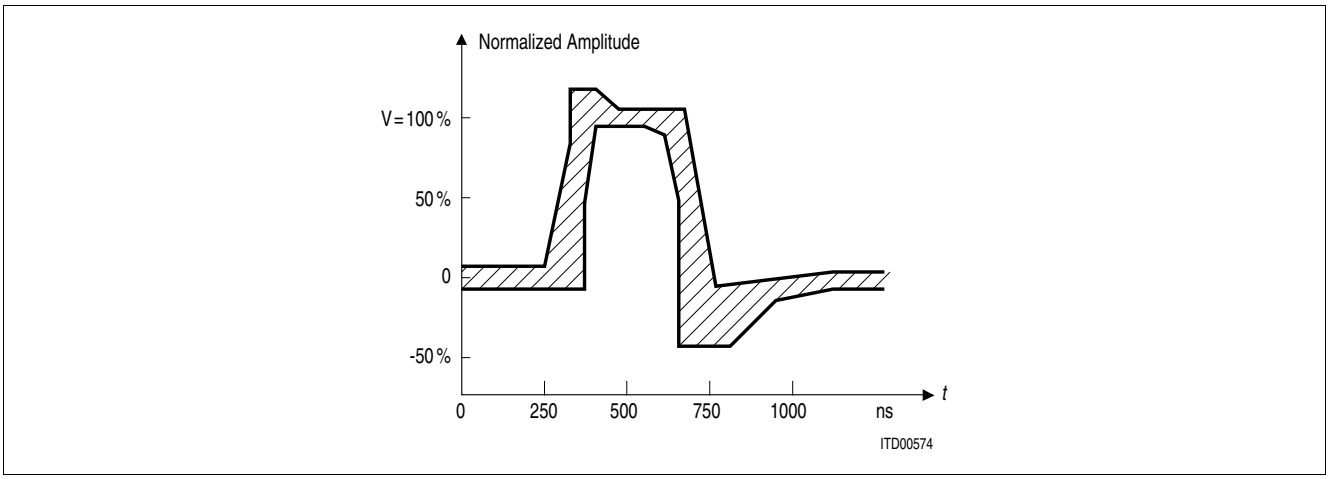



**Figure 64 T1 Pulse Shape at the Cross Connect Point**

**Table 68 T1 Pulse Template at Cross Connect Point (T1.102 [1])**

| Maximum Curve | | Minimum Curve | |
|---|---|---|---|
| **Time [ns]** | **Level [%][2]** | **Time [ns]** | **Level [%]** |
| 0 | 5 | 0 | -5 |
| 250 | 5 | 350 | -5 |
| 325 | 80 | 350 | 50 |
| 325 | 115 | 400 | 95 |
| 425 | 115 | 500 | 95 |
| 500 | 105 | 600 | 90 |
| 675 | 105 | 650 | 50 |
| 725 | -7 | 650 | -45 |
| 1100 | 5 | 800 | -45 |
| 1250 | 5 | 925 | -20 |
| | | 1100 | -5 |
| | | 1250 | -5 |

1) Requirements of ITU-T G.703 are also fulfilled

2) 100 % value must be in the range of 2.4 V and 3.6 V;
tested at 0 and 200 m using PIC 22AWG cable characteristics.

## 6.2 Capacitances

Values of capacitances of the input and of the output pins of the QuadLIU™ are listed in Table 69.

**Table 69 Capacitances**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance[1)] | $C_{IN}$ | 5 | – | 10 | pF | – |
| Output capacitance [1)] | $C_{OUT}$ | 8 | – | 15 | pF | All except XLx |
| Output capacitance [1)] | $C_{OUT}$ | 8 | – | 20 | pF | XLx |

1) Not tested in production

## 6.3 Package Characteristics

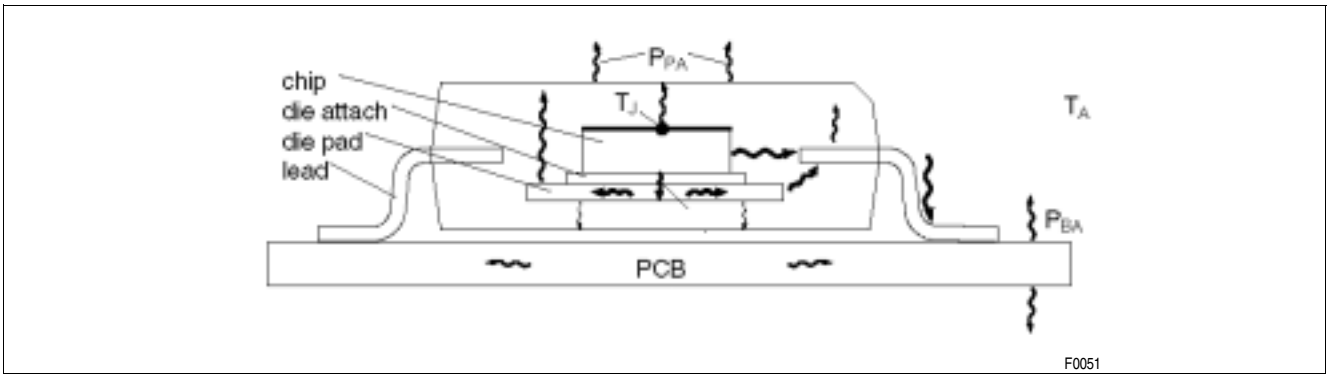



**Figure 65 Thermal Behavior of Package**

**Table 70 Package Characteristic Values**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal Resistance | $R_{thjam}$ [1)] | – | 47 | – | K/W | Single layer PCB, no convection |
| | $R_{thjc}$ [2)] | – | 9 | – | K/W | |
| Thermal Resistance BGA | $R_{thjab}$ [1)] | – | 29 | – | K/W | Single layer PCB, natural convection |
| Junction Temperature | $R_j$ | – | | 125 | °C | – |

1) $R_{thja} = (T_{junction} - T_{ambient})$/Power: Not tested in production.

2) $R_{thjc} = (T_{junction} - T_{case})$/Power: Not tested in production.

## 6.4 Test Configuration

### 6.4.1 AC Tests

The values for AC characteristics of the chapters above are based on the following definitions of levels and load capacitances:

**Table 71 AC Test Conditions**

| Parameter | Symbol | Test Values | Unit | Notes |
|---|---|---|---|---|
| Load Capacitance | $C_L$ | 50 | pF | – |
| Input Voltage high | $V_{IH}$ | 2.4 | V | All except RLx |
| Input Voltage low | $V_{IL}$ | 0.4 | V | All except RLx |
| Test Voltage high | $V_{TH}$ | 2.0 | V | All except XLx |
| Test Voltage low | $V_{TL}$ | 0.8 | V | All except XLx |

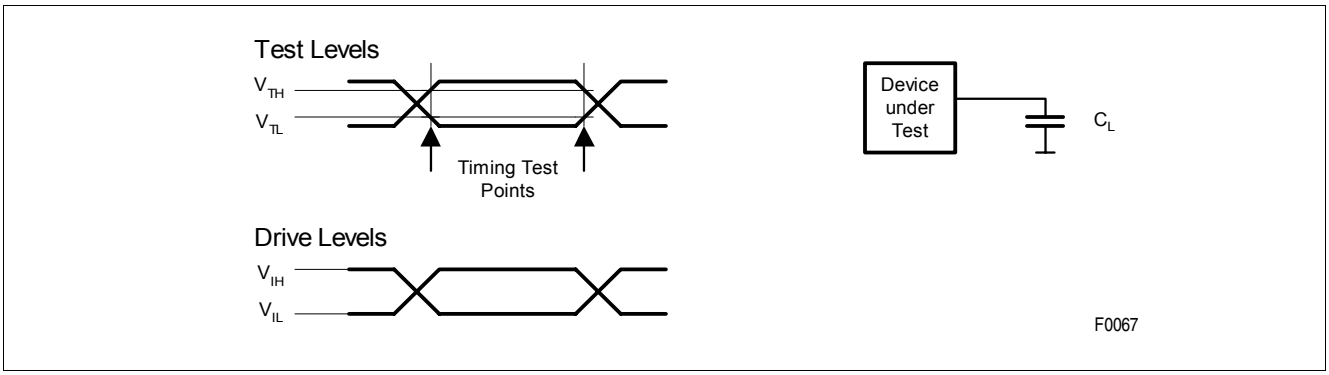



**Figure 66 Input/Output Waveforms for AC Testing**

### 6.4.2 Power Supply Test

For power supply test all eight channels of the QuadLIU™ are active. Transmitter and receiver are configured as for typical applications. The transmitted data are looped back to the receiver by a short line as shown in **Figure 67**. On the system side the interfaces of all channels work independent from another (no multiplex mode is configured).

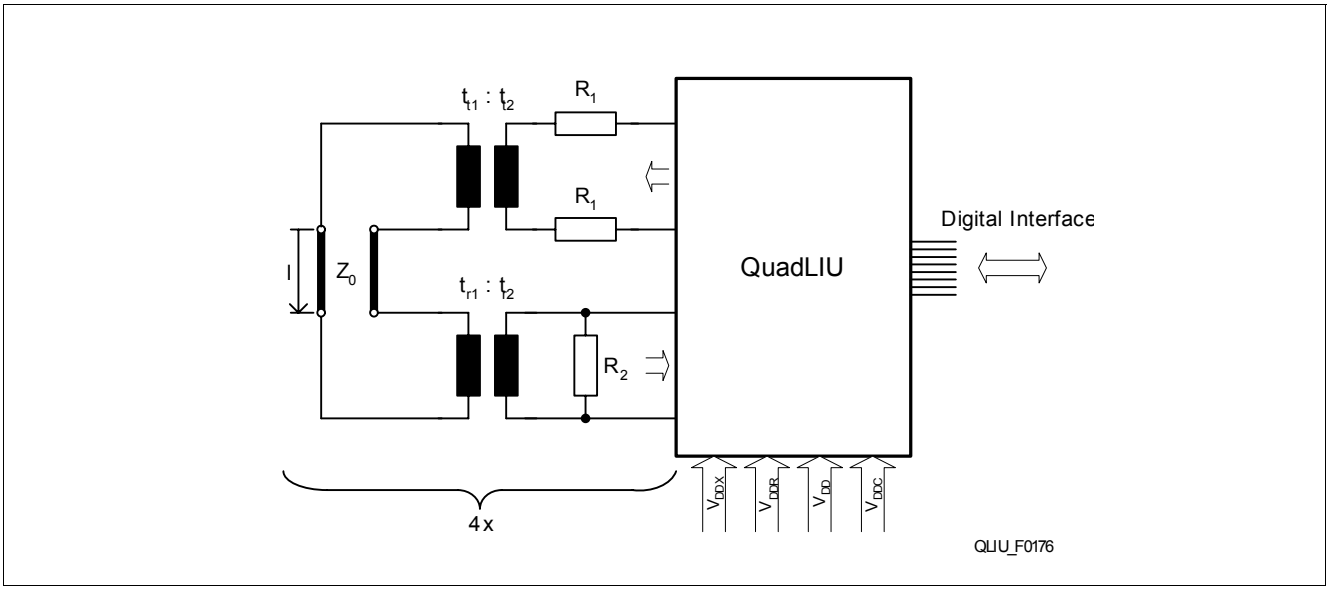



**Figure 67 Device Configuration for Power Supply Testing**

**Table 72 Power Supply Test Conditions E1**

| Parameter | Symbol | Test Values | Unit | Notes |
|---|---|---|---|---|
| Load Resistance at transmitter | $R_1$ | 7.5 | Ω | 1%; PC6.TSRE = ´0´ |
| Termination Resistance at receiver | $R_2$ | 120 | Ω | 1%; integrated receive line resistor $R_{TERM}$ is switched off (LIM0.RTRS =´0´) |
| Line Impedance | $R_L$ | 120 | Ω | – |
| Line Length | l | < 0.2 | m | – |
| Transformer Ratio Transmit | tt1 : tt2 | 2.4 : 1 | | – |
| Transformer Ratio Receive | tr1 : tr2 | 1 : 1 | | – |
| Framer interface Frequency | XCLK<br>RCLK | 2.048 | MHz | – |
| Test Signal | – | $2^{15}$-1 | – | PRBS pattern |
| Pulse Mask Programming (compatible to QuadLIU®) | XPM2 | $40_H$ | – | Pulse mask according to ITU-T G703 11/2001, see **Figure 63** |
| | XPM1 | $03_H$ | | |
| | XPM0 | $7B_H$ | | |
| Ambient Temperature | – | 85 | °C | – |

**Table 73 Power Supply Test Conditions T1/J1**

| Parameter | Symbol | Test Values | Unit | Notes |
|---|---|---|---|---|
| Load Resistance | $R_1$ | 2 | Ω | 1%; PC6.TSRE = ´0´ |
| Termination Resistance | $R_2$ | 100 | Ω | 1%; integrated receive line resistor $R_{TERM}$ is switched off (LIM0.RTRS =´0´) |
| Line Impedance | $R_L$ | 100 | Ω | – |
| Line Length | l | < 0.2 | m | – |
| Transformer Ratio Transmit | tt1 : tt2 | 2.4 : 1 | – | – |
| Transformer Ratio Receive | tr1 : tr2 | 1 : 1 | – | – |

**Table 73 Power Supply Test Conditions T1/J1** (cont'd)

| Parameter | Symbol | Test Values | Unit | Notes |
|---|---|---|---|---|
| Framer interface Frequency | XCLK<br>RCLK | 1.544 | MHz | – |
| Test Signal | – | $2^{15}$-1 | – | PRBS pattern |
| Pulse Mask Programming (compatible to QuadLIU®) | XPM2 | $02_H$ | – | Pulse mask according to ITU-T G703 11/2001, figure 10, see **Figure 64** |
| | XPM1 | $27_H$ | | |
| | XPM0 | $9F_H$ | | |
| Ambient Temperature | – | 85 | °C | – |

# 7 Operational Description

## 7.1 Operational Overview

Each of the four channels of the QuadLIU™ can be operated in two clock modes, which are either E1 mode or T1/J1 mode, selected by the register bit GCM2.VFREQ_EN, see **Chapter 3.5.5**:

- In the so called “flexible master clocking mode” (GCM2.VFREQ_EN = ´1´) all four ports can work in E1 or in T1 mode individually, independent from another.
- In the so called “clocking fixed mode” (GCM2.VFREQ_EN = ´0´) all four ports must work together either in E1 or in T1 mode.

The device is programmable via one of the three integrated micro controller interfaces which are selected by strapping of the pins IM(1:0):

- The asynchronous interface has two modes: Intel (IM(1:0) = ´$00_b$´) and Motorola (IM(1:0) = ´$01_b$´). This interface enables byte or word access to all control and status registers, see **Chapter 3.5.1**.
- SPI interface (IM(1:0) = ´$10_b$´), see **Chapter 3.5.2.2**.
- SCI interface (IM(1:0) = ´$11_b$´), see **Chapter 3.5.2.1**.

The QuadLIU™ has three different kinds of registers:

- The control registers configure the whole device and have write and read access.
- The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.
- The interrupt status registers are read-only and are cleared by reading (“rsc”). They are updated (set) continuously. Normally, the processor reads the interrupt status registers after an interrupt occurs at pin INT. Masking can be done with the appropriate interrupt mask registers. Mask registers are control registers.

All this registers can be separate into two groups:

- Global registers are not belonging especially to one of the four channels. The higher address byte is ´$00_H$´.
- The other registers are belonging to one of the four channels. The higher address bytes - marked as ´$xx_H$´ in the register description - are identical to the numbers 0 up to 3 of the appropriate channels. So every of this registers exist four time in the whole device.

## 7.2 Device Reset

After the device is powered up, the QuadLIU™ must be forced to the reset state first.

The QuadLIU™ is forced to the reset state if a low signal is input on pin $\overline{\text{RES}}$ for a minimum period of 10 µs, see **Figure 50**. During reset the QuadLIU™

- Needs an active clock on pin MCLK and
- The pin VSEL must be connect either to 3.3 V or to $V_{SS}$ to define if internal voltage regulator is used
- The pins IM(1:0) must have defined values to select the micro controller interface.
- Only if IM(1:0) = ´$11_b$´ (SCI interface is selected) the pins A(5:0) must have defined values to select the SCI source address of the device.
- Only if IM1 = ´1´ (SCI or SPI interface is selected) the pins D(15:5) must have defined values to configure the central PLL in the master clocking unit of the device.
- Only if IM1 = ´0´ (asynchronous micro controller interface is selected) the pin READY_EN must have a defined value to select if the signal $\overline{\text{READY/DTACK}}$ is used

During and after reset all internal flip-flops are reset and most of the control registers are initialized with default values.

After reset the complete device is initialized, especially to E1 operation and “flexible master clocking mode”. The complete initialization is listed in **Table 74**. Additionally all interrupt mask registers IMR1, IMR3, IMR4, IMR6 and IMR7 are initialized to ´$FF_H$´, so that not masking is performed.

After reset the QuadLIU™ must be configured first. General guidelines for configuration are described in **Chapter 7.4** for E1 mode and **Chapter 7.5** for T1/J1 mode.

For reset see also **Chapter 3.5.5.1**.

## 7.3 Device Initialization

After reset, the QuadLIU™ is initialized for E1 with register values listed in the following table.

**Table 74 Initial Values after Reset**

| Register | Reset Value | Meaning |
|---|---|---|
| GPC1 | ´$00_H$´ | Reserved mode. Must be set to ´$10_H$´ for proper operation! |
| LIM0, LIM1, PCD, PCR | ´$00_H$´, ´$00_H$´, ´$00_H$´, ´$00_H$´ | Slave Mode, local loop off<br>Analog interface selected; remote loop off; Pulse count for LOS detection cleared; Pulse count for LOS recovery cleared |
| XPM(2:0) | ´$40_H$´, ´$03_H$´, ´$7B_H$´ | E1 Transmit pulse template for 0 m but with unreduced amplitude (note that transmitter is in tristate mode) |
| IMR(7:0) | ´$FF_H$´ | All interrupts are disabled |
| GCR | ´$00_H$´ | Internal second timer, power on |
| CMR1 | ´$00_H$´ | RCLK output: DPLL clock, DCO-X enabled, DCO-X internal reference clock |
| CMR2 | ´$00_H$´ | RCLK selected, XCLK selected |
| PC(3:1) | ´$00_H$´, ´$F0_H$´ ´$00_H$´, ´$00_H$´ | Functions of ports RP(A to B) are reserved, function of port RPC is RCLK output (but is only pulled up, because PC5.CRP = ´0´ after reset), functions of ports XP(A to B) are reserved. |
| PC5 | ´$00_H$´ | FCLKR, FCLKX, RCLK configured to inputs, |
| GCM(6:1) | GCM2 = ´$10_H$´, others ´$00_H$´ | “Flexible master clocking mode” selected |
| GPC(4:3) | ´$43_H$´, ´$21_H$´ | Sources for RCLK1 up to RCLK4 are the appropriate channels |
| CMR(6:4) | ´$00_H$´ | Recovered line clock drives RCLK |
| GPC2 | ´$00_H$´ | Source for SEC and RCLK1 is channel 1 |
| TXP(16:1) | TXP(1:8) = ´$38_H$´ TXP(9:16) = ´$00_H$´ | This registers are not used after reset because XPM2.XPDIS = ´0´ |
| INBLDTR | ´$00_H$´ | Minimum In-band loop detection time |
| ALS | ´$00_H$´ | No automatic loop switching is performed |
| PRBSTS(4:1) | All ´$00_H$´ | No time slots are selected for PRBS pattern |

## 7.4 Device Configuration in E1 Mode

### E1 Configuration

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after reset goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 75** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit MR1.PMOD should always be kept low (otherwise T1/J1 mode is selected).

**Table 75 Configuration Parameters (E1)**

| | |
|---|---|
| **Basic Set Up** | |
| Master clocking mode | GCM(6:1) according to external MCLK clock frequency |
| E1 mode select | MR1.PMOD = ´0´ |
| Clock system configuration | CMR(3:1), GPC1; CMR(6:4) and GPC(6:2) |
| Specification of line interface | LIM0, LIM1, XPM(2:0) |
| Specification of transmit pulse mask | XPM(2:0) or TXP(16:1) |
| Line interface coding | MR0.XC(1:0), MR0.RC(1:0) |
| Loss-of-signal detection/recovery conditions | PCD, PCR, LIM1, LIM2 |
| Multi Function Port selection | PC(3:1) |

Features like alarm simulation etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

*Note: Read access to unused register addresses: value should be ignored. Write access to unused register addresses: should be avoided, or set to “00” hex. All control registers (except XS(16:1), CMDR, DEC) are of type Read/Write.*

### Specific E1 Register Settings

The following is a suggestion for a basic configuration to meet most of the E1 requirements. Depending on different applications and requirement any other configuration can be used.

**Table 76 Line Interface Configuration (E1)**

| | |
|---|---|
| GPC6.COMP_DIS = ´1´ | Sets the QuadLIU™ into a defined mode (necessary for proper operation) |
| MR2.DAIS = ´1´ | Disables AIS insertion into the data stream (necessary for proper operation) |
| MR2.RTM = ´1´ | Sets the receive dual elastic store in a “free running” mode (necessary for proper operation) |
| MR5.TT0 = ´1´ | Enables transmit transparent mode (necessary for proper operation) |
| MR5.XTM = ´1´ | Sets the transmitter in a “free running” mode (necessary for proper operation) |
| MR0.XC0/<br>MR0.RC0/<br>LIM1.DRS<br>MR3.CMI | The QuadLIU™ supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI and HDB3 are supported. For the digital line interface modes (dual- or single-rail) the QuadLIU™ supports AMI, HDB3, CMI (with and without HDB3 precoding). |
| PCD = ´$0A_H$´ | LOS detection after 176 consecutive “zeros” (fulfills G.775). |
| PCR = ´$15_H$´ | LOS recovery after 22 “ones” in the PCD interval. (fulfills G.775). |
| LIM1.RIL(2:0) = ´$02_H$´ | LOS threshold of 0.6 V (fulfills G.775). |

***Attention: After the device configuration a software reset should be executed by setting of bits CMDR.XRES/RRES.***

## 7.5 Device Configuration in T1/J1 Mode

After reset, the QuadLIU™ is initialized for E1 doubleframe format. To configure T1/J1 mode, bit MR1.PMOD has to be set high. After the internal clocking is settled to T1/J1mode (takes up to 20 µs), the following register values are initialized:

### T1/J1 Initialization

For a correct start up of the primary access interface a set of parameters specific to the system and hardware environment must be programmed after $\overline{\text{RES}}$ goes inactive (high). Both the basic and the operational parameters

must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 77** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, can be programmed simultaneously. The bit MR1.PMOD must always be kept high (otherwise E1 mode is selected). J1 mode is selected by additionally setting RC0.SJR = ´1´.

Features like channel loop-back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, etc. are activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

**Table 77 Configuration Parameters (T1/J1)**

| Basic Set Up | T1 | J1 |
|---|---|---|
| Master clocking mode | GCM(6:1) according to external MCLK clock frequency | |
| T1/J1 mode select | MR1.PMOD = ´1´, | MR1.PMOD = ´1´, |
| Clock system configuration | CMR(3:1), GPC1; CMR(6:4) and GPC(6:2) | |
| Specification of line interface | LIM0, LIM1, | |
| Specification of transmit pulse mask | XPM(2:0) or TXP(16:1) | |
| Line interface coding | MR0.XC(1:0), MR0.RC(1:0) | |
| Loss-of-signal detection/recovery conditions | PCD, PCR, LIM1, LIM2 | |
| AIS to framer interface | MR2.XAIS | |
| Multi Function Port selection | PC(3:1) | |

*Note: Read access to unused register addresses: value should be ignored. Write access to unused register addresses: should be avoided, or set to ´$00_H$´. All control registers (except XS(12:1), CMDR, DEC) are of type read/write*

### Specific T1/J1 Configuration

The following is a suggestion for a basic configuration to meet most of the T1/J1 requirements. Depending on different applications and requirements any other configuration can be used.

**Table 78 Line Interface Configuration (T1/J1)**

| Register | Function |
|---|---|
| GPC6.COMP_DIS = ´1´ | Sets the QuadLIU™ into a defined mode (necessary for proper operation) |
| MR2.DAIS = ´1´ | Disables AIS insertion into the data stream (necessary for proper operation) |
| LOOP.RTM = ´1´ | Sets the receive dual elastic store in a “free running” mode (necessary for proper operation) |
| MR4.TM = ´1´ | Enables transparent mode (necessary for proper operation) |
| MR5.XTM = ´1´ | Sets the transmitter in a “free running” mode (necessary for proper operation) |
| CCB(3:1) = ´$FF_H$‘ | “Clear Channel” mode is selected (necessary for proper operation only if AMI code is selected) |
| MR0.XC0/1<br>MR0.RC0/1<br>LIM1.DRS<br>CCB(3:1)<br>DIC3.CMI | The QuadLIU™ supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI (with and without bit 7stuffing) and B8ZS are supported. For the digital line interface modes (dual- or single-rail) the QuadLIU™ supports AMI (with and without bit 7 stuffing), B8ZS (with and without B8ZS precoding). |

**Table 78 Line Interface Configuration (T1/J1)** (cont'd)

| Register | Function |
|---|---|
| PCD = ´0A$_H$´ | LOS detection after 176 consecutive "zeros" (fulfills G.775/Telcordia (Bellcore)/AT&T) |
| PCR = ´15$_H$´ | LOS recovery after 22 "ones" in the PCD interval (fulfills G.775, Bellcore/AT&T). |
| LIM1.RIL(2:0) = ´02$_H$´ | LOS threshold of 0.6 V (fulfills G.775). |
| GCR.SCI = ´1´ | Additional Recovery Interrupts. Help to meet alarm activation and deactivation conditions in time. |
| LIM2.LOS1 = ´1´ | Automatic pulse-density check on 15 consecutive zeros for LOS recovery condition (Bellcore requirement) |

*Note: After the device configuration a software reset should be executed by setting of bits CMDR.XRES/RRES.*

## 7.6 Device Configuration for Digital Clock Interface Mode (DCIM)

The following table shows the necessary configuration for the Digital Clock Interface Mode (DCIM), see ITU-T G.703 11/2001, chapter 13. The receive clock at RL1/RL2 (2.048 MHz) is supported at multi function port RPC. The transmit clock at FCLKX (2.048 MHz) is transmitted at XL1/XL2.

DCIM mode is standardized only for 2.048 MHz (E1 mode, MR1.PMOD = ´0´). The QuadLIU™ can handle also 1.544 MHz if MR1.PMOD = ´1´.

**Table 79 Device Configuration for DCIM Mode**

| | |
|---|---|
| GPC6.COMP_DIS = ´1´ | Sets the QuadLIU™ into a defined mode (necessary for proper operation) |
| MR1.PMOD | Selects 2.048 MHz or 1.544 MHz, see text above |
| LIM0.DCIM = ´1´ | Selects DCIM mode. |
| LIM1.RL = ´0´ | TX clock mode. |
| CMR1.DXSS = ´0´ | |
| CMR1.DXJA = ´0´ | |
| LIM1.DRS = ´0´<br>MR0.RC(1:0) = ´$10_b$´ | Line interface mode RX |
| MR0.XC(1:0) = ´$10_b$´ | Line interface mode TX |
| PC1.RPC1(3:0) = ´$1111_b$´ | Select RCLK as output |
| PC5.CRP = ´1´ | |
| CMR1.DRSS(1:0) or<br>CMR5.DRSS(2:0) : select the appropriate channel | RX clock mode |
| CMR1.DCS = ´1´ | |
| LIM0.MAS = ´0´ | |
| CMR1.RS(1:0) = ´$10_b$´ or<br>CMR4.RS(2:0) = ´$010_b$´ | |
| GCM(1:8) see **Chapter 3.5.5** and **GCM6** | Configure clock system |
| LIM2.SCF, CMR6.SCFX, CMR2.ECFAX, CMR2.ECFAR, CMR3:CFAX(3:0), CMR3.CFAR(3:0), CMR4.IAR(4:0), CMR5.IAX(4:0): see **Chapter 3.7.8** and **Table 23** | Configure DCO-X and DCO-R |
| DIC1.RBS(1:0) = ´$10_b$´ | Configure elastic buffers |
| DIC1.XBS(1:0) = ´$11_b$´ | |

# 8 Appendix

## 8.1 Protection Circuitry

The design in **Figure 68** shows an example of how to build up a generic E1/T1/J1 platform. The circuit shown has been successfully checked against ITU-T K.20 and K.21 lightning surge tests (basic level). For values of R1 see **Table 28**.

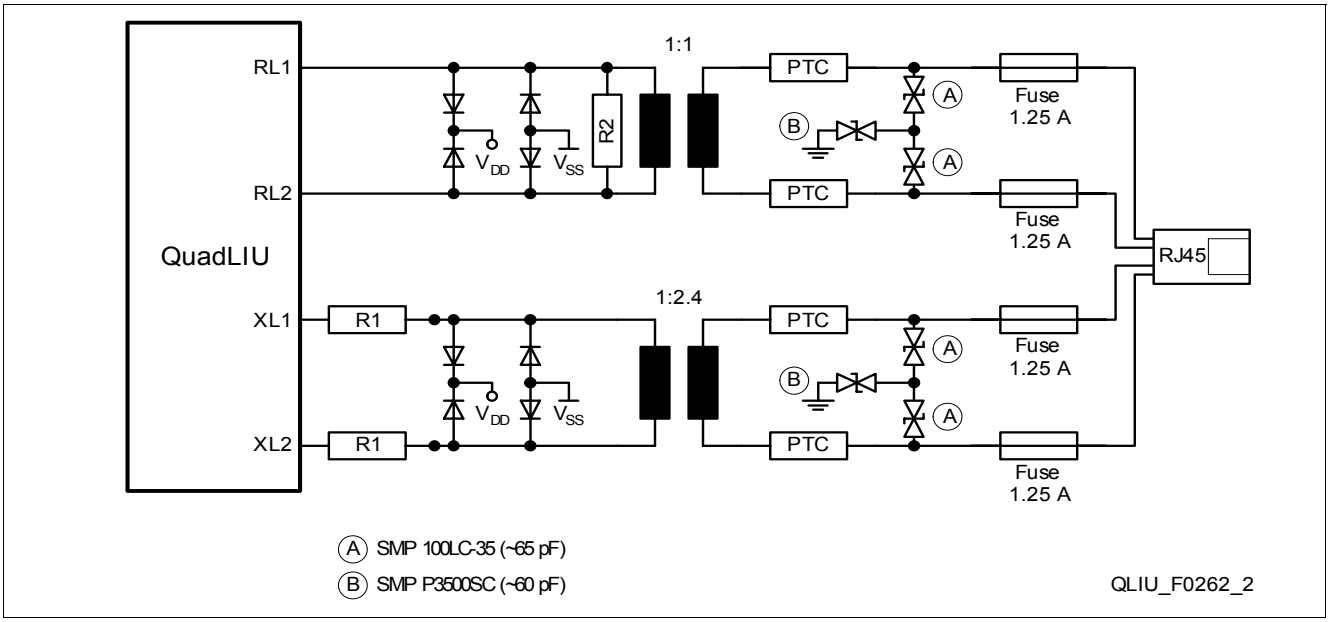



**Figure 68 Protection Circuitry Examples (shown for one channel)**

## 8.2 Application Notes

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the internet page:

**http://www.infineon.com/octalliu**

On the same page you find as well the

- Boundary Scan File for QuadLIU™ Version 2.1 (BSDL File)

## 8.3 Software Support

The following software package is provided together with the QuadLIU™ Reference System EASY 2256:

- E1 and T1 driver functions supporting different ETSI, AT&T and Telcordia (former: Bellcore) requirements
- IBIS model for QuadLIU™ Version 2.1 (according to ANSI/EIA-656)
- “Flexible Master Clock Calculator”, which calculates the required settings for the registers GCM(1:8) depending on the external master clock frequency (MCLK)
- “External Line Front End Calculator”, which provides an easy method to optimize the external components depending on the selected application type.r

The both calculators run under a Win9x/NT environment. Calculation results are traced an can be stored in a file or printed out for documentation.

Screen shots of both programs are shown in **Figure 69** and **Figure 70** below.


**Figure 69 Screen Shot of the “Master Clock Frequency Calculator”**

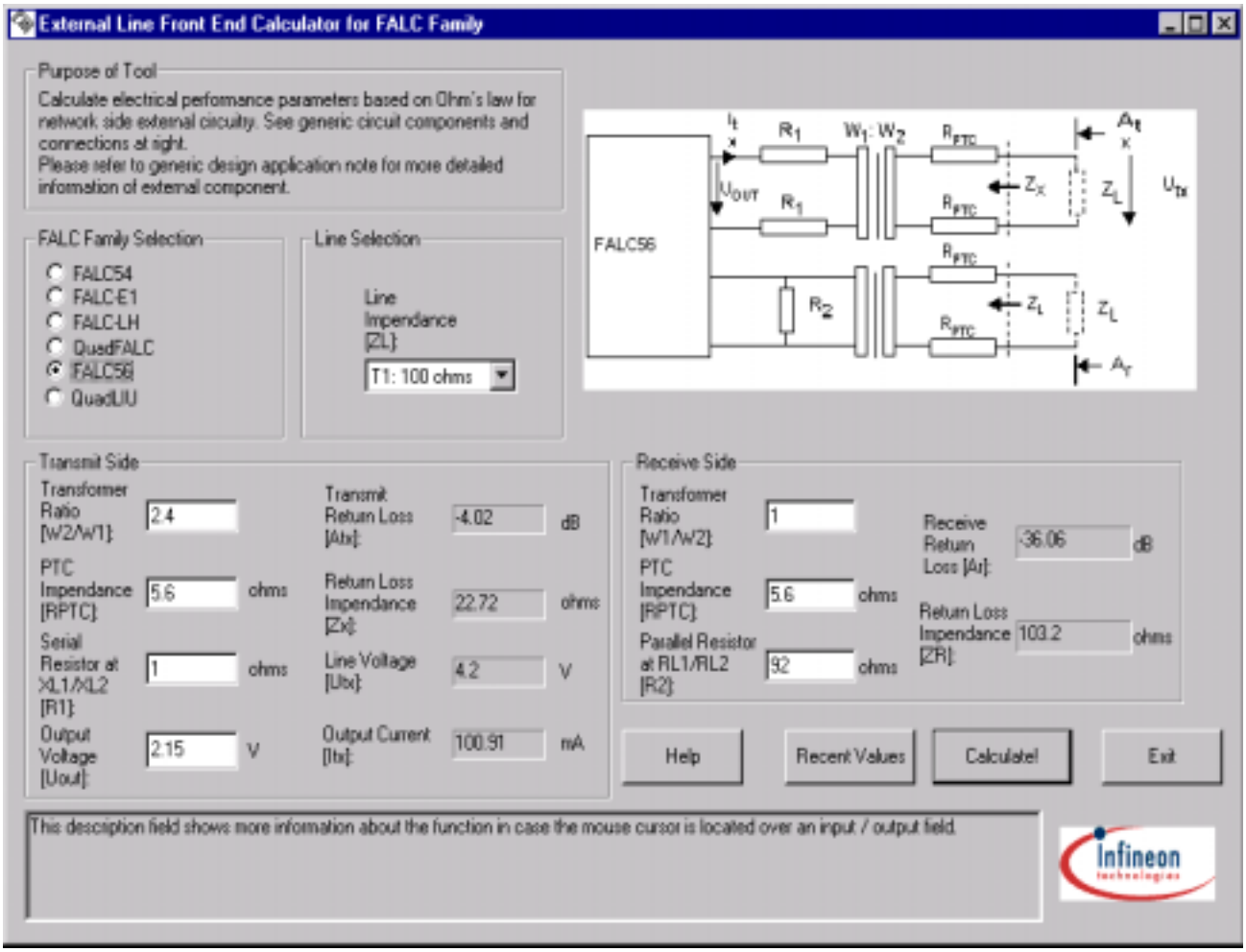



**Figure 70 Screen Shot of the "External Line Frontend Calculator"**

# Terminology

| | |
|---|---|
| **A** | |
| A/D | Analog to digital |
| ADC | Analog to Digital Converter |
| AIS | Alarm Indication Signal (blue alarm) |
| AGC | Automatic Gain Control |
| ALOS | Analog Loss Of Signal |
| AMI | Alternate Mark Inversion |
| ANSI | American National Standards Institute |
| ATM | Asynchronous Transfer Mode |
| AUXP | AUXiliary Pattern |
| **B** | |
| B8ZS | Binary 8 Zero Supression (Line coding to avoid too long strings of consecutive "0") |
| Bellcore | Bell Communications Research |
| BPV | BiPolar Violation |
| BSN | Backward Sequence Number |
| **C** | |
| CDR | Clock and Data Recovery |
| CIS | Channel Interrupt Status |
| CMI | Coded Mark Inversion code (also known as 1T2B code) |
| **D** | |
| D/A | Digital to Analog |
| DAC | Digital to Analog Converter |
| DCIM | Digital Clock Interface Mode |
| DCO | Digitally Controlled Oscillator |
| DCO-R | DCO of receiver |
| DCO-X | DCO of transmitter |
| DL | Digital Loop |
| DPLL | Digitally controlled Phase Locked Loop |
| DS1 | Digital Signal level 1 |
| **E** | |
| ESD | ElectroStatic Discharge |
| EASY | Evaluation system for FALC and LIU products |
| EQ | EQualizer |
| ETSI | European Telecommunication Standards Institute |
| **F** | |
| FALC® | Framing And Line interface Component |
| FCC | US Federal Communication Commission |
| FCS | Frame Check Sequence (used in PPR) |
| **G** | |

| | |
|---|---|
| GIS | Global Interrupt Status |
| **H** | |
| HBM | Human body model for ESD classification |
| HDB3 | High density bipolar of order 3 |
| **I** | |
| IBIS | I/O buffer information specification (ANSI/EIA-656) |
| IBL | In Band Loop |
| ISDN | Integrated Services Digital Network |
| ITU | International Telecommunications Group |
| **J** | |
| JATT | Jitter ATTenuator |
| JTAG | Joined Test Action Group |
| **L** | |
| LBO | Line Build Out |
| LCV | Line Code Violation |
| LIU | Line Interface Unit |
| LL | Local Loop |
| LLB | Line Loop Back |
| LOS | Loss of Signal (red alarm) |
| LSB | Least Significant Bit |
| **M** | |
| MFP | Multi Function Port |
| MSB | Most Significant Bit |
| MUX | MUltipleXer |
| **N** | |
| NRZ | Non Return to Zero signal |
| **P** | |
| PCM | Pulse Code Modulation |
| PD | Pull Down resistor |
| PDV | Pulse Density Violation |
| PLB | Payload Loop Back |
| PLL | Phase Locked Loop |
| PMQFP | Plastic Metric Quad Flat Pack (device package) |
| PRBS | Pseudo Random Binary Sequence |
| PTQFP | Plastic Thin Metric Quad Flat Pack (device package) |
| PU | Pull Up resistor |
| **R** | |
| RAI | Remote Alarm Indication (yellow alarm) |
| RAM | Random Access Memory |
| RDI | Remote Defect Indication |
| RL | Remote Loop |
| RLM | Receive Line Monitoring |
| ROM | Read-Only Memory |

| | |
|---|---|
| RX | Receiver |
| **S** | |
| SAPI | Service Access Point Identifier (special octet in PPR) |
| SCI | Serial ControlInterface |
| SPI | Serial Peripheral Interface |
| Sidactor | Overvoltage protection device for transmission lines |
| **T** | |
| TAP | Test Access Port |
| TEI | Terminal Endpoint Identifier (special octet in PPR) |
| TX | Transmitter |
| **U** | |
| UI | Unit Interval |
| **Z** | |
| ZCS | Zero Code Suppression |

www.infineon.com

Published by Infineon Technologies AG