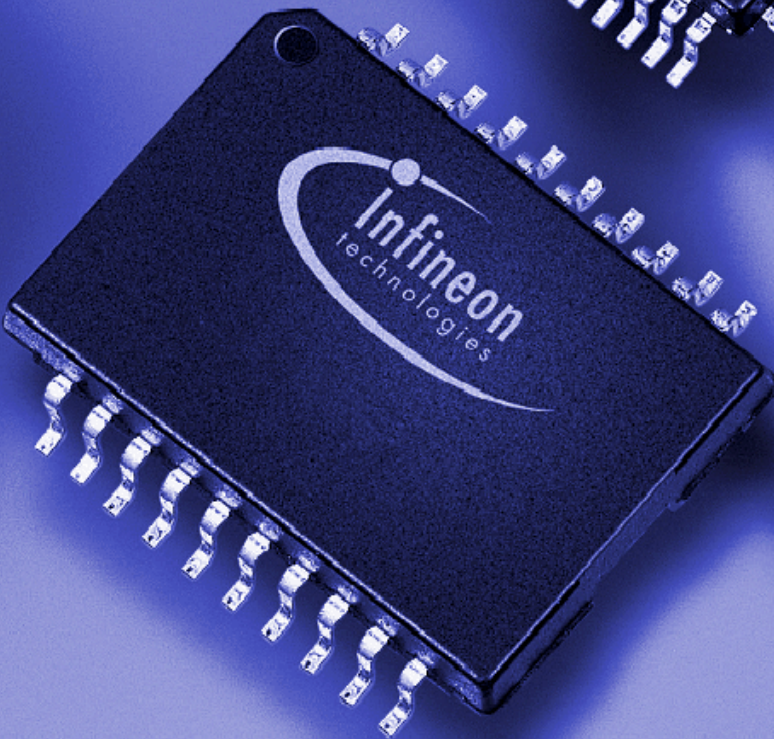


SLICOFI-2/-2S/-2S2

Dual Channel Subscriber Line
Interface Codec Filter

PEB 3265 Version 1.3

PEB 3264/-2 Version 1.3



Wired Communications



Never stop thinking.

Edition 2000-11-09

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SLICOFI-2/-2S/-2S2

Dual Channel Subscriber Line
Interface Codec Filter

PEB 3265 Version 1.3

PEB 3264/-2 Version 1.3

Preliminary

Wired Communications



Never stop thinking.

SLICOFI-2/-2S/-2S2**Preliminary****Revision History:** **2000-11-09**DS2

Previous Version: Data Sheet DS1

Page	Subjects (major changes since last revision)
all	PEB 3264, PEB 3264-2 and PEB 3265 versions changed from 1.2 to 1.3
Page 7	Pin Definitions: Description for pins IO1B, IO2B, IO1A, IO2A and SELCLK changed.
Page 11	Chapter 3.1 "Functional Overview" completely overworked.
Page 18	Table 4 "Operating Modes for <i>SLICOFI-2x</i> and SLIC": modes and footnotes added.
Page 22	Table 9 "SLIC-P Interface Code": footnote modified. Table 10 "SLIC-P Modes": modes added.
Page 24	Chapter 5 "Signal Path and Test Loops": new pictures
Page 31	Chapter 6.1.4 "Power Dissipation SLICOFI-2": max. limit values added.
Page 32	Chapter 6.1.5 "Power Dissipation SLICOFI-2S/-2S2": max. limit values added.
Page 34	Chapter 6.1.7 "Miscellaneous Characteristics": Comparator thresholds description changes
Page 41	Chapter 6.2.2 "Group Delay": description modified.
Page 43	Chapter " Input/Output Waveform for AC Tests " on Page 43 added.
Page 45	PCM interface timings " Single-Clocking Mode " on Page 45 and " Double-Clocking Mode " on Page 46 : FSC hold time (t_{FSC_h}) renamed to FSC hold time 1 (t_{FSC_h1}), FSC hold time 2 (t_{FSC_h2}) added, formula of max. value for TCA/B delay time off (t_{dTCoff}) modified
Page 49	IOM-2 interface timings " Single-Clocking Mode " on Page 49 and " Double-Clocking Mode " on Page 50 : FSC hold time (t_{FSC_h}) renamed to FSC hold time 1 (t_{FSC_h1}), FSC hold time 2 (t_{FSC_h2}) added, parameters and timing of pin DU modified
Page 52	Chapter 8.1 "List of Abbreviations" updated.

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Table of Contents		Page
1	Overview	2
1.1	Features SLICOFI-2	3
1.2	Features SLICOFI-2S/-2S2	4
1.3	Logic Symbol	5
2	Pin Descriptions	6
2.1	Pin Diagram	6
3	Functional Description	11
3.1	Functional Overview	11
3.1.1	Basic Functions available for all <i>SLICOFI-2x</i> Codecs	11
3.1.2	Additional Functions available for the SLICOFI-2 Codec	12
3.2	Block Diagrams	14
3.2.1	DTMF Generation	15
3.2.2	DTMF Detection (SLICOFI-2 only)	15
3.2.3	Caller ID Generation (SLICOFI-2 only)	17
3.2.4	Line Echo Cancelling (LEC) (SLICOFI-2 only)	17
4	Operating Modes for the DuSLIC Chip Set	18
4.1	SLICOFI-2S/-2S2 and SLIC-S/-S2 Interface	20
4.2	SLICOFI-2 and SLIC-E/-E2 Interface	21
4.3	SLICOFI-2 and SLIC-P Interface	22
5	Signal Path and Test Loops	24
5.1	Test Loops SLICOFI-2	24
5.2	Test Loops SLICOFI-2S/-2S2	26
6	Electrical Characteristics	29
6.1	Electrical Characteristics PEB 3264/PEB 3264-2/PEB 3265	29
6.1.1	Absolute Maximum Ratings	29
6.1.2	Power Up Sequence for Supply Voltages	30
6.1.3	Operating Range	30
6.1.4	Power Dissipation SLICOFI-2	31
6.1.5	Power Dissipation SLICOFI-2S/-2S2	32
6.1.6	Digital Interface	33
6.1.7	Miscellaneous Characteristics	34
6.2	AC Transmission SLICOFI-2/-2S/-2S2	35
6.2.1	Gain Tracking (Receive or Transmit)	40
6.2.2	Group Delay	41
6.3	DC Characteristics	42
6.4	SLICOFI-2/-2S/-2S2 Timing Characteristics	43
6.4.1	Input/Output Waveform for AC Tests	43
6.4.2	MCLK/FSC Timing	44
6.4.3	PCM Interface Timing	45

Table of Contents		Page
6.4.3.1	Single-Clocking Mode	45
6.4.3.2	Double-Clocking Mode	46
6.4.4	Microcontroller Interface Timing	48
6.4.5	IOM-2 Interface Timing	49
6.4.5.1	Single-Clocking Mode	49
6.4.5.2	Double-Clocking Mode	50
7	Package Outlines	51
8	Glossary	52
8.1	List of Abbreviations	52
9	Index	54

List of Figures
Page

Figure 1	Logic Symbol SLICOFI-2/-2S/-2S2	5
Figure 2	Pin Configuration SLICOFI-2/-2S/-2S2 (top view)	6
Figure 3	Line Circuit Functions included in the SLICOFI-2S/-2S2	13
Figure 4	Line Circuit Functions included in the SLICOFI-2	13
Figure 5	Block Diagram SLICOFI-2/-2S/-2S2 (PEB 3265, PEB 3264/-2)	14
Figure 6	AC Test Loops SLICOFI-2	24
Figure 7	DC Test Loops SLICOFI-2	25
Figure 8	AC Test Loops SLICOFI-2S	26
Figure 9	AC Test Loops SLICOFI-2S2	27
Figure 10	DC Test Loops SLICOFI-2S/-2S2	28
Figure 11	Hysteresis for Input Pins	34
Figure 12	Overload Compression A/D	39
Figure 13	Insertion Loss.	39
Figure 14	Gain Tracking Receive.	40
Figure 15	Gain Tracking Transmit	40
Figure 16	Group Delay Distortion Receive and Transmit.	41
Figure 17	Insertion Loss.	42
Figure 18	Waveform for AC Tests	43
Figure 19	MCLK / FSC-Timing	44
Figure 20	PCM Interface Timing - Single-Clocking Mode	45
Figure 21	PCM Interface Timing – Double-Clocking Mode	46
Figure 22	Microcontroller Interface Timing.	48
Figure 23	IOM-2 Interface Timing – Single-Clocking Mode	49
Figure 24	IOM-2 Interface Timing – Double-Clocking Mode	50
Figure 25	PEB 3265, PEB 3264, PEB 3264-2 (SLICOFI-2x).	51

Preliminary

Preface

Synonyms

To simplify matters, the following synonyms are used:

<i>SLICOFI-2x</i>	Synonym used for all codec versions SLICOFI-2/-2S/-2S2
SLIC:	Synonym used for all SLIC versions SLIC-S, SLIC-S2, SLIC-E, SLIC-E2 and SLIC-P

Organization of this Document

This Data Sheet is divided into nine chapters. It is organized as follows:

- Chapter 1, Overview
A general description of the product, a list of its key features.
- Chapter 2, Pin Descriptions
- Chapter 3, Functional Description
The main functions are presented following a functional block diagram.
- Chapter 4, Operational Description
A brief description of the three operating modes: power down, active and ringing (plus signal monitoring techniques).
- Chapter 5, Interfaces
Connection information.
- Chapter 6, Electrical Characteristics
Parameters, symbols and limit values.
- Chapter 7, Package Outlines
Illustrations and dimensions of the package outlines.
- Chapter 8, Glossary
List of abbreviations and description of symbols.
- Chapter 9, Index

1 Overview

The Subscriber Line Interface Circuit *SLICOFI-2x* is a highly flexible two channel codec solution for analog line circuits. The *SLICOFI-2x* is programmable via software and can be adapted to all different standards worldwide.

DuSLIC Architecture

The SLICOFI-2 (PEB 3265) and SLICOFI-2S/-2S2 (PEB 3264/-2) chips are part of the DuSLIC chip set and are designed for use with the SLIC-E/-E2/-P (PEB 4265/-2, PEB 4266) and SLIC-S/-S2 (PEB 4264/-2) devices. For an overview about available DuSLIC versions see the DuSLIC Chip Set Selection Guide.

The DuSLIC design splits the traditional SLIC functions to high- and low-voltage functions. The low-voltage functions are handled in the *SLICOFI-2x* device, the high-voltage functions are handled in the SLIC devices.

All *SLICOFI-2x* codec devices are manufactured in an advanced 0.35 μm 3.3 V CMOS process.

For further information see [Chapter 3.1](#).

Preliminary

Dual Channel Subscriber Line Interface Codec Filter SLICOFI-2x

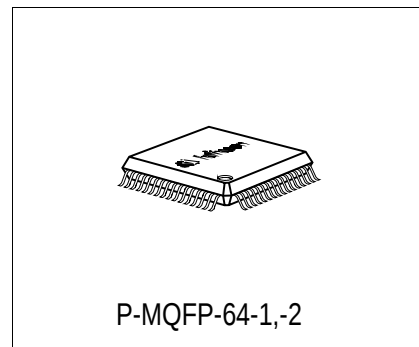
PEB 3265
PEB 3264
PEB 3264-2

Version 1.3

CMOS

1.1 Features SLICOFI-2¹⁾

- Fully programmable dual-channel codec
- Programmable battery feeding with capability for driving long loops
- Internal balanced/unbalanced ringing capability (up to 85 Vrms balanced / 50 Vrms unbalanced)
- External ringing support
- Ground/loop start signaling
- Polarity reversal
- On-hook transmission
- Programmable Teletax (TTX) generation
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (FSK) generator
- Integrated fax/modem detection (Universal Tone Detection UTD)
- Integrated Line Echo Cancellation unit (LEC)
- Optimized filter structure for modem transmission
- Message waiting lamp support (for PBX applications)
- Three-party conferencing (in PCM/ μ C mode)
- 8 and 16 kHz PCM Transmission
- IOM-2 or PCM/ μ C-interface selectable
- Power optimized architecture
- Power management capability (battery switching)
- Integrated test and diagnosis functions
- Specification in accordance with ITU-T Recommendation Q.552 for interface Z, ITU-T Recommendation G.712 and applicable LSSGR



¹⁾ Features are indicated for the DuSLIC chip set and are partially realized by the SLICOFI-2 codec.

Type	Package
PEB 3265, PEB 3264, PEB 3264-2	P-MQFP-64-1

1.2 Features SLICOFI-2S/-2S2¹⁾

- Fully programmable dual-channel codec
- Programmable battery feed with capability for driving long loops
- Internal balanced ringing capability up to 45 Vrms
- External ringing support
- Ground/loop start signaling
- Polarity reversal
- On-hook transmission
- Programmable Teletax (TTX) generation (not available with SLICOFI-2S2)
- Integrated DTMF generator
- 8 and 16 kHz PCM Transmission
- IOM-2 or PCM/μC-interface selectable
- Power optimized architecture
- Power management capability (battery switching)
- Specification in accordance with
ITU-T Recommendation Q.552 for interface Z, ITU-T Recommendation G.712 and
applicable LSSGR

¹⁾ Features are indicated for the DuSLIC chip set and are partially realized by the SLICOFI-2S/-2S2 codec.

1.3 Logic Symbol

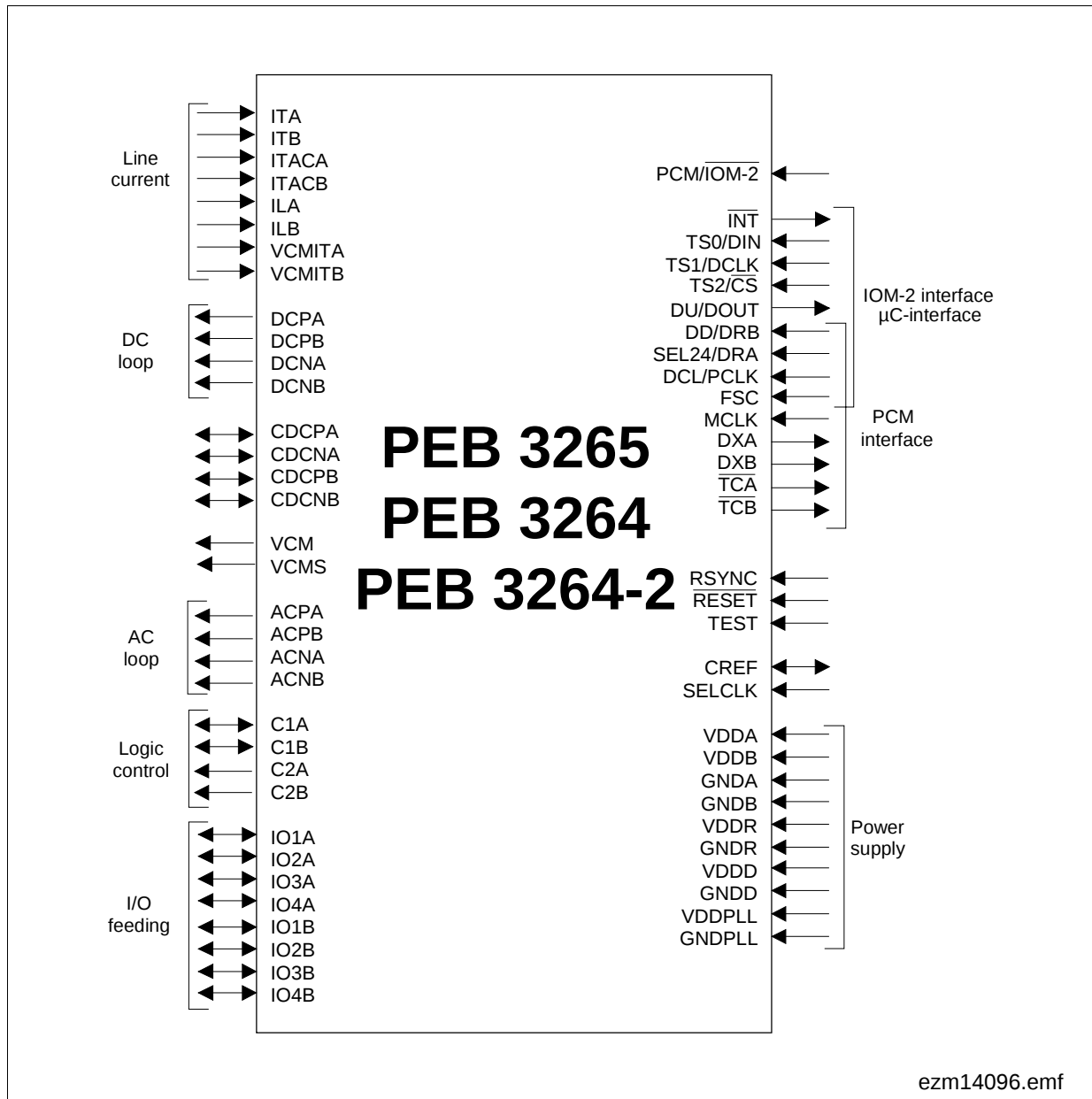


Figure 1 Logic Symbol SLICOFI-2/-2S/-2S2

2 Pin Descriptions

2.1 Pin Diagram

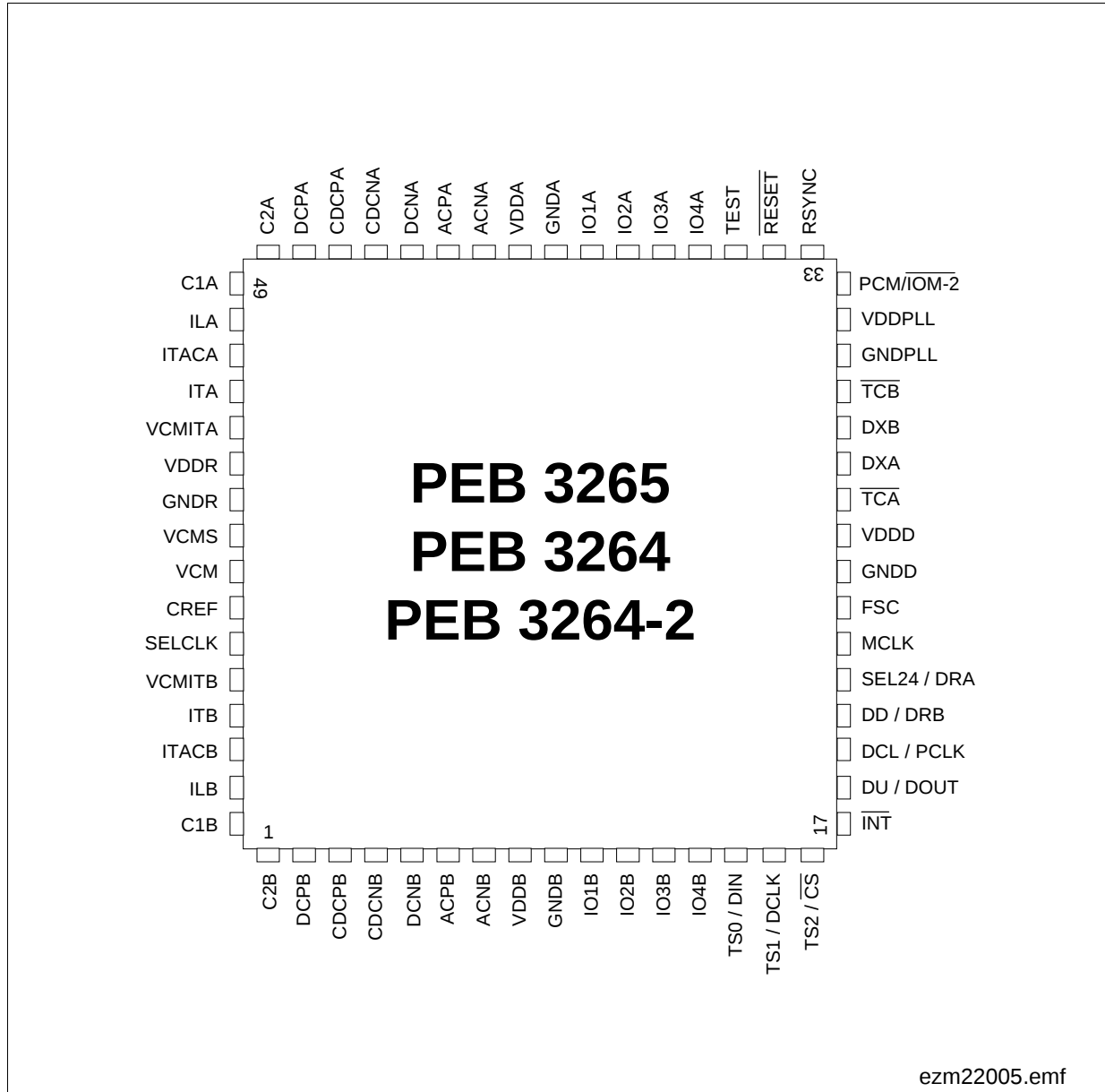


Figure 2 Pin Configuration SLICOFI-2/-2S/-2S2 (top view)

Preliminary

Pin Descriptions

Table 1 Pin Definitions and Functions SLICOFI-2/-2S/-2S2

Pin No.	Sym-bol	Input (I) Output (O)	Function
1	C2B	O	Ternary logic output for controlling the SLIC operation mode (channel B)
2	DCPB	O	Two-wire output voltage (DCP) (channel B)
3	CDCPB	I/O	External capacitance for filtering (channel B)
4	CDCNB	I/O	External capacitance for filtering (channel B)
5	DCNB	O	Two-wire output voltage (DCN) (channel B)
6	ACPB	O	Differential two-wire AC output voltage controlling the RING pin (channel B)
7	ACNB	O	Differential two-wire AC output voltage controlling the TIP pin (channel B)
8	VDDB	Power	+ 3.3 V analog supply voltage (channel B)
9	GNDB	Power	Analog ground (channel B)
10	IO1B	I/O	User-programmable I/O pin (channel B) with relay-driving capability. In external ringing mode IO1 is used to automatically control and drive the ring relay.
11	IO2B	I/O	User-programmable I/O pin (channel B) with relay-driving capability. SLICOFI-2 and SLIC-P: connected to pin C3 of SLIC-P, when two supply voltages for voice transmission and internal ringing are used. ¹⁾
12	IO3B	I/O	User-programmable I/O pin (channel B) with analog input functionality
13	IO4B	I/O	User-programmable I/O pin (channel B) with analog input functionality
14	TS0 DIN	I I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Time slot selection pin 0 PCM/ $\overline{\text{IOM-2}}$ = 1 (μC interface): Data in
15	TS1 DCLK	I I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Time slot selection pin 1 PCM/ $\overline{\text{IOM-2}}$ = 1 (μC interface): Data clock
16	TS2 $\overline{\text{CS}}$	I I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Time slot selection Pin 2 PCM/ $\overline{\text{IOM-2}}$ = 1 (μC interface): Chip select, low active
17	$\overline{\text{INT}}$	O	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): not connected PCM/ $\overline{\text{IOM-2}}$ = 1 (μC interface): Interrupt pin, low active

Preliminary
Pin Descriptions
Table 1 Pin Definitions and Functions SLICOFI-2I-2SI-2S2 (cont'd)

Pin No.	Sym-bol	Input (I) Output (O)	Function
18	DU	O	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Data upstream, open drain
	DOUT	O	PCM/ $\overline{\text{IOM-2}}$ = 1 (μC interface): Data out, push/pull
19	DCL	I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Data clock
	PCLK	I	PCM/ $\overline{\text{IOM-2}}$ = 1 (PCM interface): 128 kHz to 8192 kHz PCM clock
20	DD	I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): Data downstream
	DRB	I	PCM/ $\overline{\text{IOM-2}}$ = 1 (PCM interface): Receive data input for PCM highway B
21	SEL24	I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): SEL24 = 0: DCL = 2048 kHz selected SEL24 = 1: DCL = 4096 kHz selected
	DRA	I	PCM/ $\overline{\text{IOM-2}}$ = 1 (PCM-interface): Receive Data input for PCM-highway A
22	MCLK	I	PCM/ $\overline{\text{IOM-2}}$ = 0 (IOM-2 interface): not connected
			PCM/ $\overline{\text{IOM-2}}$ = 1 (PCM interface): master clock when PCM/ μC interface is used, clock rates are 512 kHz, 1536 kHz, 2048 kHz, 4096 kHz, 7168 kHz, 8192 kHz
23	FSC	I	Frame synchronization clock for PCM/ μC or IOM-2 interface, 8 kHz, identifies the beginning of the frame, individual time slots are referenced to this input signal.
24	GNDD	Power	Digital ground
25	VDDD	Power	+ 3.3 V digital supply voltage
26	$\overline{\text{TCA}}$	O	Transmit control output for PCM highway A, active low during transmission, open drain
27	DXA	O	Transmit data output for PCM highway A (goes tristate when inactive)
28	DXB	O	Transmit data output for PCM highway B (goes tristate when inactive)
29	$\overline{\text{TCB}}$	O	Transmit control output for PCM highway B, active low during transmission, open drain
30	GNDPLL	Power	Digital ground PLL
31	VDDPLL	Power	+ 3.3 V supply voltage PLL

Preliminary
Pin Descriptions
Table 1 Pin Definitions and Functions SLICOFI-2/-2S/-2S2 (cont'd)

Pin No.	Sym-bol	Input (I) Output (O)	Function
32	PCM/ IOM-2	I	PCM/IOM-2 = 1: PCM/μC interface selected PCM/IOM-2 = 0: IOM-2 interface selected
33	RSYNC	I	External ringing synchronization pin
34	RESET	I	Reset pin, low active
35	TEST	I	Testpin for production test, has to be connected to GNDD
36	IO4A	I/O	User-programmable I/O Pin (channel A) with analog input functionality
37	IO3A	I/O	User-programmable I/O Pin (channel A) with analog input functionality
38	IO2A	I/O	User-programmable I/O Pin (channel A) with relay-driving capability. SLICOFI-2 and SLIC-P: connected to pin C3 of SLIC-P, when two supply voltages for voice transmission and internal ringing are used. ¹⁾
39	IO1A	I/O	User-programmable I/O Pin (channel A) with relay-driving capability. In external ringing mode IO1 is used to automatically control and drive the ring relay.
40	GNDA	Power	Analog ground (channel A)
41	VDDA	Power	+ 3.3 V analog supply voltage (channel A)
42	ACNA	O	Differential two-wire AC output voltage controlling the TIP pin (channel A)
43	ACPA	O	Differential two-wire AC output voltage controlling the RING pin (channel A)
44	DCNA	O	Two-wire output voltage (DCN) (channel A)
45	CDCNA	I/O	External capacitance for filtering (channel A)
46	CDCPA	I/O	External capacitance for filtering (channel A)
47	DCPA	O	Two-wire output voltage (DCP) (channel A)
48	C2A	O	Ternary logic output for controlling the SLIC operation mode (channel A)
49	C1A	I/O	Ternary logic output, controlling the SLIC operation mode (channel A); indicating thermal overload of SLIC if a current of typically 150 μA is drawn out
50	ILA	I	Longitudinal current input (channel A)
51	ITACA	I	Transversal current input (AC) (channel A)

Preliminary
Pin Descriptions
Table 1 Pin Definitions and Functions SLICOFI-2/-2S/-2S2 (cont'd)

Pin No.	Sym-bol	Input (I) Output (O)	Function
52	ITA	I	Transversal current input (AC + DC) (channel A)
53	VCMITA	I	Reference pin for trans./long. current sensing (channel A)
54	VDDR	Power	+ 3.3 V analog supply voltage (bias)
55	GNDR	Power	Analog ground (bias)
56	VCMS	O	Reference voltage for differential two-wire interface, typical 1.5 V
57	VCM	O	Reference voltage for input pins IT, IL, ITAC
58	CREF	I/O	An external capacitor of 68 nF has to be connected to GNDR
59	SELCLK	I	Master clock select. Should be set to GND (internal master clock generation). For test purposes, external master clock generation can be selected (SELCLK = 1). In this case a clock of nominal 32.768 Mhz with a jitter time of less than 1 ns has to be applied to the MCLK pin.
60	VCMITB	I	Reference pin for transversal/longitudinal current sensing (channel B)
61	ITB	I	Transversal current input (AC + DC) (channel B)
62	ITACB	I	Transversal current input (AC) (channel B)
63	ILB	I	Longitudinal current input (channel B)
64	C1B	I/O	Ternary logic output, controlling the SLIC operation mode (channel B); indicating thermal overload of SLIC if a current of typically 150 μ A is drawn out

¹⁾ If SLIC-P is selected, IO2 cannot be controlled by the user, but is utilized by the SLICOFI-2 to control the C3 pin of SLIC-P.

3 Functional Description

3.1 Functional Overview

3.1.1 Basic Functions available for all *SLICOFI-2x* Codecs

The functions described in this chapter are integrated in all DuSLIC chip sets (see [Figure 3](#) for SLICOFI-2SI-2S2 and [Figure 4](#) for SLICOFI-2).

All BORSCHT functions are integrated:

- Battery feed
- Overvoltage protection
(realized by the robust high-voltage SLIC technology and additional circuitry)
- Ringing¹⁾
- Signaling (supervision)
- Coding
- Hybrid for 2/4-wire conversion
- Testing

An important feature of the DuSLIC design is the fact that all the SLIC and codec functions are programmable via the IOM-2 or PCM/ μ C-interface of the dual channel *SLICOFI-2x* device:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude¹⁾
- Hook thresholds
- TTX modes²⁾

Because signal processing within the *SLICOFI-2x* is completely digital, it is possible to adapt to the requirements listed above by simply updating the coefficients that control DSP processing of all data. This means, for example, that changing impedance matching or hybrid balance requires no hardware modifications. A single hardware is now capable of meeting the requirements for different markets. The digital nature of the filters and gain stages also assures high reliability, no drifts (over temperature or time) and minimal variations between different lines.

¹⁾ With SLICOFI-2S2 only external ringing is supported

²⁾ Not available with SLICOFI-2S2 codec

Preliminary

Functional Description

The characteristics for the two voice channels within *SLICOFI-2x* can be programmed independently of each other. The DuSLICOS software is provided to automate calculation of coefficients to match different requirements. DuSLICOS also verifies the calculated coefficients.

3.1.2 Additional Functions available for the SLICOFI-2 Codec

The following line circuit functions are integrated only in the SLICOFI-2 (see [Figure 4](#)):

- Teletax metering

For pulse metering, a 12/16 kHz sinusoidal metering burst has to be transmitted. The DuSLIC chip set generates the metering signal internally and has an integrated notch filter.

- DTMF

DuSLIC has an integrated DTMF generator comprising two tone generators and a DTMF decoder. The decoder is able to monitor the transmit or receive path for valid tone pairs and outputs the corresponding digital code for each DTMF tone pair.

- Caller ID Frequency Shift Keying (FSK) Modulator

DuSLIC has an integrated FSK modulator capable of sending Caller ID information. The Caller ID modulator complies with all requirements of ITU-T recommendation V.23 and Bell 202.

- LEC (Line Echo Cancellation)

DuSLIC contains an adaptive line echo cancellation unit for the cancellation of near end echos (up to 8 ms cancelable echo delay time).

- UTD (Universal Tone Detection)

DuSLIC has an integrated Universal Tone Detection unit to detect special tones in the receive or transmit path (e.g. fax or modem tones).

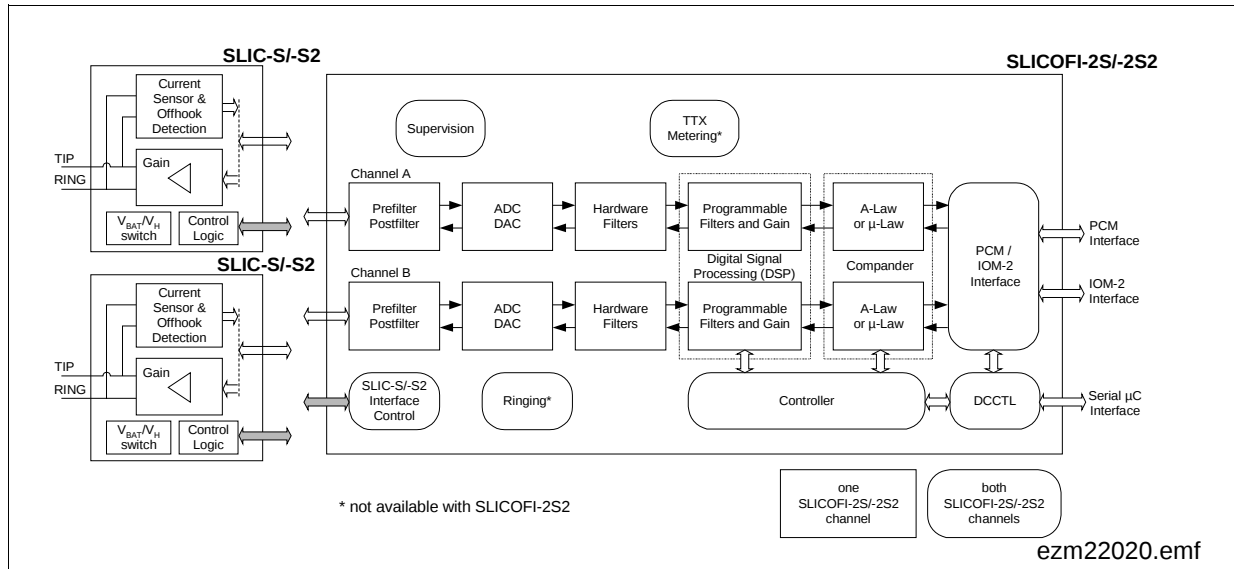


Figure 3 Line Circuit Functions included in the SLICOFI-2SI-2S2

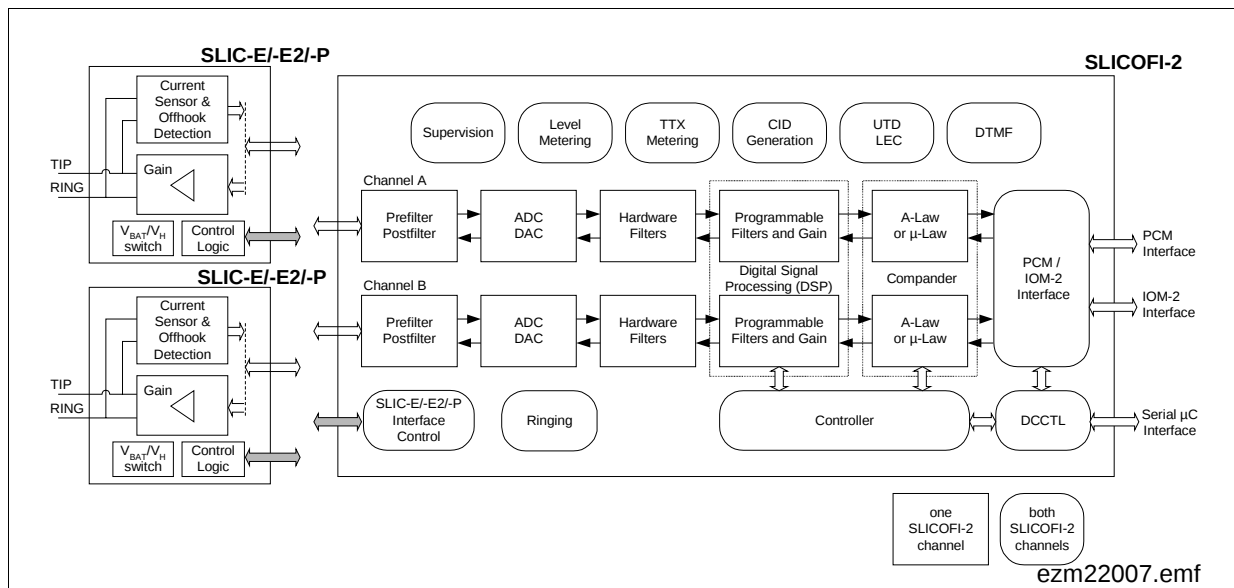


Figure 4 Line Circuit Functions included in the SLICOFI-2

3.2 Block Diagrams

PEB 3265 / PEB 3264 / PEB 3264-2

The diagram illustrates the internal architecture of the PEB 3265 / PEB 3264 / PEB 3264-2. It is organized into two main channels, Channel A and Channel B, which are connected to a central DBUS. Channel A includes components like Supervision, Prefi, ADC, HW-Fi, IMA, DAC, and Pofi. Channel B includes Supervision, Prefi, ADC, HW-Fi, IMA, DAC, and Pofi. Both channels are connected to a central CONTR block, which also interfaces with CRAM, DSP, and IOM-2. The system also includes a PEB 3265 only section with an EDSP block. External interfaces include IOM-2 Interface, PCM / μ C Interface, and various input/output pins like CDCNA, CDCPA, CDCNB, CDCPB, VCM, VCMS, IO1A, IO2A, IO3A, IO4A, IO1B, IO2B, IO3B, IO4B, GNDNA, GNDNB, GNDNR, GNDPL, VDDA, VDDNB, VDDR, VDDPL, CREF, and RESET.

PEB 3265 / PEB 3264 / PEB 3264-2

Top pins: CDCNA CDCPA CDCNB CDCPB VCM VCMS IO1A IO2A IO3A IO4A IO1B IO2B IO3B IO4B

Left pins: ILA ITA ITACA VCMITA ACNA ACPA DCNA DCPA C1A C2A ILB ITB ITACB VCMITB ACNB ACPB DCNB DCPB C1B C2B

Bottom pins: GNDNA GNDNB GNDNR GNDPL VDDA VDDNB VDDR VDDPL CREF RESET

Internal components and connections:

- Channel A:** Supervision, Prefi, ADC, HW-Fi, IMA, DAC, Pofi, HV Interf.
- Channel B:** Supervision, Prefi, ADC, HW-Fi, IMA, DAC, Pofi, HV Interf.
- Central Block:** CONTR, CRAM, DSP, IOM-2, PCM, μ C.
- PEB 3265 only:** EDSP.
- Interfacing:** IOM-2 Interface, PCM / μ C Interface.
- DBUS:** Central data bus connecting the channels and central block.

Right side labels: IOM-2 Interface, or, PCM / μ C Interface.

Bottom right: ezm22021.emf

Figure 5 **Block Diagram SLICOFI-2/-2S/-2S2 (PEB 3265, PEB 3264/-2)**

¹⁾ The add-on functions are DTMF detection, Caller ID generation, Message Waiting lamp support, Three-party Conferencing, Universal Tone Detection (UTD), Line Echo Cancellation (LEC) and Sleep Mode.

Preliminary

Functional Description

3.2.1 DTMF Generation

The *SLICOFI-2x* offers programmable DTMF generation for both channels by using the internal tone generators.

3.2.2 DTMF Detection (SLICOFI-2 only)

Both channels (A and B) of the SLICOFI-2 device have a powerful built-in DTMF decoder that will meet most national requirements. The receiver algorithm performance meets the quality criteria for central office/exchange applications. It complies among others with the requirements of ITU-T Q.24, Bellcore GR-30-CORE (TR-NWT-000506) and Deutsche Telekom network (BAPT 223 ZV 5, Approval Specification of the Federal Office for Post and Telecommunications, Germany).

The performance of the algorithm can be adapted according to the needs of the application via the digital interface (detection level, twist, bandwidth and center frequency of the notch filter).

Table 2 shows the performance characteristics of the DTMF decoder algorithm:

Table 2 Performance Characteristics of the DTMF Decoder Algorithm

	Characteristic	Value	Notes
1	Valid input signal detection level	– 48 to 0 dBm0	Programmable
2	Input signal rejection level	– 5 dB of valid signal detection level	–
3	Positive twist accept	< 8 dB	Programmable
4	Negative twist accept	< 8 dB	Programmable
5	Frequency deviation accept	< $\pm (1.5\% + 4 \text{ Hz})$ and < $\pm 1.8\%$	Related to center frequency
6	Frequency deviation reject	> $\pm 3\%$	Related to center frequency
7	DTMF noise tolerance (could be the same as 14)	– 12 dB	dB referenced to lowest amplitude tone
8	Minimum tone accept duration	40 ms	–
9	Maximum tone reject duration	25 ms	–
10	Signaling velocity	$\geq 93 \text{ ms/digit}$	–
11	Minimum inter-digit pause duration	40 ms	–
12	Maximum tone drop-out duration	20 ms	–

Preliminary

Functional Description

Table 2 Performance Characteristics of the DTMF Decoder Algorithm (cont'd)

	Characteristic	Value	Notes
13	Interference rejection 30 Hz to 480 Hz for valid DTMF recognition	Level in frequency range 30 Hz ... 480 Hz $\leq$ level of DTMF frequency + 22 dB	dB referenced to lowest amplitude tone
14	Gaussian noise influence Signal level – 22 dBm0, SNR = 23 dB	Error rate better than 1 in 10000	–
15	Pulse noise influence Impulse noise tape 201	Error rate better than 14 in 10000	–

In the event of pauses < 20 ms:

- If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
- If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, this is interpreted as two different numbers.

DTMF decoders can be switched on or off individually to reduce power consumption. In normal operation, the decoder monitors the Tip and Ring wires via the ITAC pins (transmit path). Alternatively the decoder can be switched also in the receive path. On detecting a valid DTMF tone pair, SLICOFI-2 generates an interrupt via the appropriate INT pin and indicates a change of status. The DTMF code information is provided by a register which is read via the digital interface.

The DTMF decoder also has excellent speech-rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been fully tested with the speech sample sequences in the Series-1 Digit Simulation Test Tapes for DTMF decoders from Bellcore.

3.2.3 Caller ID Generation (SLICOFI-2 only)

The SLICOFI-2 contains a FSK generation unit for sending Caller ID information.

SLICOFI-2 FSK Generation

Different countries use different standards to send Caller ID information. The SLICOFI-2 chip is compatible with the widely used standards Bellcore GR-30-CORE, British Telecom (BT) SIN227, SIN242 or the UK Cable Communications Association (CCA) specification TW/P&E/312. Continuous phase binary frequency shift keying (FSK) modulation is used for coding which is compatible with BELL 202 (see [Table 3](#)) and ITU-T V.23, the most common standards. The SLICOFI-2 can be easily adapted to these requirements by programming via the microcontroller interface. Coefficient sets are provided for the most common standards.

Table 3 FSK Modulation Characteristics

Characteristic	ITU-T V.23	Bell 202
Mark (Logic 1)	1300 ± 3 Hz	1200 ± 3 Hz
Space (Logic 0)	2100 ± 3 Hz	2200 ± 3 Hz
Modulation	FSK	
Transmission rate	1200 ± 6 baud	
Data format	Serial binary asynchronous	

3.2.4 Line Echo Cancelling (LEC) (SLICOFI-2 only)

The SLICOFI-2 line echo canceller is compatible with applicable standards ITU-T G.165 and G.168. An echo cancellation delay time of up to 8 ms can be programmed (for restrictions see chapter “MIPS requirements for EDSP Capabilities” in the DuSLIC Data Sheet).

4 Operating Modes for the DuSLIC Chip Set

Table 4 Operating Modes for *SLICOFI-2x* and SLICS

<i>SLICOFI-2x</i> Mode	SLIC Type			CIDD/ CIOP ¹⁾			Additional Bits used (Note ²⁾)
	SLIC-S/ SLIC-S2	SLIC-E/ SLIC-E2	SLIC-P	M2	M1	M0	
Sleep (SL)	–	PDRH	PDRH	1	1	1	SLEEP-EN = 1
			PDRR	1	1	1	SLEEP-EN = 1, ACTR = 1
Power Down Resistive (PDR)	PDRH	PDRH	PDRH	1	1	1	SLEEP-EN = 0
			PDRR	1	1	1	SLEEP-EN = 0, ACTR = 1
Power Down High Impedance (PDH)	PDH	PDH	PDH	0	0	0	–
Active High (ACTH)	ACTH	ACTH	ACTH	0	1	0	–
Active Low (ACTL)	ACTL	ACTL	ACTL	0	1	0	ACTL = 1
Active Ring (ACTR)	ACTR	ACTR	ACTR	0	1	0	ACTR = 1
Ringing (Ring)	ACTR ³⁾	ACTR	ACTR	1	0	1	–
	–	–	ROT	1	0	1	HIT = 1
	–	–	ROR	1	0	1	HIR = 1
Active with HIT	HIT	HIT		0	1	0	HIT = 1
			HIT	0	1	0	HIT = 1, ACTR = 0
Active with HIR	HIR	HIR		0	1	0	HIR = 0
			HIR	0	1	0	HIR = 0, ACTR = 0
Active with Ring to Ground			ROT	0	1	0	HIT = 1, ACTR = 1
Active with Tip to Ground			ROR	0	1	0	HIR = 1, ACTR = 1
HIRT	–	HIRT	HIRT	0	1	0	HIR = 1, HIT = 1
Active with Metering	ACTx ³⁾ ⁴⁾	ACTx ⁴⁾	ACTx ⁴⁾	1	1	0	TTX-DIS to select Reverse Polarity or TTX Metering

Preliminary
Operating Modes for the DuSLIC Chip Set
Table 4 Operating Modes for *SLICOFI-2x* and *SLICS* (cont'd)

<i>SLICOFI-2x</i> Mode	SLIC Type			CIDD/ CIOP¹⁾			Additional Bits used (Note ²⁾)
	SLIC-S/ SLIC-S2	SLIC-E/ SLIC-E2	SLIC-P	M2	M1	M0	
Ground Start	HIT	HIT	HIT	1 1	0 0	0 0	– ACTR = 0
Ring Pause	ACTR ³⁾	ACTR	ACTR ROR ROT	0	0	1	HIR = 1 HIT = 1

¹⁾ CIDD = Data Downstream Command/Indication Channel Byte (IOM-2 interface)
 CIOP = Command/Indication Operation
 For *SLICOFI-2x* command structure and programming see DuSLC Data Sheet chapter 6.

²⁾ if not otherwise stated in the table, the bits ACTL, ACTR, HIT, HIR have to be set to 0.

³⁾ only for SLIC-S

⁴⁾ ACTx means ACTH, ACTL or ACTR.

For a functional description of the operating modes see the DuSLIC Data Sheet.

Preliminary
Operating Modes for the DuSLIC Chip Set
4.1 SLICOFI-2S/-2S2 and SLIC-S/-S2 Interface

The SLIC-S/-S2 (PEB 4264/-2) operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 5 SLIC-S/-S2 Interface Code

		C2 (Pin 17)		
		L	M	H
C1 (Pin 18)	L ¹⁾	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	unused	HIT	HIR

¹⁾ no "Overtemp" signaling possible via pin C1 if C1 is low

Table 6 SLIC-S/-S2 Modes

SLIC Mode	Mode Description	Used SLIC-S/-S2 Battery Voltage
PDH	Power Down High Impedance	V_{BATH}
PDRHL	Power Down Load Resistive on V_{BATH} and V_{BGND}	V_{BATH}
PDRH	Power Down Resistive on V_{BATH} and V_{BGND}	V_{BATH}
ACTH	Active with V_{BATH} and V_{BGND}	V_{BATH}
ACTR	Active with V_{BATH} and V_{HR}	V_{BATH} , V_{HR}
ACTL	Active with V_{BATL} and V_{BGND}	V_{BATL}
HIT	High Impedance on Tip	V_{BATH} , V_{HR}
HIR	High Impedance on Ring	V_{BATH} , V_{HR}

For the usage of the SLIC-S/-S2 modes see the DuSLIC Data Sheet.

4.2 SLICOFI-2 and SLIC-E/-E2 Interface

The SLIC-E/-E2 (PEB 4265/-2) operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 7 SLIC-E/-E2 Interface Code

		C2		
		L	M	H
C1	L ¹⁾	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

¹⁾ no "Overtemp" signaling possible via pin C1 if C1 is low.

Table 8 SLIC-E/-E2 Modes

SLIC Mode	Mode Description	Used SLIC-E/-E2 Battery Voltage
PDH	Power Down High Impedance	V_{BATH}
PDRHL	Power Down Load Resistive on V_{BATH} and V_{BGND}	V_{BATH}
PDRH	Power Down Resistive on V_{BATH} and V_{BGND}	V_{BATH}
ACTH	Active with V_{BATH} and V_{BGND}	V_{BATH}
ACTR	Active with V_{BATH} and V_{HR}	V_{BATH} , V_{HR}
ACTL	Active with V_{BATL} and V_{BGND}	V_{BATL}
HIRT	High Impedance on Ring and Tip	V_{BATH} , V_{HR}
HIT	High Impedance on Tip	V_{BATH} , V_{HR}
HIR	High Impedance on Ring	V_{BATH} , V_{HR}

For the usage of the SLIC-E/-E2 modes see the DuSLIC Data Sheet.

Preliminary

Operating Modes for the DuSLIC Chip Set

4.3 SLICOFI-2 and SLIC-P Interface

The SLIC-P (PEB 4266) operates in the following modes controlled by a ternary logic signal at the C1, C2 inputs and a binary logic signal at C3 input

Table 9 SLIC-P Interface Code

		C2		
		L	M	H
C1	L ¹⁾	PDH	PDRR	PDRRL
			PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR
			ROT	ROR
			C3 = L ²⁾	
			C3 = H ²⁾	

¹⁾ no "Overtemp" signaling possible via pin C1 if C1 is low.

²⁾ C3 pin of SLIC-P is typically connected to IO2 pin of SLICOFI-2. For extremely power-sensitive applications using external ringing the C3 pin can be connected to GND.

Operating Modes for SLIC-P with Two Battery Voltages (V_{BATH} , V_{BATL}) for Voice and an Additional Voltage (V_{BATR}) for Ringing:

The I/O2 pin is used for the C3 pin of SLIC-P.

Table 10 SLIC-P Modes

SLIC Mode	Mode Description	Used SLIC-P Battery Voltage
PDH	Power Down High Impedance	V_{BATR}
PDRH	Power Down Resistive High	V_{BATH}
PDRHL	Power Down Load Resistive High Load	V_{BATH}
PDRR	Power Down Resistive Ring	V_{BATR}
PDRRL	Power Down Load Resistive Ring Load	V_{BATR}
ACTL	Active Low	V_{BATL}
ACTH	Active High	V_{BATH}
ACTR	Active Ring	V_{BATR}
HIRT	High Impedance on RING and TIP	V_{BATR}

Preliminary

Operating Modes for the DuSLIC Chip Set

Table 10 SLIC-P Modes (cont'd)

SLIC Mode	Mode Description	Used SLIC-P Battery Voltage
HIT	High Impedance on TIP	V_{BATR}
HIR	High Impedance on RING	V_{BATR}
ROR	Ring on RING	V_{BATR}
ROT	Ring on TIP	V_{BATR}

For the usage of the SLIC-P modes see the DuSLIC Data Sheet.

Operating Modes for SLIC-P with Three Battery Voltages (V_{BATH} , V_{BATL} , V_{BATR}) for voice and External Ringing

The C3 pin of SLIC-P has to be set to GND. The I/O2 pin is free usable.

Table 11 SLIC-P Modes

SLIC Mode	Mode Description	Used SLIC Battery Voltage
PDH	Power Down High Impedance	V_{BATR}
PDRR	Power Down Resistive on V_{BATR} and V_{BGND}	V_{BATR}
PDRRL	Power Down Load Resistive on V_{BATR} and V_{BGND}	V_{BATR}
ACTH	Active with V_{BATH} and V_{BGND}	V_{BATH}
ACTR	Active with V_{BATR} and V_{BGND}	V_{BATR}
ACTL	Active with V_{BATL} and V_{BGND}	V_{BATL}
HIRT	High Impedance on Ring and Tip	V_{BATR}
HIT	High Impedance on Tip	V_{BATR}
HIR	High Impedance on Ring	V_{BATR}

For the usage of the SLIC-P modes see the DuSLIC Data Sheet.

5 Signal Path and Test Loops

The following figures show the main AC and DC signal path and the integrated analog and digital loops of SLICOFI-2, SLICOFI-2S and SLICOFI-2S2.

Please note the interconnections between the AC and DC pictures of the respective chip set. For further information on the shown registers and bits/switches please see the DuSLIC Data Sheet.

5.1 Test Loops SLICOFI-2

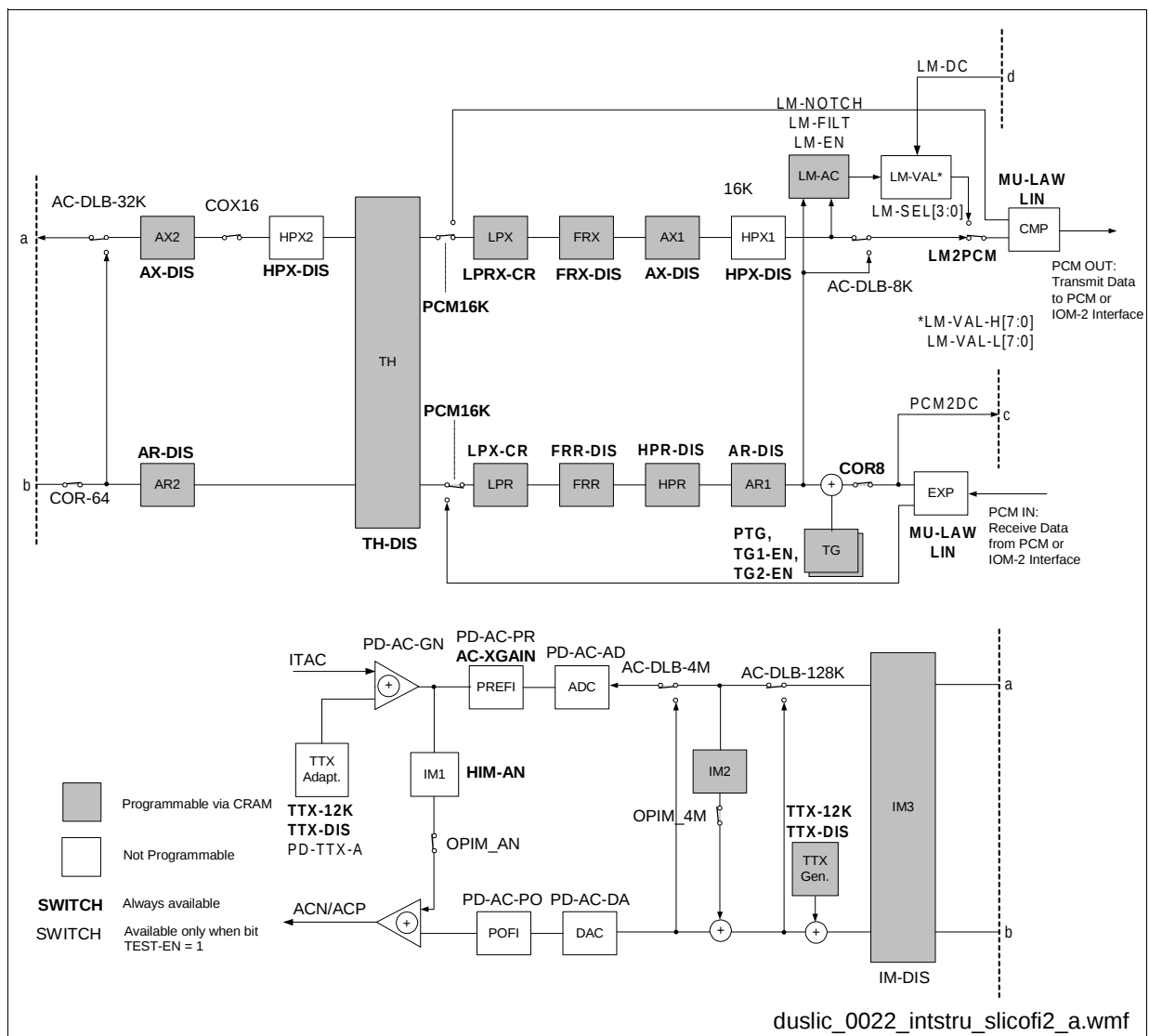


Figure 6 AC Test Loops SLICOFI-2



5.2 Test Loops SLICOFI-2S/-2S2

The AC test loops for SLICOFI-2S (Figure 8) and SLICOFI-2S2 (Figure 9) are different since Teletax (TTX) is not available with SLICOFI-2S2. The DC test loops are identical.

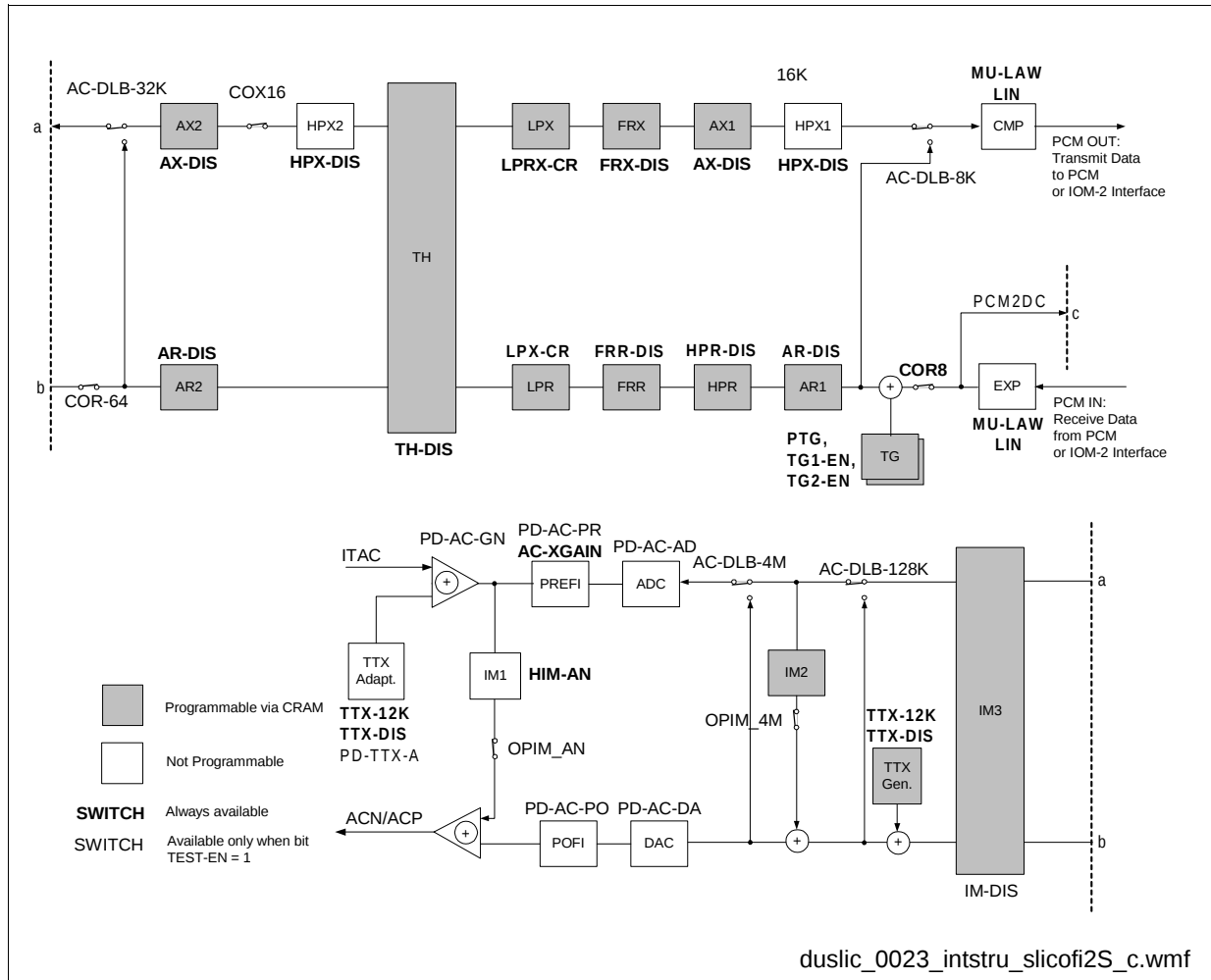


Figure 8 AC Test Loops SLICOFI-2S

Preliminary

Signal Path and Test Loops

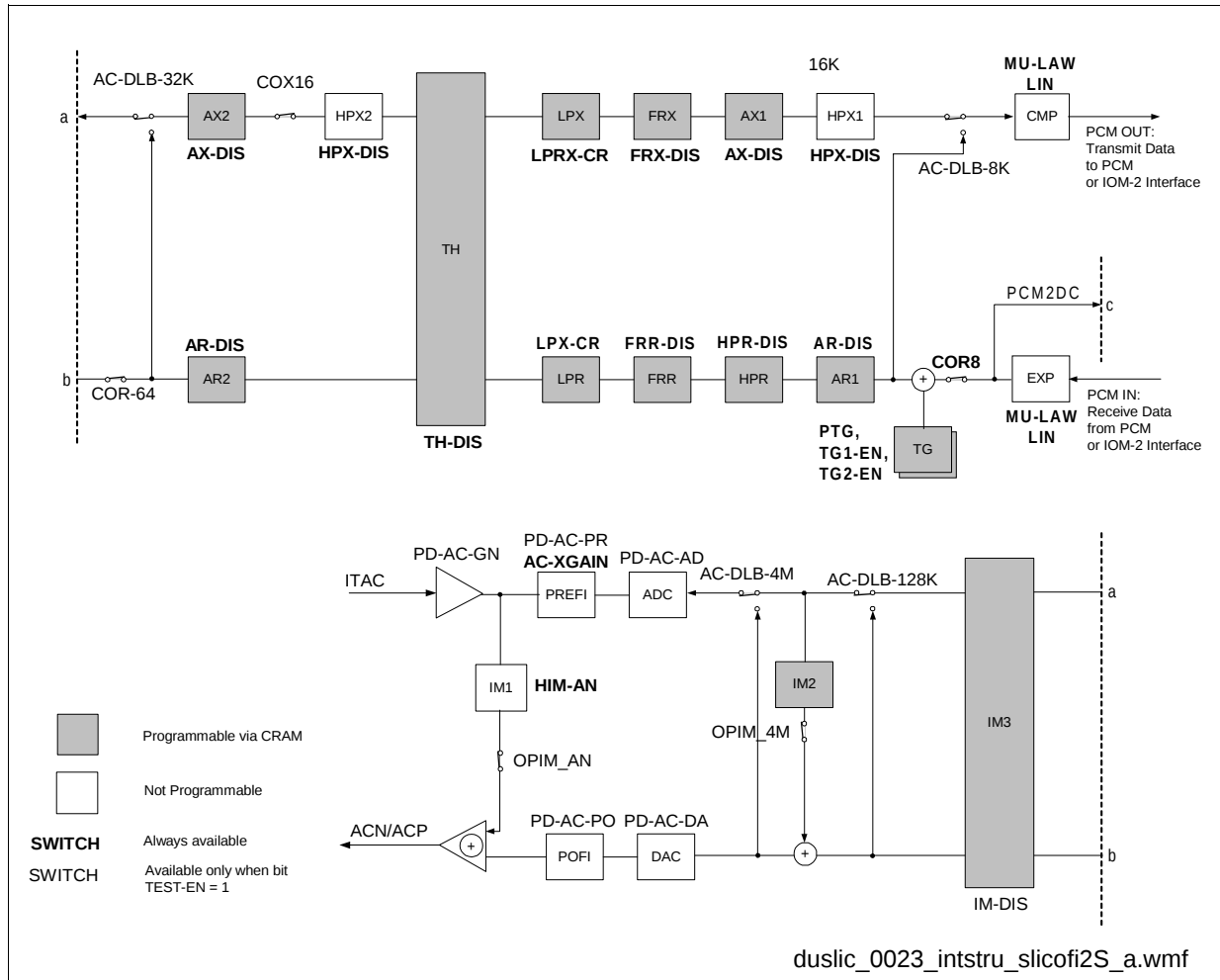


Figure 9 AC Test Loops SLICOFI-2S2

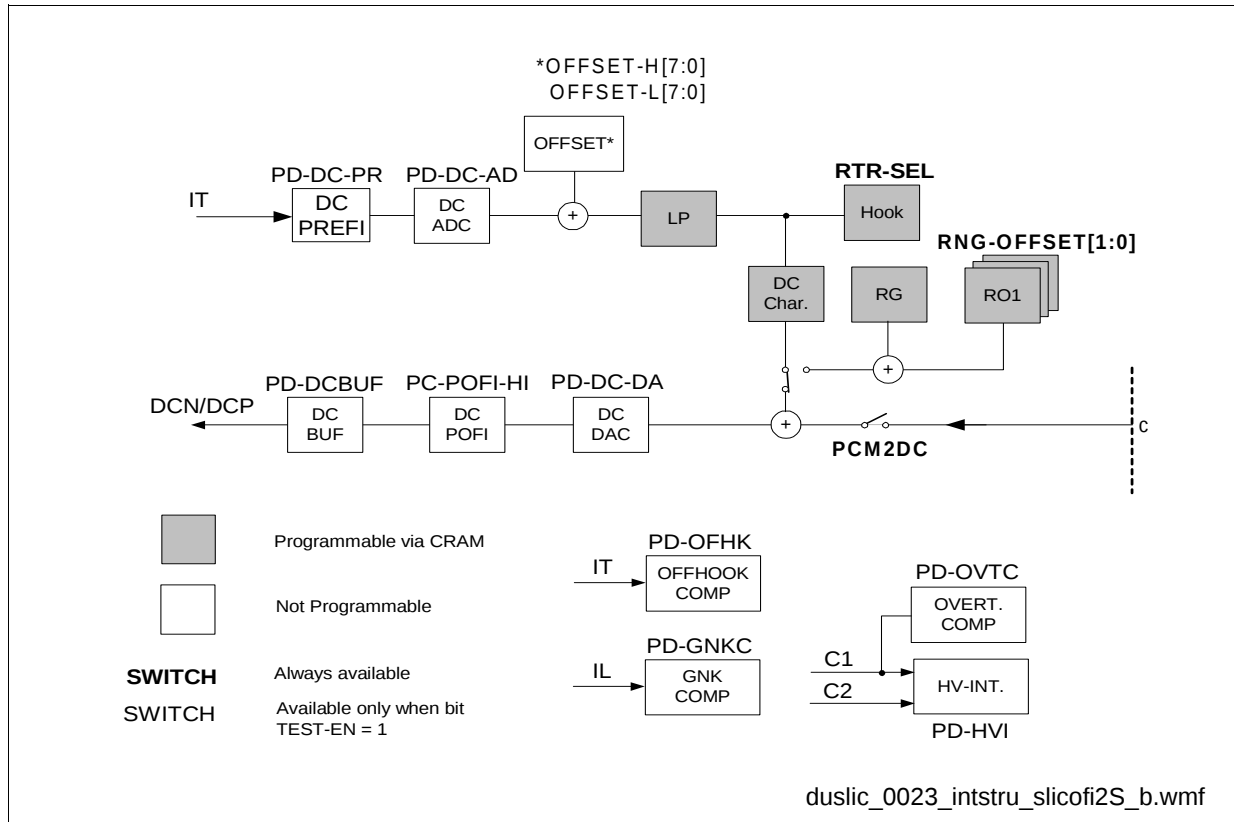


Figure 10 DC Test Loops SLICOFI-2S/-2S2

6 Electrical Characteristics

6.1 Electrical Characteristics PEB 3264/PEB 3264-2/PEB 3265

6.1.1 Absolute Maximum Ratings

Parameter ¹⁾	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply pins (VDDi) referred to the corresponding ground pin (GNDi)	–	– 0.3	4.6	V	–
Ground pins (GNDi) referred to any other ground pin (GNDj)	–	– 0.3	0.3	V	–
Supply pins (VDDi) referred to any other supply pin (VDDj)	–	– 0.3	0.3	V	–
Analog input and output pins	–	– 0.3	3.6	V	$V_{DDA} = 3.3 \text{ V}$, $V_{GNDA/B} = 0 \text{ V}$
Digital input and output pins	–	– 0.3	5.5	V	$V_{DDD} = 3.3 \text{ V}$, $V_{GNDD} = 0 \text{ V}$
DC input and output current at any input or output pin (free from latch-up)	–	–	100	mA	–
Storage temperature	T_{STG}	– 65	125	°C	–
Ambient temperature under bias	T_A	– 40	85	°C	–
Power dissipation	P_D	–	1	W	–
ESD voltage	–	–	2	kV	Human body model ²⁾
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model) ³⁾

1) i, j = A, B, D, R, PLL

2) MIL STD 883D, method 3015.7 and ESD Assn. standard S5.1-1993.

3) EOS/ESD Assn. Standard DS5.3-1993.

Preliminary

Electrical Characteristics

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation under these conditions is not guaranteed. Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.

6.1.2 Power Up Sequence for Supply Voltages

The power up of VDDA, Vddb, VDDR, VDDD and VDDPLL should be performed simultaneously. No voltage should be supplied to any input or output pin before the VDD voltages are applied.

6.1.3 Operating Range

$$V_{\text{GNDD}} = V_{\text{GNDPLL}} = V_{\text{GNDR}} = V_{\text{GNDA/B}} = 0 \text{ V}$$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply pins (VDDi) referred to the corresponding ground pin (GNDi) (I = A, B, D, R, PLL)		3.135	3.3	3.465	V	
Analog input pins referred to the ground pin (GNDj) (j = A, B) ITj, ILj, ITACj, VCMITj		0	–	3.3	V	$V_{\text{DDj}} = 3.3 \text{ V}$ $V_{\text{GNDj}} = 0 \text{ V}$
Analog output pins referred to the ground pin (GNDj) (j = A, B) ACpj, DCPj, ACNj, DCNj, VCMS, VCM C1, C2						$V_{\text{DDj}} = 3.3 \text{ V}$ $V_{\text{GNDj}} = 0 \text{ V}$
		0.3	–	2.7	V	
		1.3	–	1.7	V	
		0	–	3.3	V	
Analog pins for passive devices to ground pin (GNDj) (j = A, B) CDCpj, CDCNj CREF						$V_{\text{DDj}} = 3.3 \text{ V}$ $V_{\text{GNDj}} = 0 \text{ V}$
		0	–	3.3	V	
		1.3	–	1.7	V	
Digital input and output pins		0	–	5	V	
Ambient temperature	T_A	– 40	–	+ 85	°C	

Preliminary

Electrical Characteristics

6.1.4 Power Dissipation SLICOFI-2

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise stated.

$V_{DD} = V_{DDA} = V_{ddb} = V_{DDR} = V_{DDPLL} = 3.3\text{ V} \pm 5\%$;

$V_{GND A} = V_{GND B} = V_{GND R} = V_{GND D} = V_{GND PLL} = 0\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current ¹⁾						
Sleep both channels	$I_{DDSleep}$	–	5	7	mA	(MCLK, PCLK = 2 MHz)
Power Down both channels	$I_{DDPDown}$	–	24	30	mA	–
Active one channel	I_{DDAct1}	–	39	46	mA	without EDSP ²⁾
		–	43	50	mA	with 8 MIPS (DTMF detection)
		–	47	55	mA	with 16 MIPS
Active both channels	I_{DDAct2}	–	55	70	mA	without EDSP
		–	70	90	mA	with 32 MIPS
Power dissipation ¹⁾						
Sleep both channels	$P_{DDSleep}$	–	17	25	mW	(MCLK, PCLK = 2 MHz)
Power Down both channels	$P_{DDPDown}$	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	without EDSP
		–	142	174	mW	with 8 MIPS (DTMF detection)
		–	155	191	mW	with 16 MIPS
Active both channels	P_{DDAct2}	–	182	243	mW	without EDSP
		–	231	315	mW	with 32 MIPS

¹⁾ Power dissipation and supply currents are target values

²⁾ EDSP features are DTMF detection, Caller ID generation and Universal Tone Detection (UTD).

Preliminary

Electrical Characteristics

6.1.5 Power Dissipation SLICOFI-2S/-2S2

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{ddb} = V_{DDR} = V_{DDPLL} = 3.3\text{ V} \pm 5\%$;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL} = 0\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current ¹⁾						
Power Down both channels	$I_{DDPDown}$	–	24	30	mA	–
Active one channel	I_{DDAct1}	–	39	46	mA	–
Active both channels	I_{DDAct2}	–	55	70	mA	–
Power dissipation ¹⁾						
Power Down both channels	$P_{DDPDown}$	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	–
Active both channels	P_{DDAct2}	–	182	243	mW	–

¹⁾ Power dissipation and supply currents are target values

Preliminary

Electrical Characteristics

6.1.6 Digital Interface

$T_A = -40$ to $+85$ °C, unless otherwise stated.

$V_{DD} = V_{DDD} = V_{DDA/B} = 3.3 \text{ V} \pm 5\%$; $V_{GNDD} = V_{GNDA/B} = 0 \text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
For all input pins (including IO pins):						
Low-input pos.-going	V_{T+}	–	1.70	1.82	V	see Figure 11
High-input neg.-going	V_{T-}	1.13	1.20	–	V	see Figure 11
Input hysteresis	V_H	0.48	0.5	0.56	V	$V_H = V_{T+} - V_{T-}$
Spike rejection for reset	t_{rej}	1	–	4	µs	–
For all output pins except DU, DXA, DXB, IO1, IO2 (including IO pins):						
Low-output voltage	V_{OL}	–	0.35	0.4	V	$I_O = -3.6 \text{ mA}$
High-output voltage	V_{OH}	2.7	3.0	–	V	$I_O = 3.3 \text{ mA}$
for pins DU, DXA, DXB						
Low-output voltage	V_{OLDU}	–	0.35	0.4	V	$I_O = -6 \text{ mA}$
High-output voltage	$V_{OH DU}$	2.7	3.0	–	V	$I_O = 5.3 \text{ mA}$
for pins IO1, IO2						
Low-output voltage	V_{OLDU}	–	0.35	0.4	V	$I_O = -50 \text{ mA}$ (SLICOFI-2)
	V_{OLDU}	–	0.35	0.4	V	$I_O = -30 \text{ mA}$ (SLICOFI-2S/-2S2)
High-output voltage	$V_{OH DU}$	2.7	3.0	–	V	$I_O = 3.3 \text{ mA}$

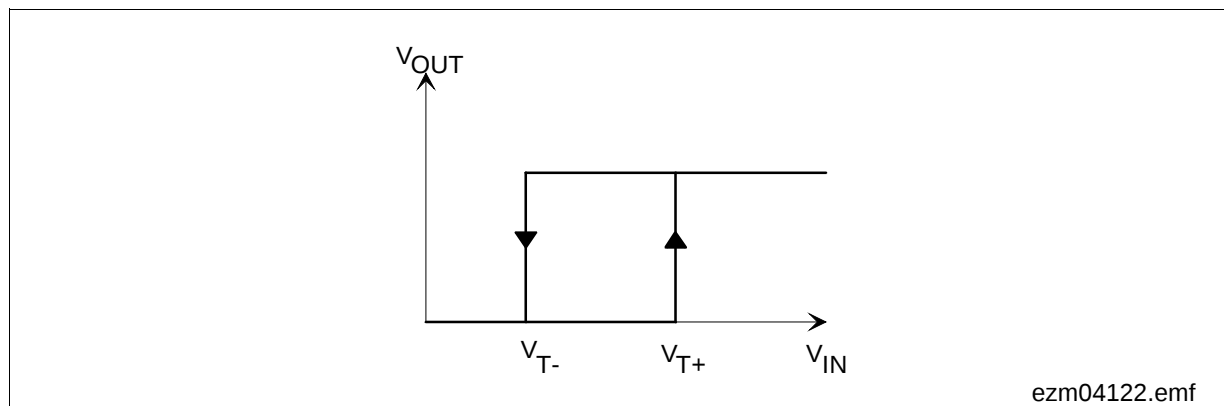


Figure 11 Hysteresis for Input Pins

6.1.7 Miscellaneous Characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise stated.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Leakage

all digital input and input/output pins all analog input pins	I_L	-3	-	3	μA	-
--	-------	----	---	---	---------------	---

Comparator Thresholds

Off Hook comparator threshold	V_{THRESH}	-	$V_{\text{CM}} - 0.275$	-	V	$V_{\text{DD}} = 3.3\text{ V}$
GNDkey comparator positive threshold	$V_{\text{THRESH+}}$	-	$V_{\text{CM}} + 0.275$	-	V	
negative threshold	$V_{\text{THRESH-}}$	-	$V_{\text{CM}} - 0.275$	-	V	
threshold hysteresis	$V_{\text{THR-hyst.}}$	-	0.045	-	V	
Overttemperature comparator	I_{Overtemp}	10	-	130	μA	

6.2 AC Transmission SLICOFI-2/-2S/-2S2

The specification is based on the subscriber linecard requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires the consideration of the complete analog environment of the *SLICOFI-2x* device.

Functionality and performance is guaranteed for $T_A = 0$ to 70 °C by production testing. Extended temperature range operation at $-40\text{ °C} < T_A < 85\text{ °C}$ is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Test Conditions

$T_A = -40\text{ °C}$ to 85 °C , unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL} = 3.3\text{ V} \pm 5\%$;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL} = 0\text{ V}$

Register BCR4: TH-DIS = 1, IM-DIS = 1, AX-DIS = 1, AR-DIS = 1

Register LMCR2: TEST-EN = 1

Register TSTR4: OPIM-AN = 1, OPIM-4M = 1

If not otherwise stated, the default settings are used.

The 0 dBm0 definitions for receive and transmit are:

A 0 dBm0 AC signal in transmit direction is equivalent to 0.5911 Vrms measured at pins ITACi/VCMITi (i = A, B).

A 0 dBm0 AC signal in receive direction is equivalent to 0.5911 Vrms measured at pins ITACi/VCMITi (i = A, B).

Table 12 AC Transmission

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	

Insertion Loss

A-D (see Figure 13)	PCM _{OUT}	$V_G = -11.88\text{ dBm0}$ $f = 1015.625\text{ Hz}$	- 0.2	0	+ 0.2	dBm0
D-A (see Figure 13)	V _{AC}	PCM _{in} = 0 dBm0 $f = 1015.625\text{ Hz}$	- 2.668	- 2.868	- 3.068	dBm0

Preliminary

Electrical Characteristics

Table 12 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	

Frequency Response

Receive loss Frequency variation	G_{RAF}	Reference frequency 1014 Hz, signal level 0 dBm0, $H_{FRR} = 1$				
		$f = 300 \text{ Hz}$	- 0.17	0.03	0.23	dB
		$f = 2400 \text{ Hz}$	- 0.08	0.12	0.32	dB
		$f = 3000 \text{ Hz}$	- 0.04	0.16	0.36	dB
Transmit loss Frequency variation	G_{XAF}	Reference frequency 1014 Hz, signal level 0 dBm0, $H_{FRX} = 1$				
		$f = 300 \text{ Hz}$	- 0.16	0.04	0.24	dB
		$f = 2400 \text{ Hz}$	- 0.15	0.05	0.25	dB
		$f = 3000 \text{ Hz}$	- 0.14	0.06	0.26	dB

Gain Tracking (see Figure 14 and Figure 15)

Transmit gain Signal level variation	G_{XAL}	Sinusoidal test method $f = 1014 \text{ Hz}$, reference level 0 dBm0				
		$V_{FXI} = - 55 \text{ to}$ $- 50 \text{ dBm0}$	- 1.4	-	1.4	dB
		$V_{FXI} = - 50 \text{ to}$ $- 40 \text{ dBm0}$	- 0.5	-	0.5	dB
		$V_{FXI} = - 40 \text{ to}$ $+ 3 \text{ dBm0}$	- 0.25	-	0.25	dB
Receive gain Signal level variation	G_{RAL}	Sinusoidal test method $f = 1014 \text{ Hz}$, reference level 0 dBm0				
		$D_{R0} = - 55 \text{ to}$ $- 50 \text{ dBm0}$	- 1.4	-	1.4	dB
		$D_{R0} = - 50 \text{ to}$ $- 40 \text{ dBm0}$	- 0.5	-	0.5	dB
		$D_{R0} = - 40 \text{ to}$ $+ 3 \text{ dBm0}$	- 0.25	-	0.25	dB

Preliminary

Electrical Characteristics

Table 12 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	

Group Delay (see Figure 16)

Transmit delay, absolute	D_{XA}	$f = 500 - 2800 \text{ Hz}$	400	490	585	μs
Receive delay, absolute	D_{RA}	$f = 500 - 2800 \text{ Hz}$	290	380	475	μs
Group delay distortion, Receive and Transmit, relative to 1500 Hz, (see Figure 16)	D_{XR}					
		$f = 500 - 600 \text{ Hz}$	–	–	300	μs
		$f = 600 - 1000 \text{ Hz}$	–	–	150	μs
		$f = 1000 - 2600 \text{ Hz}$	–	–	100	μs
		$f = 2600 - 2800 \text{ Hz}$	–	–	150	μs
		$f = 2800 - 3000 \text{ Hz}$	–	–	300	μs

Overload compression A/D (see Figure 12)

Total Harmonic Distortion

Transmit	THD4	– 7 dBm0, 300 - 3400 Hz	–	– 50	– 44	dB
Receive	THD2	– 7 dBm0, 300 - 3400 Hz	–	– 50	– 44	dB

Idle Channel Noise

at ACN, ACP (receive) A-law	N_{RP}	Psophometric	–	– 103	– 92	dBmp
PCM side (transmit) A-Law	N_{TP}	Psophometric	–	– 84	– 75	dBmp

Preliminary

Electrical Characteristics

Table 12 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	

Distortion (Sinusoidal Test Method)

Signal to total distortion Transmit	STD _X	$f = 1014 \text{ Hz}$ (C message-weighted for μ -law, psophometrically weighted for A-law)				
		Add – 45 dBm0	27	29.7	–	dB
		Add – 40 dBm0	32	35	–	dB
		Add 0 dBm0	36.5	41	–	dB
Signal to total distortion Receive	STD _R	$f = 1014 \text{ Hz}$ (C message-weighted for μ -law, psophometrically weighted for A-law)				
		Add – 45 dBm0	22	25	–	dB
		Add – 40 dBm0	29	32	–	dB
		Add 0 dBm0	36.5	40	–	dB

Power Supply Rejection Ratio

Power supply rejection ratio	PSRR	ripple: 1 kHz, 70 mVrms	–	–	–	–
Receive V_{DD}	–	at DCP/DCN at ACP/ACN	48	70	–	dB
Transmit V_{DD}	–	at IOM-2 / PCM	32	70	–	dB

Crosstalk

Same channel	–	0 dBm0, 1014 Hz				
TX or RX	–		–	–	– 75	dBm0
RX to TX	–		–	–	– 75	dBm0
Between channels	–	0 dBm0, 1014 Hz				
TX or RX to TX	–		–	–	– 75	dBm0
TX or RX to RX	–		–	–	– 75	dBm0

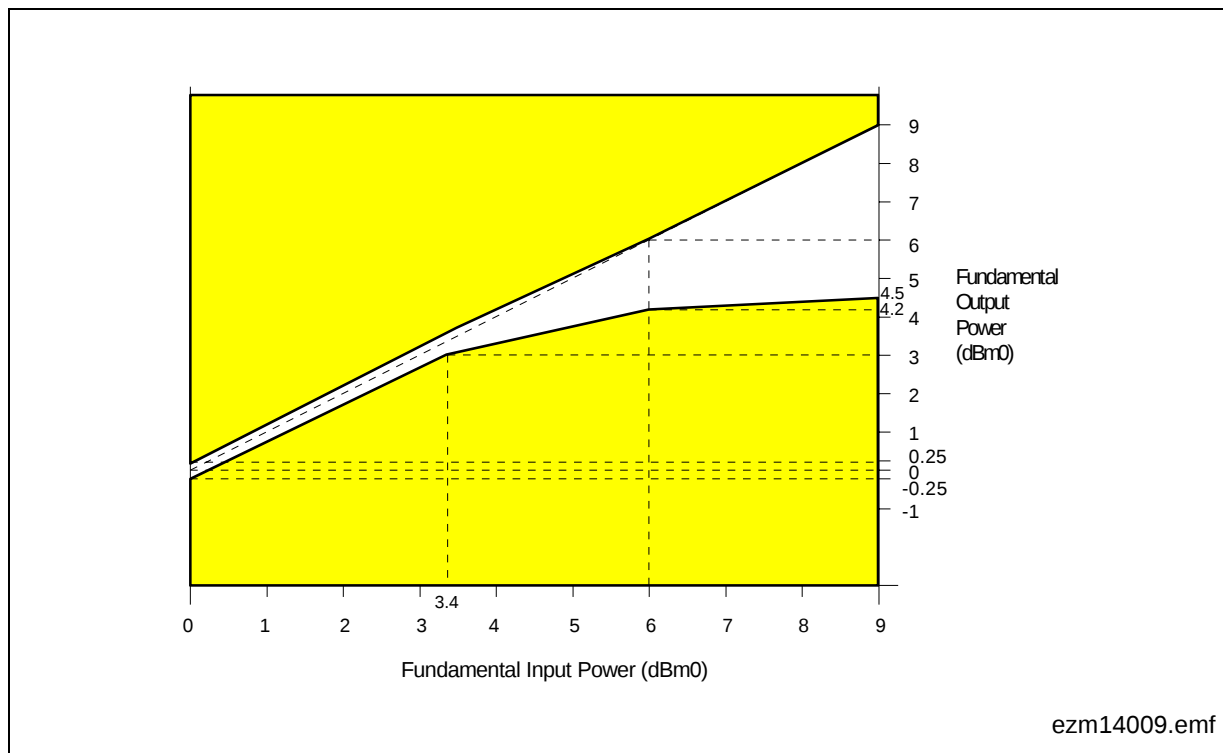


Figure 12 Overload Compression A/D

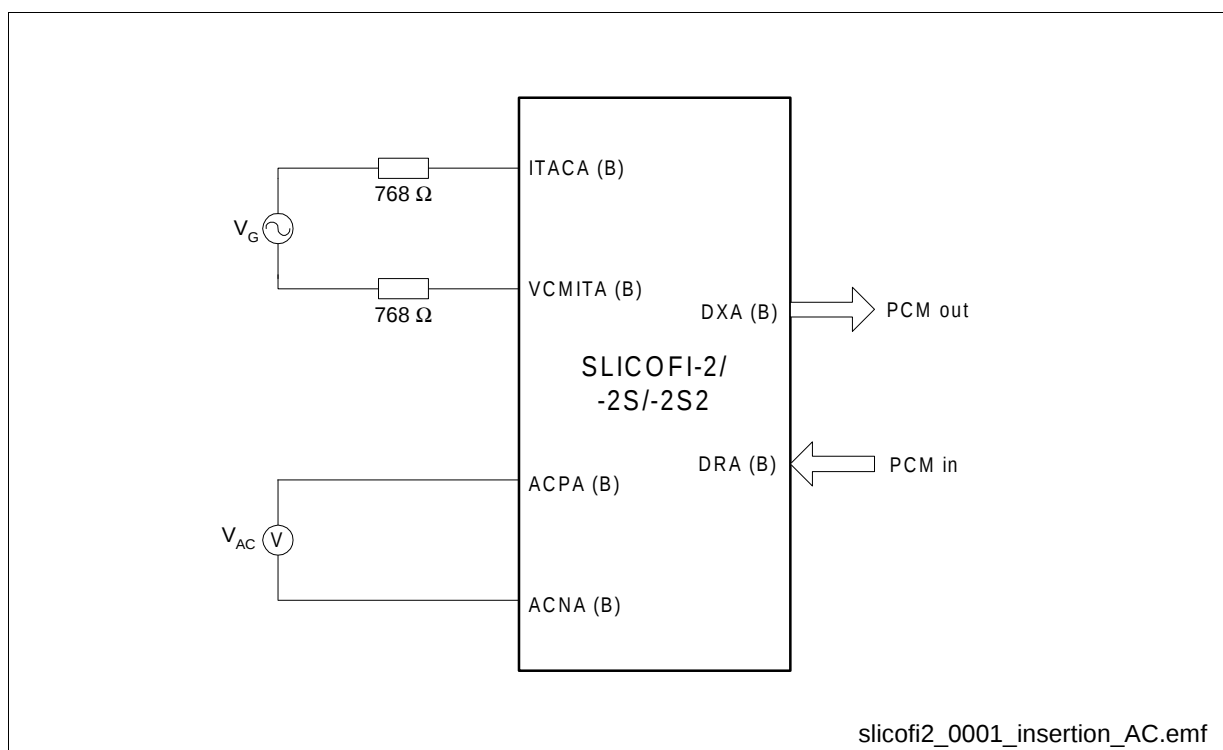


Figure 13 Insertion Loss

6.2.1 Gain Tracking (Receive or Transmit)

The gain deviations stay within the limits in the figures below.

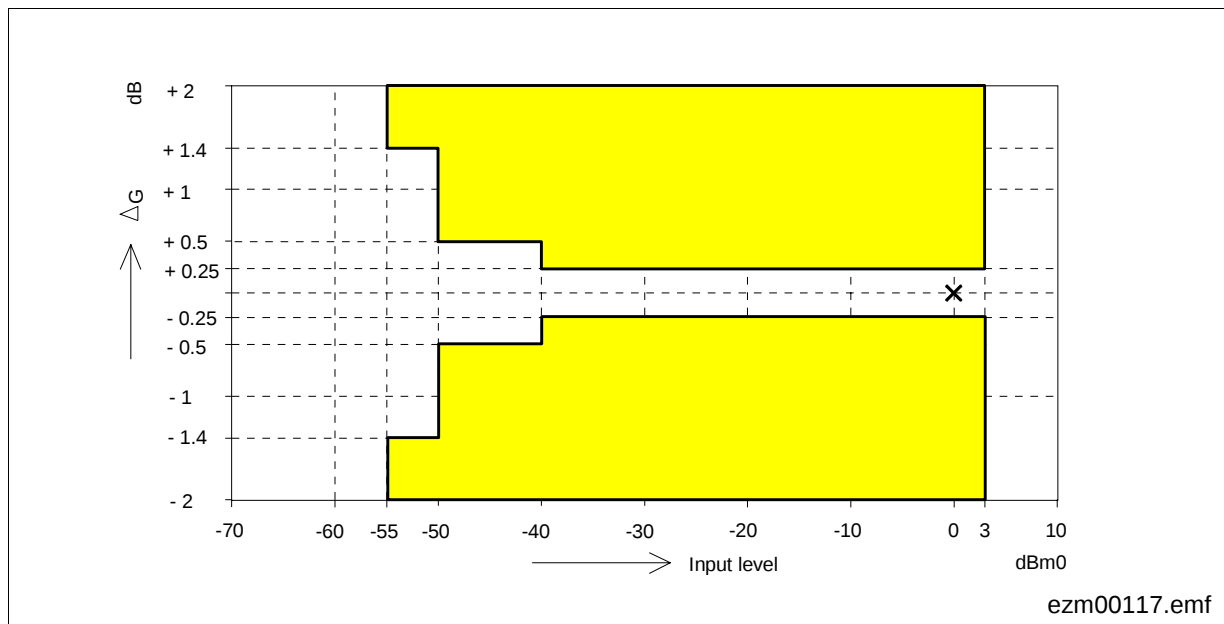


Figure 14 Gain Tracking Receive

Measured with a sine wave of $f = 1014$ Hz, the reference level is -0 dBm0.

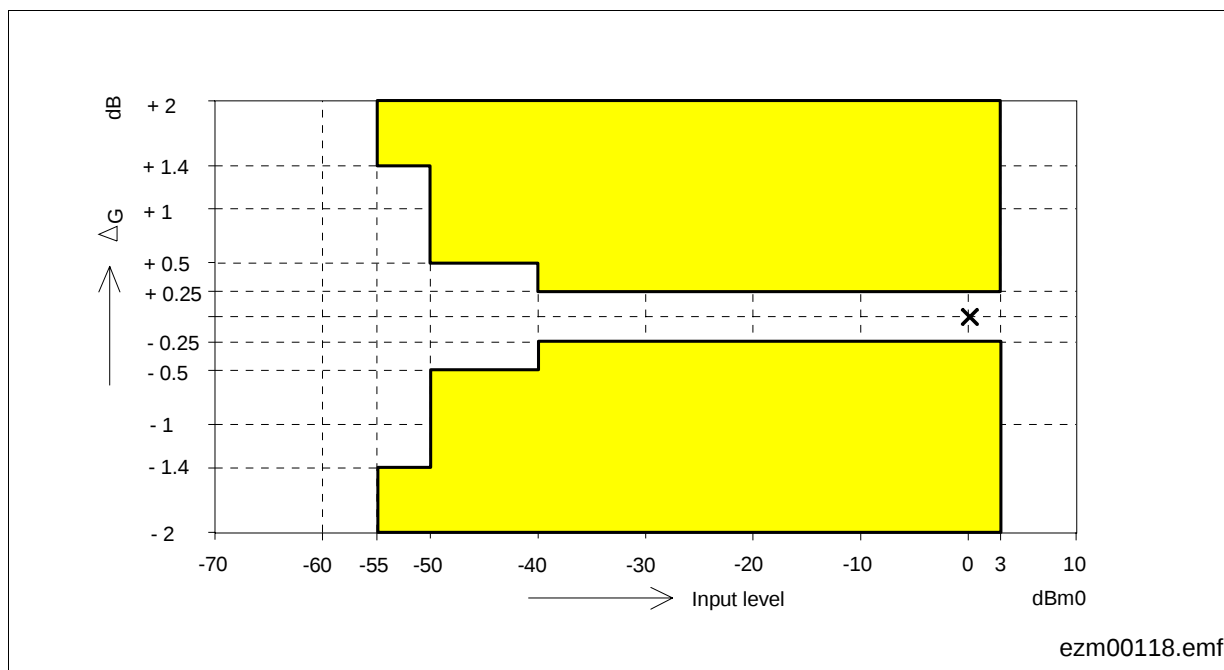


Figure 15 Gain Tracking Transmit

Measured with a sine wave of $f = 1014$ Hz, the reference level is -0 dBm0.

6.2.2 Group Delay

Minimum delays occur when the *SLICOFI-2x* is operating with disabled Frequency Response Receive and Transmit filters including the delay through A/D and D/A converters. Specific filter programming may cause additional group delays. Absolute Group delay also depends on the programmed time slot.

Group delay deviations stay within the limits in the figures below.

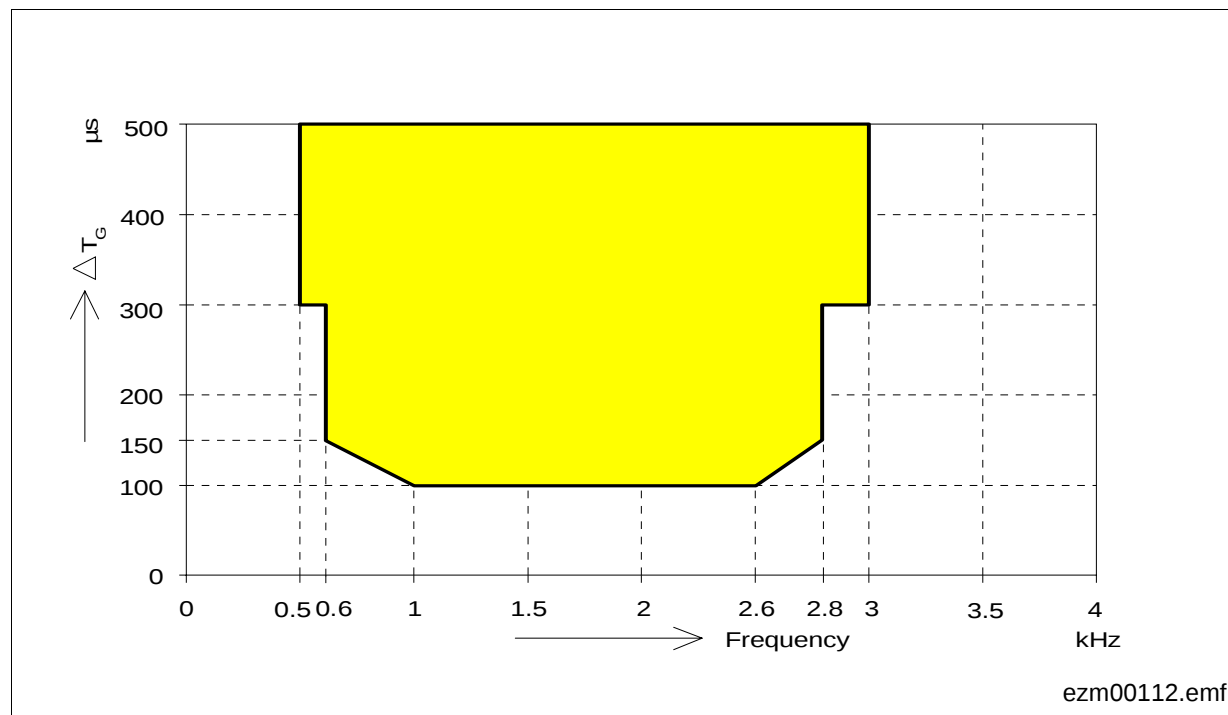


Figure 16 Group Delay Distortion Receive and Transmit

Signal level 0 dBm0

Preliminary

Electrical Characteristics

6.3 DC Characteristics

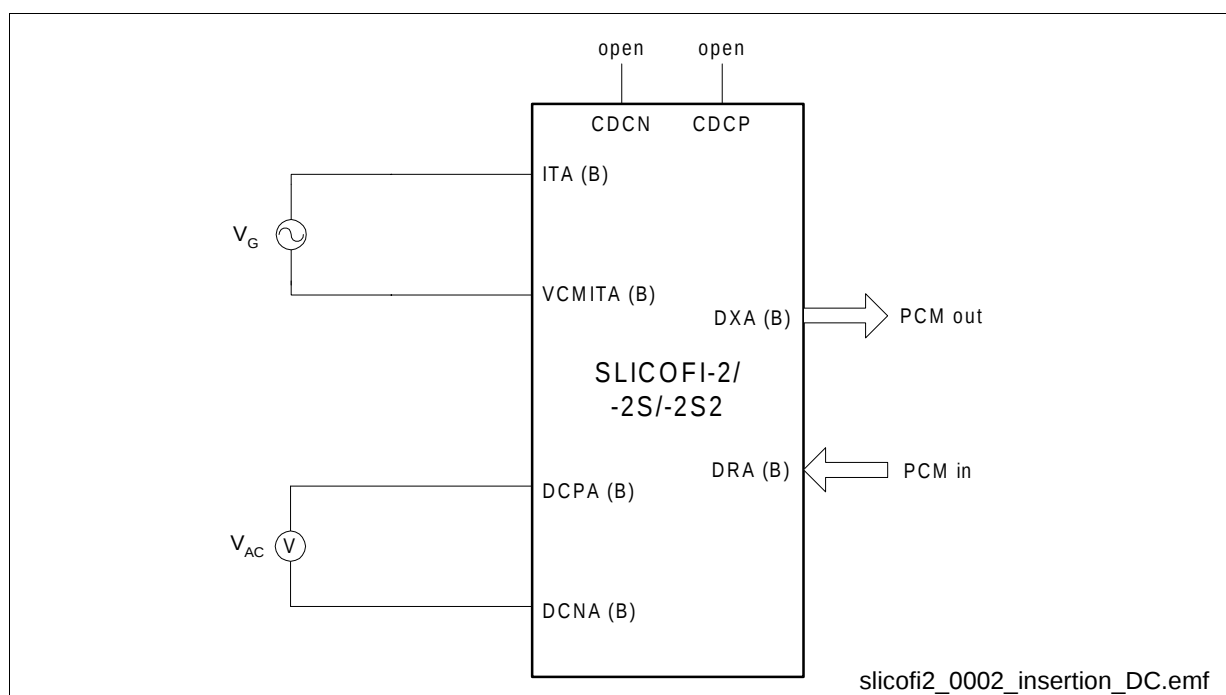
$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise stated.

Table 13 DC Characteristics

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	

Insertion Loss

A-D (see Figure 17)	PCM_{OUT}	$V_G = 0.728\text{ dBm0}$ A-law, Bits LMSEL[3:0] = 0101 (register LMCR2) Bit LM2PCM = 1 (register LMCR1) $f = 296.875\text{ Hz}$	- 0.2	0	+ 0.2	dBm0
D-A (see Figure 17)	V_{AC}	$\text{PCM}_{\text{in}} = 0\text{ dBm0}$ Bit PCM2DC = 1 (register LMCR1) Bit RNG-OFFSET[1:0] = 10 (register LMCR3) $f = 296.875\text{ Hz}$	5.775	5.975	6.175	dBm0


Figure 17 Insertion Loss

Preliminary

Electrical Characteristics

6.4 SLICOFI-2/-2S/-2S2 Timing Characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise stated.

6.4.1 Input/Output Waveform for AC Tests

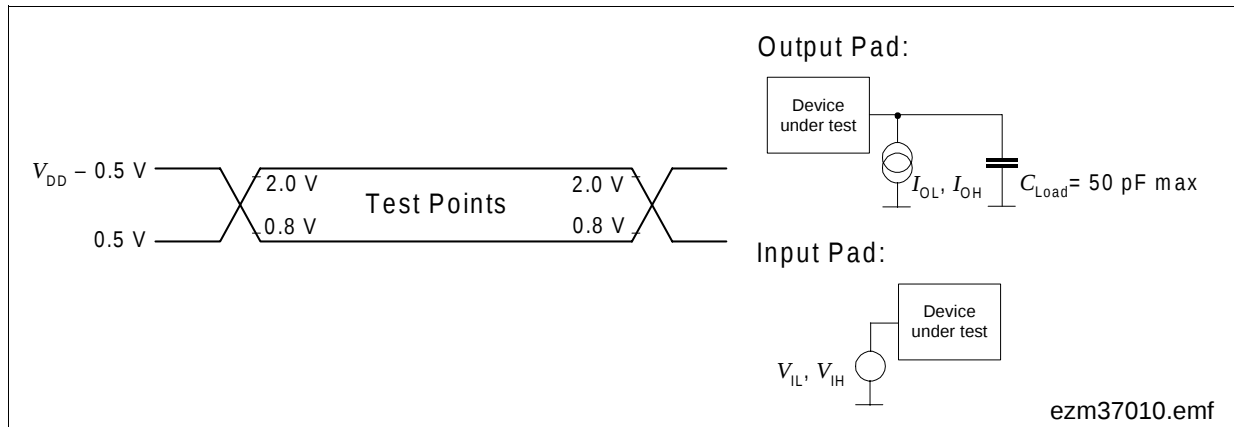


Figure 18 Waveform for AC Tests

During AC-Testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V . The CMOS outputs are measured at 0.5 V and $V_{DD} - 0.5\text{ V}$ respectively.

6.4.2 MCLK/FSC Timing

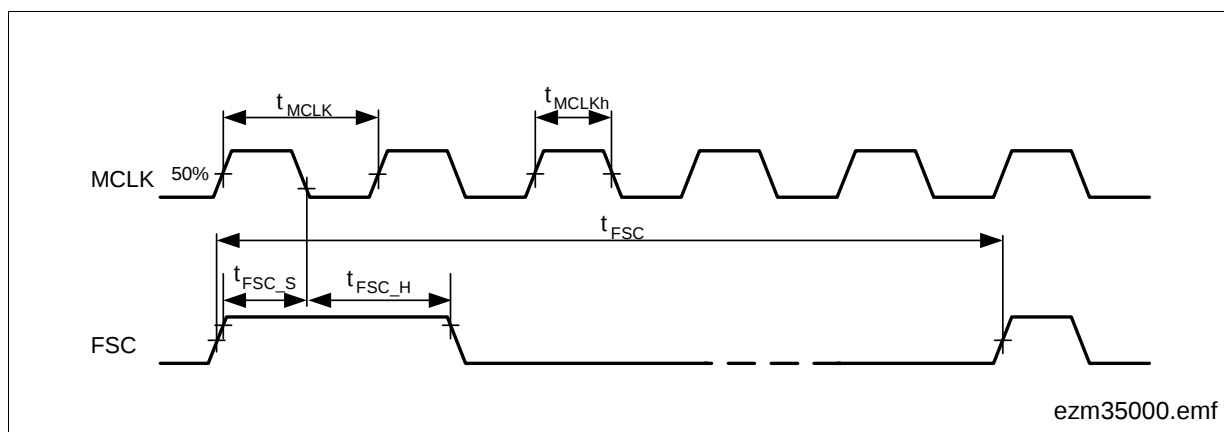


Figure 19 MCLK / FSC-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period MCLK ¹⁾ 512 kHz ± 100 ppM 1536 kHz ± 100 ppM 2048 kHz ± 100 ppM 4096 kHz ± 100 ppM 7168 kHz ± 100 ppM 8192 kHz ± 100 ppM	t_{MCLK}	1952.93 650.98 488.23 244.116 139.495 122.058	1953.13 651.04 488.28 244.141 139.509 122.070	1953.32 651.11 488.33 244.165 139.523 122.082	ns
MCLK high time	t_{MCLKh}	$0.4 \times t_{MCLK}$	$0.5 \times t_{MCLK}$	$0.6 \times t_{MCLK}$	ns
Period FSC ¹⁾	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
FSC (or PCM) jitter time		$-0.2 \times t_{MCLK}$		$+0.2 \times t_{MCLK}$	ns

¹⁾ The MCLK frequency must be an integer multiple of the FSC frequency.

6.4.3 PCM Interface Timing

6.4.3.1 Single-Clocking Mode

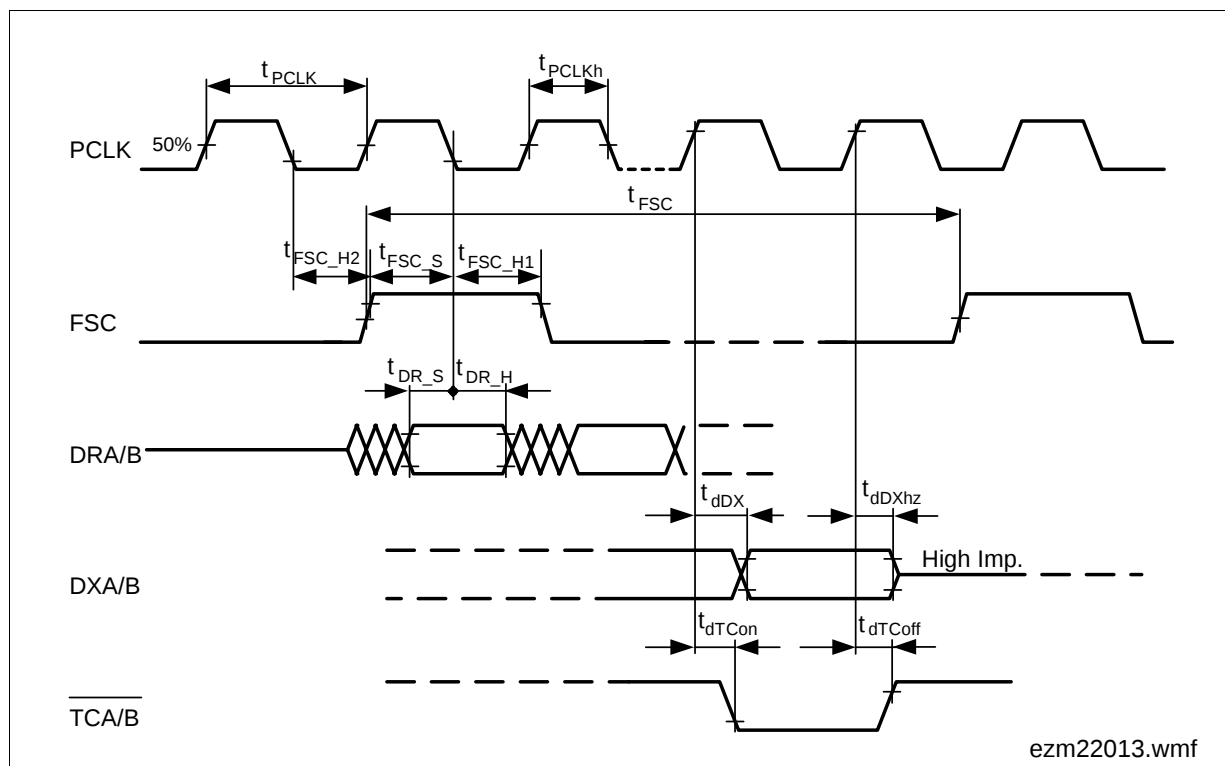


Figure 20 PCM Interface Timing - Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK ¹⁾	t_{PCLK}	1/8192	$1/(n \cdot 64)$ with $2 \leq n \leq 128$	1/128	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	$0.5 \times t_{PCLK}$	$0.6 \times t_{PCLK}$	μs
Period FSC ¹⁾	t_{FSC}	—	125	—	μs
FSC setup time	t_{FSC_s}	10	50	—	ns
FSC hold time 1	$t_{FSC_{h1}}$	40	50	$t_{FSC} - t_{PCLK} - t_{FSC_s}$	ns
FSC hold time 2	$t_{FSC_{h2}}$	40	50	—	ns
DRA/B setup time	t_{DR_s}	10	50	—	ns
DRA/B hold time	t_{DR_h}	10	50	—	ns

Preliminary

Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DXA/B delay time ²⁾	t_{dDX}	25	—	$t_{dDX_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns
DXA/B delay time to high Z	t_{dDXhz}	25	—	50	ns
TCA/B delay time on	t_{dTCon}	25	—	$t_{dTCon_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns
TCA/B delay time off	t_{dTCoFF}	25	—	$t_{dTCoFF_min} + 2 \times R_{Pullup}[k\Omega] \times C_{Load}[pF]$	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency.

2) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load} , $R_{Pullup} > 1.5\text{ k}\Omega$)

6.4.3.2 Double-Clocking Mode

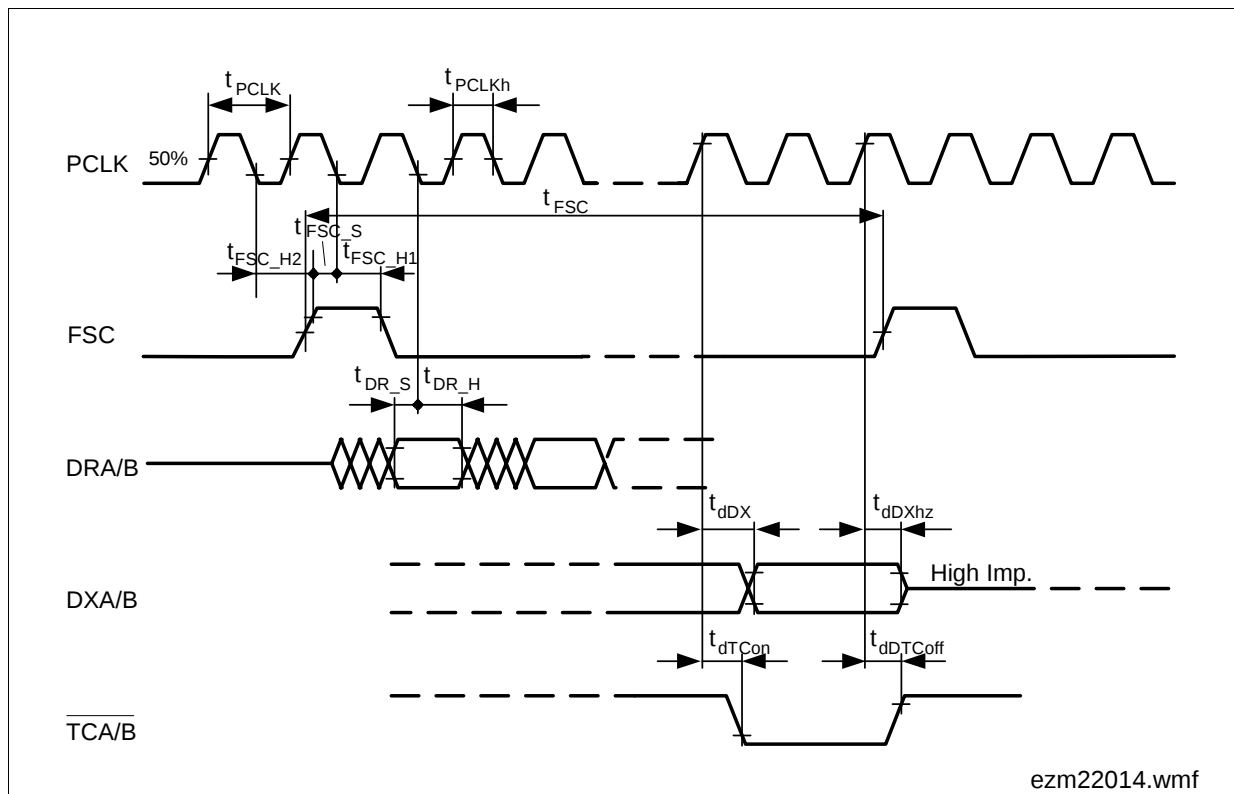


Figure 21 PCM Interface Timing – Double-Clocking Mode

Preliminary

Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK ¹⁾	t_{PCLK}	1/8192	$1/(n \cdot 64)$ with $2 \leq n \leq 64$	1/256	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	$0.5 \times t_{PCLK}$	$0.6 \times t_{PCLK}$	μs
Period FSC ¹⁾	t_{FSC}	–	125	–	μs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{PCLK} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns
DXA/B delay time ²⁾	t_{dDX}	25	–	$t_{dDX_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	$t_{dTCon_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns
TCA/B delay time off	t_{dTCoFF}	25	–	$t_{dTCoFF_min} + 2 \times R_{Pullup}[k\Omega] \times C_{Load}[pF]$	ns

¹⁾ The PCLK frequency must be an integer multiple of the FSC frequency.

²⁾ All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load} , $R_{Pullup} > 1.5 \text{ k}\Omega$)

6.4.4 Microcontroller Interface Timing

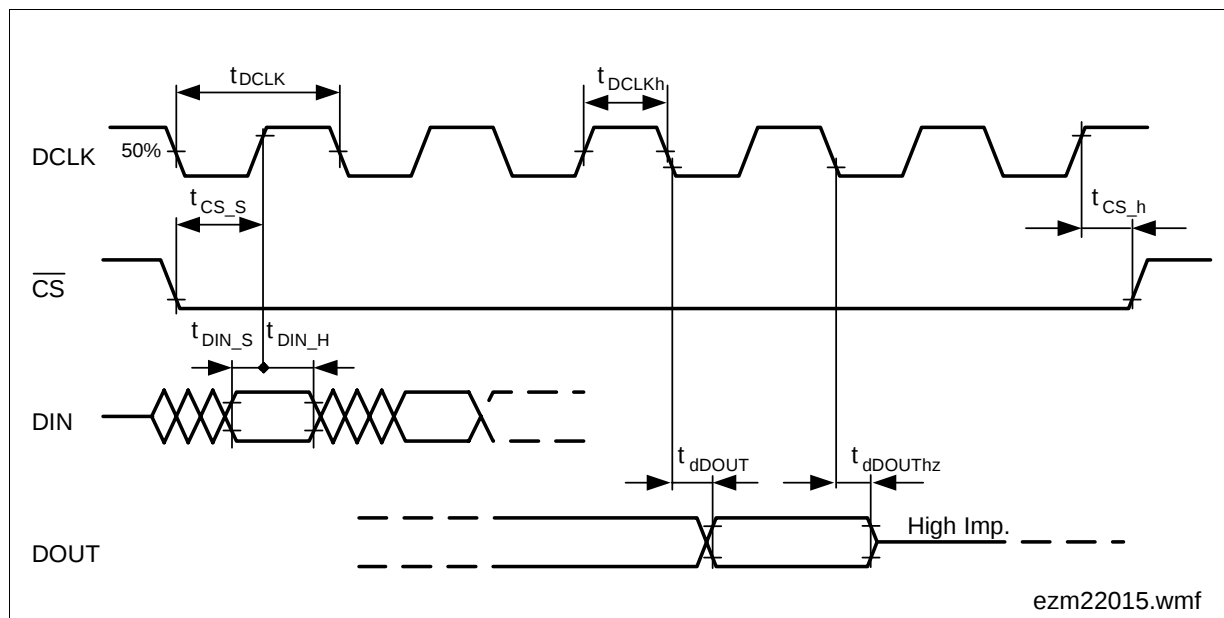


Figure 22 Microcontroller Interface Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of DCLK	t_{DCLK}	1/8192	–	–	ms
DCLK high time	t_{DCLKh}	–	$0.5 \times t_{DCLK}$	–	μ s
CS setup time	t_{CS_s}	10	50	–	ns
CS hold time	t_{CS_h}	30	50	–	ns
DIN setup time	t_{DIN_s}	10	50	–	ns
DIN hold time	t_{DIN_h}	10	50	–	ns
DOUT delay time ¹⁾	t_{dDOUT}	30	–	$t_{dDOUT_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns
DOUT delay time to high Z	$t_{dDOUTHz}$	30	–	50	ns

¹⁾ All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load})

Preliminary

Electrical Characteristics

6.4.5 IOM-2 Interface Timing

6.4.5.1 Single-Clocking Mode

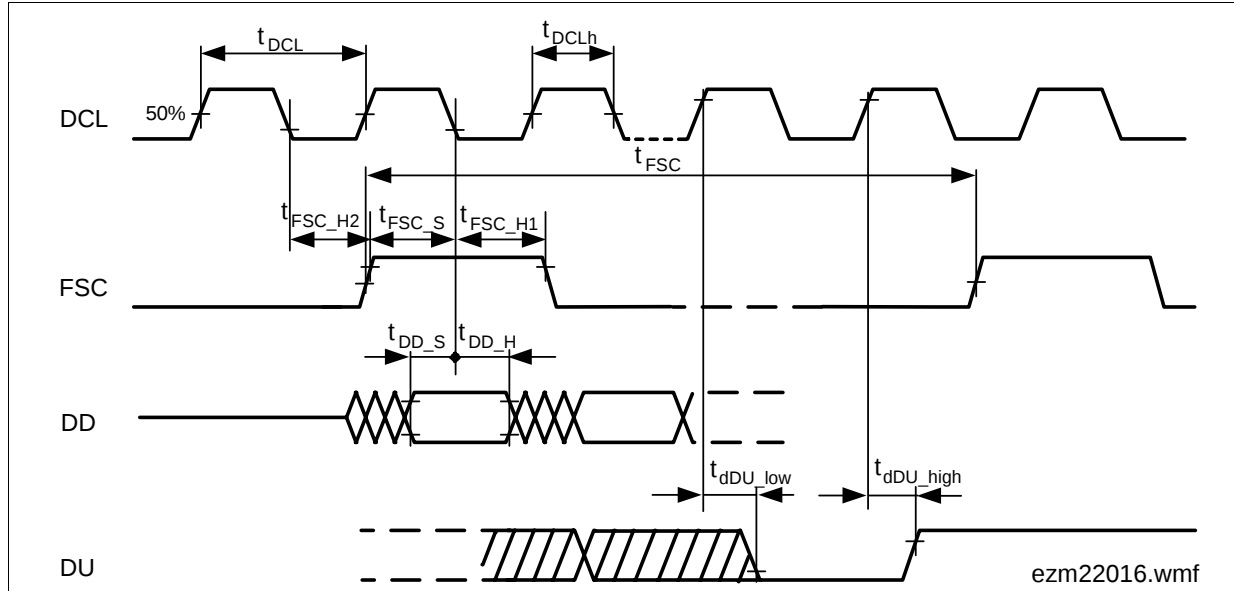


Figure 23 IOM-2 Interface Timing – Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL ¹⁾	t_{DCL}	–	1/2048	–	ms
DCL high time	t_{DCLh}	$0.4 \times t_{DCL}$	$0.5 \times t_{DCL}$	$0.6 \times t_{DCL}$	μs
Period FSC ¹⁾	t_{FSC}	–	125	–	μs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{DCL} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns
DU low time ²⁾	t_{dDU_low}	25	–	$t_{dDU_low (min)} + 0.4[\text{ns/pF}] \times C_{Load}[\text{pF}]$	ns
DU high time ²⁾	t_{dDU_high}	25	–	$t_{dDU_high (min)} + 2 \times R_{pull-up}[\text{k}\Omega] \times C_{Load}[\text{pF}]$	ns

¹⁾ The DCL frequency must be an integer multiple of the FSC frequency.

²⁾ DU low and high times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load} , $R_{Pullup} > 1.5 \text{ k}\Omega$)

6.4.5.2 Double-Clocking Mode

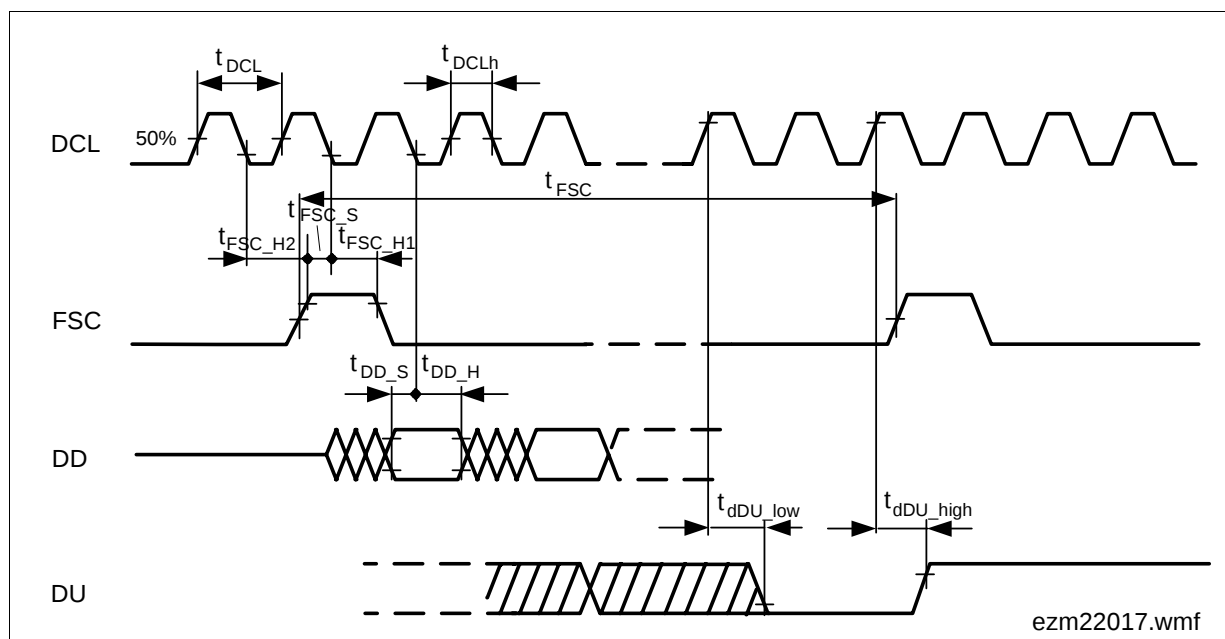


Figure 24 IOM-2 Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL ¹⁾	t_{DCL}	–	1/4096	–	ms
DCL high time	t_{DCLh}	$0.4 \times t_{DCL}$	$0.5 \times t_{DCL}$	$0.6 \times t_{DCL}$	μs
Period FSC ¹⁾	t_{FSC}	–	125	–	μs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{DCL} - t_{FSC_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns
DU low time ²⁾	t_{dDU_low}	25	–	$t_{dDU_low} (min) + 0.4[ns/pF] \times C_{Load}[pF]$	ns
DU high time ²⁾	t_{dDU_high}	25	–	$t_{dDU_high} (min) + 2 \times R_{pull-up}[k\Omega] \times C_{Load}[pF]$	ns

¹⁾ The DCL frequency must be an integer multiple of the FSC frequency.

²⁾ DU low and high times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load} , $R_{Pullup} > 1.5 \text{ k}\Omega$)

8 Glossary

8.1 List of Abbreviations

ACTL	Active with V_{BATL} and V_{BGND}
ACTH	Active with V_{BATH} and V_{BGND}
ACTR	Active with V_{BATR} and V_{GND} or V_{HR} and V_{BATH}
ADC	Analog Digital Converter
AR	Attenuation Receive
AX	Attenuation Transmit
BP	Band Pass
CMP	Compander
Codec	Coder Decoder
COP	Coefficient Operation
CRAM	Coefficient RAM
DAC	Digital Analog Converter
DSP	Digital Signal Processor
DUP	Data Upstream Persistence Counter
DuSLIC	Dual Channel Subscriber Line Interface Concept
EXP	Expander
FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
LSSGR	Local area transport access Switching System Generic Requirements
PCM	Pulse Code Modulation
PDH	Power Down High Impedance

Preliminary
Glossary

PDRHL	Power Down Load Resistive on V_{BATH} and V_{BGND}
PDRRL	Power Down Load Resistive on V_{BATR} and V_{BGND}
PDRH	Power Down Resistive on V_{BATH} and V_{BGND}
PDRR	Power Down Resistive on V_{BATR} and V_{BGN}
POFI	Post Filter
PREFI	Antialiasing Pre Filter
RECT	Rectifier (Testloops, Levelmetering)
SLIC	Subscriber Line Interface Circuit (synonym for all versions)
SLIC-S/-S2	Subscriber Line Interface Circuit Standard Feature Set PEB 4264/-2
SLIC-E/-E2	Subscriber Line Interface Circuit Enhanced Feature Set PEB 4265/-2
SLIC-P	Subscriber Line Interface Circuit Enhanced Power Management PEB 4266
<i>SLICOFI-2x</i>	Dual Channel Subscriber Line Interface Codec Filter (synonym for all versions)
SLICOFI-2	Dual Channel Subscriber Line Interface Codec Filter PEB 3265
SLICOFI-2S/-2S2	Dual Channel Subscriber Line Interface Codec Filter PEB 3264/-2
SOP	Status Operation
TG	Tone Generator
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TS	Time Slot
TTX	Teletax

Preliminary

Index

9 Index**A**

Active 23
Active High 18
Active Low 18
Active Ring 18
Active with HIR 18
Active with HIT 18
Active with Metering 18

B

Battery feed 3, 4, 11

C

Caller ID 3, 12, 17
Coding 11

D

DTMF 12
DTMF decoder 3, 12
DTMF generator 3, 4, 12
DuSLICOS 12

E

External Ringing 9

F

Frequency response 11, 36
FSK 12

H

Hybrid 11
Hybrid balance 11

I

Impedance matching 11
IOM-2 interface 7

L

Line Echo Cancellation 12

M

Message waiting 3
Metering 3, 4

O

Overvoltage protection 11

P

PCM interface 8, 45
Polarity Reversal 3, 4
Power Down High Impedance 18, 22
Power Down Resistive 18, 20, 21, 22, 23
Power Management 3, 4

R

Receive gain 11
Ring Pause 19
Ringing 11, 18

S

Signaling 11, 15
Sleep 18, 31
SLIC Interface 20, 21
Supervision 11

T

Teletax Metering 12
Transmit gain 11, 36
TTX 11

U

Universal Tone Detection 12

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