IR1110 Soft Start IC Reference Design Kit

For AC Motor Drives, UPS, Welders, and other applications

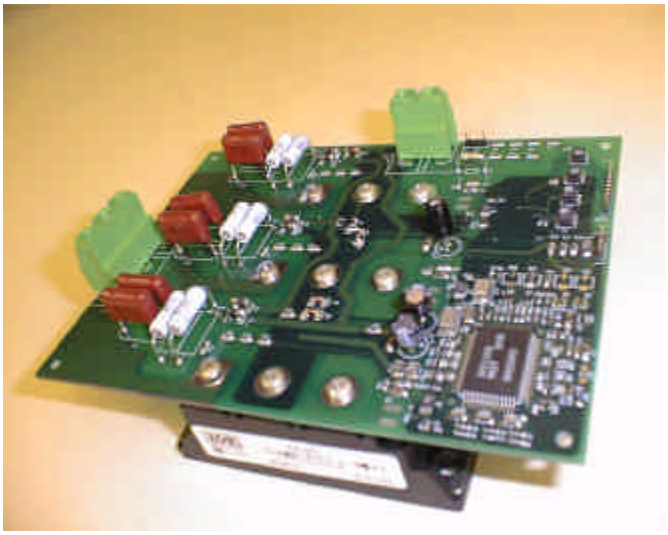


Figure 1 IRMDSS1 IR1110 Reference Design Kit

- Complete stand alone converter system
- IR1110 advanced monolithic soft start IC
- IRKH SCR/Diode Modules
- Up to 20HP drive capability and expansion option of 60HP with added busbars
- Easily detachable SCR/Diode modules
- 230/460/575V AC input voltage with 320V-550V factory setting
- On-board snubber derived +15V, +5V, and –5V power supply
- Automatic soft charging of DC bus capacitor with adjustable ramp rate
- Controllable DC bus voltage output
- Isolated control inputs for DC bus reference command and override reset function
- Isolated diagnostics outputs for line status
- Protection against DC bus short condition and AC line loss condition
- Fast automatic ramp-back of the DC bus voltage after transient loss of line
- Terminal blocks for 3-phase AC input and DC bus output, up to 40A.

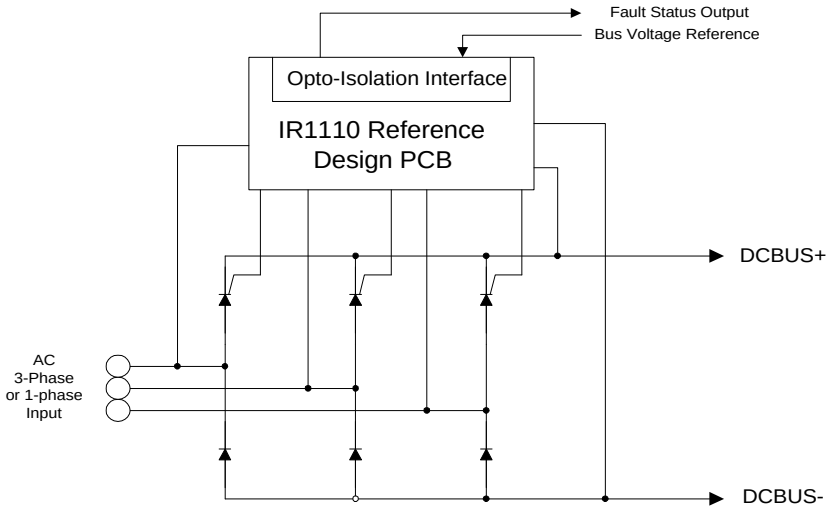


Figure 2 Block Diagram

1. Introduction

The IR 1110 Soft Start Control IC for a 3-phase half-controlled SCR bridge offers a superior means of precharging the dc bus capacitor, in systems such as variable frequency motor drives. It eliminates the commonly used capacitor precharge resistor, and offers other major system operating advantages, as highlighted below.

The purpose of the IR 1110 Reference Design is to provide the potential user of the IR 1110 ASIC with a fully functional front-end converter, that can be quickly and easily connected into an overall system, for the purpose of demonstrating the operation, evaluating system performance, and reducing design-in time.

The IR 1110 Reference Design, shown in Fig. 1, is a self-contained input converter assembly, that accepts three phase or one phase ac line power and delivers controlled dc output to an external bus capacitor and load. A basic schematic is shown in Fig 2.

The Reference Design consists of a PCB, containing IR 1110 Soft Start Controller IC and peripheral components, and three attached IRKH SCR/Diode Add-a-pak modules. The IR 1110 and peripheral circuits float at the potential of the positive terminal of the rectifier, and drive the SCR gates directly without isolation. Opto-couplers mounted on the PCB deliver isolated line fault feedback signals.

Snubbers mounted on the PCB provide dv/dt protection for the SCRs. DC supply voltage for the IR 1110 is derived from the snubber current, and no additional external power supply is required when operating from 3-phase input. When operating continuously from one phase input, an external power supply may be required. (see Section 4 (j))

It is necessary only to mount the SCR modules to a heatsink, connect ac power to the input terminals, and dc bus capacitor and load to the output terminals. The IR 1110 Reference Design is then ready for operation.

This Manual provides information necessary to operate the IR 1110 Reference Design as a functional unit. It is recommended that the user also review the data sheet for the IR 1110 ASIC.

2. Input voltage and output current ratings.

The IR 1110 Reference design is fitted with IR's 1600V rated IRKH series Addapak SCR-diode modules. Components on the PCB are factory set for an input operating voltage range of 320V to 550V rms, 3-phase, 47 to 63Hz. Operation at other input line voltages is possible by changing component values on the PCB, as specified in Table 1.

The IR 1110 Reference Design can be set up for dedicated 1-phase operation, as detailed in Table 1.

The rated continuous dc output current for 3-phase operation with the factory-fitted terminal blocks (JP2 and JP3), is 25A at 30°C.

Higher output current, to 40A DC continuous, can be obtained by replacing JP2 and JP3 with the larger optional terminal blocks, (see Bill of Material), mounted into holes provided on the PCB. For this current, air flow of approximately 20CFM should be directed across the surface of the PCB. A small muffin fan is suitable for this purpose.

Output current above 40A can be obtained by removing the JP2 and JP3 terminal blocks, remounting the SCR snubber components on the underside of the PCB, and attaching spacers and busbars to the top of the PCB, as illustrated in Fig. 3.

Table 2 gives typical dc output current ratings for 3-phase operation with added busbars, for IRKH Addapak modules of different ratings.

Module type	DC Current	Total power per Module	Continuous motor HP
	A	W	
IRKH41	65	75	25
IRKH56	90	86	30
IRKH71	120	112	50
IRKH91	145	149	60
IRKH105	180	196	75

TABLE2. OUTPUT CURRENT OF THREE PHASE BRIDGE AT MAXIMUM OUTPUT VOLTAGE FOR VARIOUS IRKH SERIES MODULES

Note: 1. Tcase = 90°C max, Tjpk = 115°C
2. SCR conduction assumed to be just continuous. Actual conduction angle is governed by ac and dc inductance.
3. Continuous motor HP based on 150% output for 1 minute.

3. Setting up the IR 1110 Reference Design for use.

1. Mount the three IRKH Addapaks on a heatsink. A drill plan for the mounting holes in the heatsink are shown in Fig 4.
   The heatsink must be able to maintain the case temperature of the Addapaks at less than 90°C, at full output current. Typical losses in each Addapak module, for 3-phase operation, are given in Table 2.

2. Position the PCB over the Addapak modules, fitting the gate and auxiliary cathode fast-on terminals attached to the modules into the slots in the PCB. Insert washers between the module terminals and the holes in the PCB. Insert M5 screws with washers through the holes on the PCB, through the washers on the underside of the PCB, into the terminal holes of the modules, and tighten. Solder the top stems of the fast-on terminals into the PCB.
   For dc current greater than 40A, remove JP2 and JP3 and assemble as illustrated in Fig 3.

3. Make electrical connections as shown in Fig 5.

The IR 1110 Reference Design is now ready for use.

4. Operating features.

4(a) *Soft charging of the dc bus capacitor.*

When ac input voltage is switched on, the voltage across the dc bus capacitor ramps up automatically, by phase-control of the SCRs.

The ramp-up rate is determined by capacitor (C24 + C24A). The factory-fitted value is 3µF. The corresponding ramp-up time is approximately 330ms.

The ramp-up time can be reduced by reducing the paralleled combination of C24 and C24A. For example, with C24A removed, and C24 = 1.0uF, the ram-up time is approximately 150ms.

4(b) *Regulation of the dc bus voltage.*

The operating bus voltage can be regulated by one of the following methods:

(1) Control of an externally applied 1.4 to 4.0V (nominal) reference voltage, VBUSREF, applied between JP4/1 and JP4/2. (JP4/1 negative with respect to JP4/2)

For test purposes, the bus voltage can be controlled manually, by connecting a 50k0 potentiometer between JP4/1 and JP4/3, and changing R52 to 4.53k, (1%).

Control of the potentiometer resistance from 0 to 50k controls VBUSREF from approximately 4.0V to 1.4V . This controls the dc bus voltage from maximum to approximately 35% of the maximum value obtained at maximum input line voltage; e.g. for the factory setting of 550V rms maximum input voltage, the minimum regulated bus voltage is about 270V dc.

It should be noted that the potentiometer floats at the potential of the positive terminal of the SCR bridge. Care must be taken to ensure that **the knob of the potentiometer is properly isolated**, to avoid the possibility for electrical shock when manually adjusting the potentiometer.

(2) A PWM signal can be applied to the input of opto-coupler U5, between JP5/1 and JP5/2, as shown in Fig 6. The opto-coupler provides isolation between the PWM input source and the IR 1110, which floats at the potential of the positive terminal of the rectifier.

The frequency of the PWM signal should be in the 1 to 5kHz range.

The relationship between the ON/OFF duty cycle, D, of the PWM input and the dc bus voltage is approximately:

$$VBUS = VBUSmax\ (0.35 + 0.65D)$$

VBUSmax is the maximum bus voltage at maximum input voltage.

The bus voltage is regulated to within approximately +-8V, for a change of line voltage of +-80V.

Rise and fall rates of the bus voltage that are driven by changes in the duty cycle, D, (hence in the average value of VBUSREF), are determined by the rate of change of D, and by the load characteristics. The rate of increase of D should be limited to avoid excessive bus capacitor charging current.

4(c) *Adjusting the dc loop gain.*

The voltage regulation loop can exhibit uneven timing between successive SCR firing points, with loads that have abnormally high ripple voltage. Such ripple instability - should it occur - can be corrected by reducing the dc loop gain.

Remove the zero ohm link R58. Re-insert R58, and insert R54 with values calculated as follows.

The dc loop gain will be reduced by a factor of R54/(R54+R58). R54 and R58 should be chosen so that their sum is 200-250k Ohms.

4(d) *Deactivating the voltage regulation function.*

If regulation of the bus voltage is not required, i.e. the rectifier is always required to deliver maximum possible dc bus voltage in normal operation, connect JP4/1 to JP4/3.

Note that the soft start function is always activated, whether or not the voltage regulation function is used.

4(e) *Low line voltage.*

If the input line voltage falls below the specified minimum operating value, as shown in Table 1, the rectifier is deactivated by removal of the SCR firing pulses. When the line voltage returns to normal, the bus voltage is automatically ramped back to the set value.

4(f) *Temporary loss of all three input line voltages.*

When all three input phases are temporarily lost, the dc bus voltage starts to decreases during the outage.

(a) If the bus voltage does not dip below a set fraction, k, of the initial operating bus voltage, VBUS1, then when the input voltage returns, the bus capacitor is recharged without phase-control of the SCRs. This allows the bus voltage to be restored as quickly as possible for relatively minor dips of bus voltage, and minimizes the effect of the line outage on system operation.

k is given approximately by the following relationship:

$$k\ VBUS1 = \left(\frac{R80}{R79 + R80} VBUS1\right) - 0.1\ VLLmax$$

$$= 0.75\ VBUS1 - 0.1\ VLLmax$$

Note that the value of k can be adjusted, if needed, by changing the value of R79.

(b) If the bus voltage dips below k VBUS1 during the line outage, then when the input voltage returns, the dc bus voltage is ramped back by SCR phase control.

4(g) *Temporary loss of one input phase.*

If one input phase is lost during 3-phase operation, for more than 1 to 1 1/2 cycles, the SCR firing pulses are removed, deactivating the rectifier. When the missing phase returns, the bus voltage ramps back to the set value.

Without this one-phase shut-down function, the following operating problems could occur:

(a) If one input phase is lost while the bus voltage is being regulated to less than the maximum value, the rectifier output voltage can transiently jump to the maximum value when the missing phase returns.

This is undesirable, unless there is sufficient inductance in the ac input lines, or in the dc smoothing inductor, (if used), to limit the resulting current.

(b) Transient loss of one phase during the early part of initial ramp-up can cause a jump of bus voltage to the maximum value, if the missing phase returns while ramp-up is still in progress.

For these reasons, the IR 1110 Reference Design is factory-set with the one-phase shut-down function enabled.

4(h) *Disabling one-phase shut-down at maximum bus voltage, if the voltage regulation function is not used.*

If the bus voltage regulation function is not used, it may be desired to disable the one phase shut-down function in normal

operation, allowing the rectifier to operate as a one phase bridge when one phase is missing.

Note that these remarks apply to loss of one phase when the IR1110 is set for normal 3-phase operation. If the IR1110 is set for dedicated 1-phase operation (See Table 1), the 1-phase shut down function is inactive.

The following modifications disable the one-phase shut-down function at full bus voltage - but keep this function enabled when the output voltage is below a set value during ramp-up.

(1) Cut traces and add link as illustrated in Fig 7.
(2) Remove R92, R7.
(3) Add D14, R6, R95, R96, D15, Q5, Q6. Connect 0.1µF across base and emitter of Q7. Add diode (MA 116CT) across the open R85 pads, with cathode towards pin 41 of the IR 1110.

(4) Change R101 to 220k, R100 to 0 Ohm link.
(5) Change R53 to 470k, 5%, 1/16W. Change C19 to 0.1µF, 6.3V, 10%. Remove R58, insert R57 (0 Ohm, link).

4(i) *DC bus short-circuit.*

When operating from a 3-phase supply, the IR 1110 Reference Design automatically limits the fault current when the dc bus is short-circuited.

If a bus short-circuit exists when the line voltage is switched on, the SCR firing angle will not advance to more than about 35 electrical degrees ahead of the line voltage crossover.

If a bus short-circuit occurs during operation, the SCR firing angle is phased back in less than half a cycle, to within about 35 electrical degrees of the line voltage crossover.

Short circuit current is thus limited to a much lower level than would be obtained with an uncontrolled rectifier bridge.

Note that this function is active when the IR 1110 Reference Design is set up for 3-phase operation, but not for dedicated 1-phase operation.

4(j) *Omission of on-board SCR Snubbers/use of external-power supply.*

The on-board SCR snubbers may not be required for dv/dt protection, if external ac line filters are fitted.

If the on-board snubbers are omitted, it will be necessary to provide external isolated +-15V (20mA) power to the PCB. The required power supply connections to the PCB are shown in Fig 8.

Remove the following snubber and associated components: C13, C14, R43, R44, D1, D2, R45, D3, C15, C16, R46, R47, D5, D6, R48, D7, C17, C18, R49, R50, D9, D10, D11.

On-board dropping resistors and zener diodes create the required internal +5V and -5V power for the IR 1110, from the applied +-15V input. The rise time of the +-15V voltages during power-up should not be less than 1 millisecond.

The primary source for the power supply must be derived from the ac input voltage of the rectifier bridge. It cannot be taken from the main dc bus voltage, because this voltage does not exist until after the IR 1110 has been energized. During power-up, the input to the power supply must be switched on synchronously with the rectifier input voltage.

4(k) *External shut-down.*

External shut-down of the rectifier bridge is implemented by applying a 15mA input to opto-coupler U7, at JP5/3 (+) and JP5/4.

5 . Fault feedback signals.

Isolated fault feedback signals are delivered at the outputs of opto-couplers U6 and U4, as shown in Fig 9(a) for the IR 1110 Reference Design, as factory-set. U6 delivers a multiplexed 3-phase loss/1-phase loss signal; U4 delivers a low line-voltage signal.

An integral part of the circuit modification described in Section 4(h), is that opto coupler U6 delivers a 3-phase loss fault signal only, without the multiplexed 1-phase loss signal. The one-phase loss signal is now multiplexed with the low line signal. The fault signals for this mode are illustrated in Fig 9(b).

6 . Use of the PCB with an external SCR half-controlled bridge.

For test purposes, the IR 1110 Reference Design PCB by itself can be used with an external SCR half-controlled bridge. This is done by detaching the PCB from the IRKH Addapak modules, and making wired connections between the PCB and the external SCR bridge.

Fig 10 shows a connection diagram. Note that the wires from JP2, U, V, W, and the wire from JP3/1, should be run as a twisted bundle. The gate and auxiliary cathode leads for each SCR should be run as twisted pairs. Also note that zero ohm links must be connected across the open pads R13, R17, R21 that connect to the auxiliary cathode slots on the PCB.

7 . Inductance.

During ramp-up, as the SCR firing angle advances, the bus capacitor is charged by a succession of current pulses. The peak value of these pulses depends upon the dc bus capacitance, the ramp rate, and the total inductance, i.e. the sum of the ac line inductance and dc smoothing inductance, (if present), in series with the bus capacitor.

The inductance needed to limit the normal peak operating current at full bus voltage will typically also limit the peak current during ramp-up to an acceptable level. Typically, the source inductance of the line voltage will be sufficient for this purpose.

Table 3 shows typical maximum peak values of the current pulses during ramp-up, for various values of bus capacitance and line inductance, based on the assumption that there is no dc smoothing inductance. Compatible values of full load dc current are shown. These line inductance values correspond to an ac source reactance of about 2%, i.e. the voltage across each line inductance at full current is about 2% of the line to neutral voltage at 50Hz.

8 . Schematics and Bill of Material.

Schematics and Bill of Materials for the IR1110 Reference Design are shown on the following pages.

Option	Input Voltage (47 - 63Hz)	Phase	Nominal low line shut-down	R1 through R11, R25 through R36	C23 C26 C29	R82	R90	R86 R87 R88	C13 through C18	R43 R44 R46 R47 R49 R50	R55	R56	Components Omitted
	Vrms		Vrms										
Factory setting	320-550	3	290	464k 1% 1/8W	.0082uF 2%	453k 1% 1/16W	1.0M 5% 1/16W	866k 1% 1/16W	.33uF 630V	47 Ohm 5W	IN	OUT	
1	380-660	3	345	562k 1% 1/8W	.0082uF 2%	536k 1% 1/16W	1.0M 5% 1/16W	866k 1% 1/16W	.27uF 630V	47 Ohm 8W	IN	OUT	
2	160-280	3	145	232k 1% 1/8W	.0082uF 2%	226k 1% 1/16W	1.0M 5% 1/16W	866k 1% 1/16W	C14 C16 C18 = .33uF, 630V	R44 , R47 , R50 = 47 Ohm 5W	IN	OUT	Replace C13,C15 C17,R43,R46,R49 with shorting links
3	160-280	1	145	232k 1% 1/8W	.0068uF 2%	226k 1% 1/16W	3.0M 5% 1/16W	1.0M 1% 1/16W	C14 C16 C18 = .33uF, 630V	R44 , R47 , R50 = 47 Ohm 5W	OUT	IN	Replace C13,C15 C17,R43,R46,R49 with shorting links. Omit R25, R26,R27,R61,R76 R78,R88,C29,C34
4	80-140	1	72	115k 1% 1/8W	.0068uF 2%	113k 1% 1/16W	3.0M 5% 1/16W	1.0M 1% 1/16W	C14 C16 C18 = .68uF, 400V	R44 , R47 , R50 = 22 Ohm 3W	OUT	IN	Replace C13,C15 C17,R43,R46,R49 with shorting links. Omit R25, R26,R27,R61,R76 R78,R88,C29,C34

TABLE 1. INPUT LINE VOLTAGE OPTIONS AND CORRESPONDING COMPONENT VALUES.

TABLE 3. TYPICAL PEAK PULSED CHARGING CURRENT DURING RAMP-UP

Bus Capacitance	Inductance per line	Approx. peak pulsed charging current (2ms typ.)	Typical full load dc current
uF	uH	A	A
1500	625	80	20
2000	420	115	30
2500	340	140	40
4000	210	240	70
6000	135	330	100
8500	105	460	140

NOTES
(1) 460V 50HZ line input
(2) Zero DC Inductance
(3) Values of line inductance correspond to about 2% line reactance for the full load current.

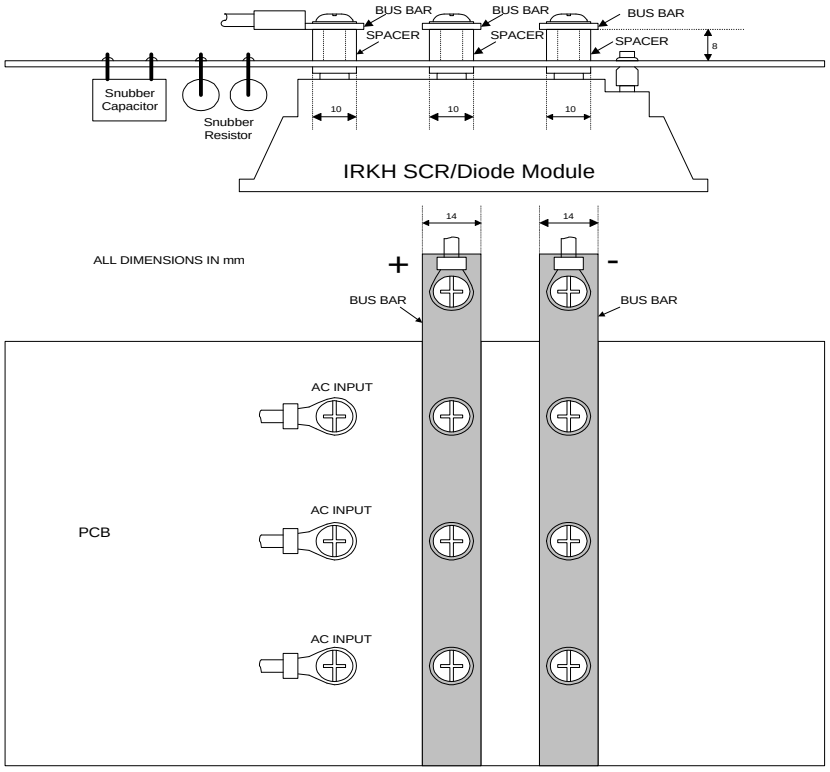


Figure 3 AC input / DC output Power Connections for high (>40A) current

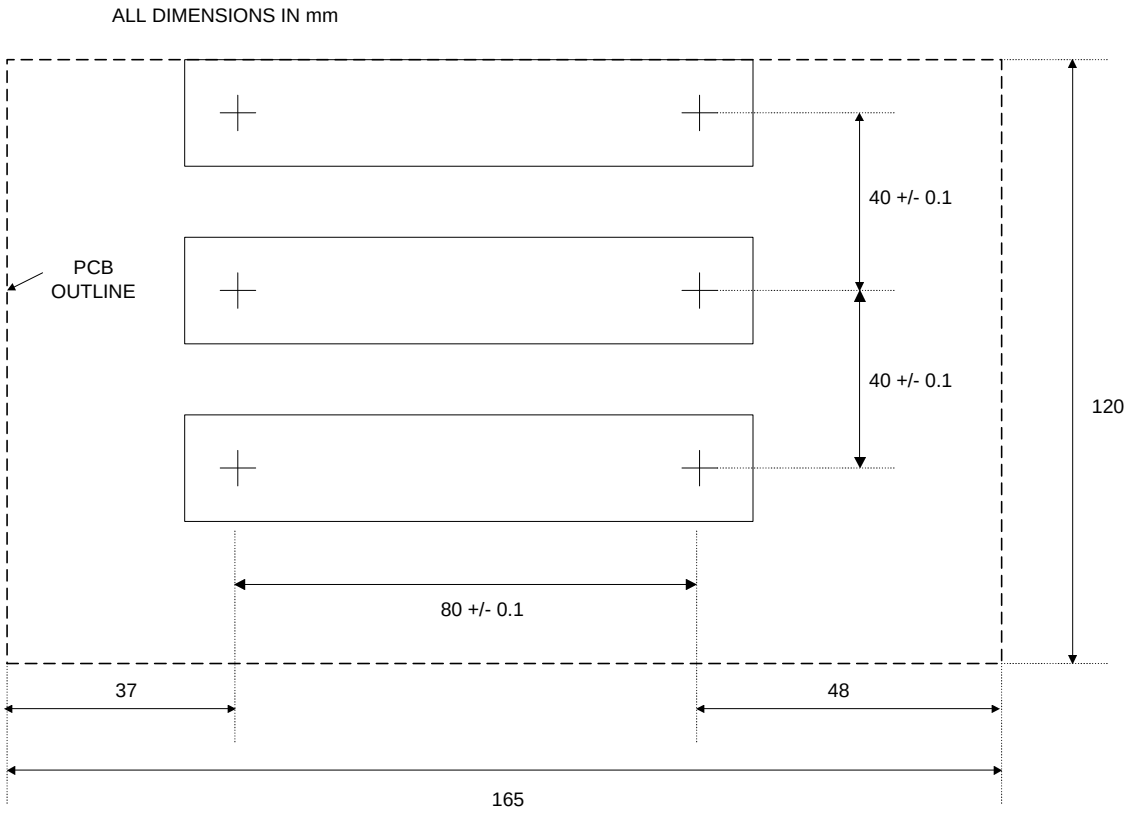
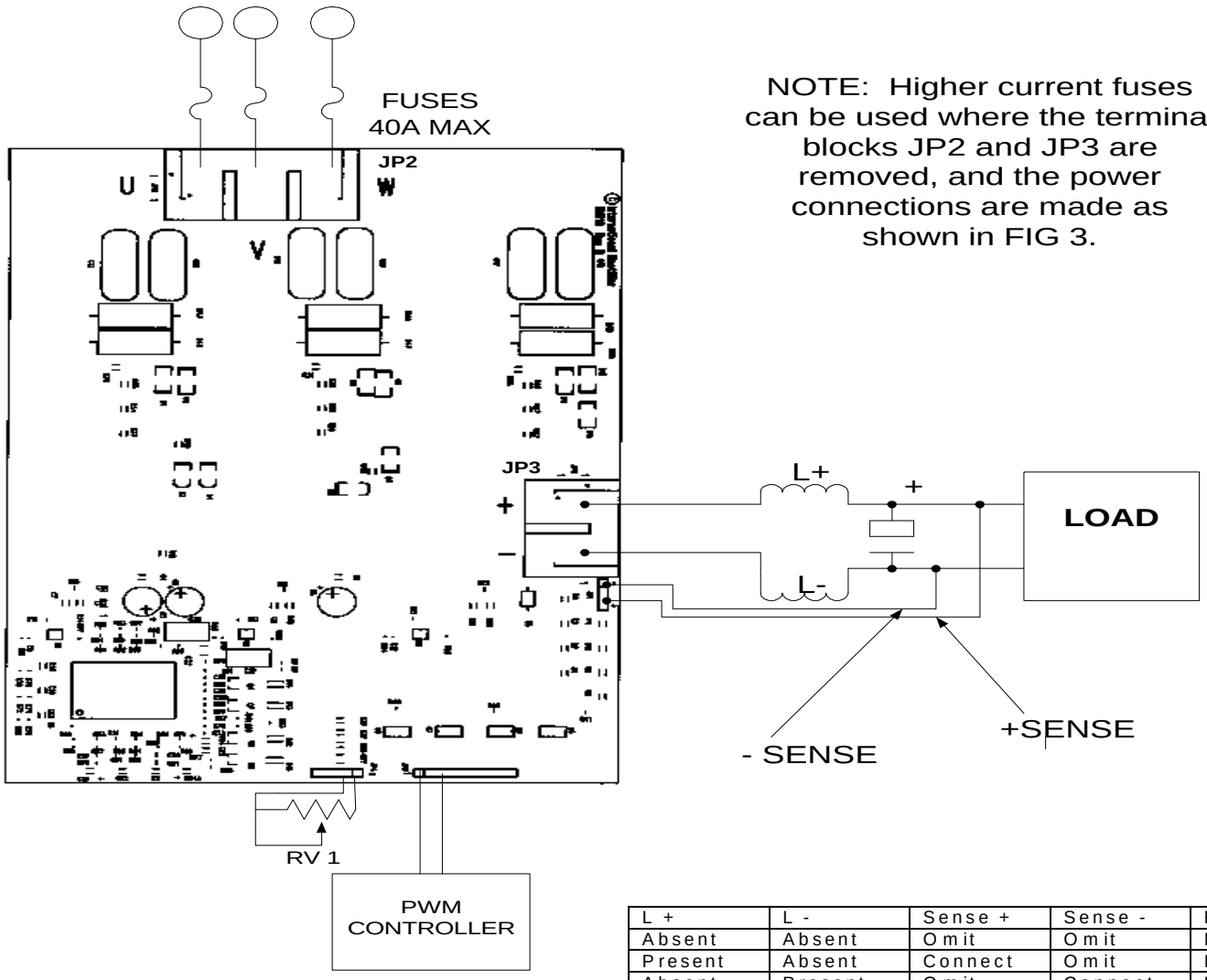


Figure 4 Mounting Holes Dimension for Heatsink

FIG 5 . Electrical Connections to the IR1110 Reference Design.



NOTE: Higher current fuses can be used where the terminal blocks JP2 and JP3 are removed, and the power connections are made as shown in FIG 3.

L +	L -	Sense +	Sense -	R5
Absent	Absent	Omit	Omit	Inserted
Present	Absent	Connect	Omit	Inserted
Absent	Present	Omit	Connect	Remove
Present	Present	Connect	Connect	Remove

Bus voltage regulation	RV 1	PWM Controller	Comments
Max voltage only	Not needed. Connect JP4/1 to JP4/3	Not needed.	
Manual potentiometer control	Connect RV 1 (50k) . Change R52 to 4.53k 1%. See sect. 4(b)	Not needed.	CAUTION: RV1 at potential of rectifier pos. term .
Isolated PWM input	Not needed. No connection to JP4/1	Connect to JP5/1 (+) and JP5/2. See also Fig6	

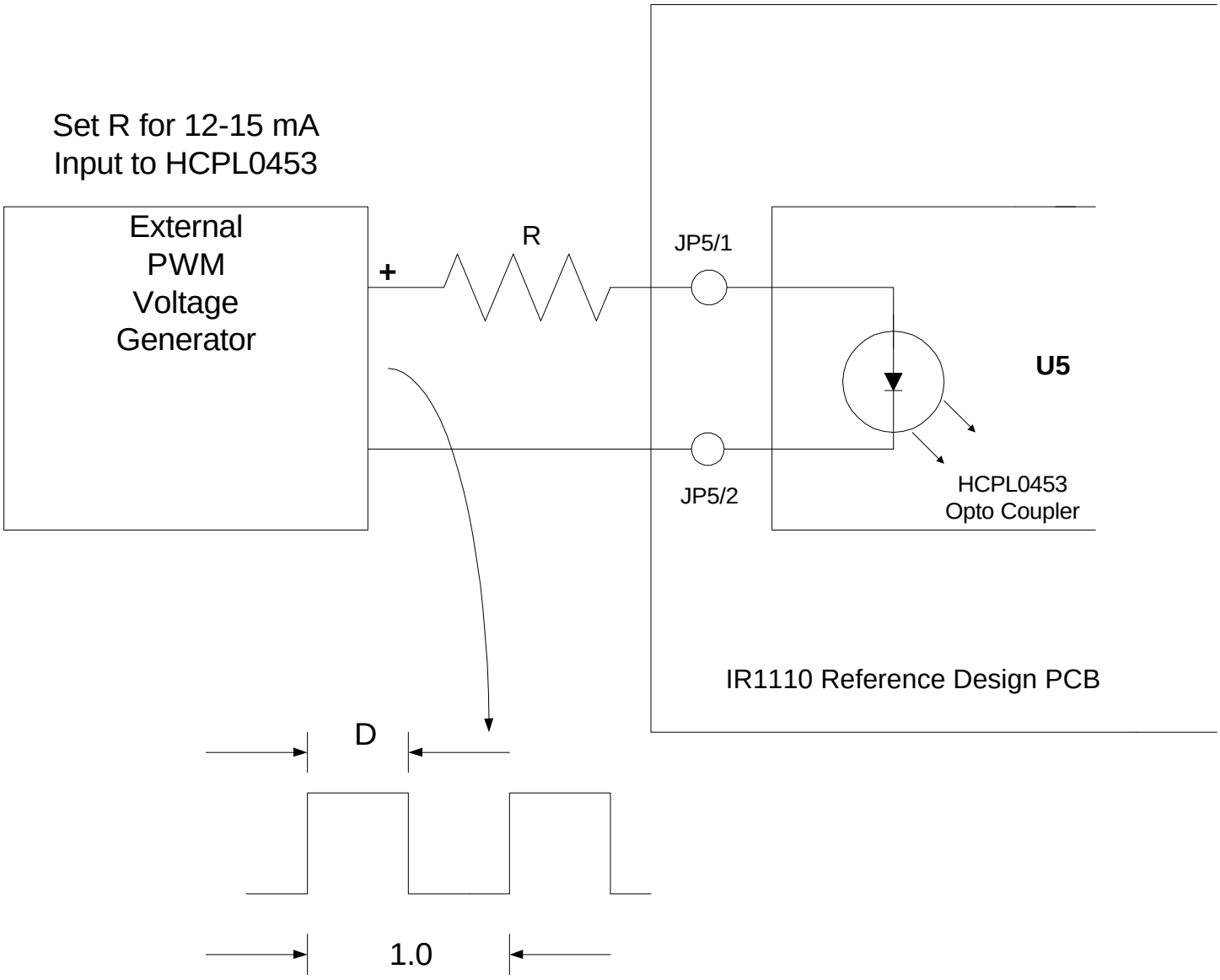
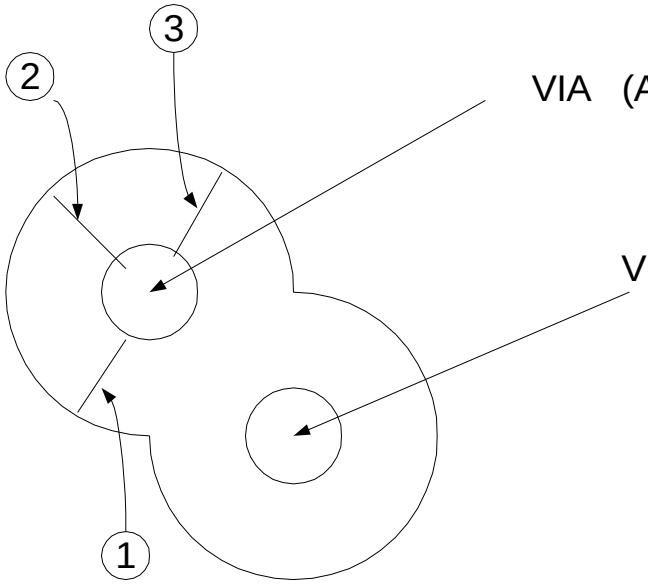


FIG 6 . PWM INPUT FOR CONTROLLING THE DC BUS VOLTAGE.

(a) BEFORE CHANGE

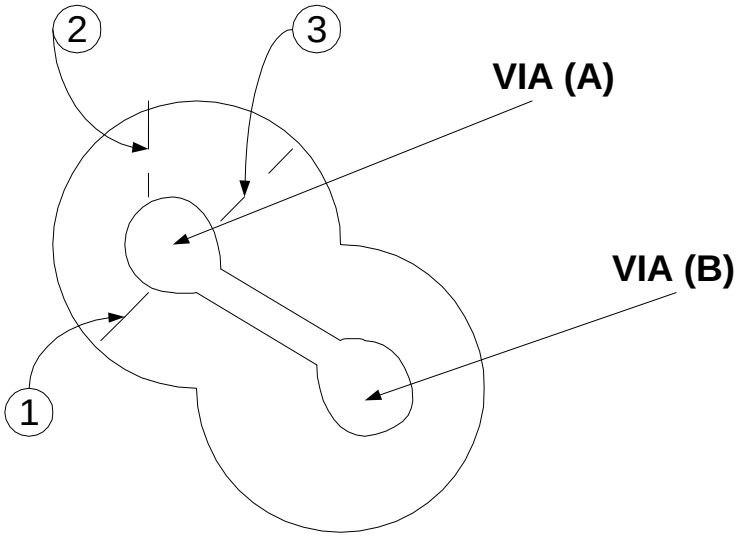


VIA (A) CONNECTED TO PIN 13 OF IR1110

VIA (B) CONNECYED TO PIN 14 OF IR1110

BOTTOM OF PCB

(b) AFTER CHANGE



CUT TRACE (1), (2), (3), LINK VIA (A) TO VIA (B)

FIG7. PCB Trace changes for the modification described in section 4(h).

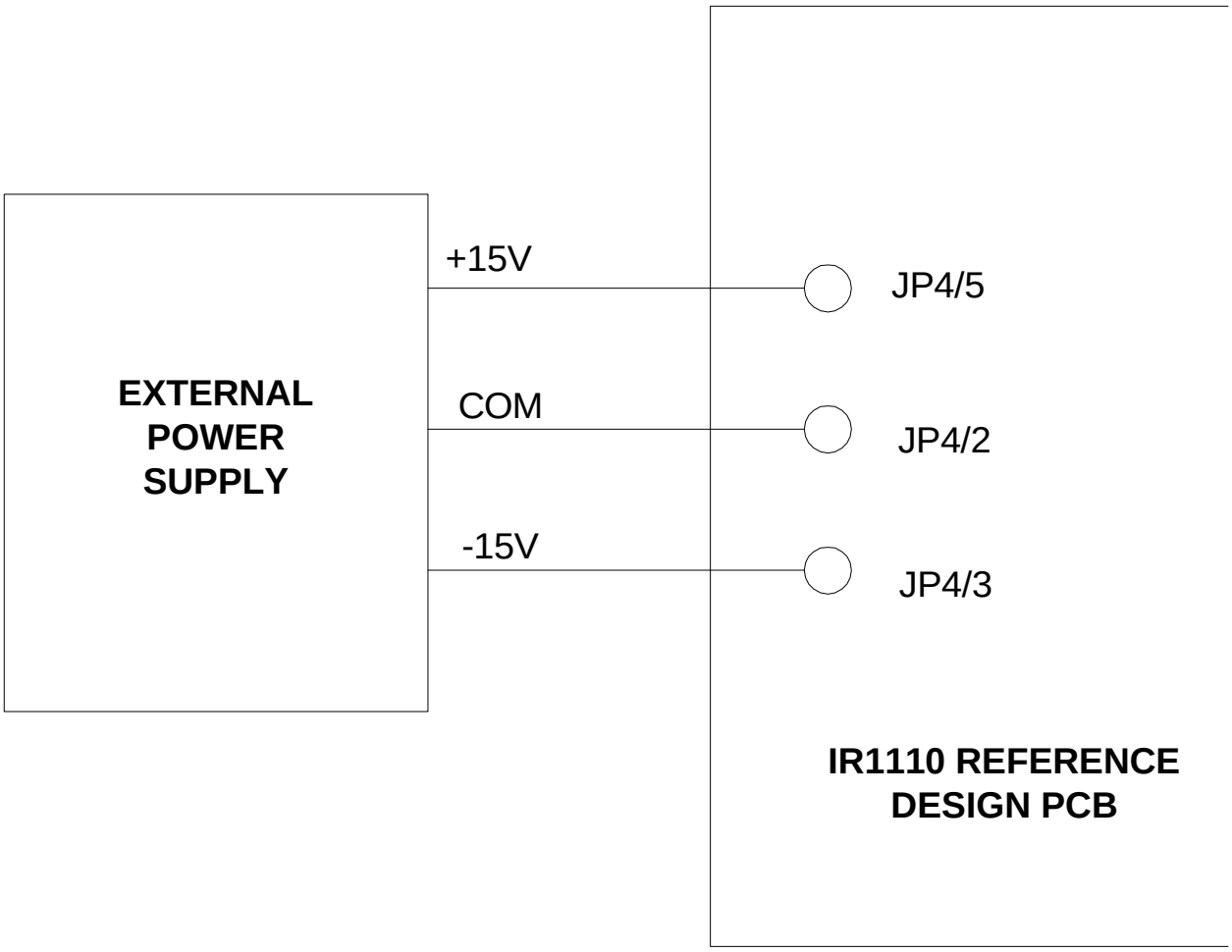
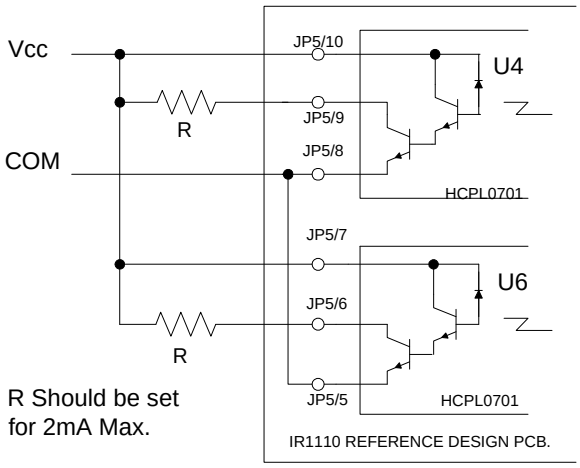


FIG8. CONNECTION OF EXTERNAL POWER SUPPLY.



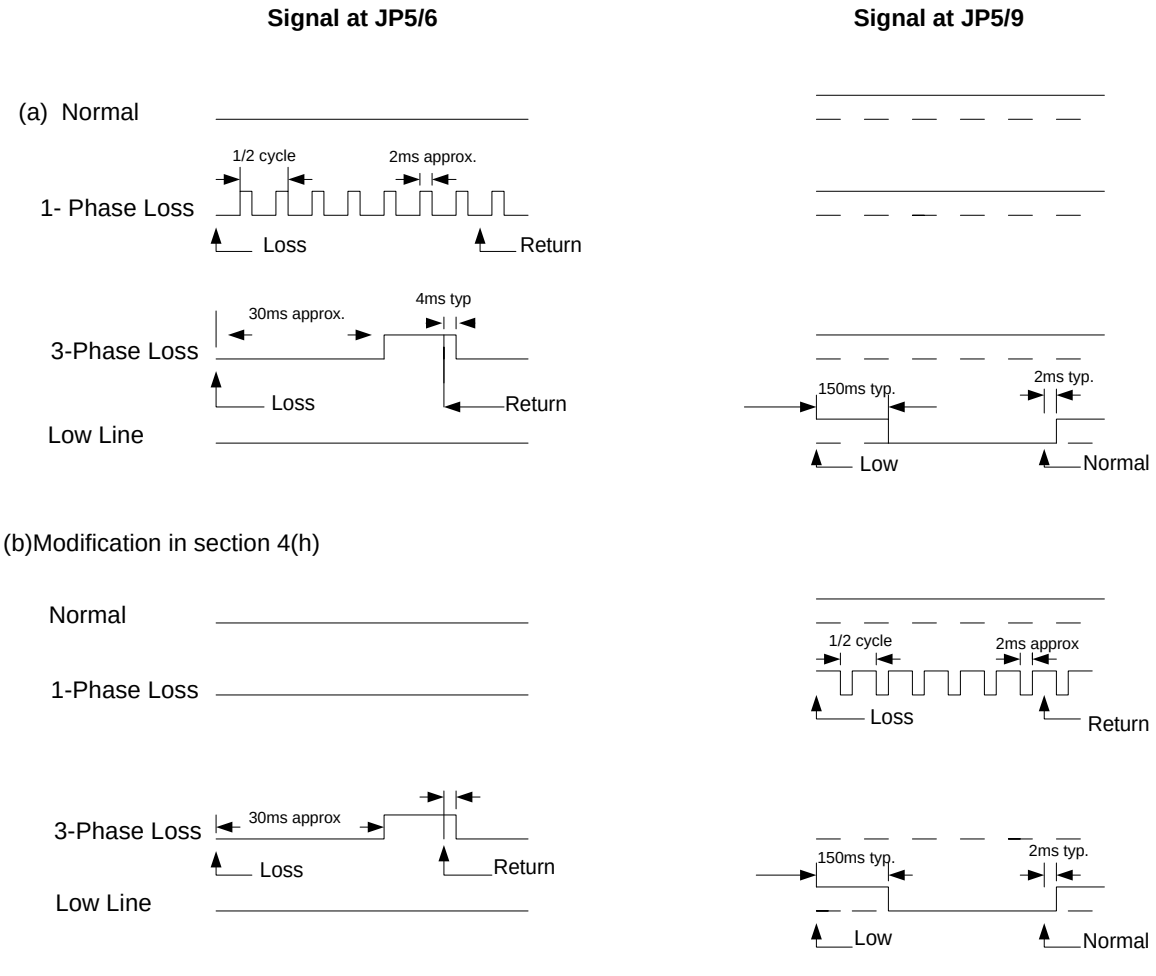


FIG9 FAULT SIGNALS (THREE PHASE OPERATION)

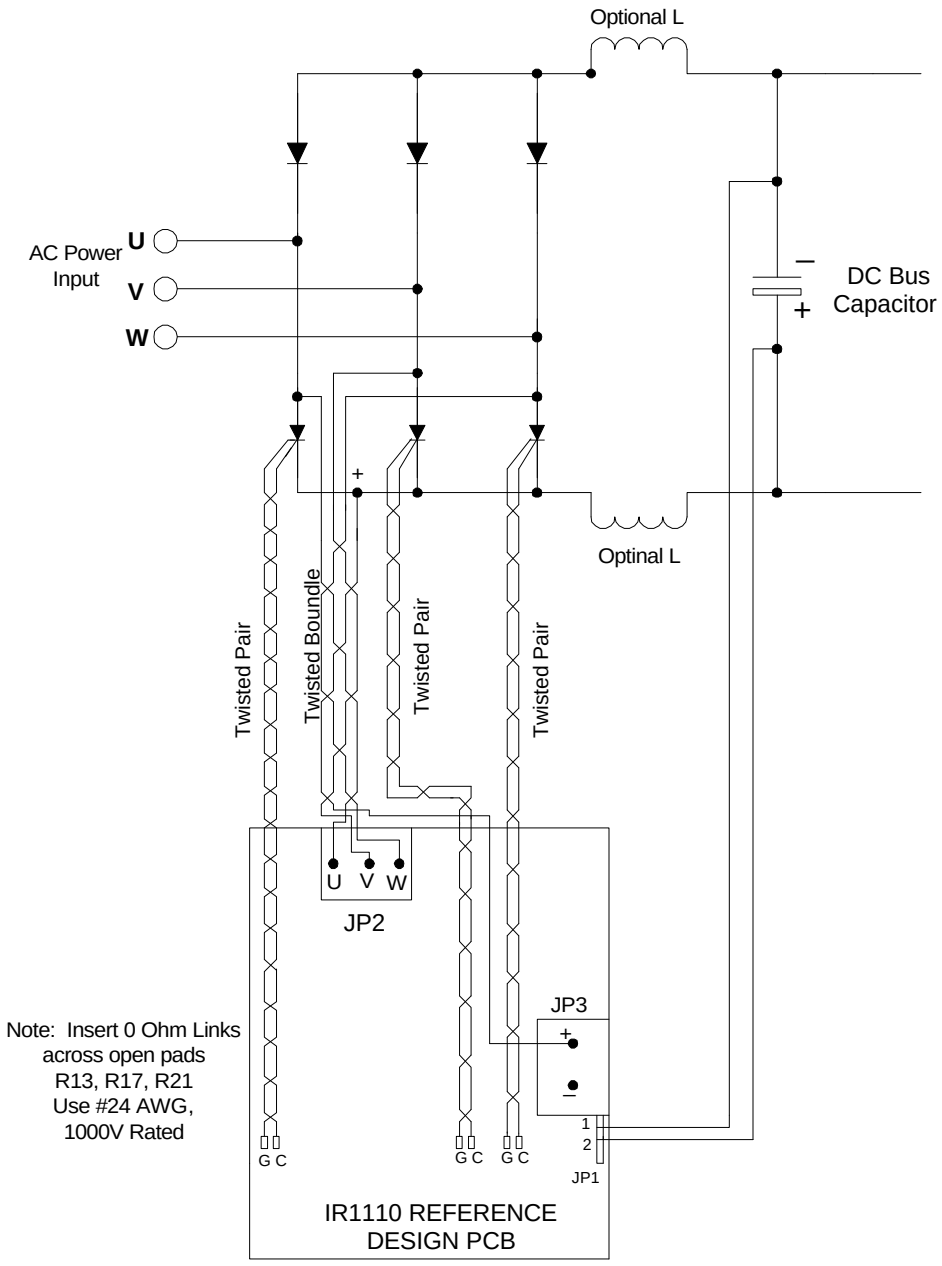


FIG 10 Connection Diagram for use of PCB with external SCR Half-Controlled Bridge.

SOFT START REFERENCE DESIGN KIT Revised: Tuesday, February 16, 1999
IRMDSS1 Revision: 1.0

Bill Of Materials February 18,1999 9:54:44 Page1

Item	Quantity	Reference	Part
1	2	C1,C3	330u 6.3V
2	7	C2,C4,C6,C7,C9,C11,C25	.1uF 10% 50V
3	1	C5	100u 16V
4	3	C8,C10,C12	.0047uF 25V
5	6	C13,C14,C15,C16,C17,C18	.33u 630V
6	1	C19	.22u
7	1	C20	.001u
8	1	C21	.022u
9	1	C22	.1u 10% 50V (Not inserted)
10	3	C23,C26,C29	.0082uF 50V
11	2	C24,C24A	1.5u
12	1	C27	.1uF 5% 16V
13	1	C28	1000P
14	1	C30	3300P
15	2	C31,C35	.33uF 16V
16	3	C32,C33,C34	.027u
17	6	D1,D2,D5,D6,D9,D10	DL4002
18	3	D3,D4,D8	5.1V 500mW 5%
19	1	D7	6.8V 5% 1W
20	1	D11	15V 5% 1W
21	4	D12,D13,D14,D15	MA116CT (Note: D12, D14, D15 Not inserted)
22	1	JP1	DC BUS KELVIN INPUTS
23	1	JP2	630V 32A 3P
24	1	JP3	630V 32A 2P
25	1	JP4	5PIN HEADER
26	1	JP5	10PIN HEADER
27	3	Q1,Q2,Q3	IRKH91-16
28	4	Q4,Q5,Q6,Q7	FMMT4401CT (Note: Q5, Q6 Not inserted)
29	8	R1,R2,R3,R4,R8,R9,R10, R11	442k 1%
30	1	R5	1 5%
31	12	R7,R13,R17,R21,R39,R55, R56,R57,R58,R64,R85,R94	0 link (Note: R13,R17,R21,R56,R57, R85,R94 Not inserted.)
32	1	R12	150
33	3	R14,R18,R22	56
34	3	R15,R19,R23	43
35	3	R16,R20,R24	5.6K
36	12	R25,R26,R27,R28,R29,R30, R31,R32,R33,R34,R35,R36	464K 1%
37	2	R38,R37	1K 5% 1/8W
38	1	R40	1.69K 1%
39	1	R41	2K 5% 1/16W

SOFT START REFERENCE DESIGN KIT Revised: Tuesday, February 16, 1999
IRMDSS1 Revision: 1.0

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Item	Quantity	Reference	Part
40	2	R92,R42	6.2K
41	6	R43,R44,R46,R47,R49,R50	47 5W
42	1	R45	220
43	1	R48	75
44	1	R51	16.9K 1%
45	1	R52	6.34K 1%
46	1	R53	2M 5% 1/16W
47	3	R54,R71,R101	100K (Note: R54 Not inserted)
48	5	R59,R60,R61,R62,R63	9.09K 1%
49	1	R65	430K
50	4	R66,R67,R69,R77	2.0M 1%
51	3	R68,R72,R76	33.2K 1%
52	4	R70,R74,R78,R80	1M 1% 1/16W
53	1	R73	82k
54	1	R75	249K 1%
55	1	R79	332K 1%
56	1	R81	15K
57	1	R82	453K 1%
58	1	R83	47K 5% 1/16W
59	1	R84	10K 1%
60	3	R86,R87,R88	866K 1%
61	1	R89	56.2K 1%
62	1	R90	1M 5% 1/16W
63	1	R91	78.7K 1%
64	1	R93	357K 1%
65	1	R95	75k (Not inserted)
66	1	R96	470k (Not inserted)
67	3	R97,R98,R99	470 5% 1/16W
68	1	R100	330K
69	3	U1,U2,U3	IR7509
70	2	U6,U4	HCPL0701
71	2	U5,U7	HCPL0453
72	1	U8	IR1110

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IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
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