

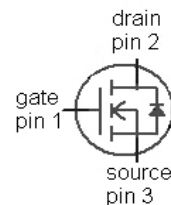
OptiMOS® 2 Power-Transistor

Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$ (SMD Version)	5.0	mΩ
I_D	50	A



Type	IPD06N03LZ	IPS06N03LZ	IPU06N03LZ
			
Package	P-TO252-3-11	P-TO251-3-11	P-TO251-3-21
Marking	06N03LZ	06N03LZ	06N03LZ

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}^{2)}$	50	A
		$T_C=100\text{ °C}$	50	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{3)}$	350	
Avalanche energy, single pulse	E_{AS}	$I_D=45\text{ A}$, $R_{GS}=25\text{ Ω}$	225	mJ
Reverse diode dv/dt	dv/dt	$I_D=50\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A/μs}$, $T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage ⁴⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	83	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.8	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ⁵⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=40\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=30\text{ A}$	-	7.6	9.5	m Ω
		$V_{GS}=4.5\text{ V}, I_D=30\text{ A},$ SMD version	-	7.5	9.4	
		$V_{GS}=10\text{ V}, I_D=30\text{ A}$	4.1	4.6	5.1	
		$V_{GS}=10\text{ V}, I_D=30\text{ A},$ SMD version	4.0	4.5	5.0	
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max},$ $I_D=30\text{ A}$	29	59	-	S

¹⁾ J-STD20 and JESD22

²⁾ Current is limited by bondwire; with an $R_{thJC}=1.8\text{ K/W}$ the chip is able to carry 94 A.

³⁾ See figure 3

⁴⁾ $T_{j,max}=150\text{ °C}$ and duty cycle $D<0.25$ for $V_{GS}<-5\text{ V}$

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	2093	2783	pF
Output capacitance	C_{oss}		-	800	1064	
Reverse transfer capacitance	C_{rss}		-	98	147	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=25\text{ A}, R_G=2.7\ \Omega$	-	10	14	ns
Rise time	t_r		-	7.2	11	
Turn-off delay time	$t_{d(off)}$		-	29	43	
Fall time	t_f		-	4.6	6.9	

Gate Charge Characteristics⁶⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=25\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	6.7	9.0	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.3	4.5	
Gate to drain charge	Q_{gd}		-	4.6	6.9	
Switching charge	Q_{sw}		-	8.0	11	
Gate charge total	Q_g		-	17	22	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	15	20	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	17	23	

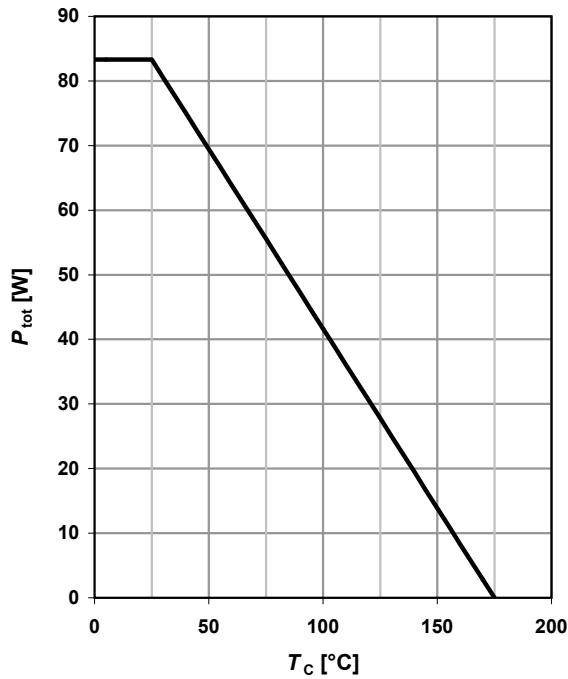
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	350	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ °C}$	-	0.92	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

⁶⁾ See figure 16 for gate charge parameter definition

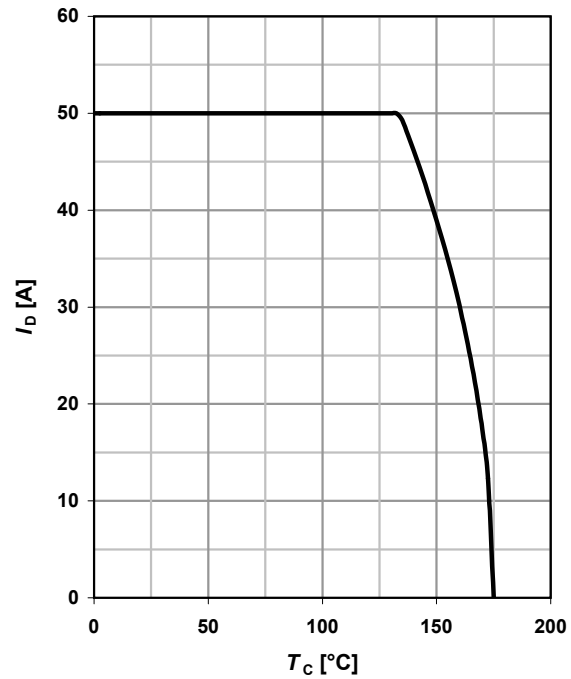
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

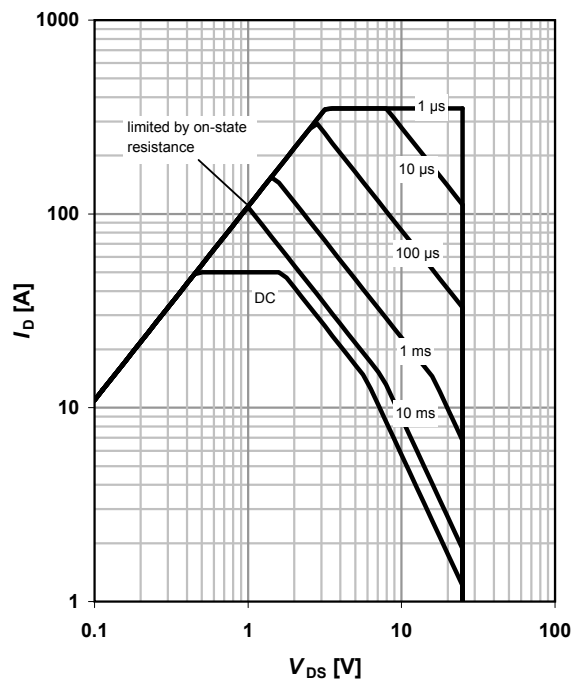
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

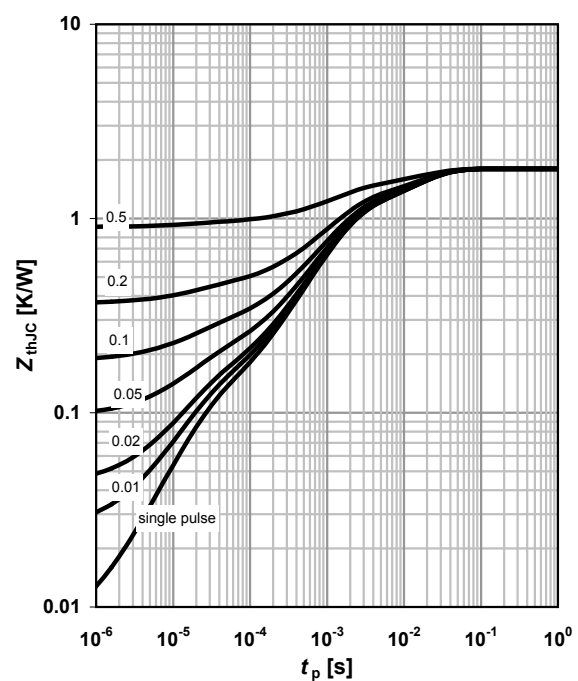
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

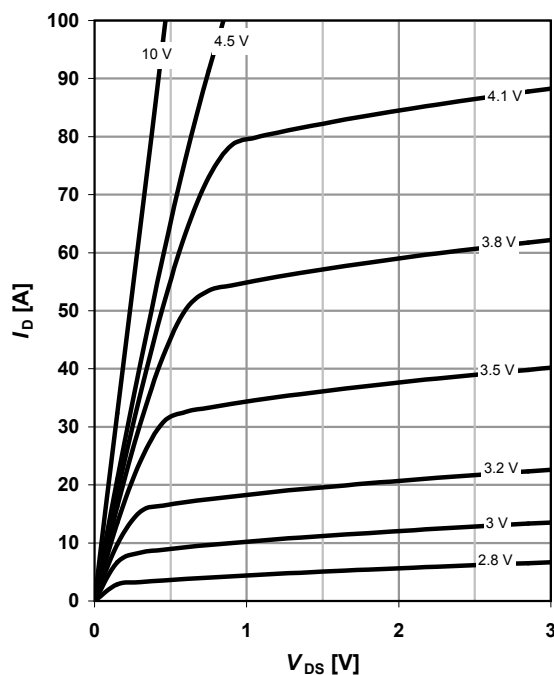
parameter: $D = t_p/T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

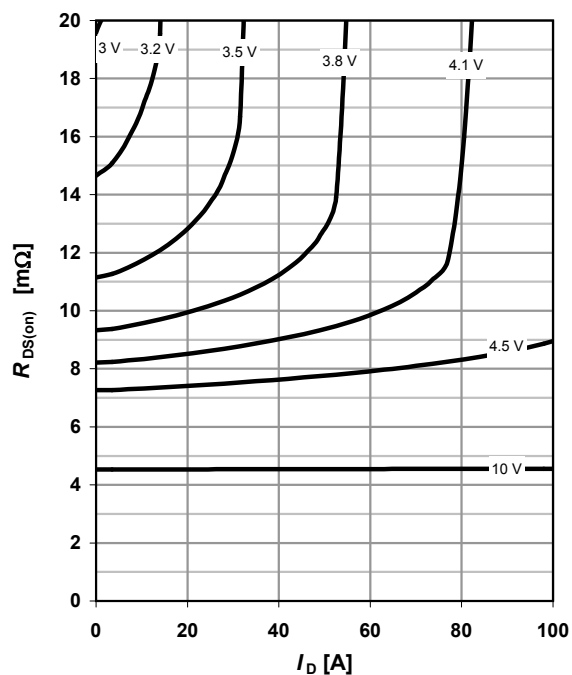
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

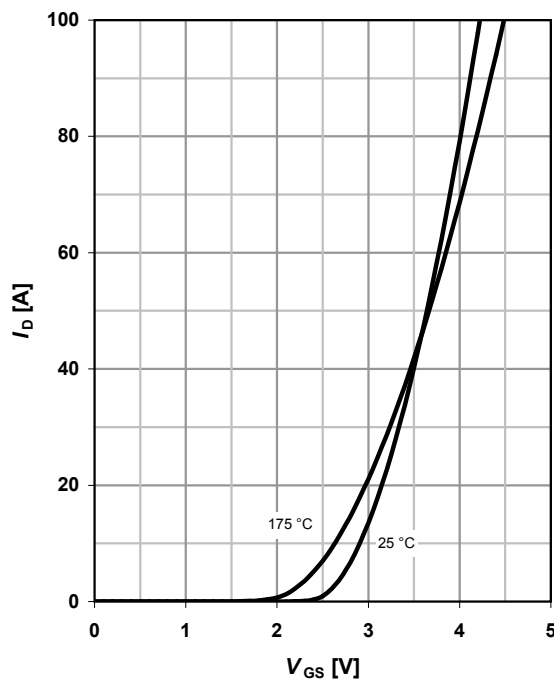
parameter: V_{GS}



7 Typ. transfer characteristics

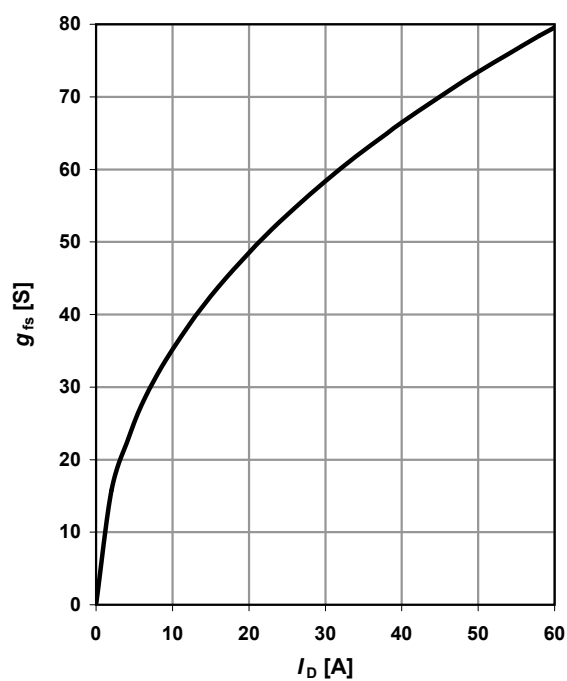
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_j



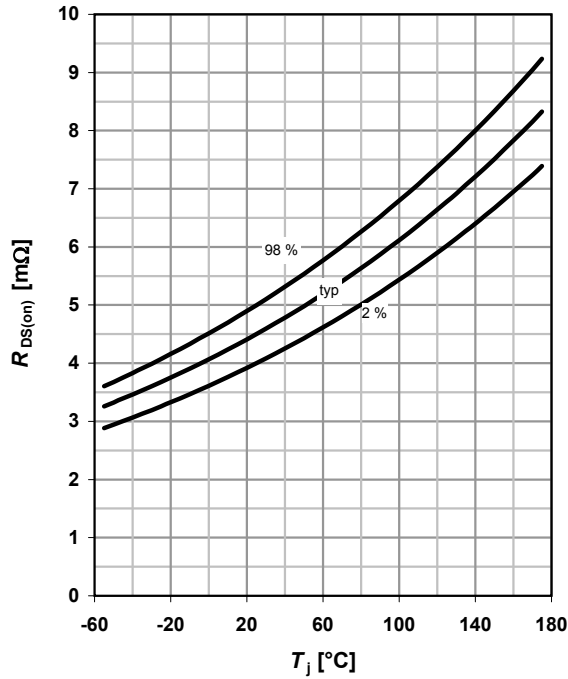
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



9 Drain-source on-state resistance

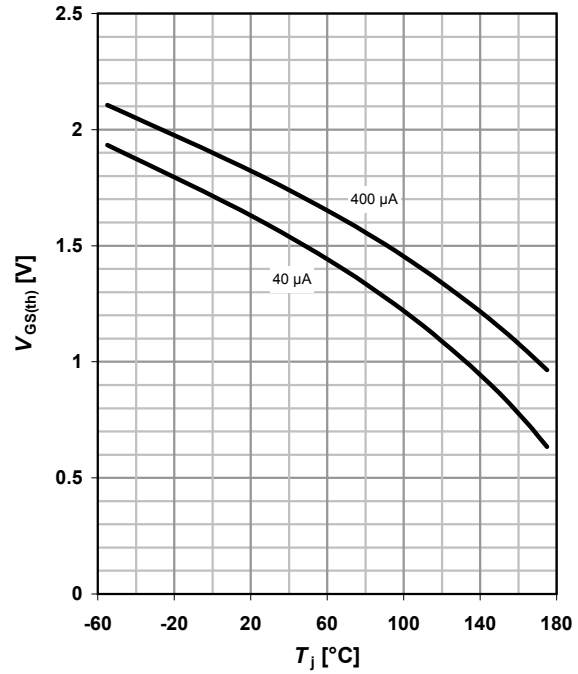
$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

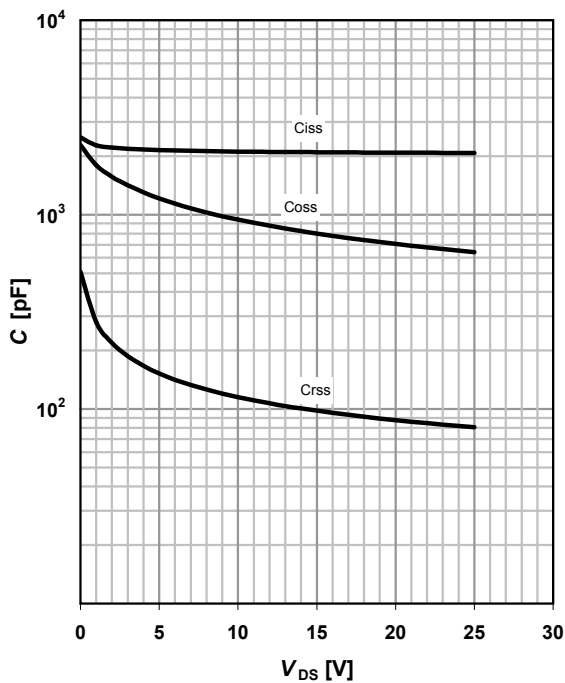
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

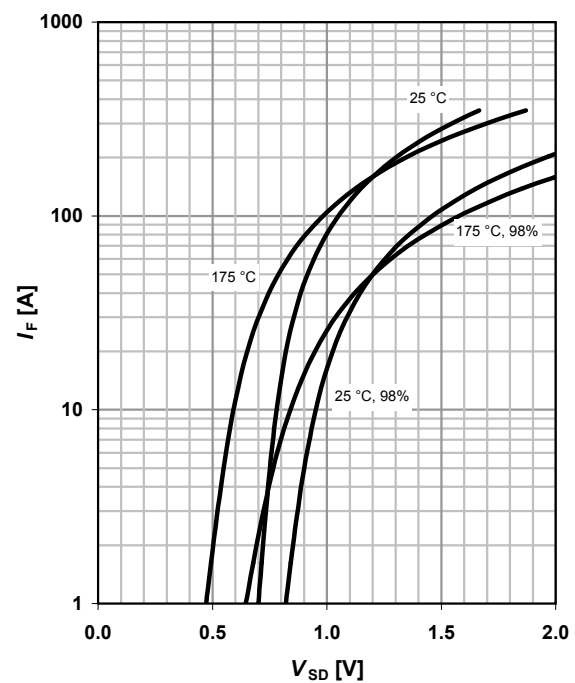
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

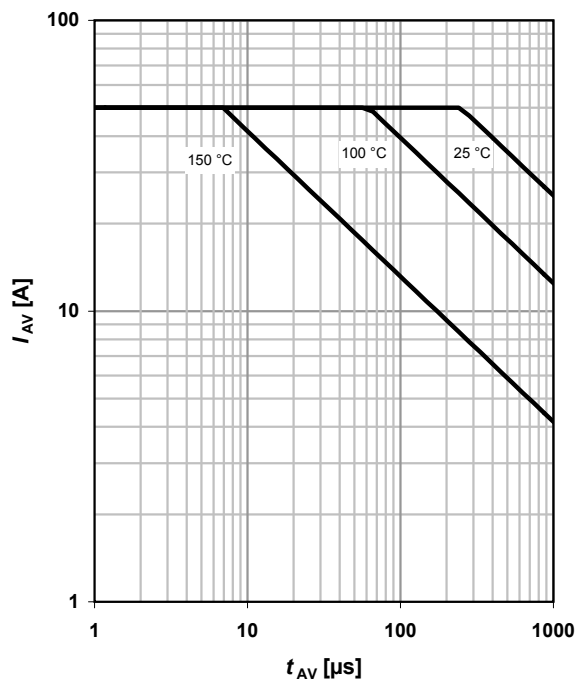
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

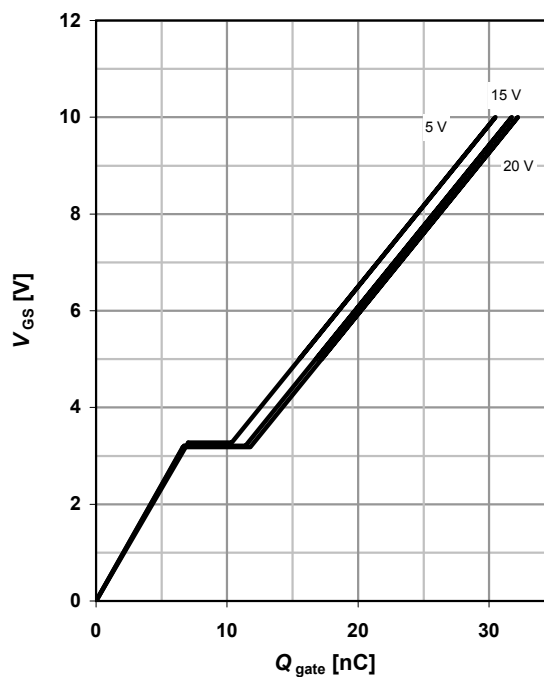
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

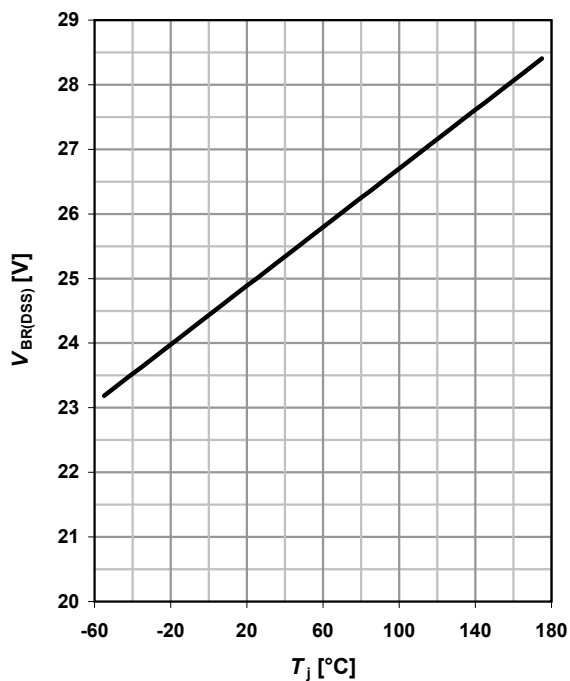
$$V_{GS}=f(Q_{\text{gate}}); I_D=25\ \text{A pulsed}$$

parameter: V_{DD}

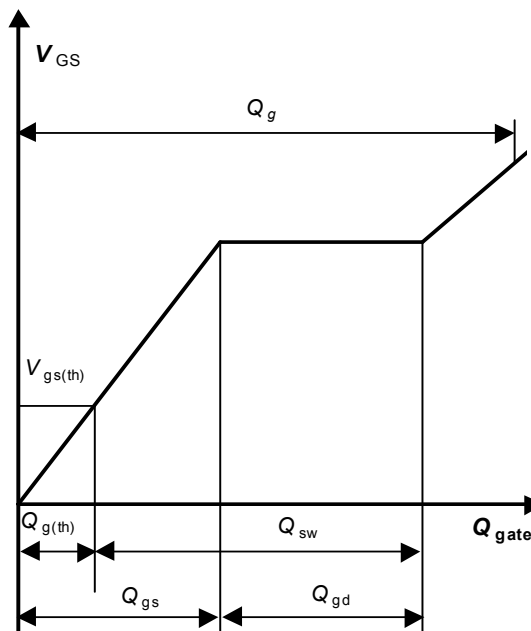


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$



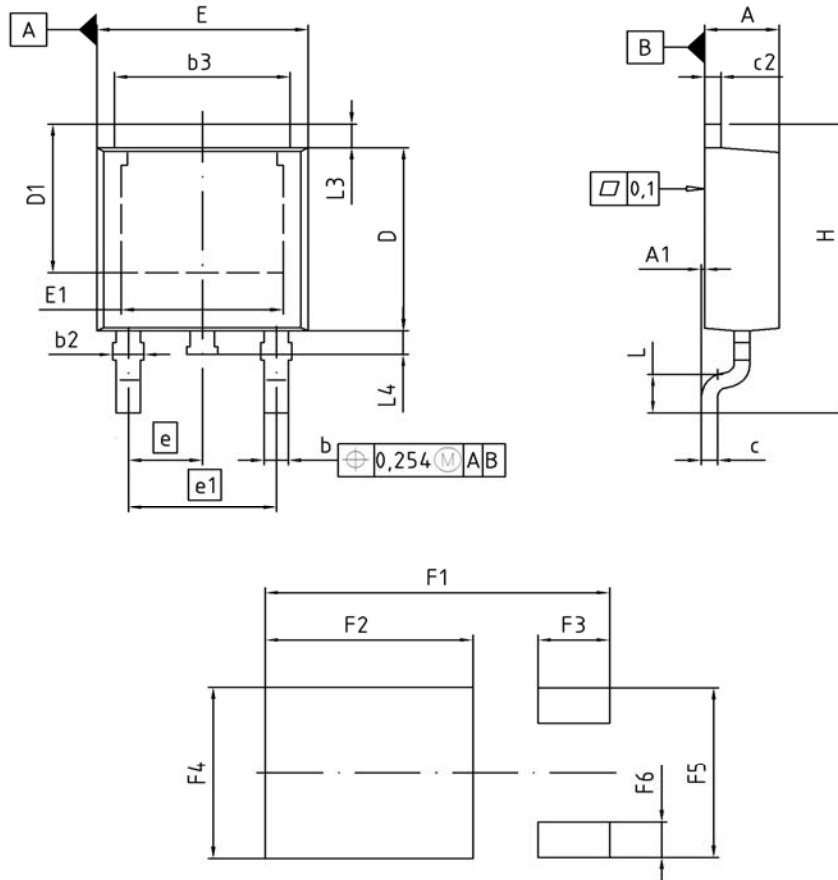
16 Gate charge waveforms



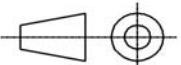
Package Outline

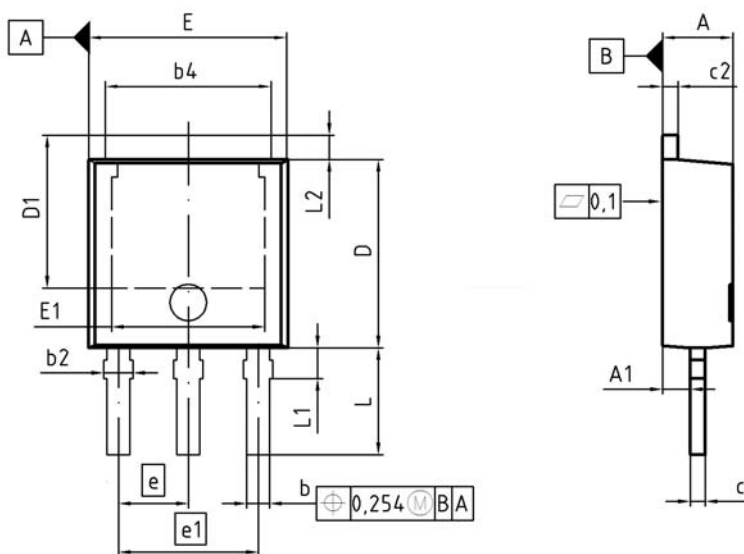
PG-TO252-3-11

PG-TO252-3-11: Outline

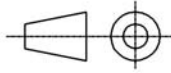


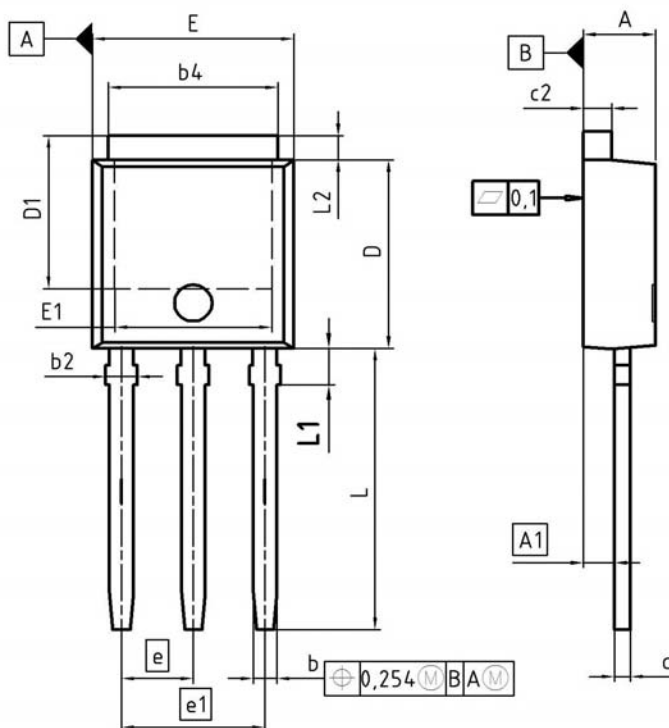
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.44	0.198	0.214
E	6.35	6.73	0.250	0.265
E1	4.90	5.10	0.193	0.201
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.40	3.60	0.134	0.142
L1	0.90	1.10	0.035	0.043
L2	0.90	1.10	0.035	0.043

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REVISION 03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.90	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.77	0.198	0.227
E	6.35	6.73	0.250	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	8.89	9.65	0.350	0.380
L1	1.90	2.29	0.075	0.090
L2	0.89	1.37	0.035	0.054

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