

IPS031R

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

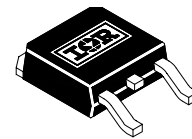
Description

The IPS031R are fully protected three terminal SMART POWER MOSFETs that feature over-current, over-temperature, ESD protection and drain to source active clamp. These devices combine a HEXFET® POWER MOSFET and a gate driver. They offer full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when the temperature exceeds 165°C or when the drain current reaches 14A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

Product Summary

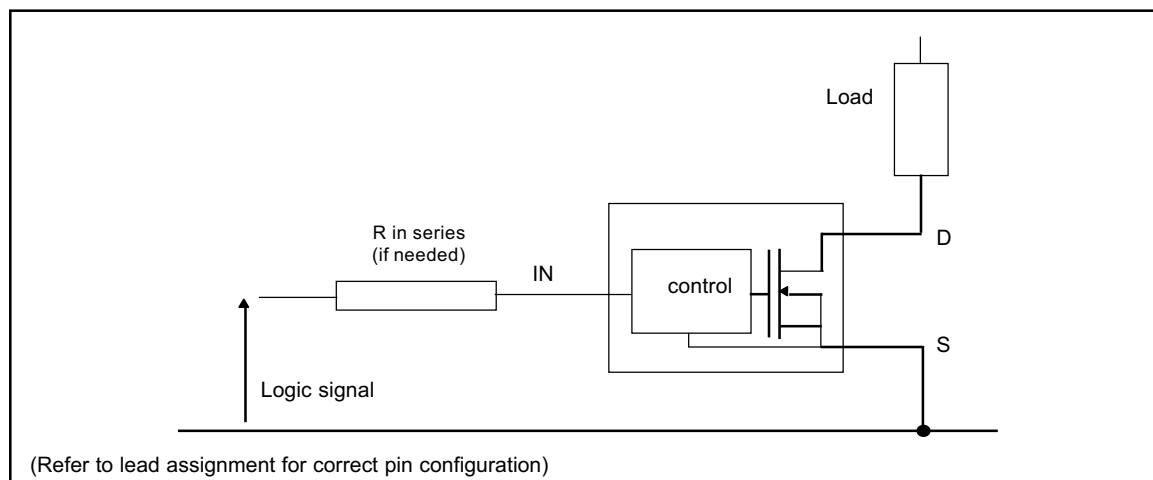
$R_{ds(on)}$	60m Ω (max)
V_{clamp}	50V
$I_{shutdown}$	14A
T_{on}/T_{off}	1.5 μ s

Package



3-Lead D-Pak

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{\text{Ambient}} = 25^{\circ}\text{C}$ unless otherwise specified). PCB mounting uses the standard footprint with 70 μm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{\text{in, max}}$	Maximum IN current	-10	+10	mA	
$I_{\text{sd cont.}}$	Diode max. continuous current ⁽¹⁾			A	
	$r_{\text{th}}=100^{\circ}\text{C/W}$	—	1.6		D-Pak Std footprint
	$r_{\text{th}}=5^{\circ}\text{C/W}$	—	18		D-Pak with $R_{\text{th}}=5^{\circ}\text{C/W}$
	$r_{\text{th}}=50^{\circ}\text{C/W}$	—	3		D-Pak with sq. footprint
$I_{\text{sd pulsed}}$	Diode max. pulsed current ⁽¹⁾	—	18		
P_{d}	Maximum power dissipation ⁽¹⁾			W	
	$r_{\text{th}}=50^{\circ}\text{C/W}$	—	2.5		
	$r_{\text{th}}=100^{\circ}\text{C/W}$	—	1.25		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500 Ω ,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0 Ω , L=10 μH
$T_{\text{stor.}}$	Max. storage temperature	-55	150	$^{\circ}\text{C}$	
$T_{\text{j max.}}$	Max. junction temperature	-40	+150		
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{\text{th 1}}$	Thermal resistance with standard footprint	—	100	—	$^{\circ}\text{C/W}$	D-PAK
$R_{\text{th 2}}$	Thermal resistance with 1" square footprint	—	50	—		
$R_{\text{th 3}}$	Thermal resistance junction to case	—	3	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{\text{ds (max)}}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} $T_{\text{amb}}=85^{\circ}\text{C}$	Continuous drain current			A
	$T_{\text{Ambient}} = 85^{\circ}\text{C}$, $I_{\text{N}} = 5\text{V}$, $r_{\text{th}} = 50^{\circ}\text{C/W}$, $T_{\text{j}} = 125^{\circ}\text{C}$ 1" sq. footprint	—	3.3	
	$T_{\text{Ambient}} = 85^{\circ}\text{C}$, $I_{\text{N}} = 5\text{V}$, $r_{\text{th}} = 100^{\circ}\text{C/W}$, $T_{\text{j}} = 125^{\circ}\text{C}$ Std. footprint	—	2	
R_{in}	Recommended resistor in series with IN pin	0.2	5	k Ω
$T_{\text{r-in(max)}}$	Max recommended rise time for IN signal (see fig. 2)	—	1	μs
$F_{\text{r-Isc}}^{(2)}$	Max. frequency in short circuit condition ($V_{\text{cc}} = 14\text{V}$)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)

(2) Operations at higher switching frequencies is possible. See Application. Notes.

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R _{ds(on)}	ON state resistance T _j = 25°C	20	45	60	mΩ	V _{in} = 5V, I _{ds} = 1A
R _{ds(on)}	ON state resistance T _j = 150°C	—	75	100		
I _{dss} @T _j =25°C	Drain to source leakage current	0	0.5	25	μA	V _{cc} = 14V, T _j = 25°C
I _{dss2} @T _j =25°C	Drain to source leakage current	0	5	50		V _{cc} = 40V, T _j = 25°C
V _{clamp 1}	Drain to source clamp voltage 1	47	52	56	V	I _d = 20mA (see Fig.3 & 4)
V _{clamp 2}	Drain to source clamp voltage 2	50	53	60		I _d =I _{shutdown} (see Fig.3 & 4)
V _{in clamp}	IN to source clamp voltage	7	8.1	9.5		I _{in} = 1 mA
V _{th}	IN threshold voltage	1	1.6	2		I _d = 50mA, V _{ds} = 14V
I _{in, -on}	ON state IN positive current	25	90	200	μA	V _{in} = 5V
I _{in, -off}	OFF state IN positive current	50	130	250		V _{in} = 5V over-current triggered

Switching Electrical Characteristics

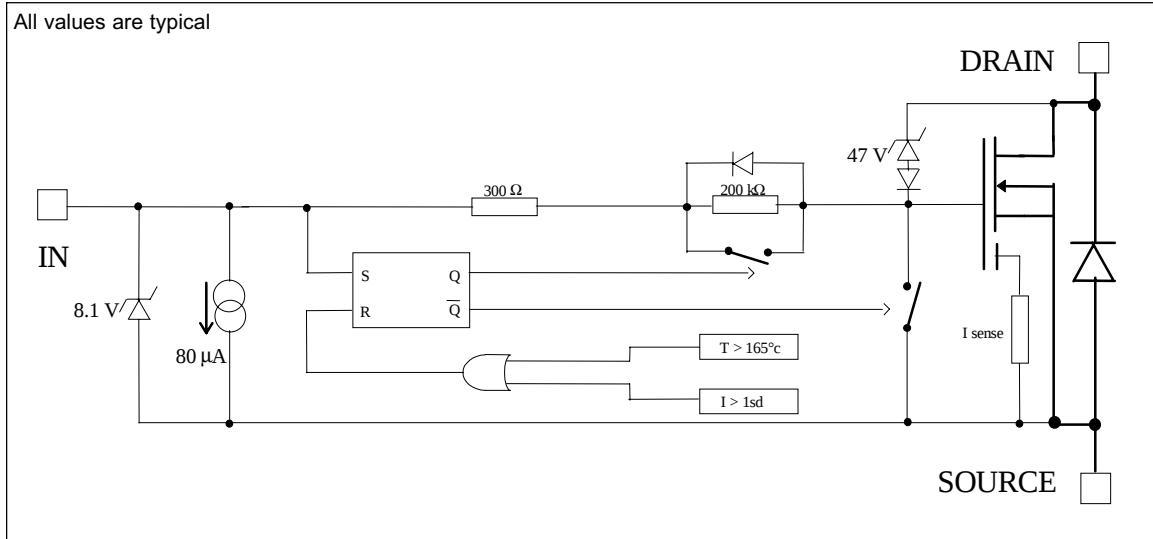
V_{cc} = 14V, Resistive Load = 5Ω, R_{input} = 50Ω, 100μs pulse, T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T _{on}	Turn-on delay time	0.05	0.3	0.6	μs	See figure 2
T _r	Rise time	0.4	1	2		
T _{rf}	Time to 130% final R _{ds(on)}	—	8	—		See figure 2
T _{off}	Turn-off delay time	0.8	2	3.5		
T _f	Fall time	0.5	1.5	2.5		
Q _{in}	Total gate charge	—	11	—	nC	V _{in} = 5V

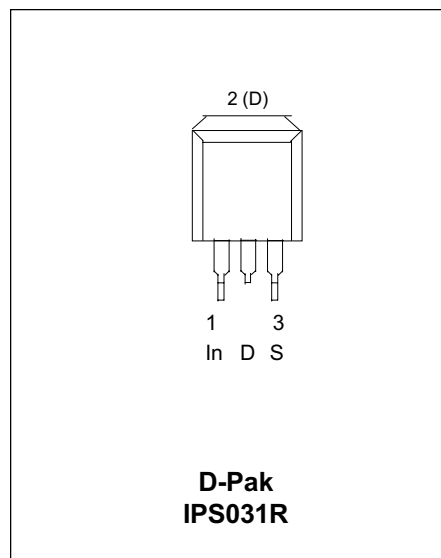
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T _{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I _{sd}	Over current threshold	10	14	18	A	See fig. 1
V _{reset}	IN protection reset threshold	1.5	2.3	3	V	
T _{reset}	Time to reset protection	2	10	40	μs	V _{in} = 0V, T _j = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	μJ	V _{cc} = 14V

Functional Block Diagram



Lead Assignments



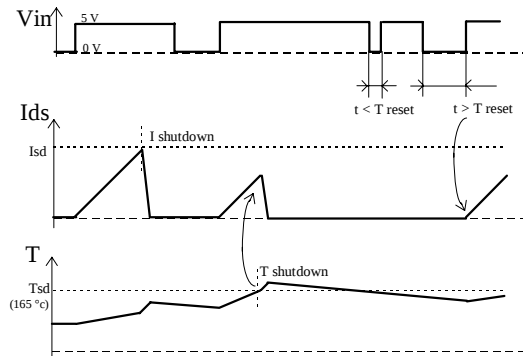


Figure 1 - Timing diagram

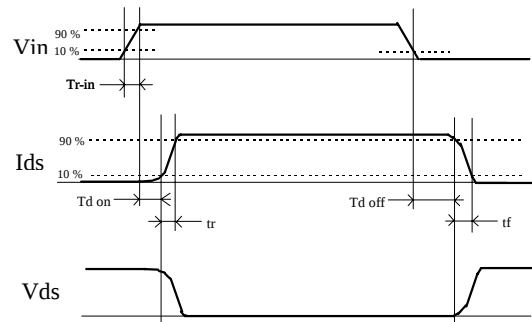


Figure 2 - IN rise time & switching time definitions

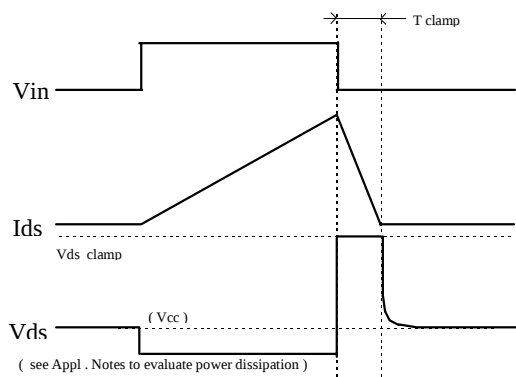


Figure 3 - Active clamp waveforms

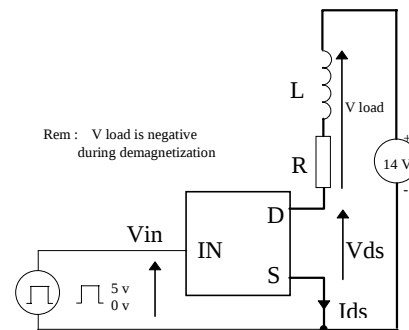


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

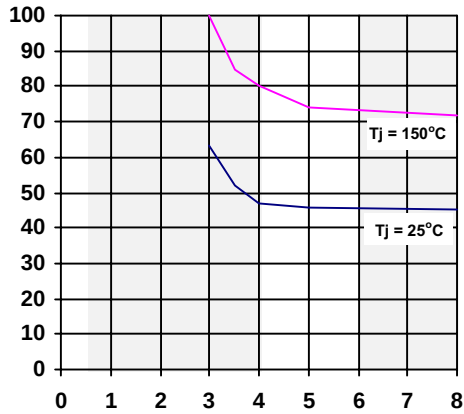


Figure 5 - $R_{DS(on)}$ (mΩ) Vs Input Voltage (V)

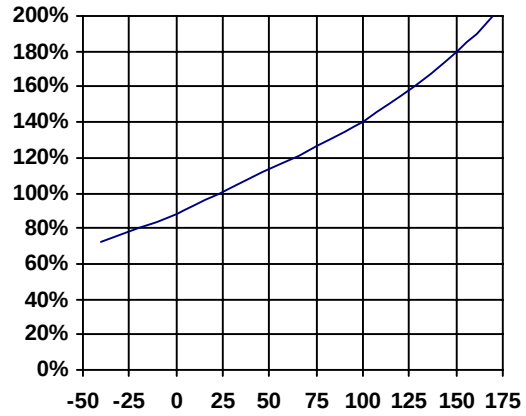


Figure 6 - Normalised $R_{DS(on)}$ (%) Vs T_j (°C)

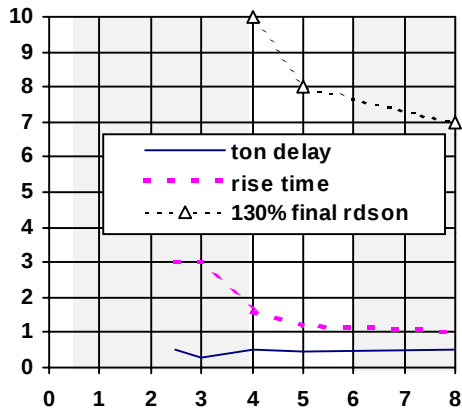


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{DS(on)}$ (us) Vs Input Voltage (V)

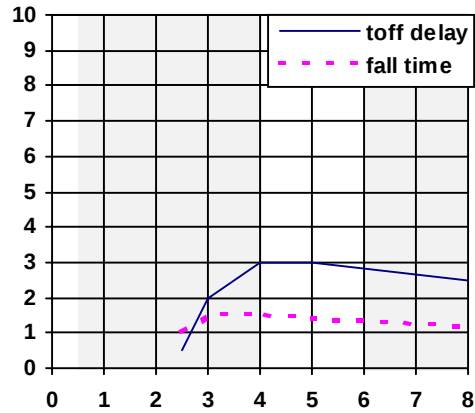


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

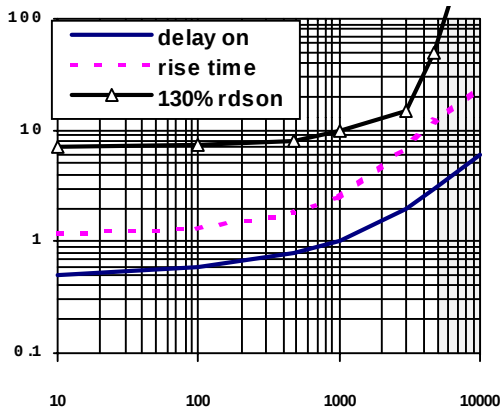


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{DS(on)}$ (us) Vs IN Resistor (Ω)

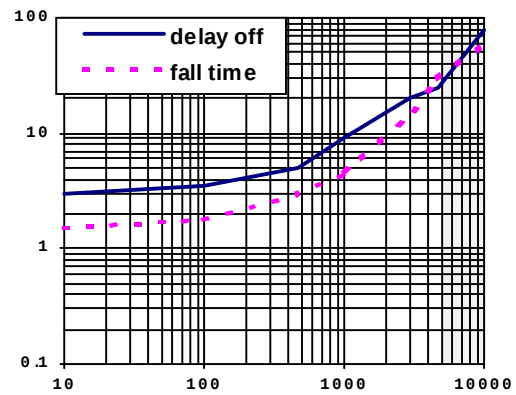


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

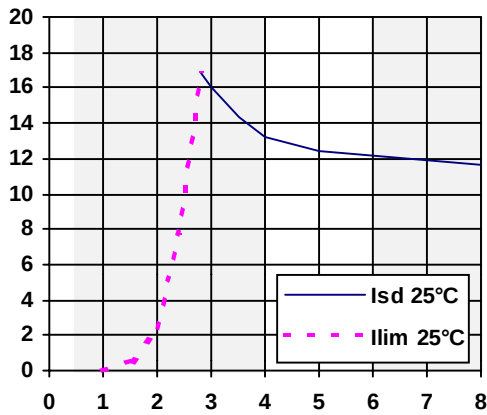


Figure 11 - Current limitation & I shutdown (A) Vs V_{in} (V)

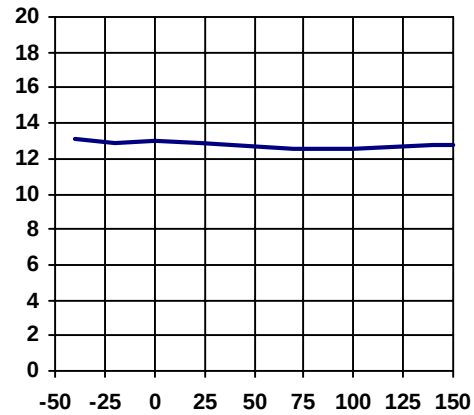


Figure 12 - I shutdown (A) Vs Temperature (°C)

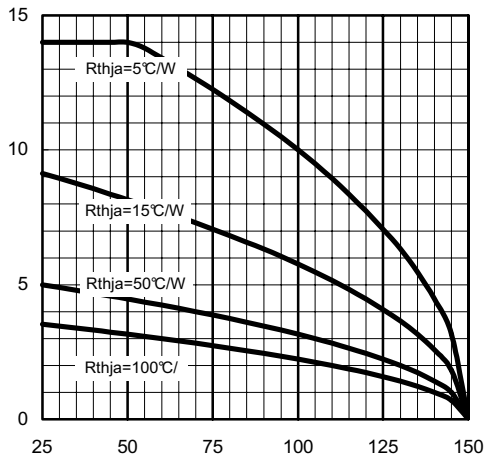


Figure 13 - Max. I load current (A) Vs Tamb (°C)
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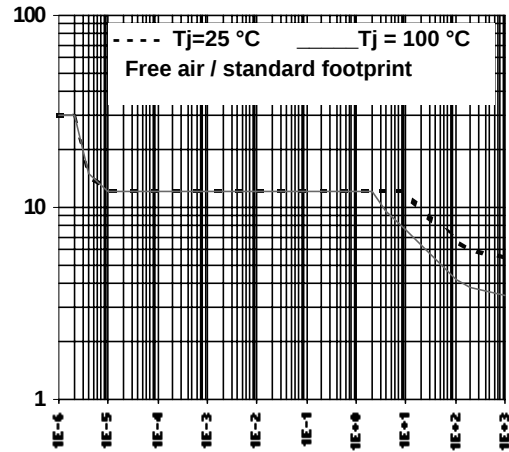


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
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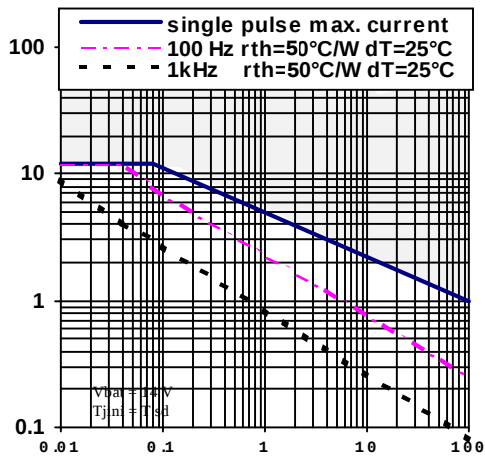


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

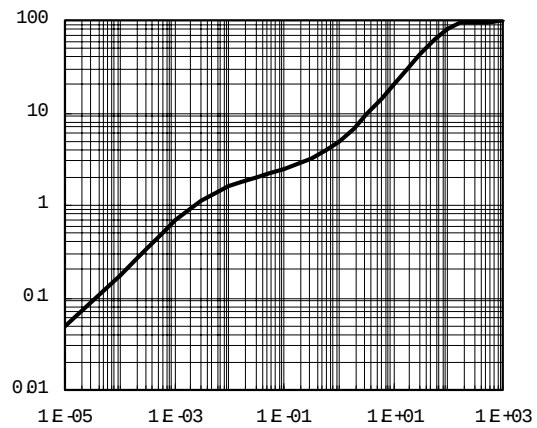


Fig.16 - Transient Thermal Impedance (°C/W)
Vs Time (s) - IPS031R

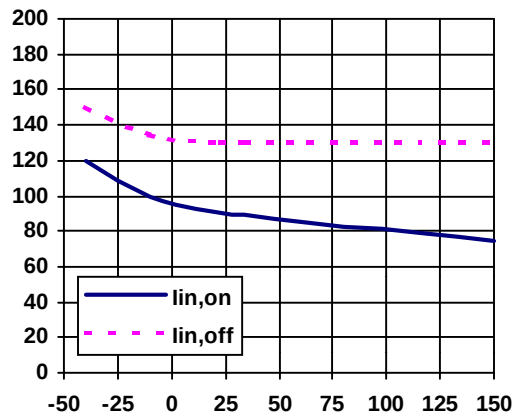


Figure 17 - Input current (μA) Vs Junction (°C)

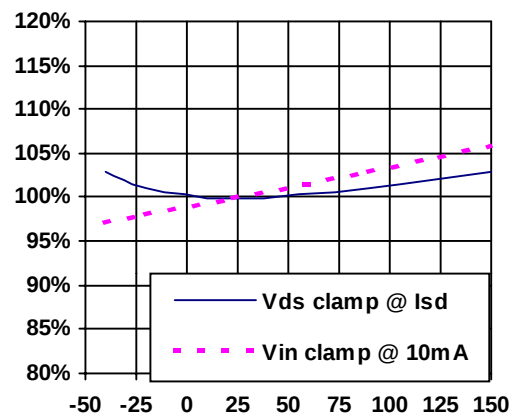


Figure 18 - Vin clamp and V clamp2 (%)
Vs Tj (°C)

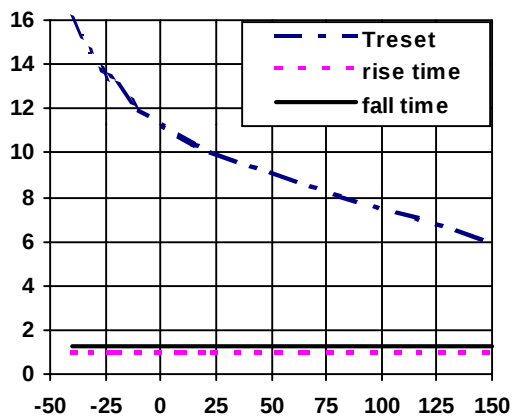
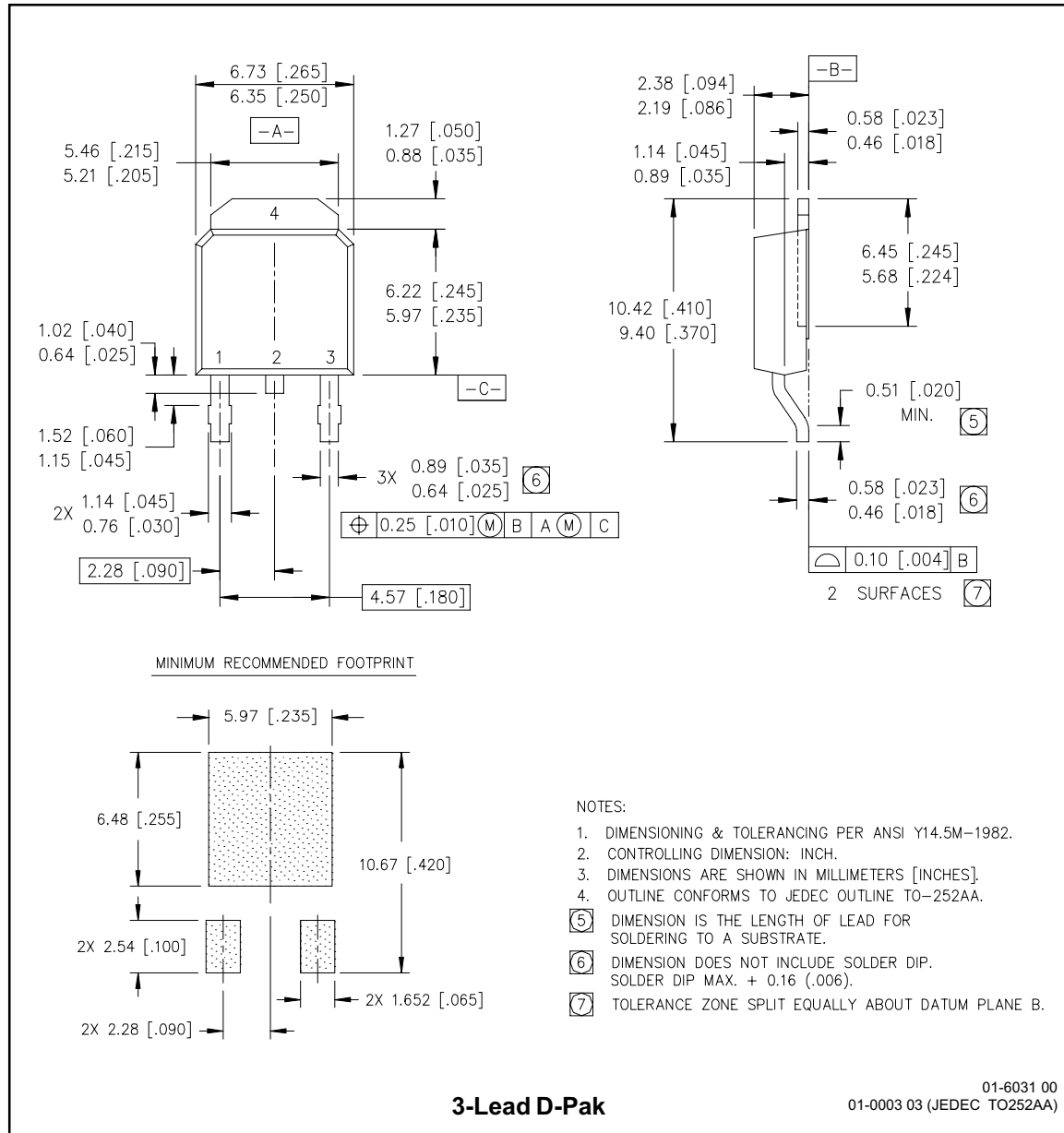
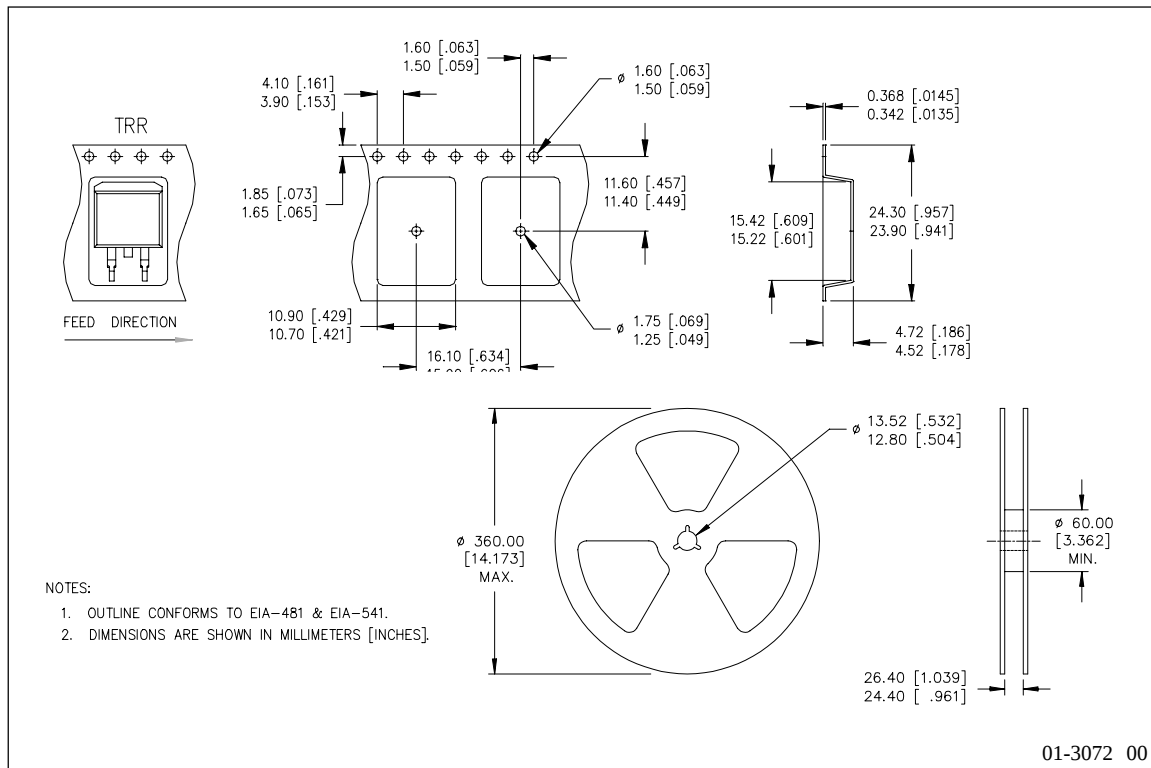


Figure 19 - Turn-on, Turn-off, and treset (μs)
Vs Tj (°C)

Case Outline



Tape & Reel - D-PAK



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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>