

## Smart High-Side Power Switch

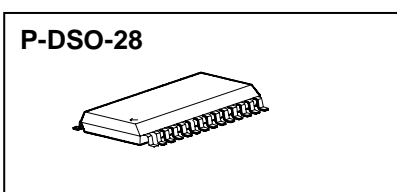
### Four Channels: 4 x 35mΩ

### Advanced Current Sense

#### Product Summary

Operating Voltage	$V_{bb(on)}$	5.0 ... 40V	
Active channels		one	four parallel
On-state Resistance	$R_{ON}$	35mΩ	9mΩ
Nominal load current	$I_{L(NOM)}$	5.4A	11.1A
Current limitation	$I_{L(SCr)}$	40A	40A

#### Package



#### General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology.
- Providing embedded protective functions

#### Applications

- $\mu$ C compatible high-side power switch with diagnostic feedback for 12V and 24V grounded loads
- All types of resistive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

#### Basic Functions

- Very low standby current
- Improved electromagnetic compatibility (EMC)
- CMOS compatible input
- Stable behaviour at undervoltage
- Wide operating voltage range

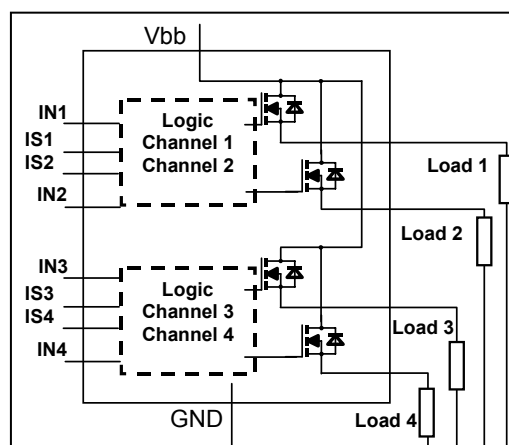
#### Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Reverse battery protection with external resistor
- Overvoltage protection with external resistor (incl. load dump)
- Loss of ground protection
- Electrostatic discharge protection (ESD)

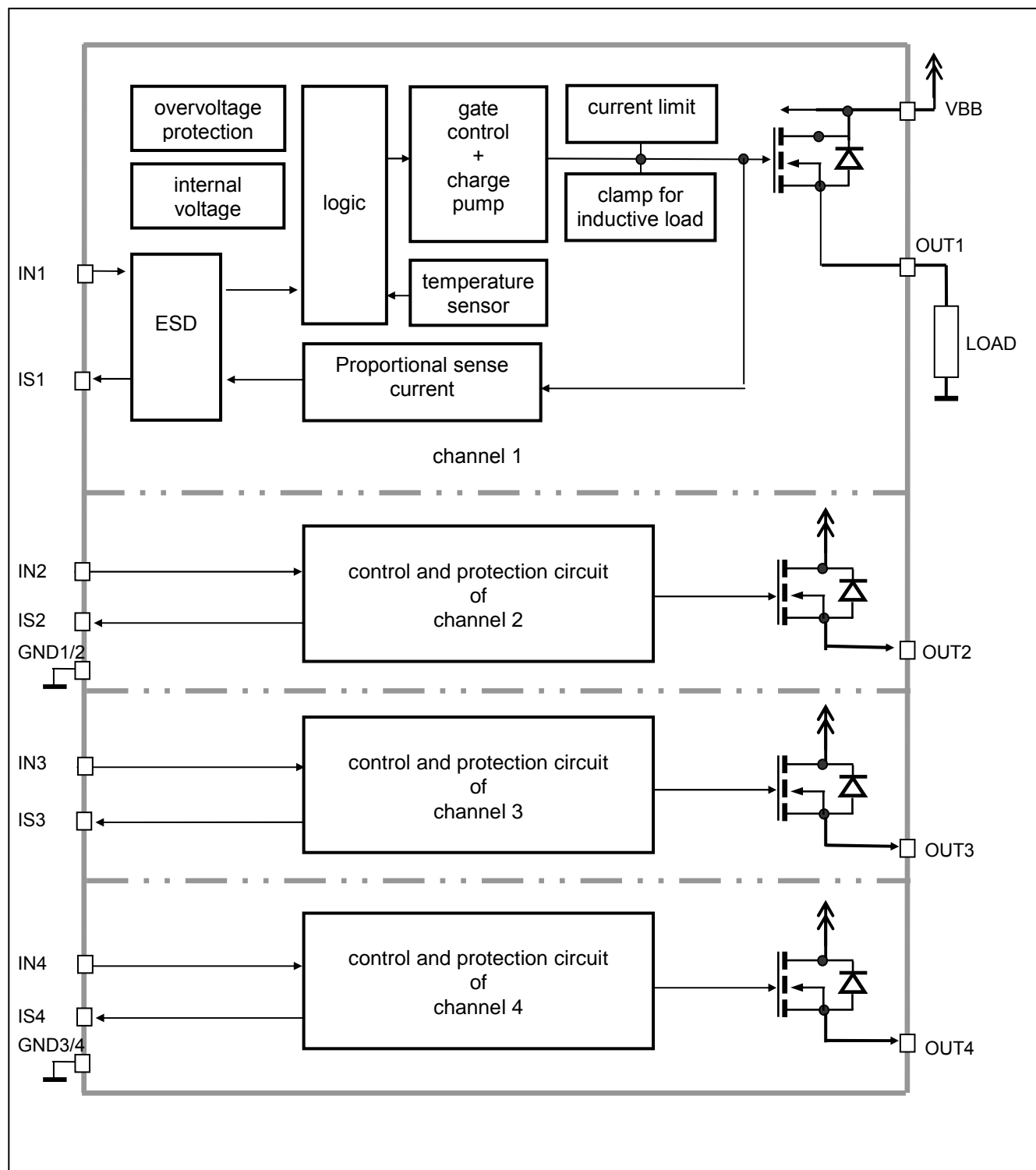
#### Diagnostic Function

- Proportional load current sense (with defined fault signal during thermal shutdown and current limit)

#### Block Diagram



## Functional diagram



**Pin Definitions and Functions**

Pin	Symbol	Function
1, 7, 8, 14, 15, 28	$V_{bb}$	<b>Positive power supply voltage.</b> Design the wiring for the simultaneous max. short circuit currents from channel 1 to 4 and also for low thermal resistance
4	IN1	<b>Input 1,2, 3,4</b> activates channel 1,2,3,4 in case of logic high signal
3	IN2	
11	IN3	
10	IN4	
25,26,27	OUT1	<b>Output 1,2,3,4</b> protected high-side power output of channel 1,2,3,4. Design the wiring for the max. short circuit current
22,23,24	OUT2	
19,20,21	OUT3	
16,17,18	OUT4	
5	IS1	<b>Diagnostic feedback 1 .. 4</b> of channel 1 to 4 Providing a sense current, proportional to the load current
6	IS2	
12	IS3	
13	IS4	
2	GND1/2	<b>Ground</b> of chip 1 (channel 1,2)
9	GND3/4	<b>Ground</b> of chip 2 (channel 3,4)

**Pin configuration**

(top view)

$V_{bb}$	1	28	$V_{bb}$
GND1/2	2	27	OUT1
IN2	3	26	OUT1
IN1	4	25	OUT1
IS1	5	24	OUT2
IS2	6	23	OUT2
$V_{bb}$	7	22	OUT2
$V_{bb}$	8	21	OUT3
GND3/4	9	20	OUT3
IN4	10	19	OUT3
IN3	11	18	OUT4
IS3	12	17	OUT4
IS4	13	16	OUT4
$V_{bb}$	14	15	$V_{bb}$

**Maximum Ratings** at  $T_j = 25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 6)	$V_{bb}$	40	V
Supply voltage for full short circuit protection <sup>1)</sup> $T_{j,start} = -40 \dots +150^\circ\text{C}$	$V_{bb}$	36	V
Load current (Short-circuit current, see page 6)	$I_L$	$I_{L(lim)}^2$	
Load dump protection <sup>3)</sup> $V_{LoadDump} = V_A + V_S$ , $V_A = 13.5\text{ V}$ $R_l^{4)} = 2\ \Omega$ , $t_d = 400\text{ ms}$ ; IN= low or high, each channel loaded with $R_L = 4.7\ \Omega$ ,	$V_{Load\ dump}^{5)}$	60	V
Operating temperature range	$T_j$	$-40 \dots +150$	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	$-55 \dots +150$	
Power dissipation (DC) <sup>6)</sup> (all channels active)	$P_{tot}$	$T_a = 25^\circ\text{C}: 3.7$ $T_a = 85^\circ\text{C}: 1.9$	W
Maximal switchable inductance, single pulse $V_{bb} = 12\text{V}$ , $T_{j,start} = 150^\circ\text{C}^{6)}$ , $I_L = 4.0\text{ A}$ , $E_{AS} = 0.8\text{J}$ , $0\ \Omega$ one channel: $I_L = 6.0\text{ A}$ , $E_{AS} = 1.0\text{J}$ , $0\ \Omega$ two parallel channels: $I_L = 9.5\text{ A}$ , $E_{AS} = 1.5\text{J}$ , $0\ \Omega$ four parallel channels: see diagrams on page 10	$Z_L$	33 37 64	mH
Electrostatic discharge capability (ESD) IN: (Human Body Model) IS: out to all other pins shorted: acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993 $R=1.5\text{k}\Omega$ ; $C=100\text{pF}$	$V_{ESD}$	1.0 4.0 8.0	kV
Input voltage (DC)	$V_{IN}$	$-10 \dots +16$	V
Current through input pin (DC)	$I_{IN}$	$\pm 0.3$	mA
Current through sense pin (DC) see internal circuit diagram page 9	$I_{IS}$	$\pm 0.3$	

1) Single pulse

2) Current limit is a protection function. Operation in current limitation is considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

3) Supply voltages higher than  $V_{bb(AZ)}$  require an external current limit for the GND and status pins (a  $75\ \Omega$  resistor for the GND connection is recommended).

4)  $R_l$  = internal resistance of the load dump test pulse generator

5)  $V_{Load\ dump}$  is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

6) Device on  $50\text{mm} \times 50\text{mm} \times 1.5\text{mm}$  epoxy PCB FR4 with  $6\text{cm}^2$  (one layer,  $70\ \mu\text{m}$  thick) copper area for  $V_{bb}$  connection. PCB is vertical without blown air. See page 15



## Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit
		min	typ	Max	
Thermal resistance junction - soldering point <sup>7)</sup> <sup>8)</sup> , each channel: junction – ambient <sup>8)</sup> @ 6 cm <sup>2</sup> cooling area one channel active: all channels active:	$R_{thjs}$ $R_{thja}$	--	--	11	K/W
		--	40	--	
		--	33	--	

## Electrical Characteristics

Parameter and Conditions, each of the four channels at $T_j = -40...+150^{\circ}\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	

## Load Switching Capabilities and Characteristics

On-state resistance ( $V_{bb}$ to OUT); $I_L = 5\text{ A}$ each channel, $T_j = 25^{\circ}\text{C}$ : see diagram, page 11 $T_j = 150^{\circ}\text{C}$ :	$R_{ON}$	--	30 55	35 64	m $\Omega$
Nominal load current one channel active: two parallel channels active: four parallel channels active: Device on PCB <sup>8)</sup> , $T_a = 85^{\circ}\text{C}$ , $T_j \leq 150^{\circ}\text{C}$	$I_{L(NOM)}$	5.0 6.7 10.5	5.4 7.4 11.1	-- -- --	A
Output current while GND disconnected, $V_{IN} = 0$ , see diagram page 10; (not subject to production test - specified by design)	$I_{L(GNDhigh)}$	--	--	1	mA
Turn-on time <sup>9)</sup> IN  to 90% $V_{OUT}$ :	$t_{on}$	--	50	150	$\mu\text{s}$
Turn-off time IN  to 10% $V_{OUT}$ : $R_L = 12\ \Omega$	$t_{off}$	--	120	250	$\mu\text{s}$
Slew rate on <sup>9)</sup> $V_{OUT}$ rising from 10 to 30% of $V_{bb}$ , $R_L = 12\ \Omega$ :	$dV/dt_{on}$	0.2	--	0.9	V/ $\mu\text{s}$
Slew rate off <sup>9)</sup> $V_{OUT}$ falling from 70 to 40% of $V_{bb}$ , $R_L = 12\ \Omega$ :	$-dV/dt_{off}$	0.1	--	0.9	V/ $\mu\text{s}$

<sup>7)</sup> Soldering point: upper side of solder edge of device pin 7,8. See page 16.

<sup>8)</sup> Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70 $\mu\text{m}$  thick) copper area for  $V_{bb}$  connection. PCB is vertical without blown air. See page 15

<sup>9)</sup> See timing diagram on page 12.

**Operating Parameters**

Operating voltage	$V_{bb(on)}$	5.0	--	40	V
Overvoltage protection <sup>10)</sup> $I_{bb} = 40 \text{ mA}$	$V_{bb(AZ)}$	41	47	52	V
Standby current <sup>11)</sup> $V_{IN} = 0$ ; see diagram page 12	$T_j = -40...25^\circ\text{C}$ : $I_{bb(off)}$	--	10	25	$\mu\text{A}$
	$T_j = 150^\circ\text{C}$ :	--	40	80	
	$T_j = 125^\circ\text{C}$ :		--	25	
(not subject to production test - specified by design)					
Off-State output current (included in $I_{bb(off)}$ ) $V_{IN} = 0$ ; each channel; $T_j = 150^\circ\text{C}$ :	$T_j = -40...25^\circ\text{C}$ : $I_{L(off)}$	--	1	6	$\mu\text{A}$
		--	--	15	
Operating current, $V_{IN} = 5\text{V}$ , $I_{GND} = I_{GND1/2} + I_{GND3/4}$ , one channel on: four channels on:	$I_{GND}$	-- --	1.6 6.0	-- --	mA

**Protection Functions<sup>12)</sup>**

Current limit, (see timing diagrams, page 13)	$I_{L(lim)}$	36	45	58	A
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two, three or four parallel channels (see timing diagrams, page 13)	$I_{L(SCr)}$	--	40	--	A
		--	40	--	
Initial short circuit shutdown time $T_{j,start} = 25^\circ\text{C}$ : (see timing diagrams on page 13)	$t_{off(SC)}$	--	4	--	ms
Output clamp (inductive load switch off) <sup>13)</sup> at $V_{ON(CL)} = V_{bb} - V_{OUT}$ , $I_L = 40 \text{ mA}$	$V_{ON(CL)}$	41	47	52	V
Thermal overload trip temperature	$T_{jt}$	150	--	--	$^\circ\text{C}$
Thermal hysteresis	$\Delta T_{jt}$	--	10	--	K

**Reverse Battery<sup>14)</sup>** (not subject to production test - specified by design)

Reverse battery voltage	$-V_{bb}$	--	--	14	V
Drain-source diode voltage ( $V_{out} > V_{bb}$ ) $I_L = -2\text{A}$ ; $T_j = +150^\circ\text{C}$ :	$-V_{ON}$	--	500	--	mV

<sup>10)</sup> Supply voltages higher than  $V_{bb(AZ)}$  require an external current limit for the GND and status pins (a 75 $\Omega$  resistor for the GND connection is recommended). See also  $V_{ON(CL)}$  in table of protection functions and circuit diagram on page 9.



<sup>11)</sup> Measured with load; for the whole device; all channels off.

<sup>12)</sup> Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

<sup>13)</sup> If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest  $V_{ON(CL)}$ .

<sup>14)</sup> Requires a 75 Ohm resistor in the GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Note that the power dissipation is higher compared to normal operating conditions due to the voltage drop across the intrinsic drain-source diode. The temperature protection and sense functionality is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 4 and circuit page 9).

**Input<sup>15)</sup>**

Input resistance (see circuit page 9)	$R_i$	2.5	3.5	6.0	k $\Omega$
Input turn-on threshold voltage 	$V_{IN(T+)}$	1.7	--	3.2	V
Input turn-off threshold voltage 	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.3	--	V
Off state input current $V_{IN} = 0.4 \text{ V}$ :	$I_{IN(off)}$	1	--	35	$\mu\text{A}$
On state input current $V_{IN} = 5 \text{ V}$ :	$I_{IN(on)}$	20	50	90	$\mu\text{A}$

**Diagnostic Characteristics**

Current sense ratio, static on-condition, $k_{ILIS} = I_L : I_{IS}$	$k_{ILIS}$	--	5 300	--	
$I_L = 10 \text{ A}$ :		4575	5300	6000	
$I_L = 2 \text{ A}$ :		4100	5300	6300	
$I_L = 1 \text{ A}$ :		4200	5300	6600	
$I_L = 0.5 \text{ A}$ :		3580	5800	8080	
Sense signal in case of fault-conditions <sup>16)</sup>	$V_{\text{fault}}$	5.4	6.3	7.5	V
Sense signal delay after thermal shutdown <sup>17)</sup> (not subject to production test - specified by design)	$t_{\text{delay(fault)}}$	--	--	1	ms
Sense current saturation	$I_{IS,lim}$	4	--	--	mA
Current sense output voltage limitation $I_{IS} = 0, I_L = 5 \text{ A}$ :	$V_{IS(lim)}$	5.4	6.3	7.5	V
Current sense leakage/offset current $V_{IN}=0, V_{IS} = 0, I_L = 0$ :	$I_{IS(LL)}$	--	--	1	$\mu\text{A}$
$V_{IN}=5 \text{ V}, V_{IS} = 0, I_L = 0$ :	$I_{IS(LH)}$	--	2.5	--	
Current sense settling time to $I_{IS \text{ static}} \pm 10\%$ after positive input slope, $I_L = 0 \rightarrow 5 \text{ A}$ , (not subject to production test - specified by design)	$t_{\text{son}(IS)}$	--	--	300	$\mu\text{s}$

<sup>15)</sup> If ground resistors  $R_{GND}$  are used, add the voltage drop across these resistors.

<sup>16)</sup> In the case of current limitation or thermal shutdown the sense signal is no longer a current proportional to the load current, but a fixed voltage of typ. 6 V.

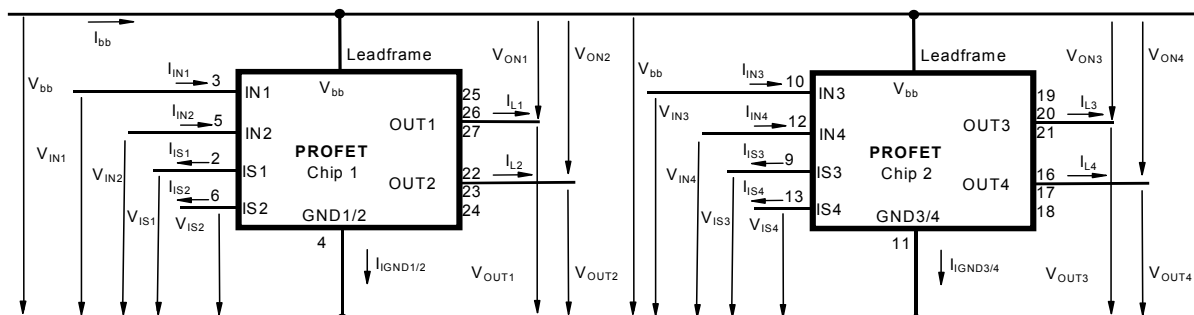
<sup>17)</sup> In the case of thermal shutdown the  $V_{\text{fault}}$  signal remains for  $t_{\text{delay(fault)}}$  longer than the restart of the switch (see diagram on page 14).

## Truth Table

	Input level	Output level	Current Sense $I_{IS}$
Normal Operation	L H	L H	0 nominal
Current-Limitation <sup>18)</sup>	H	H	$V_{\text{fault}}$
Short circuit to GND	L H	L L	0 $V_{\text{fault}}$
Overtemperature	L H	L L	0 $V_{\text{fault}}$
Short circuit to $V_{bb}$	L H	H H	0 <nominal <sup>19)</sup>
Open load	L H	Z H	0 0
Negative output Voltage clamp	L	L	0

L = "Low" Level      X = don't care      Z = high impedance, potential depends on external circuit  
 H = "High" Level       $V_{\text{fault}} = 6\text{V typ}$ , constant voltage independent of external used sense resistor.  
 Parallel switching of channels is possible by connecting the inputs and outputs in parallel. The current sense outputs have to be connected with a single sense resistor.

## Terms



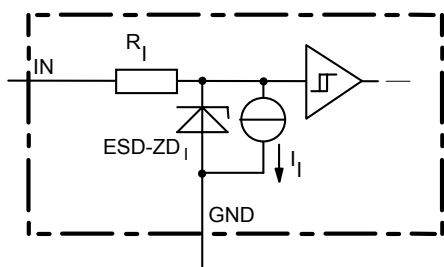
Leadframe ( $V_{bb}$ ) is connected to pin 1, 7, 8, 14, 15, 28.

<sup>18)</sup> Current limitation is only possible while the device is switched on.

<sup>19)</sup> Low ohmic short to  $V_{bb}$  may reduce the output current  $I_L$  and therefore also the sense current  $I_{IS}$ .



### Input circuit (ESD protection), IN1 to IN4



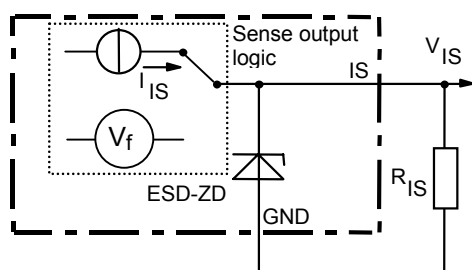
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

### Sense output

Normal operation:  $I_S = I_L / k_{ILIS}$

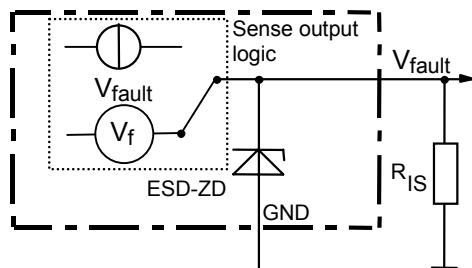
$V_{IS} = I_S \cdot R_{IS}$ ;  $R_{IS} = 1 \text{ k}\Omega$  nominal

$R_{IS} > 500 \Omega$



ESD-Zener diode:  $V_{ESD} = 6.1 \text{ V typ.}, \text{ max } 14 \text{ mA};$

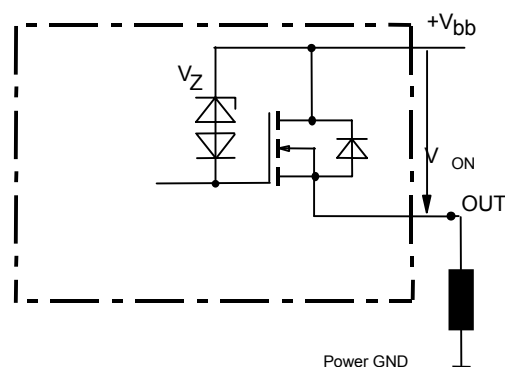
Operation under fault condition  
so as thermal shut down or current limitation



$V_{\text{fault}} = 6 \text{ V typ}$

$V_{\text{fault}} < V_{ESD}$  under all conditions

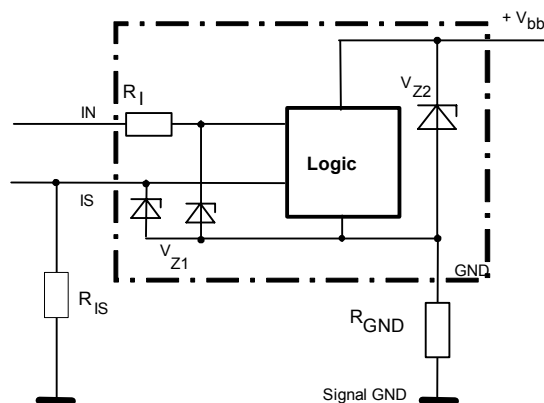
### Overvoltage output clamp, OUT1 or OUT2



$V_{ON}$  clamped to  $V_{ON(CL)} = 47 \text{ V typ.}$

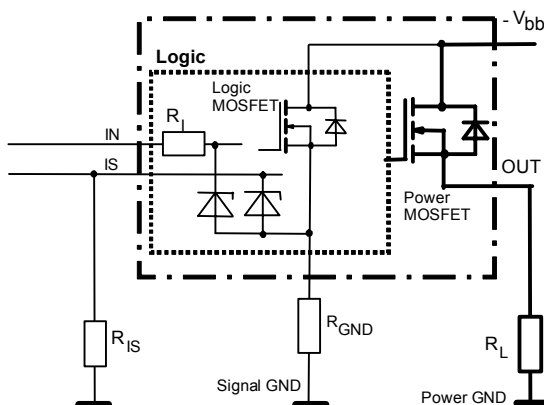
### Overvoltage protection of logic part

GND1/2 or GND3/4



$V_{Z1} = 6.1 \text{ V typ.}, V_{Z2} = 47 \text{ V typ.}, R_I = 3.5 \text{ k}\Omega \text{ typ.},$   
 $R_{GND} = 75 \Omega$

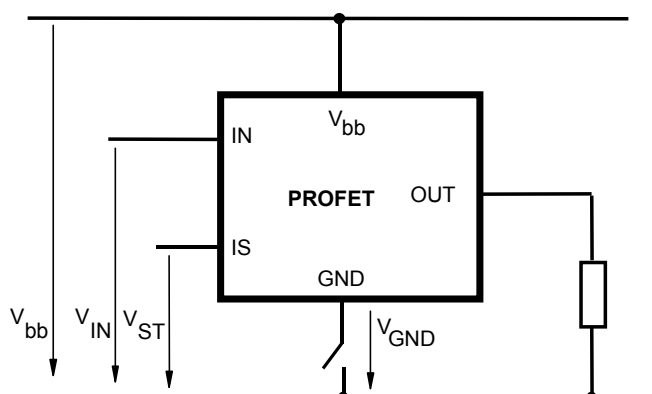
### Reverse battery protection



$R_{GND} = 75 \Omega, R_I = 3.5 \text{ k}\Omega \text{ typ.}$

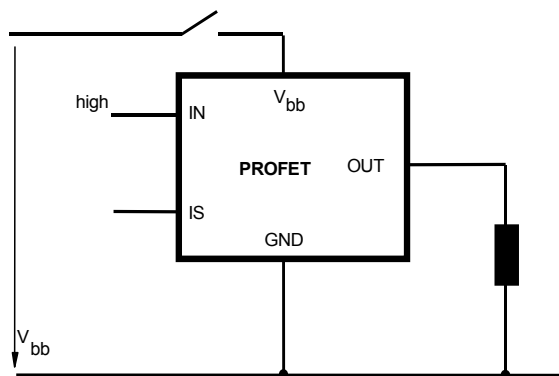
Temperature protection and sense functionality is not active during inverse current operation.

### GND disconnect



Any kind of load. In case of IN=high is  $V_{OUT} \approx V_{IN} - V_{IN}(T+)$ . Due to  $V_{GND} > 0$ , no  $V_{ST}$  = low signal available.

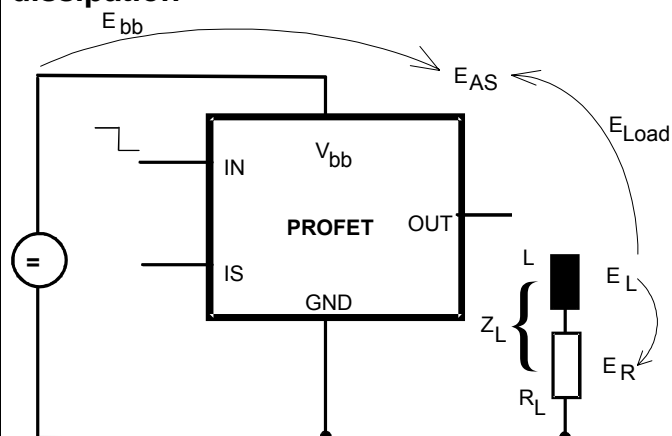
### V<sub>bb</sub> disconnect with energized inductive load



For inductive load currents up to the limits defined by  $Z_L$  (max. ratings and diagram on page 10) each switch is protected against loss of  $V_{bb}$ .

Consider at your PCB layout that in the case of  $V_{bb}$  disconnection with energized inductive load all the load current flows through the GND connection.

### Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = \frac{1}{2} \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t) dt,$$

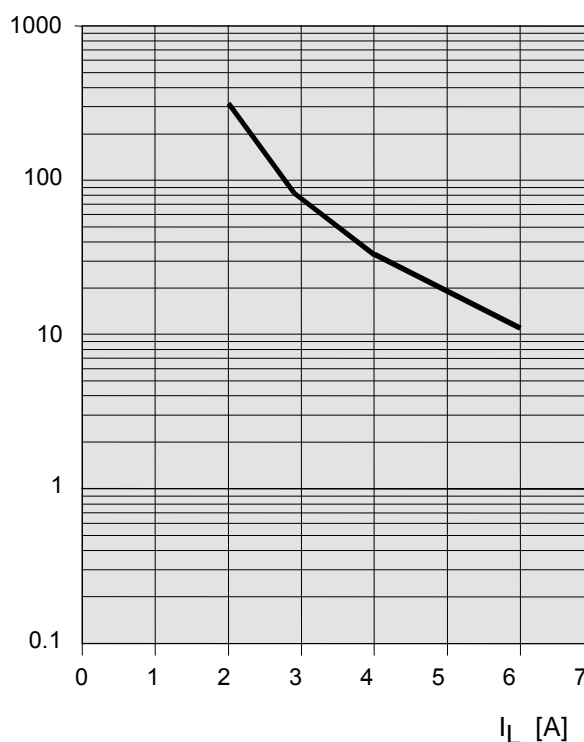
with an approximate solution for  $R_L > 0 \Omega$ :

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left( 1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

### Maximum allowable load inductance for a single switch off (one channel)<sup>6)</sup>

$L = f(I_L)$ ;  $T_{j,start} = 150^\circ\text{C}$ ,  $V_{bb} = 12\text{ V}$ ,  $R_L = 0 \Omega$

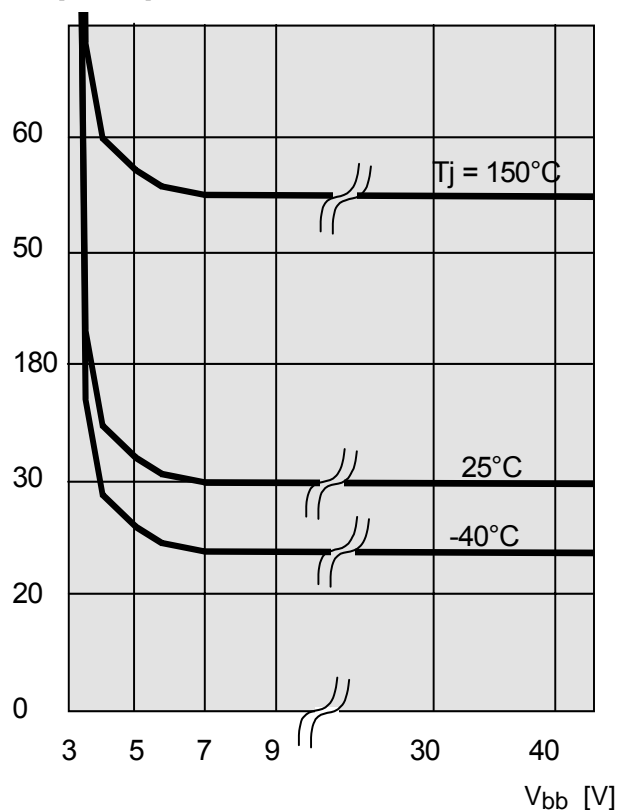
$Z_L$  [mH]



**Typ. on-state resistance**

$R_{ON} = f(V_{bb}, T_j)$ ;  $I_L = 2\text{ A}$ ,  $I_N = \text{high}$

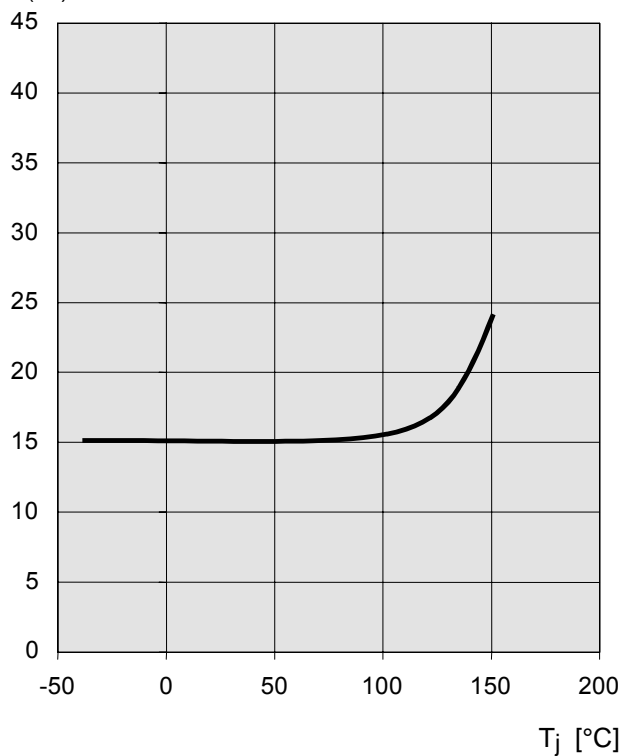
$R_{ON}$  [mOhm]



**Typ. standby current**

$I_{bb(off)} = f(T_j)$ ;  $V_{bb} = 9\text{...}34\text{ V}$ ,  $I_{N1,2,3,4} = \text{low}$

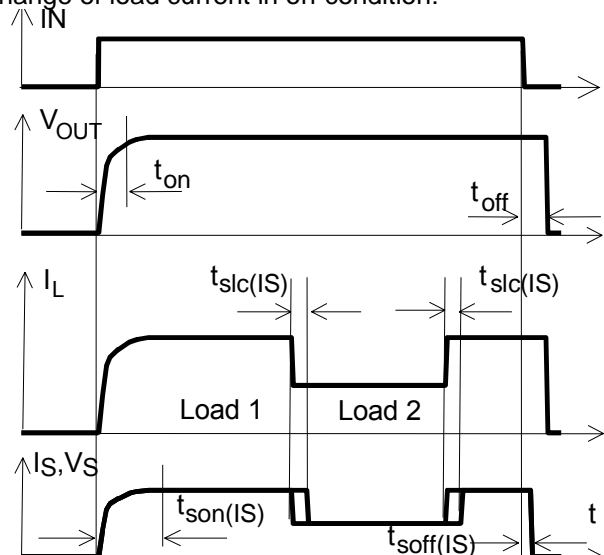
$I_{bb(off)}$  [ $\mu\text{A}$ ]



## Functionality diagrams

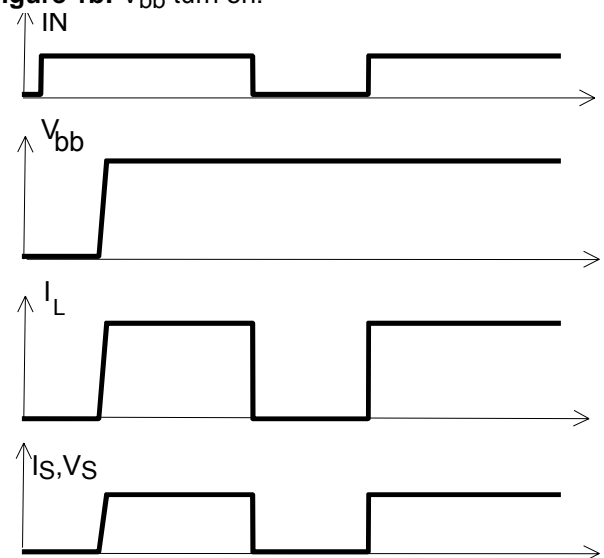
All diagrams are shown for chip 1 (channel 1/2). For chip 2 (channel 3/4) the diagrams are valid too. The channels 1 and 2, respectively 3 and 4, are symmetric and consequently the diagrams are valid for each channel as well as for permuted channels

**Figure 1a:** Switching a resistive load, change of load current in on-condition:



The sense signal is not valid during settling time after turn on or change of load current.

**Figure 1b:**  $V_{bb}$  turn on:

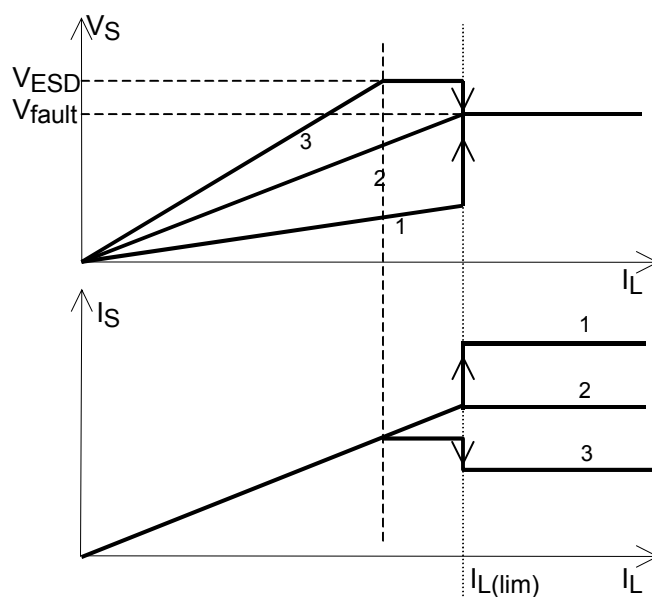


proper turn on under all conditions

**Figure 1c:** Behaviour of sense output:

Sense current ( $I_S$ ) and sense voltage ( $V_S$ ) as function of load current dependent on the sense resistor

Shown is  $V_S$  and  $I_S$  for three different sense resistors. Curve 1 refers to a low resistor, curve 2 to a medium-sized resistor and curve 3 to a big resistor. Note, that the sense resistor may not fall short of a minimum value of  $500\Omega$ .

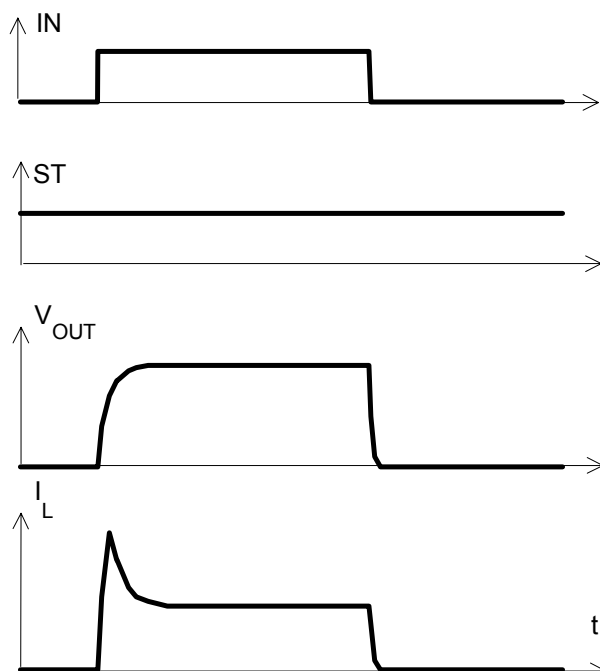


$$I_S = I_L / k_{ILIS}$$

$$V_{IS} = I_S \cdot R_{IS}; R_{IS} = 1 \text{ k}\Omega \text{ nominal}$$

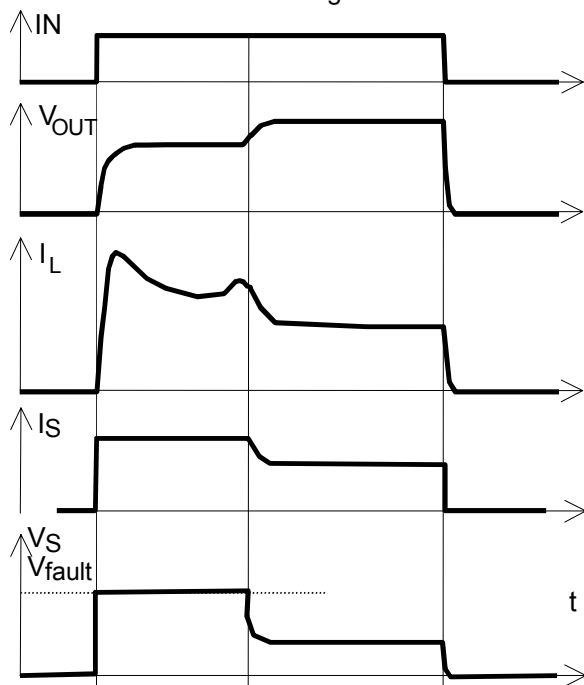
$$R_{IS} > 500\Omega$$

**Figure 2a:** Switching a lamp:

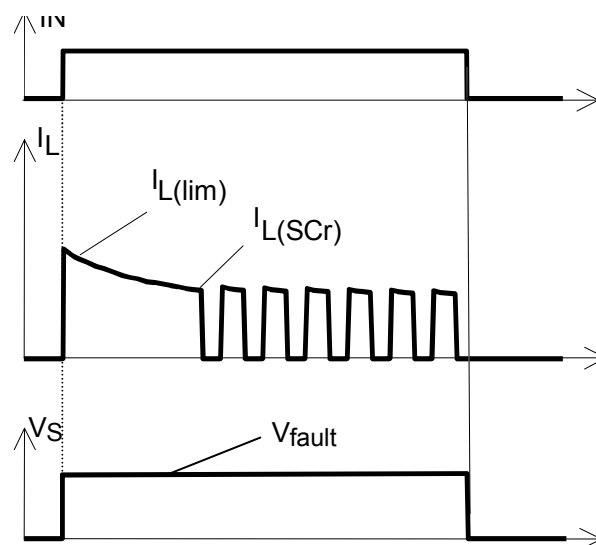


The initial peak current should be limited by the lamp and not by the current limit of the device.

**Figure 2b:** Switching a lamp with current limit:  
The behaviour of IS and VS is shown for a resistor,  
which refers to curve 1 in figure 1c

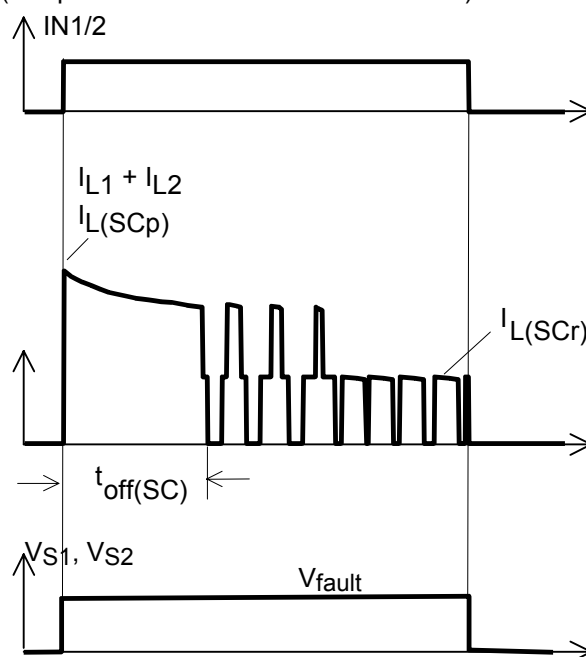


**Figure 3a:** Short circuit:  
shut down by overtemperature, reset by cooling



Heating up may require several milliseconds, depending on external conditions  
 $I_{L(lim)} = 45 \text{ A typ.}$  increases with decreasing temperature.

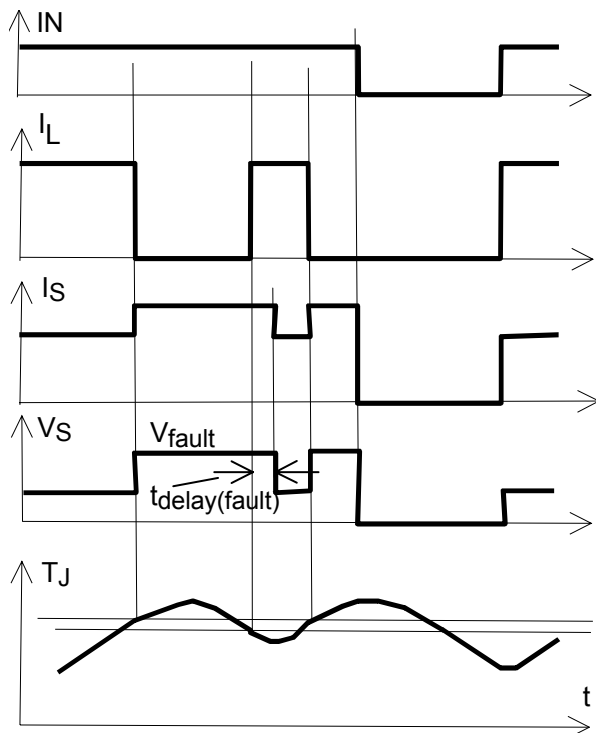
**Figure 3b:** Turn on into short circuit:  
shut down by overtemperature, restart by cooling  
(two parallel switched channels 1 and 2)



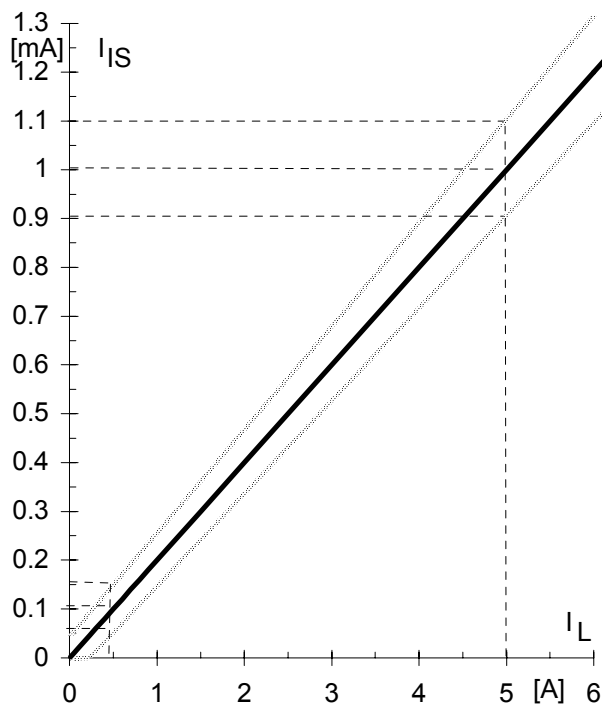
**Figure 4a: Overtemperature:**

Reset if  $T_j < T_{jt}$

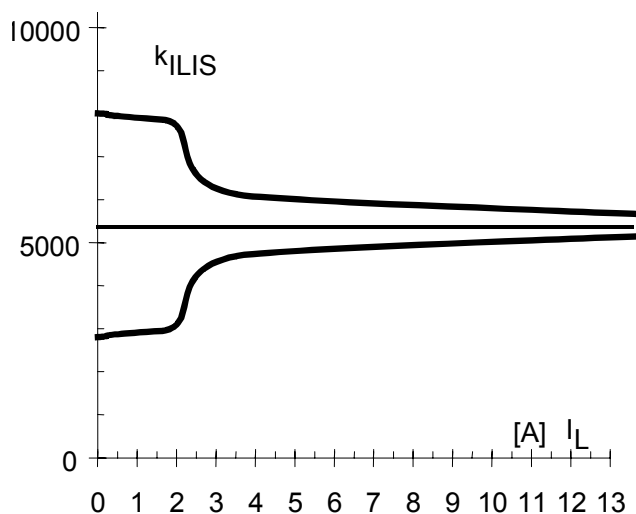
The behaviour of IS and VS is shown for a resistor, which refers to curve 1 in figure 1c



**Figure 6a: Current sense versus load current:**



**Figure 6b: Current sense ratio<sup>20)</sup>:**

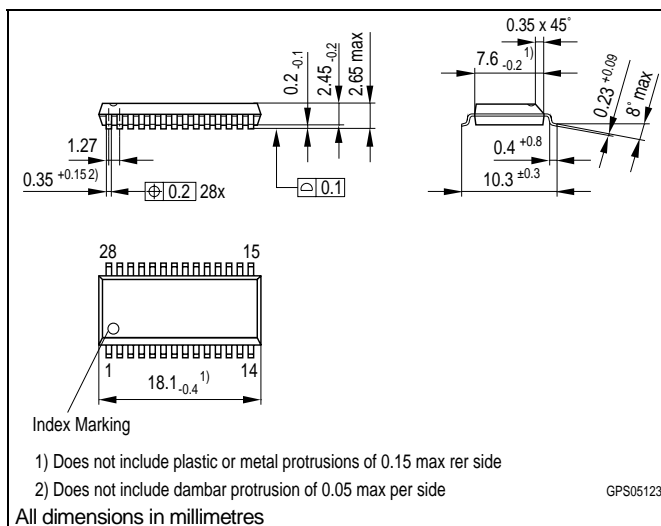


<sup>20)</sup> This range for the current sense ratio refers to all devices. The accuracy of the  $k_{ILIS}$  can be raised at least by a factor of two by calibrating the value of  $k_{ILIS}$  for every single device.

## Package and Ordering Code

### Standard: P-DSO-28-16

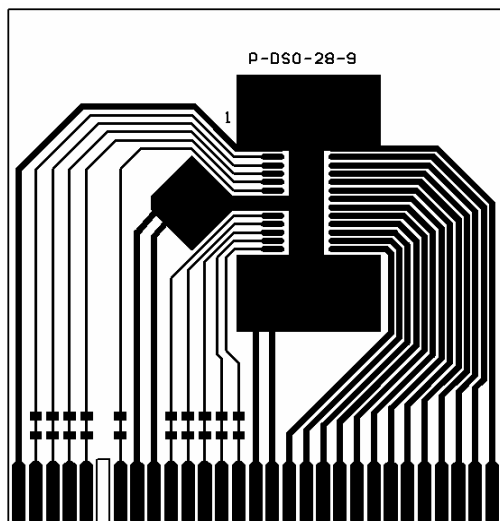
Sales Code	BTS 737 S3
Ordering Code	Q67060-S6133



Definition of soldering point with temperature  $T_s$ :  
upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer  
70 $\mu$ m, 6cm<sup>2</sup> active heatsink area) as a reference for  
max. power dissipation  $P_{tot}$ , nominal load current  
 $I_{L(NOM)}$  and thermal resistance  $R_{thja}$



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