5.8 ... 58

two parallel

125

2.8

65

٧

٧

 $\mathsf{m}\Omega$

Α



Smart Two Channel Highside Power Switch

Features

- Overload protection
- Current limitation
- Short-circuit protection
- Thermal shutdown
- Overvoltage protection
- Fast demagnetization of inductive loads
- Reverse battery protection¹)
- Open drain diagnostic output
- Open load detection in OFF-state
- CMOS compatible input
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge (ESD) protection

 $V_{\rm bb(AZ)}$

 $V_{\rm bb(on)}$

one

250

1.9

Application

- μC compatible power switch with diagnostic feedback for 12 V and 24 V DC grounded loads
- Most suitable for inductive loads
- Replaces electromechanical relays, fuses and discrete circuits

General Description

N channel vertical power FET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology. Providing embedded protective functions.

Product Summary

Overvoltage Protection

active channels:

RON

I_{L(NOM)}

Operating voltage

On-state resistance

Nominal load current

Pin Definitions and Functions

Pin	Symbol	Function		
1,10,	V_{bb}	Positive power supply voltage. Design the		
11,12,		wiring for the simultaneous max. short circuit		
15,16,		currents from channel 1 to 2 and also for low		
19,20		thermal resistance		
3	IN1	Input 1,2, activates channel 1,2 in case of		
7	IN2	logic high signal		
17,18	OUT1	Output 1,2, protected high-side power output		
13,14	OUT2	of channel 1,2. Design the wiring for the max.		
		short circuit current		
4	ST1	Diagnostic feedback 1,2 of channel 1,2,		
8	ST2	open drain, low in on state on failure or high in		
		off state on failure		
2	GND1	Ground 1 of chip 1 (channel 1)		
6	GND2	Ground 2 of chip 2 (channel 2)		
5,9	N.C.	Not Connected		

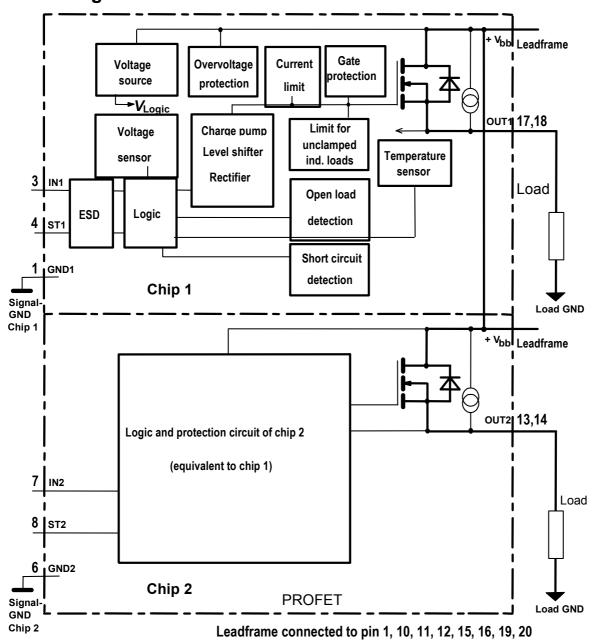
Pin configuration (top view)

-			
V_{bb}	1 •	20	V_{bb}
GND1	2	19	V_{bb}
IN1	3	18	OUT1
ST1	4	17	OUT1
N.C.	5	16	V_{bb}
GND2	6	15	V_{bb}
IN2	7	14	OUT2
ST2	8	13	OUT2
N.C.	9	12	V_{bb}
V_{bb}	10	11	V_{bb}

With external current limit (e.g. resistor R_{GND} =150 Ω) in GND connection, resistor in series with ST connection, reverse load current limited by connected load.



Block diagram



Maximum Ratings at $T_j = 25$ °C unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 4)	$V_{\rm bb}$	65	V
Supply voltage for full short circuit protection $T_{j,start} = -40 \dots +150$ °C	$V_{ m bb}$	40	V
Load current (Short-circuit current, see page 5)	<i>I</i> L	self-limited	Α
Operating temperature range	T _j	-40+150	°C
Storage temperature range	$T_{\rm stg}$	-55+150	



Maximum Ratings at $T_j = 25$ °C unless otherwise specified

Parameter	Symbol	Values	Unit	
Power dissipation (DC) ²⁾	P _{tot}	3	W	
(all channels active)	$T_a = 85$ °C:		1.6	
Electrostatic discharge capability (ESD) (Human Body Model) all o	V _{ESD}	1.0 1.0	kV	
Input voltage (DC)	V _{IN}	-0.5 +36	V	
Current through input pin (DC)	I _{IN}	±2.0	mA	
Current through status pin (DC)	I _{ST}	±5.0		
see internal circuit diagram page 7				

Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit	
			min	typ	max	
Thermal resistance						
junction - soldering point ^{2),3)}	each channel:	R_{thjs}			18	K/W
junction - ambient ²⁾	one channel active:	$R_{\rm thja}$		45		
	all channels active:			37		

Electrical Characteristics

Parameter and Conditions, each of the two channels			Symbol		Values		Unit
at Tj = 25 °C, V_{bb} = 12	V unless otherwise spec	cified		min	typ	max	
Load Switching C	apabilities and Cha	aracteristics					
On-state resistance	e (V _{bb} to OUT)						
$I_L = 2 A$	each channel,	$T_{\rm j} = 25^{\circ}{\rm C}$:	Ron		225	250	mΩ
$V_{\rm bb} = 24 \text{ V}$		$T_{\rm j} = 150^{\circ}{\rm C}$:			400	500	
tw	o parallel channels,	$T_{\rm j} = 25^{\circ}{\rm C}$:			113	125	
Nominal load curre	nt one cha	nnel active:	I _{L(NOM)}	1.60	1.9		Α
two parallel channels active:				2.4	2.8		
Device on PCB ²), $T_a = 85$ °C, $T_j \le 150$ °C							
•	e GND disconnected $f_{ extsf{IN}} = 0$, see diagram	•	I _{L(GNDhigh)}			1.1	mA

Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70μm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 12

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³⁾ Soldering point: upper side of solder edge of device pin 15. See page 12



Parameter and Conditions, each of the two channels	Symbol	Values			Unit
at T _j = 25 °C, V_{bb} = 12 V unless otherwise specified		min	typ	max	
Turn-on time to 90% V_{OUT} :	<i>t</i> on	15		80	μs
Turn-off time to 10% V_{OUT} :	$t_{ m off}$	20		70	·
$R_L = 12 \Omega$, $V_{bb} = 20 \text{ V}$, $T_j = -40 + 150 ^{\circ}\text{C}$					
Slew rate on	d V/dt _{on}			6	V/μs
10 to 30% V_{OUT} , $R_{\text{L}} = 12 \Omega$, $V_{\text{bb}} = 20 \text{V}$, $T_{\text{j}} = -40+150 ^{\circ}\text{C}$:					
Slew rate off	-d V/dt _{off}			7	V/μs
70 to 40% V_{OUT} , $R_{\text{L}} = 12 \Omega$, $V_{\text{bb}} = 20 \text{ V}$, $T_{\text{j}} = -40 + 150 ^{\circ}\text{C}$:					
Operating Parameters					
Operating voltage ⁴⁾ $T_i = -40 + 150$ °C:	V _{bb(on)}	5.8		58	V
Undervoltage shutdown $T_i = -40+150$ °C:		2.7		4.7	V
Undervoltage restart $T_j = -40 + 150$ °C:	V _{bb(u rst)}			4.9	V
Undervoltage restart of charge pump see diagram page 10 $T_j = -40+150$ °C:	$V_{\rm bb(ucp)}$		5.6	7.5	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u rst)} - V_{bb(under)}$	$\Delta V_{ m bb(under)}$		0.4		V
Overvoltage protection ⁵⁾ $T_j = -40 + 150$ °C:	$V_{\mathrm{bb}(AZ)}$	65	70		V
$I_{bb} = 40 \text{ mA}$					
Standby current, all channels off	I _{bb(off)}		20	70	μΑ
$V_{IN} = 0$ $T_j = 150$ °C:					
Operating current 6), $V_{IN} = 5V$, $T_j = -40 + 150$ °C	_				
$I_{\text{GND}} = I_{\text{GND1}} + I_{\text{GND2}},$ one channel on:			2.2 4.4		mA
two channels on:			7.7		
Protection Functions ⁷⁾	T	T	ı	7	
Initial peak short circuit current limit, (see timing diagrams, page 9)					
each channel, $T_j = -40$ °C:	I _{L(SCp)}			19	Α
<i>T</i> _j =25°C:			10		
$T_{j} = +150$ °C:		4.0			
two parallel channels		the curre	nt of one	channel	
Output clamp (inductive load switch off) ⁸⁾ at $V_{ON(CL)} = V_{bb} - V_{OUT}$	V _{ON(CL)}	59		75	V
Thermal overload trip temperature	T_{jt}	150			°C
Thermal hysteresis	ΔT_{jt}		10		K

⁴⁾ At supply voltage increase up to V_{bb} = 5.6 V typ without charge pump, $V_{OUT} \approx V_{bb}$ - 2 V

Semiconductor Group

⁵⁾ see also $V_{\rm ON(CL)}$ in circuit diagram on page 7.

⁶⁾ Add I_{ST} , if $I_{ST} > 0$

⁷⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

⁸⁾ If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest VON(CL)



Parameter and Conditions, each of the two channels	Symbol		Values		Unit
at $T_j = 25$ °C, $V_{bb} = 12$ V unless otherwise specified		min	typ	max	•
Reverse Battery					
Reverse battery voltage ⁹⁾	- V _{bb}			32	V
Diagnostic Characteristics					
Open load detection current	$I_{L(off)}$		6		μΑ
Open load detection voltage $T_j = -40+150$ °C:	$V_{\rm OUT(OL)}$	2.4	3	4	V
Short circuit detection voltage (pin 3 to 5)	V _{ON(SC)}		2.5		V
Input and Status Feedback ¹⁰⁾					
Input resistance (see circuit page 7)	R_{I}		20	-	kΩ
Input turn-on threshold voltage	$V_{\text{IN(T+)}}$	1		2.5	V
Input turn-off threshold voltage	$V_{IN(T-)}$	0.8			V
Input threshold hysteresis	$\Delta V_{\rm IN(T)}$		0.5		V
Off state input current $V_{IN} = 0.4 \text{ V}$:	I _{IN(off)}	1		30	μΑ
On state input current $V_{IN} = 2.5 \text{ V}$:	I _{IN(on)}	10	25	70	μΑ
Delay time for status with open load (see timing diagrams, page 10)	t _{d(ST OL3)}		200		μs
Status output (open drain)					
Zener limit voltage $T_j = -40 + 150$ °C, $I_{ST} = +1.6$ mA:	V _{ST(high)}	5.4	6.1		V
ST low voltage $T_j = -40 + 150$ °C, $I_{ST} = +1.6$ mA:	V _{ST(low)}			0.4	

⁹⁾ Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Note that the power dissipation is higher compared to normal operating conditions due to the voltage drop across the intrinsic drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 7).

 $^{^{\}rm 10)}\,$ If ground resistors $\rm R_{\rm GND}$ are used, add the voltage drop across these resistors.

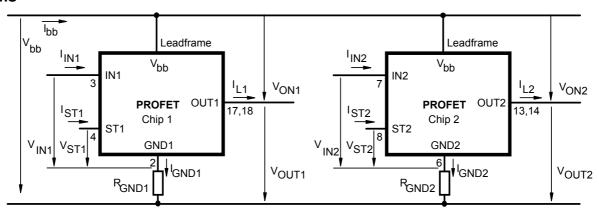


Truth Table

Channel 1	nel 1 Input 1		Status 1	
Channel 2	Input 2	Output 2	Status 2	
	level	level	BTS 707	
Normal	L	L	L	
operation	Н	Н	Н	
Open load	L	Z	Н	
	Н	Н	Н	
Short circuit	L	L	L	
to GND	Н	L	L	
Short circuit	L	Н	Н	
to V _{bb}	Н	Н	Н	
Overtem-	L	L	L	
perature	Н	L	L	
Under-	L	L	L	
voltage	Н	L	L	
Overvoltage	no overvoltage shutdown, see normal operation			

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

Terms

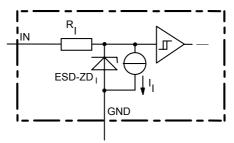


Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20

External R_{GND} optional; two resistors R_{GND1}, R_{GND2} = 150 Ω or a single resistor R_{GND} = 75 Ω for reverse battery protection up to the max. operating voltage.

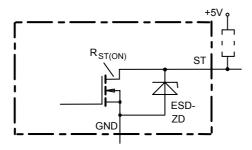


Input circuit (ESD protection), IN1 or IN2



ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

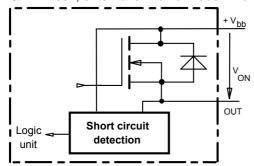
Status output, ST1 or ST2



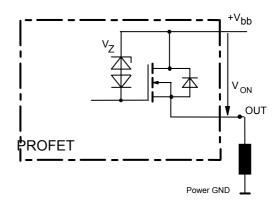
ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)} < 0~\Omega$ at 1.6 mA, ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

Short Circuit detection

Fault Signal at ST-Pin: $V_{\rm ON} > 2.5$ V typ, no switch off by the PROFET itself, external switch off recommended!

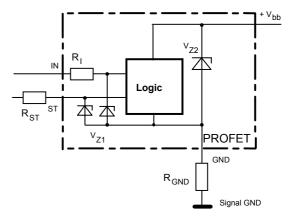


Inductive and overvoltage output clamp, OUT1 or OUT2



VON clamped to VON(CL) = -- V typ.

Overvoltage protection of logic part GND1 or GND2

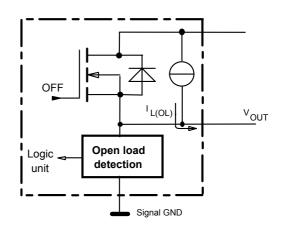


 $V_{Z1} = 6.1 \text{ V typ.}, V_{Z2} = 70 \text{ V typ.}, R_{I} = 20 \text{ k}\Omega \text{ typ.}, R_{GND} = 150 \Omega, R_{ST} = 15 \text{ k}\Omega \text{ nominal.}$

Open-load detection, OUT1 or OUT2

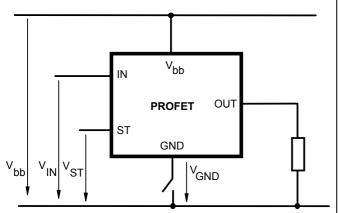
OFF-state diagnostic condition:

 $V_{OUT} > 3 \text{ V typ.; IN low}$



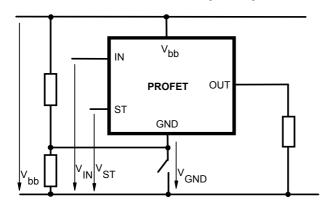


GND disconnect



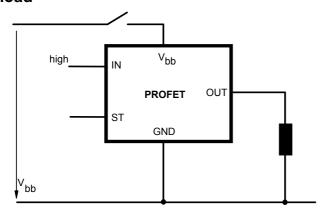
Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN}(T+)$. Due to $V_{GND} > 0$, no $V_{ST} = low$ signal available.

GND disconnect with GND pull up



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off Due to $V_{GND} > 0$, no $V_{ST} =$ low signal available.

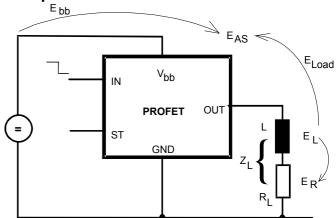
V_{bb} disconnect with energized inductive load



For an inductive load current up to the limit defined by E_{AS} (max. ratings) each switch is protected against loss of V_{bb} .

Consider at your PCB layout that in the case of Vbb disconnection with energized inductive load the whole load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = \frac{1}{2} \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \cdot i_L(t) dt$$

with an approximate solution for $R_L > 0 \Omega$:

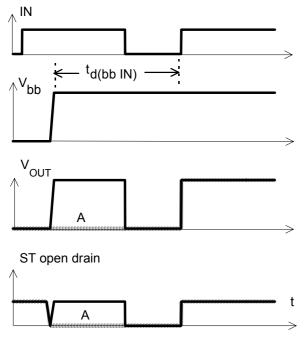
$$E_{\text{AS}} = \frac{|\underline{\mathsf{L}} \cdot \underline{\mathsf{L}}}{2 \cdot \mathsf{R}_{\mathsf{L}}} (|\mathsf{V}_{\text{bb}} + |\mathsf{V}_{\text{OUT}(\mathsf{CL})}|) \ ln \ (1 + \frac{|\underline{\mathsf{L}} \cdot \mathsf{R}_{\mathsf{L}}}{|\mathsf{V}_{\text{OUT}(\mathsf{CL})}|})$$



Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: V_{bb} turn on, :



in case of too early $V_{\rm IN}$ =high the device may not turn on (curve A) $t_{\rm d(bb\ IN)}$ approx. 150 $\mu \rm s$

Figure 2a: Switching an inductive load

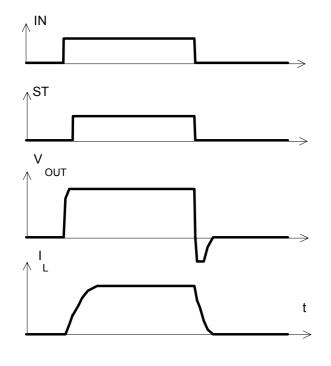
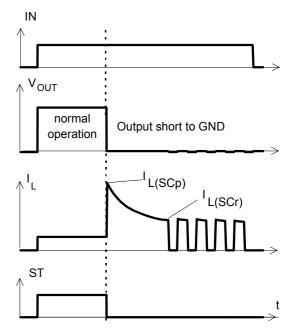


Figure 3a: Short circuit: shut down by overtempertature, reset by cooling



Heating up requires several milliseconds, depending on external conditions. External shutdown in response to status fault signal recommended.

Figure 4a: Overtemperature: Reset if $T_j < T_{jt}$

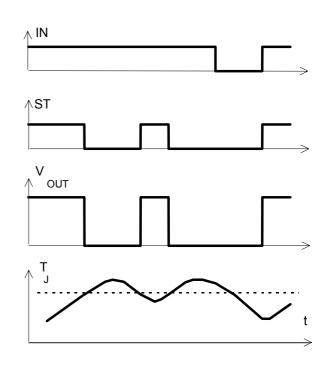
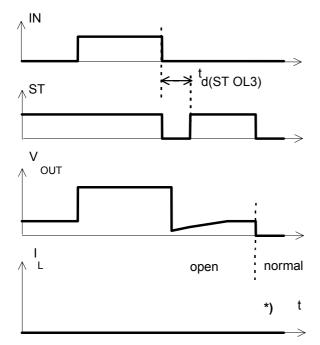




Figure 5a: Open load, : detection in OFF-state, turn on/off to open load



 $t_{\text{d(ST,OL3)}}\,\text{depends}$ on external circuitry because of high impedance

*) $I_L = 6 \mu A typ$

Figure 5b: Open load, : detection in OFF-state, open load occurs in off-state

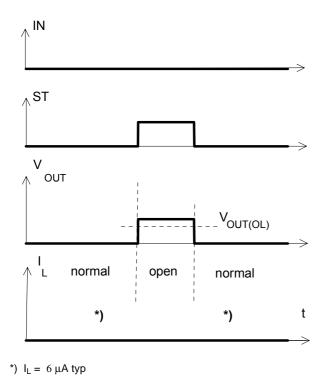


Figure 6a: Undervoltage:

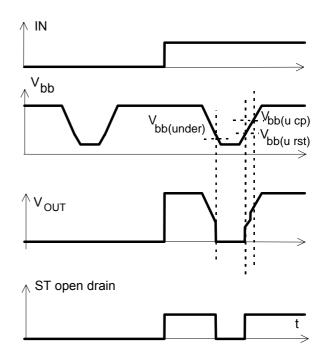
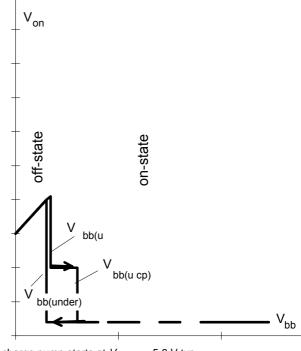


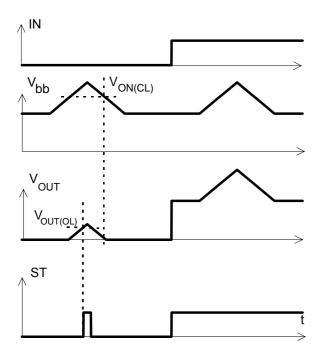
Figure 6b: Undervoltage restart of charge pump



charge pump starts at $V_{\rm bb(ucp)}$ =5.6 V typ.



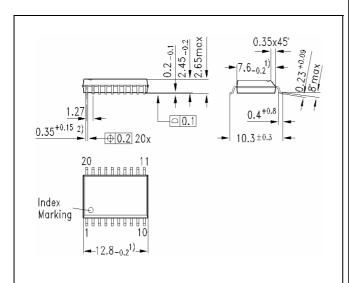
Figure 7a: Overvoltage, no shutdown:





Package and Ordering Code

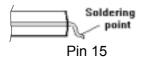
Standard P-DSO-2	20-9	Ordering Code
BTS 707		Q67060-S7010-A2



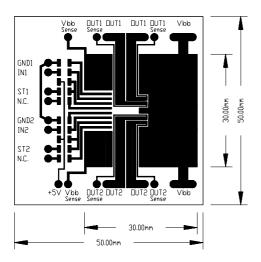
All dimensions in millimetres

- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

Definition of soldering point with temperature T_s : upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer 70 μ m, 6cm² active heatsink area) as a reference for max. power dissipation P_{tot}, nominal load current I_{L(NOM)} and thermal resistance R_{thja}



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