

BGF110

SD Card Interface ESD Protection

Small Signal Discretes



Never stop thinking

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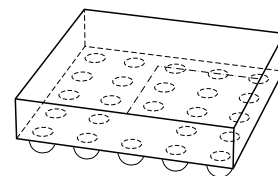
BGF110**Revision History: 2007-07-04, V2.2****Previous Version: 2006-10-17**

Page	Subjects (major changes since last revision)
4	EMI and cross talk feature added
4	Contact discharge added

SD Card Interface ESD Protection

Feature

- ESD protection for SD Card interface
- Integrated ESD protection up to 15 kV contact discharge
- Very good EMI filtering with very low cross talk
- Green wafer level package with SnAgSu solder balls
- 400 μm solder ball pitch



WLP-24-2



Description

The BGF110 is an ESD protection for the SD Card interface using a green wafer level package. External pins are protected up to 15 kV contact discharge according to IEC61000-4-2. A RF filter functionality provides very good RF and EMI suppression on the digital lines with very low cross talk. Sensitivity of the line capacitance on the bias voltage is very low. The wafer level package has a 400 μm solder ball pitch and 250 μm ball diameter (before ball attach).

Type	Package	Marking	Chip
BGF110	WLP-24-2	BGF110	N0720

Table 1 Maximum Ratings

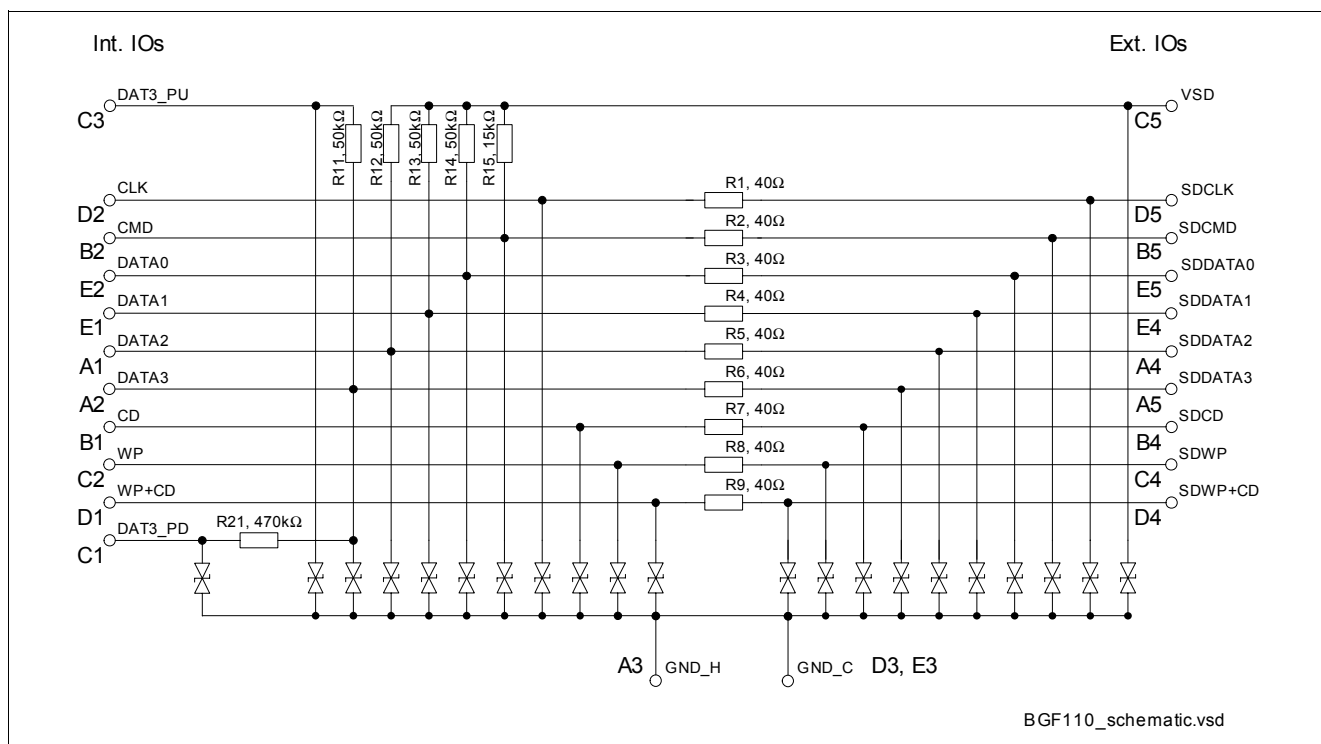
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_P	-14		14	V	
Operating temperature range	T_{OP}	-40		+85	$^{\circ}\text{C}$	
Storage temperature range	T_{STG}	-65		+150	$^{\circ}\text{C}$	
Maximum current at all pins	I_{max}			113 ¹⁾	mA	
Electrostatic discharge according to IEC61000-4-2 (contact discharge)						
Ext. IOs: A4, A5, B4, B5, C4, C5, D4, D5, E4, E5	V_E	-15		15	kV	
Int. IOs: A1, A2, B1, B2, C1, C2, C3, D1, D2, E1, E2	V_I	-2		2	kV	

1) Can be applied for 24 hours if thermal power dissipation into PCB is considered properly

Table 2 Electrical Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Series Resistors						
$R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8, R_9$	$R_{1...9}$	32	40	48	Ω	
$R_{11}, R_{12}, R_{13}, R_{14}$	$R_{11...14}$	35	50	65	k Ω	
R_{15}	R_{15}	10.5	15	19.5	k Ω	
R_{21}	R_{21}	329	470	611	k Ω	
Reverse current of ESD protection diodes	I_R		0.1	120	nA	$V_R = 3 \text{ V}$
			0.1	120	μA	$V_R = 14 \text{ V}$
Line capacitance	C_T		13.5	20	pF	$V_R = 0 \text{ V}$
Capacitance of each line to GND ²⁾			11.5			$V_R = 5 \text{ V}$

1) at $T_A = 25^\circ\text{C}$

2) Without line coupling by resistors $R_{11} - R_{21}$

Figure 1 Schematic

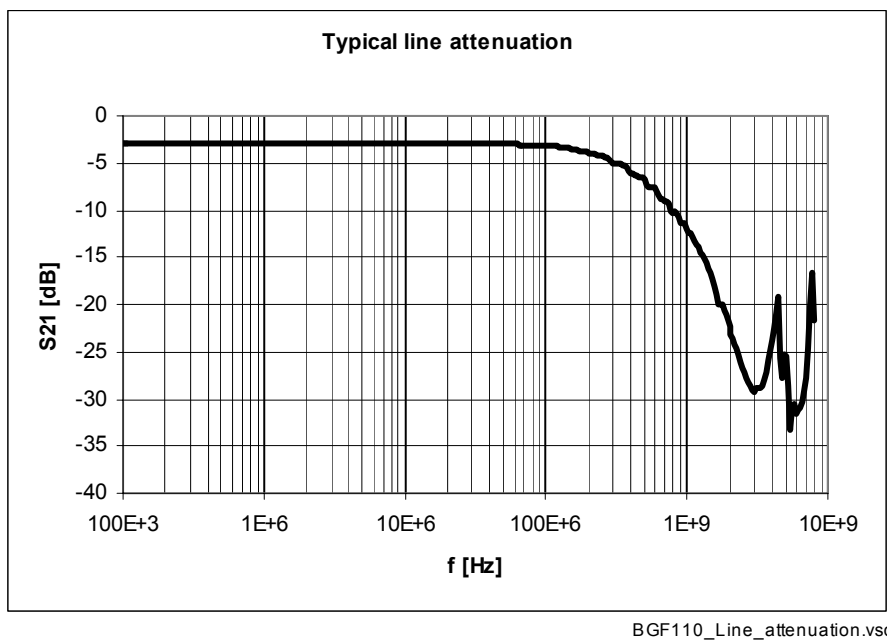


Figure 2 Line attenuation $Z_S = Z_L = 50 \Omega$

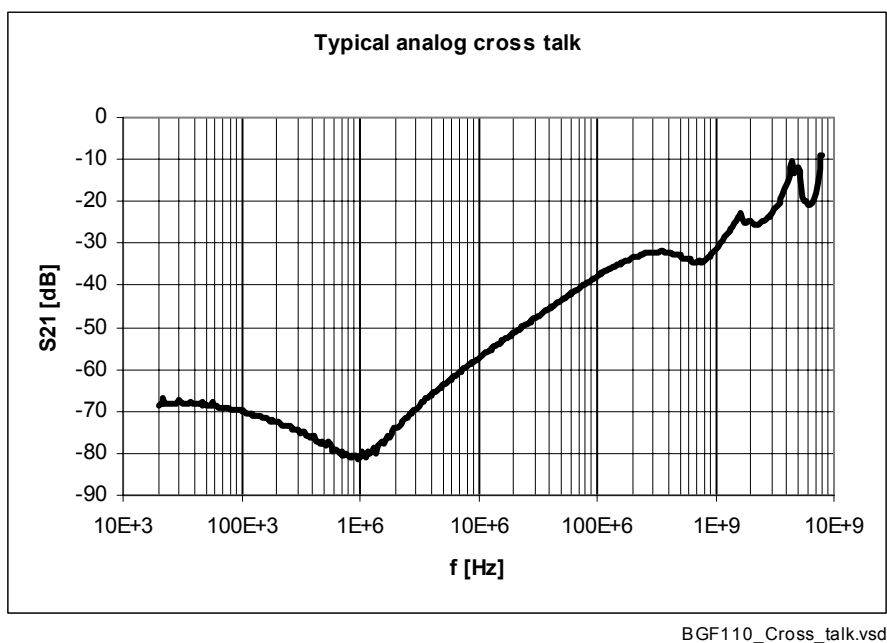


Figure 3 Analog cross talk, $Z_S = Z_L = 50 \Omega$

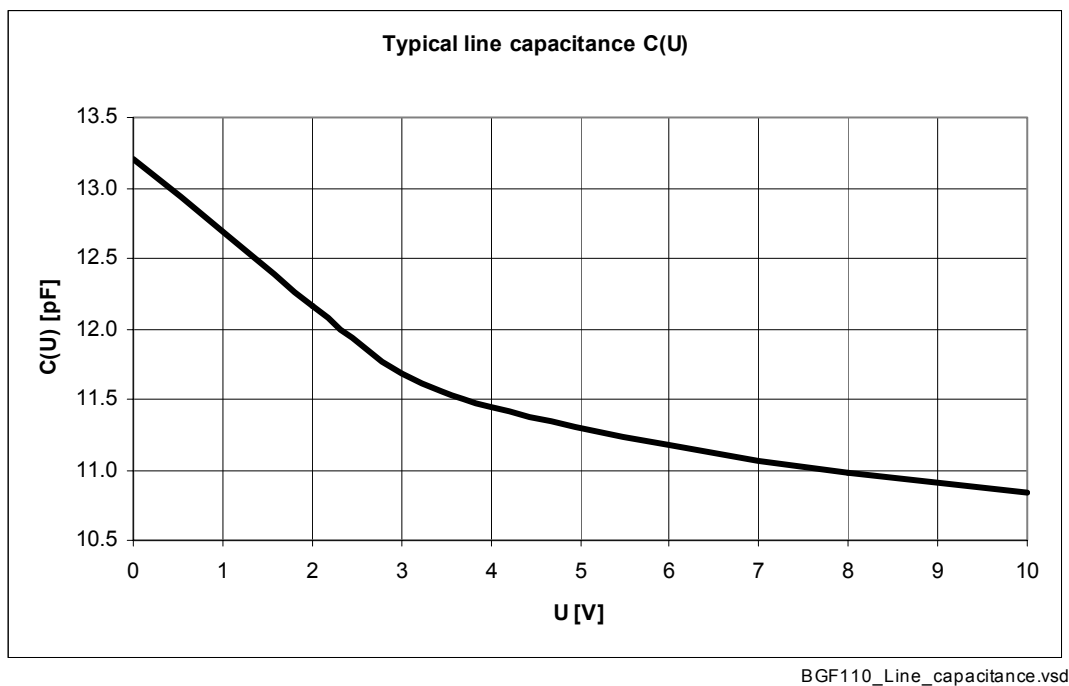


Figure 4 Line capacitance versus bias voltage

Package Outline

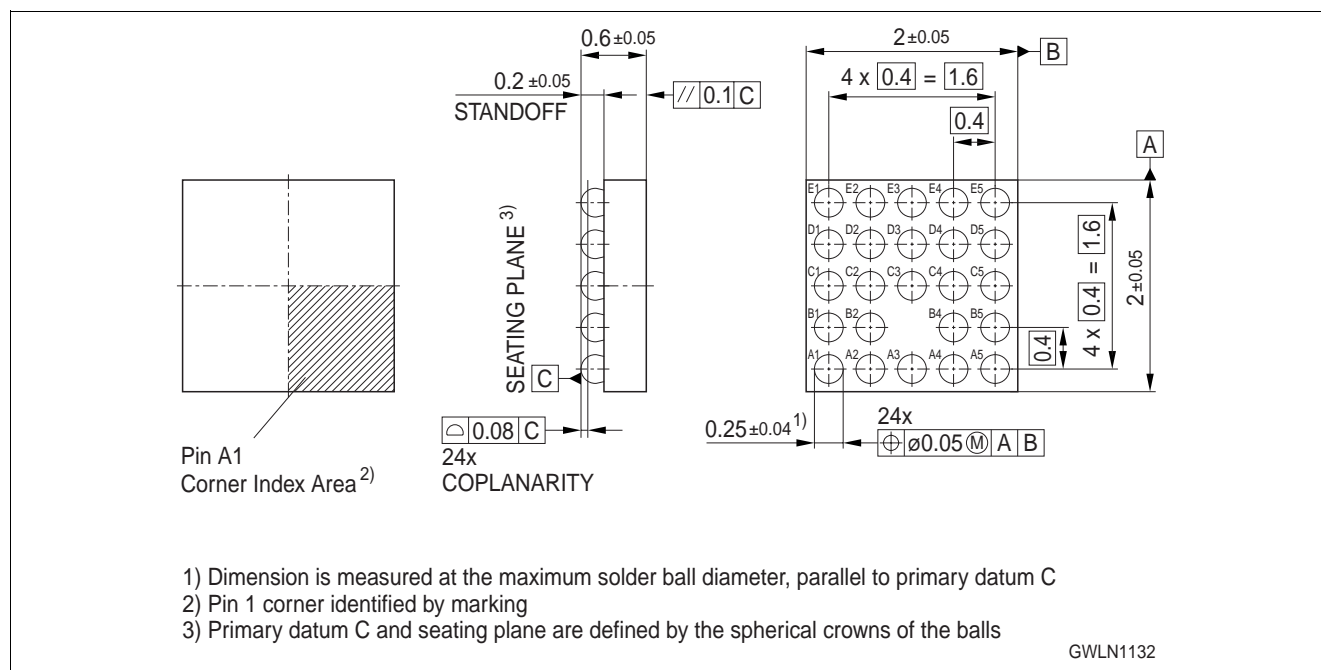


Figure 5 Package WLP-24-2

